32 KHz CLOCK OSCILLATION MARGIN STUDY

DECEMBER 2023

SECURE CONNECTIONS FOR A SMARTER WORLD

FIRST EXPERIMENT: ESR_RANGE EFFECT CONFIRMATION

Summary

4 parameters have tried to test the oscillation margin:

1. The series resistor
2. The ESR_range (current) =3
3. The Fine Amp Gain = 10
4. The SOX_EN = 0

During this analysis, the series resistor could go up to 1MΩ thanks to an ESR_range to 3.

The 2 other parameters are not improving the oscillation start and steady state.
It is NOT recommended to use SOX_EN=0 because it makes the 32kHz clock slowly stop.

Series resistor on 32kHz pin + ESR range + Fine Amp Gain

Resistor	ESR range	FineAmp Gain	CapSel	32kHz Osc	32kHz freq	32kHz output
0	ESR_range0	no	8pF		Stable	OK
150k	ESR_range0	no	8pF	260 mVpp	Stable	OK
240k	ESR_range0	no	8pF	176 mVpp	Stable	OK
300k	ESR_range0	no	8pF	-	Not stable	KO
300k	ESR_range3	no	8pF	500 mVpp	stable	OK
560k	ESR_range0	No or 10	8pF	-	-	KO
560k	ESR_range3	No or 10	8pF	520mVpp	Stable (189ppm)	OK
680k	ESR_range0	No or 10	8pF	-	-	KO
680k	ESR_range3	No or 10	8pF	600mVpp	stable	OK
1M	ESR_range0	no	8pF	-	-	KO
1M	ESR_range3	No or 10	8pF	600mVpp	Stable (253ppm)	OK

2ND EXPERIMENT: MCAL EFFECT ON CLOCK PROPAGATION

Summary

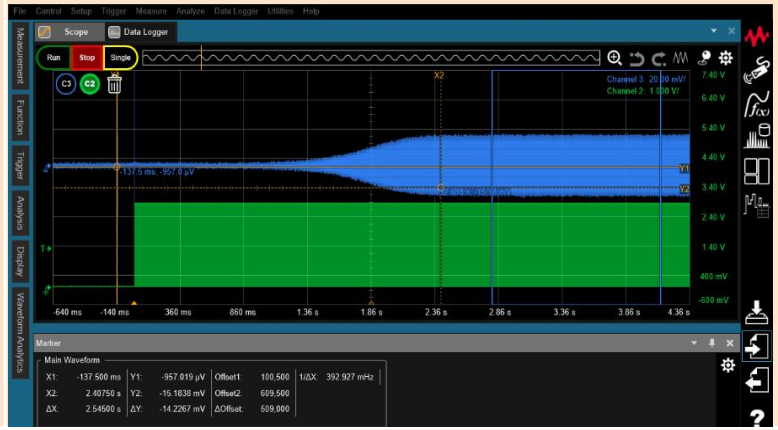
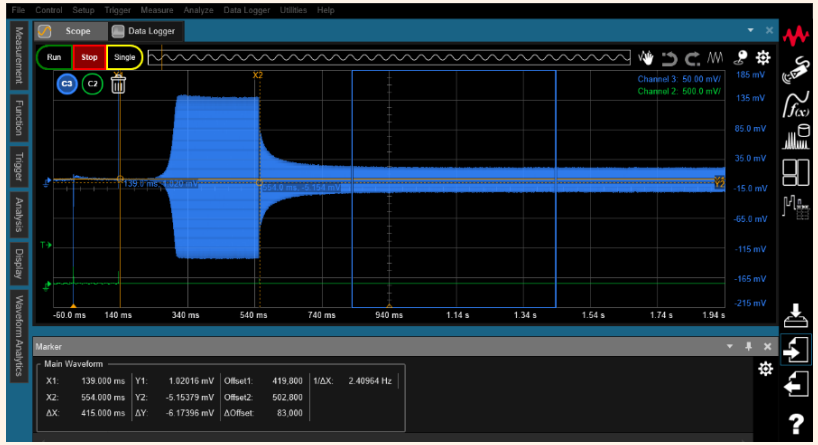
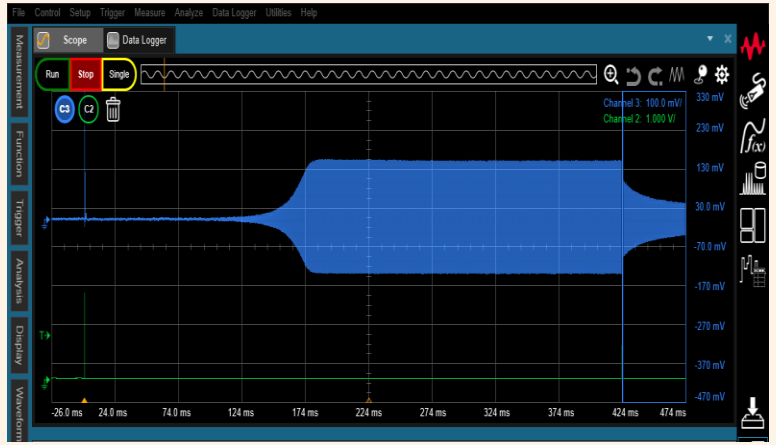
- The MCAL implemented on MR3 permits
  - to start the clock with an **high oscillation margin** (here 13.5 /1MΩ / ESR_Range =3),
  - in some case (max CapSel / ESR_Range low) to get the steady state **earlier** than with MR2 (no MCAL) – (see example slide 6)
  - to **propagate** the clock in the blocks (criteria from the ref manual instructions –cf slide 8)

MCAL enablement could be reserved to the **extreme* cases** since for most of the normal** cases MR2 provides the same clock voltage in a shorter time.

(*): close to the limit where the clock can't start

(**): typically with low CapSel and high ESR_range values

Example: Start&Steady states versus ESR_Range = 1 / Series Resistor 1MΩ

SDK	Start delay (ms)	Steady Voltage (mV)	Osc RDY at power ON	Scope measurement Start delay	Scope measurement Osc Rdy test (green) Toggle: OSC RDY=0
MR2	2546	144	No		
MR3 MCAL	415	145	Yes		

Summary: configurations for a 32kHz clock propagation

@ ESR_Range = 3
Same result in MR2 and MR3

Osc Margin	CapSel < 8pF	CapSel = 8pF	CapSel = 10pF	CapSel = 12pF	CapSel = 14pF	CapSel > 14 pF
10.3	OK	OK	OK (183 ppm)	KO	KO	KO
8.8	OK	OK	OK	OK (152 ppm)	KO	KO
7.4	OK	OK	OK	OK (122 ppm)	KO	KO
6.4	OK	OK	OK	OK	OK (91 ppm)	KO

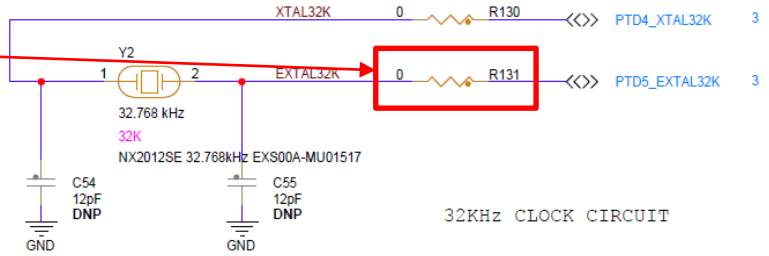
Clock propagation: Extracted criteria from the reference manual

6 CLOCK_DET	Clock Detect The Clock monitor has detected an error. 0b - Clock error is not detected 1b - Clock error is detected
5 CLK_SEL_32K	32 kHz clock source selection bit 0b - FRO32K clock output is selected as clock source 1b - OSC32K clock output is selected as clock source

- OSC32K as clock source
  1. Set OSC32K_CTRL[OSC_EN] and OSC32K_CTRL[SOX_EN] as 1b,
  2. Select internal capacitance bank value through OSC32K_CTRL[XTAL_CAP_SEL] and OSC32K_CTRL[EXTAL_CAP_SEL] if internal capacitance back is enabled (OSC32K_CTRL[CAP_SEL_EN]).
  3. Wait until the STATUS[OSC32K_ACTIVE] is 1b to identify OSC32K available.
  4. Set CGC32K[CLK_SEL_32K] as 1b to select OSC32K as clock source.

Test conditions

- KW45 EVK board – Series resistor on the Xtal path
- CX3322 Keysight analyzer
- SW*: customized from SDK MR2 then SDK MR3 with MCAL
- 32kHz frequency is measured versus:
  - The XTAL_CAP_SEL and EXTAL_CAP_SEL values
  - ESR_RANGE: 0 to 3
- The clock is measured on PTC7 (J6-10)
- For the SW MR3, some GPIOs are measured in order to check the propagation in the blocks (see slide 11-12):
  - PTA 18 : OSC32K_RDY
  - PTB 1 : CAP_SEL
  - PTB 2 : OSC_EN
  - PTB 3 : CLK_DET
  - PTC 6 : CLK_SEL_32K

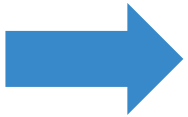


(*): MR2_MR3_081223.zip

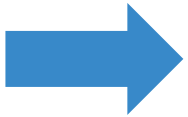
Test flow

Flash the code to KW45 EVK under iAR

Check in debug mode if the register is at the right CapSel/ESR_Range values

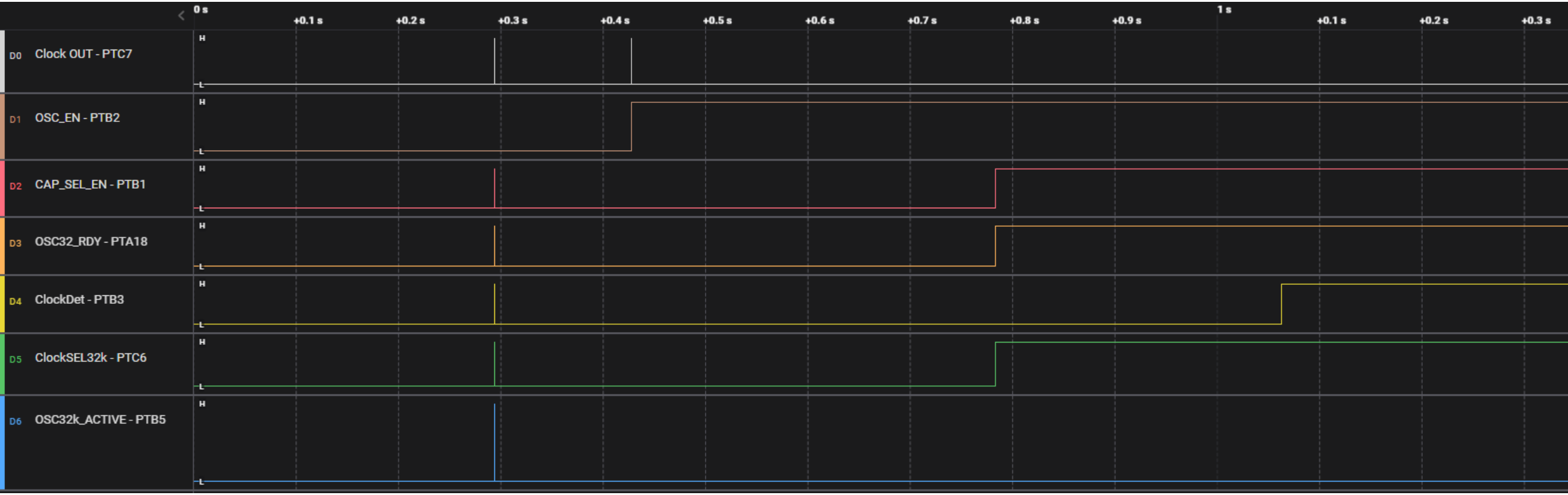


Exit debug mode, unplug the USB link from the EVK board

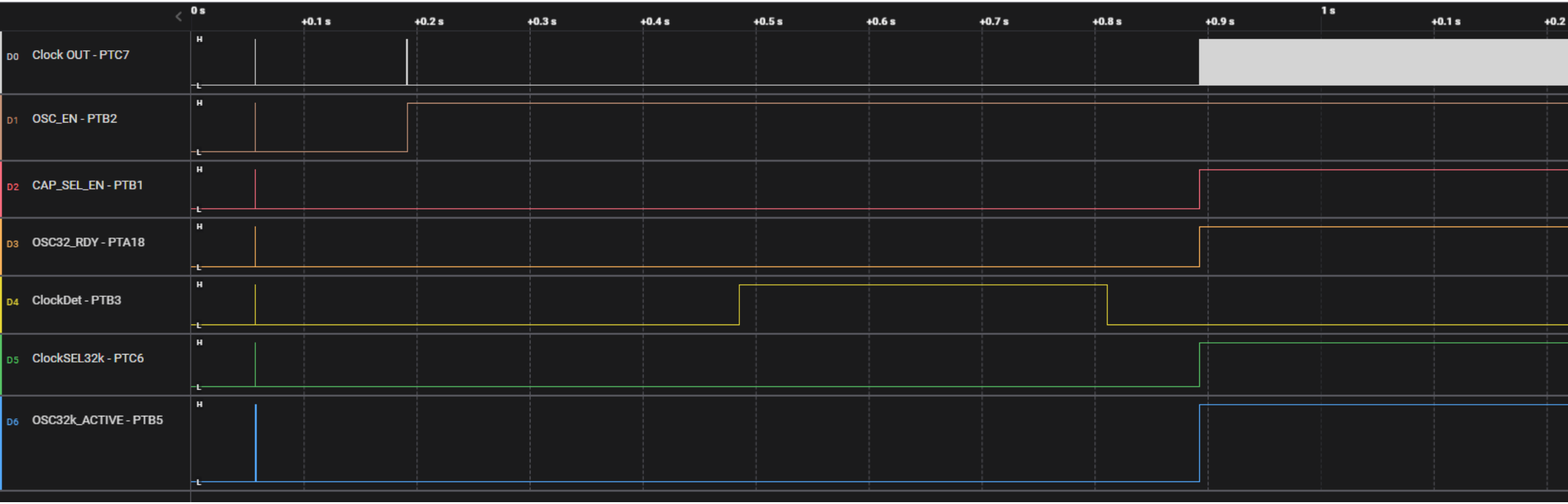


Connect the Saleae probes , open Logic aps, run it and plug the USB link

Example 1: MR3/Osc Margin10/ESR_Range=0/CapSel=8pF



Example 2: MR3/Osc Margin10/ESR_Range=0/CapSel=8pF



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