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# SMSC Ethernet PHY Daughter Card

## *Revision A1*

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with Vybrid processors. Although best design practices have been applied, some areas may not be suitable for a mass production design. For an added resource, refer to Vybrid Hardware Development Guide document.

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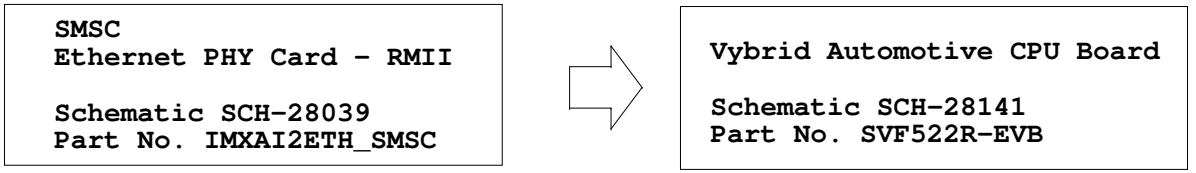
ICAP Classification: FCP: FIUO: PUBI: X

| | | | |
|---|---|---|---|
| Designer: Utkarsh G. | Drawing Title: IMXAI2ETH_SMSC | | |
| Drawn by: Utkarsh G. | Page Title: Introduction | | |
| Approved: David B. | Size C | Document Number SCH-28039 PDF: SPF-28039 | Rev A1 |
| | Date: Wednesday, October 15, 2014 | Sheet 1 of 6 | |

# System Block Diagram

Board set for customers shown below.




Components with "Hard_Location" displayed have unalterable reference designators. These common components have the same designators on the Atheros daughter card.

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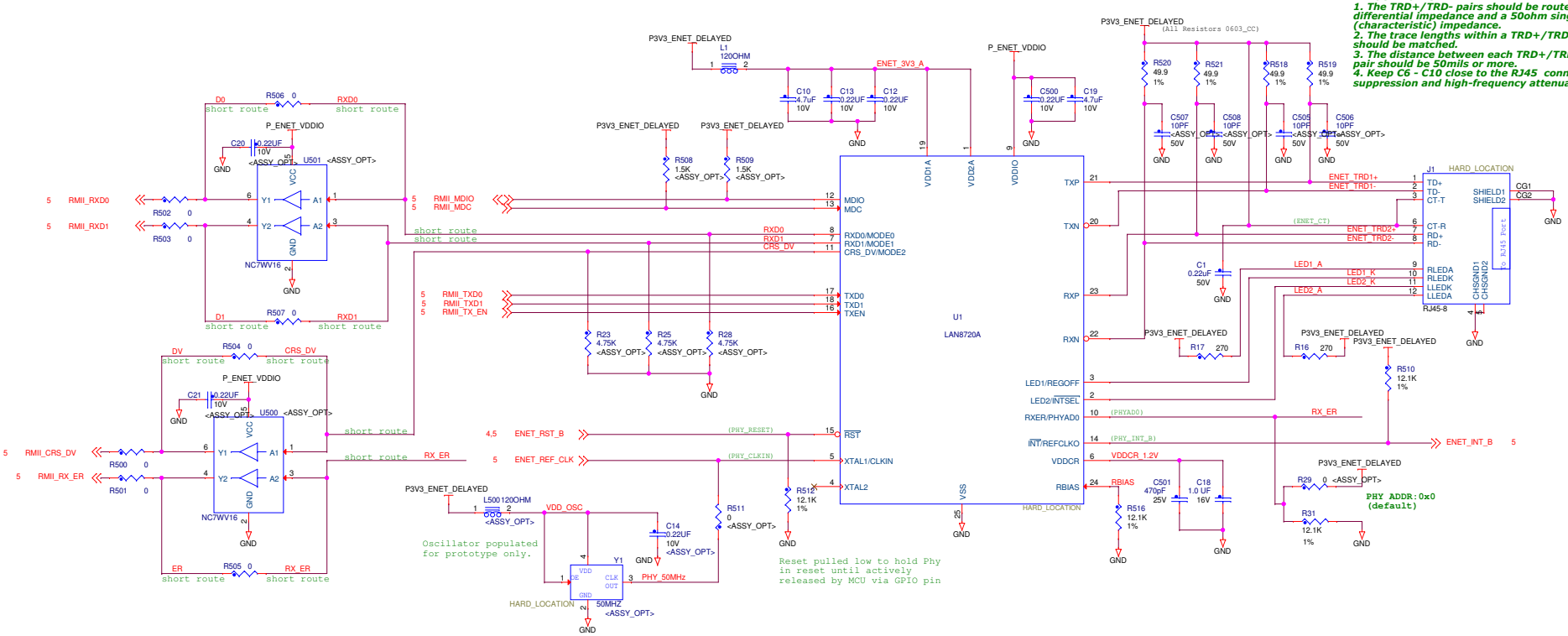
| Drawn by: Utkarsh G. | Page Title: Block Diagram | | |
| Approved: <Approver> | Size C | Document Number SCH-28039 PDF: SPF-28039 | Rev A1 |
| | Date: Wednesday, October 15, 2014 | Sheet 2 of 6 | |

# Ethernet PHY



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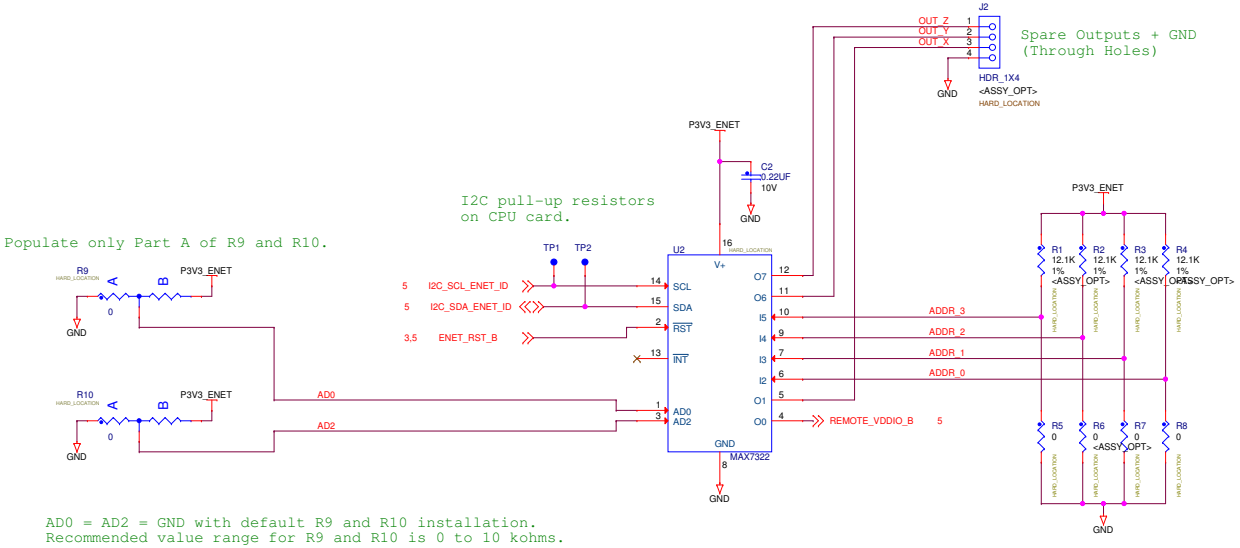
|---|---|---|---|
| Designer: Utkarsh G. | Drawing Title: IMXAI2ETH_SMSC | | |
| Drawn by: Utkarsh G. | Page Title: Ethernet PHY | | |
| Approved: <Approver> | Size C | Document Number SCH-28039 PDF: SPF-28039 | Rev A1 |
| | Date: Wednesday, October 22, 2014 | Sheet 3 of 6 | |

# Card ID




AD0 = AD2 = GND with default R9 and R10 installation.
Recommended value range for R9 and R10 is 0 to 10 kohms.

Default I2C 8-bit Write Address = 0xD0
Default I2C 8-bit Read Address = 0xD1

**Default Card ID**

| Addr 3 | Addr 2 | Addr 1 | Addr 0 |
|---|---|---|---|
| 0 | 1 | 0 | 0 |

270 ohm to 68 kohm are acceptable values for pull-up resistors R1 - R4.

Some I2C address selections per AD0 and AD2 also enable on-chip pull-up resistors on I2-I5. Acceptable values for pull-downs R5 - R8 are 0 to 270 ohms for good noise margin.

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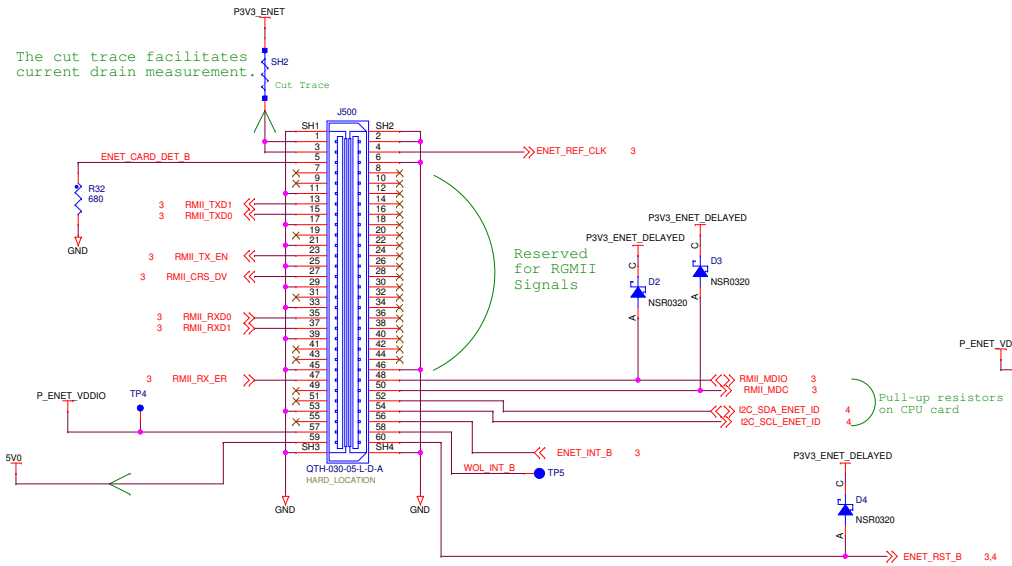
| | Date: Wednesday, October 22, 2014 | Sheet 4 of 6 | |

# Board to Board Interface

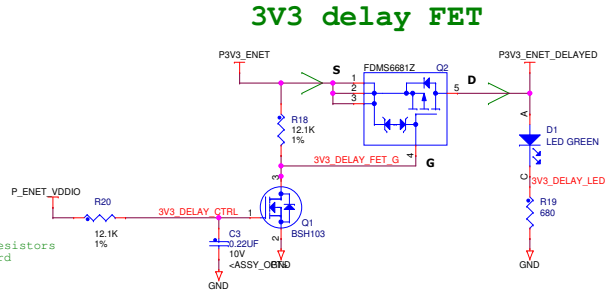



Connector pin assignment per Agile document DOC-01898.

Mating connector part number: QSH-030-01-L-D-A-K-TR

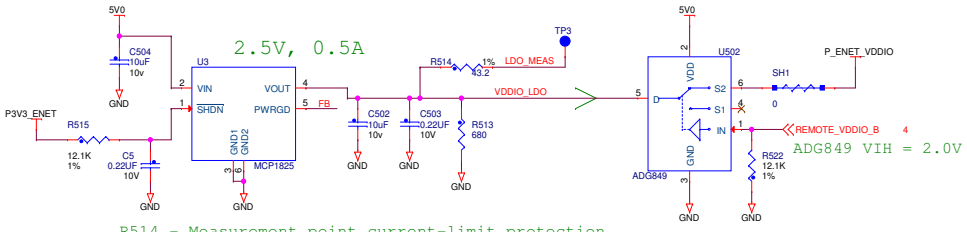
Mating height to CPU Card = 19 mm (clearance required by CPU Card)

# P3V3_ENET Delay




# Local I/O Power Option

Switch default = S1




R514 - Measurement point current-limit protection
R513 - Ensures reg min load > 1mA

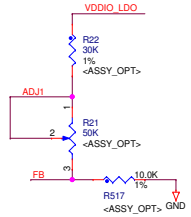
R522 ensures U502.1 = low at power up.

REMOTE_VDDIO_B from U2 controls P_ENET_VDDIO supply. For Vybrid operation, P_ENET_VDDIO comes from CPU card, so U502 has to be open.

# Adjustable Voltage (test purposes only)

Vo = 0.41 x (1 + Ru/Rd)

1.64<P_ENET_VDDIO<3.69




U3 Adjustable version: MCP1825T-ADJE/DC

From LAN8720 DS: 1.62<P_ENET_VDDIO<3.6

*Assembly Drawing Info*

*Two board standoffs are required.*
*SAMTEC SO-1915-05-01-01*
*Freescale internal part number 280-76823*

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| Drawn by: Utkarsh G. | Page Title: Board Connection | | |
| Approved: <Approver> | Size C | Document Number SCH-28039 PDF: SPF-28039 | Rev A1 |
| | Date: Wednesday, October 22, 2014 | Sheet 5 of 6 | |

## Versions of Rev A

| | | |
|---|---|---|
| A | Initial version for review. | 12/11/13 |

| | | |
|---|---|---|
| A1 | Sheet 1 - Added disclaimer boilerplate.<br>Updated table of contents.<br>Sheet 3 - Populated R504 - R507<br>DNP U500, U501, C20 and C21<br>Sheet 5 - Replaced R19 and R32 (1.5K) with 680 Ohms | 10/14/14 |

1. Unless Otherwise Specified:
   All resistors are in ohms, 5%.
   All voltages are DC.
   All polarized capacitors are aluminum electrolytic.

2. Interrupted lines coded with the same letter or
   letter combinations are electrically connected.

3. Device type number is for reference only. The
   number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals
   Green Text Denotes - Extra Notes to be considered.

5. Interpret diagram in accordance with American
   National Standards Institute specifications,
   current revision, with the exception of
   logic block symbology.

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| Drawn by: Utkarsh G. | Page Title: Revision History | | |
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| | Date: Friday, October 17, 2014 | Sheet 6 of 6 | |