4 Requirements for Power Management

4.1 Voltage domains

The Vybrid device has multiple voltage domains that need to be supplied with different and properly sequenced voltages. Table 24 provides this information for the 364-ball BGA case; in the 176-lead LQFP one, the irrelevant domains should be ignored.

Table 24 Power sequencing

Vybrid power domain	Board-level power source	Power-up order
VDD33_LDOIN	VDD33	1
VDDREG		
VDD33		
VDDA33_ADC	VDDA33_ADC	
VREFH_ADC	VREFH_ADC	
VDDA33_AFE	VDDA33_AFE	
VDD12_AFE	VDD12_AFE	2
VDD	VDD	
USB0_VBUS	USB0_VBUS	Don't care
USB1_VBUS	USB1_VBUS	
VBAT	VBAT	
SDRAMC_VDD1P5	SDRAMC_VDD1P5 *	

* If used for the processor core power, see additional board-level timing requirement in section 4.2.

NOTE

There are no sequencing restrictions among supply pins with the same "Power-Up Order" number.

NOTE

If no DDR used, the SDRAMC_VDD1P5 pins may be left floating.

NOTE

The power-down order is opposite to the power-up one.

Advantageous is that Vybrid has been designed to use a single 3.3 V power source (VDD33 from Table 24), the rest of the device domains being powered from its fully controlled built-in linear regulators.

4.2 Processor core power

The flipside of the purely linear approach is quite low voltage-conversion efficiency. E.g., it causes significant heat dissipation on the linear regulator serving the power-hungriest processor core (VDD) domain, especially at high current values. Due to that, an external ballast NPN transistor is used in this regulator, whose simplified topology is shown in Figure 1-1-1-1-1-1-1-1-30.

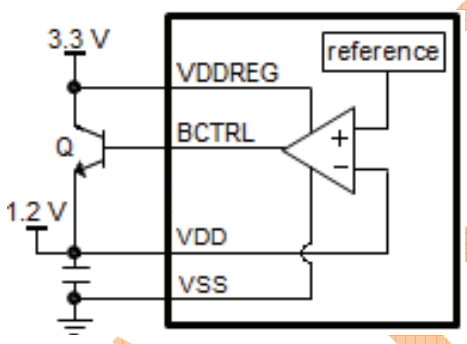

Figure 1-1-1-1-1-1-1-1-30 Simplified topology of VDD voltage regulator

To decrease heat dissipation (thus improving the voltage-conversion efficiency), the transistor collector may be powered from a source lower than 3.3 V, e.g. 1.5 V available in the system configuration using a DDR3 memory device. The only timing requirement in this core-powering scheme is that the transistor collector voltage shall appear no later than signal on its base connected to Vybrid BCTRL (base-control) pin, otherwise its output current exceeds the maximum value of 20 mA. The most reliable way to meet this new requirement is to turn on 1.5 V on the board prior to 3.3 V, which alters the single-rail Vybrid power sequencing shown in Table 24.

Refer to the AN4807 "Vybrid Power Consumption and Options" Application Note for details.

The Vybrid reference designs offer both 1.5 V and 3.3 V options (see Figure 1-1-1-1-1-1-1-1-31).

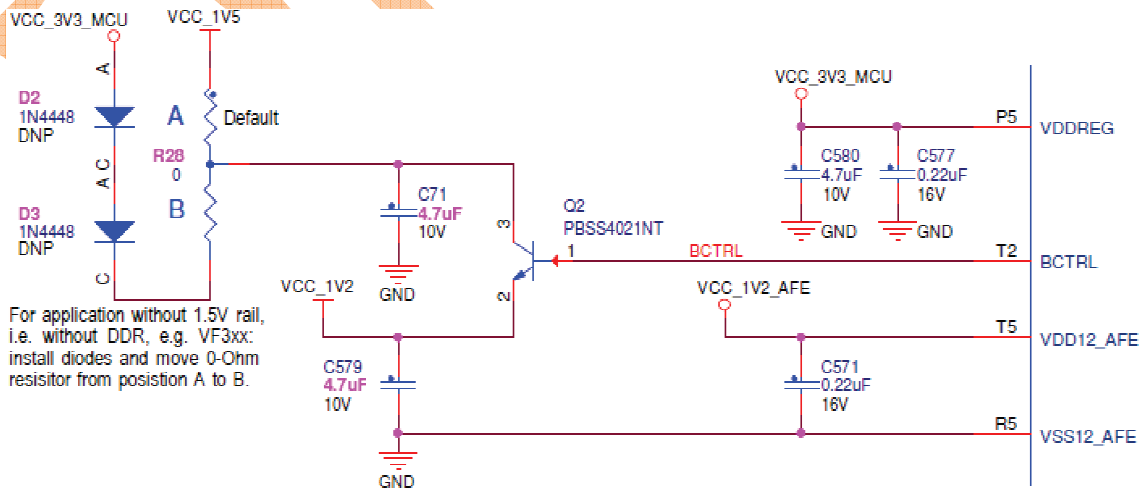

Figure 1-1-1-1-1-1-1-1-31 VDD voltage regulator in reference design

4.2.1 Transistor type selection

The Vybrid data sheet requirements for proper ballast NPN transistor type selection are applicable to the collector voltage down to 1.8 V.

If lower value used, e.g. 1.5 V, the following method, based on the transistor operation theory (and using its terminology), shall be applied while selecting the transistor type:

- For the application of interest, with its known operating temperature range and highest Ic, select a transistor candidate with a linear-region Hfe of 100…150 (quite common for inexpensive NPN transistors nowadays) or higher,
- With high Ic, Ib is usually quite high and drives Vbe up to 1V or even higher; with Vce of 0.3 V (i.e. Vc of 1.5 V), the transistor operates in the saturation region, i.e. the base-collector junction is forward-biased and "steels" part of Ib, so that Hfe degrades (this is why a relatively high linear-region Hfe is required),
- Based on Ic and Hfe (from the transistor data sheet for this Ic value), Ib is calculated,
- Based on Ib and the transistor data sheet, Vbe is defined,
- Based on Vbe and the transistor data sheet, the lowest possible Vce is defined, which in turn defines the lowest possible Vc,
- Based on Ic and Vce, the heat dissipation is calculated and checked against the transistor data sheet.

Applying this method is easier with a higher linear-region Hfe for the below reasons:

- It guarantees lower Ib ==> lower Vbe ==> less deep saturation ==> lower Hfe degradation,
- Even with degraded Hfe, Ib does not exceed 20mA (the maximum Vybrid BCTRL output current).

If a specific transistor candidate appears to have a sufficient Vce margin, it is possible to:

- Keep Vc and try a transistor candidate with lower linear-region Hfe, usually less expensive,
- Keep Hfe and lower Vc, which in turn:

Decreases heat dissipation,

Saves power,

Improves voltage-conversion efficiency,

Allows switching to a smaller transistor case, less expensive and occupying less space of the board.

NOTE

Even for the above-mentioned Vc of 1.8V, the collector-base junction is already somewhat forward-biased, but the Ib-"stealing" effect is still negligible.

4.3 Analog power rails

Each of the 4 analog rails, VDD12_AFE, VCC_3V3_AFE, VCC_3V3_ADC, and VREF_3V3, has 2 powering options (see Figure 1-1-1-1-1-1-1-1-32):

- The cost-efficient one (default in our reference designs) - through a filtering ferrite bead from the relevant main power rail,
- The more expensive one when high-quality AFE, ADC, and DAC performance required - from a dedicated linear voltage regulator.

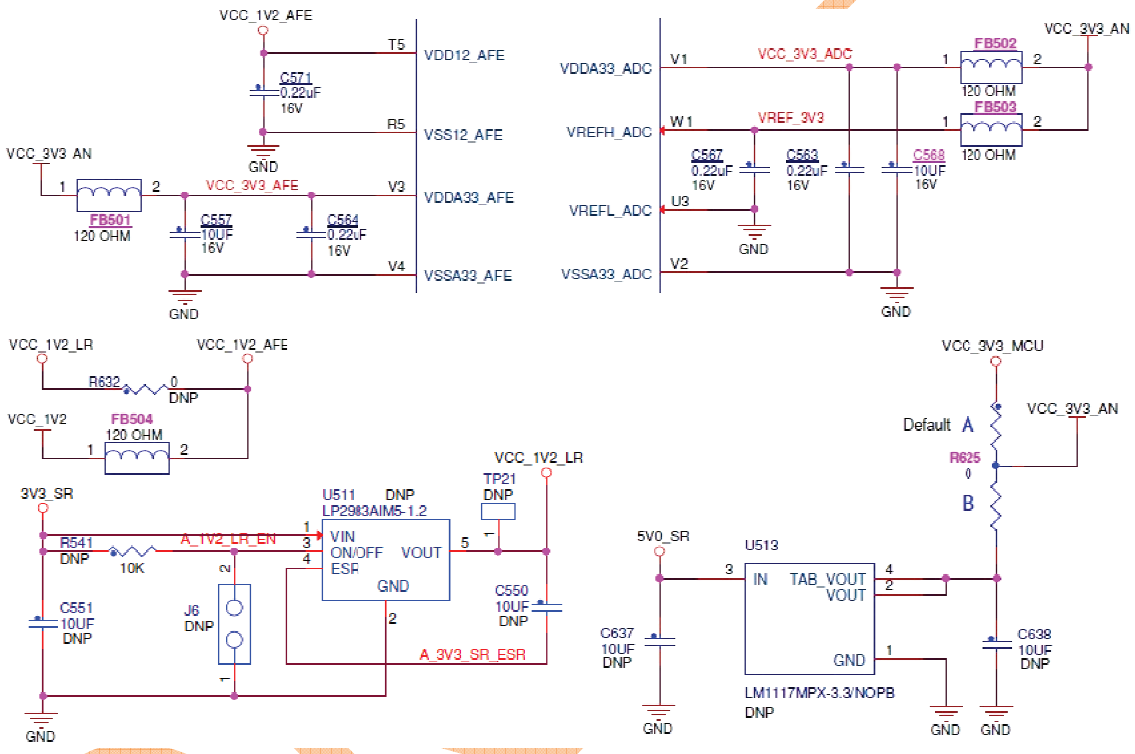

Figure 1-1-1-1-1-1-1-1-32 Powering options for analog power rails

4.3.1 AFE block power consumption

While selecting linear voltage regulator types for the scheme shown in Figure 1-1-1-1-1-1-1-1-32, the worst-case data (fast silicon and maximum voltage values) shall be used:

- VCC_3V3_AFE @ 3.6V - 41mA,
- VDD12_AFE @ 1.3V - 14mA.

Based on the above, the overall worst-case power consumption of the entire AFE block approximately equals 150mW (vs. 110mW typical @ nominal '3.3V' and '1.2V' rails' values).

5 Root Clocks

Clock connectivity is described in the “High Level Clocking Diagram” section in the “Clocking Overview” chapter of the processor reference manual. This section contains a series of tables that describe the clock inputs of each module and which clock is connected to it.