TWR-VF65GS10 Tower Module

User's Manual

Rev. 1.1

Freescale Semiconductor Inc.

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1 TWR-VF65GS10 Overview

The TWR-VF65GS10 is a development board featuring the heterogeneous dual core Vybrid VF6xx family. It consists of a 500MHz 32-bit ARM® Cortex™-A5 + 167MHz ARM® Cortex™-M4 MPU that operates across the full -40C to 85C temperature range.

The TWR-VF65GS10 is a Tower Controller Module compatible with the Freescale Tower System. It can function as a stand-alone, low-cost platform for the evaluation of the Vybrid family of devices. The TWR-VF65GS10 features a Vybrid VF6xx family MPU based on ARM® Cortex™-A5 and ARM® Cortex™-M4 architecture with dual TFT display, dual USB OTG with built in HS/FS/LS PHY, dual 10/100 Ethernet with L2 switch, and advanced security.

The TWR-VF65GS10 is available as a stand-alone product, or can be obtained as part of a kit (TWR-VF65GS10-KIT, TWR-VF65GS10-DS5, TWR-VF65GS10-PRO). The kit includes the Tower Elevator Modules (TWR-ELEV), the Tower Serial Module (TWR-SER) or Tower Serial2 Module (TWR-SER2), and/or Tower LCD Display (TWR-LCD-RGB). The TWR-VF65GS10 can also be combined with other Freescale Tower peripheral modules to create development platforms for a wide variety of applications. Please visit www.freescale.com/tower for an overview of the Freescale Tower System.

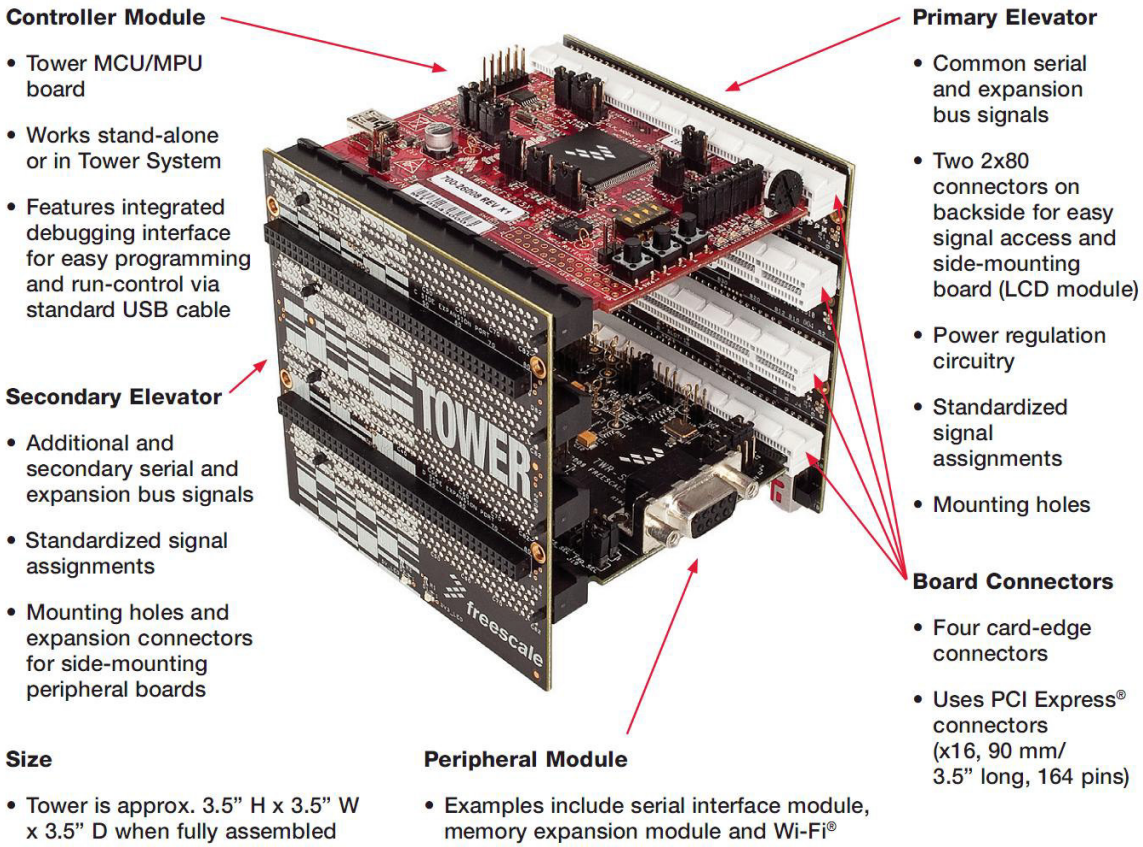


Figure 1: Freescale Tower System Overview

1.1 Contents

The available TWR-VF65GS10 kits are detailed below.

The **TWR-VF65GS10** contents include:

- TWR-VF65GS10 MPU module
- Dual headed USB cable
- Printed insert containing DS-5 license and links for software tools.
- Quick Start Guide

The **TWR-VF65GS10-KIT** contents include:

- TWR-VF65GS10 MPU module
- TWR-ELEV – Primary and Secondary Elevator Modules
- TWR-SER – Serial module including USB host/device/OTG, Ethernet, CAN, RS232 and RS485
- Dual headed USB cable
- Printed insert containing DS-5 license and links for software tools.
- Quick Start Guide

The **TWR-VF65GS10-DS5** contents include:

- TWR-VF65GS10 MPU module
- TWR-ELEV – Primary and Secondary Elevator Modules
- TWR-SER2 – Serial module including USB host/device, Dual Ethernet, CAN, RS232 and RS485
- TWR-LCD-RGB display
- Dual headed USB cable
- Printed insert containing DS-5 license and links for software tools.
- Quick Start Guide

The **TWR-VF65GS10-PRO** contents include:

- TWR-VF65GS10 MPU module
- TWR-ELEV – Primary and Secondary Elevator Modules
- TWR-SER2 – Serial module including USB host/device, Dual Ethernet, CAN, RS232 and RS485
- TWR-LCD-RGB display
- Dual headed USB cable
- Printed insert containing DS-5 license and links for software tools.
- Quick Start Guide

1.2 Tower Features

Figure 2 and Figure 3 show the TWR-VF65GS10 with some its key features called out. The following list summarizes the features of the TWR-VF65GS10 Tower Module:

- Vybrid VF61NS151CMK50 Controller (Dual Core ARM Cortex A5 @ 500 MHz + ARM Cortex M4 @167 MHz, 1.0 MB SRAM, Dual Ethernet, Dual USB, Advanced Security)
- Kinetis K20DX128VFM5 based OpenSDA circuit
- 1Gb x 16 (128 MB) DDR3 in 96 FBGA package (Samsung)
- 2Gb x 16 (256 MB) NAND flash (Micron)
- Two 128 Mb (16MB) Quad-I/O Serial Flash (Spansion)
- Dual USB with on-chip PHY
- Interfaces to TWR-LCD-RGB board
- Four user-controlled status LEDs
- Two mechanical push buttons for user input, and one for reset
- Potentiometer and MMA8451Q three-axis digital accelerometer
- Micro SD Card slot
- Independent battery-operated power supply for real-time clock and tamper detection modules

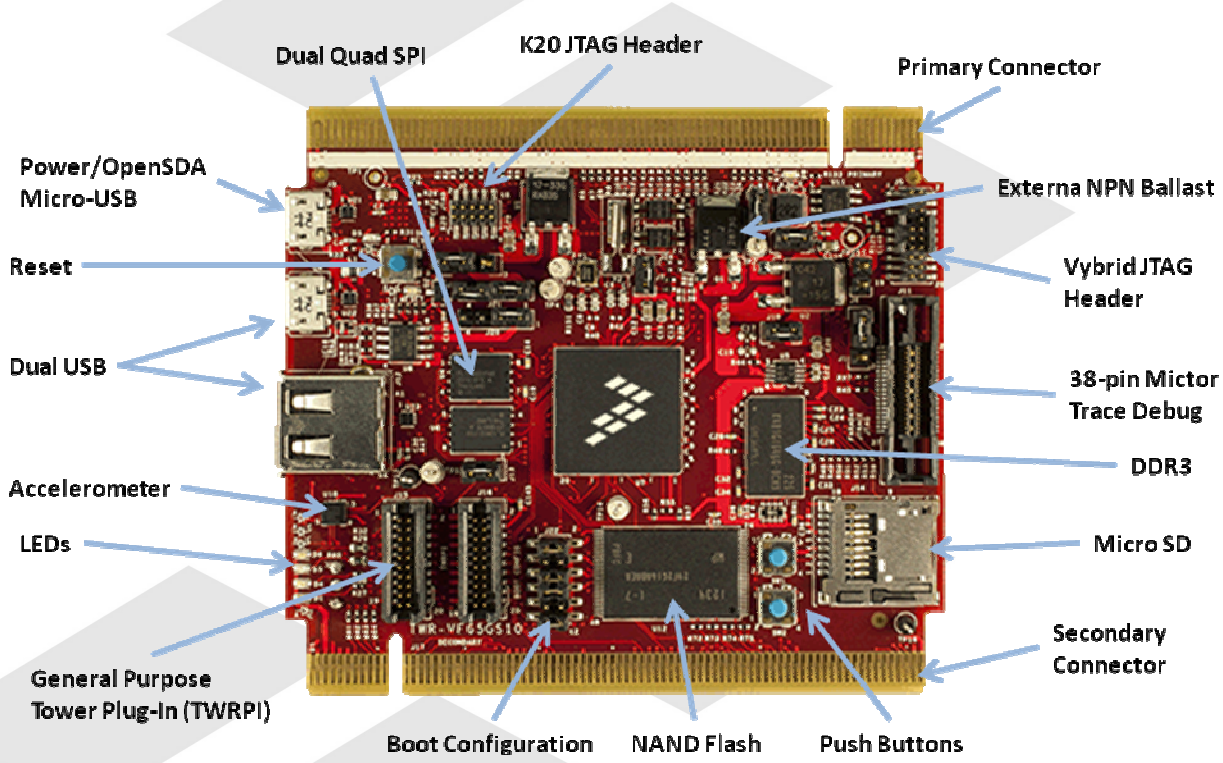


Figure 2: Front side of TWR-VF65GS10

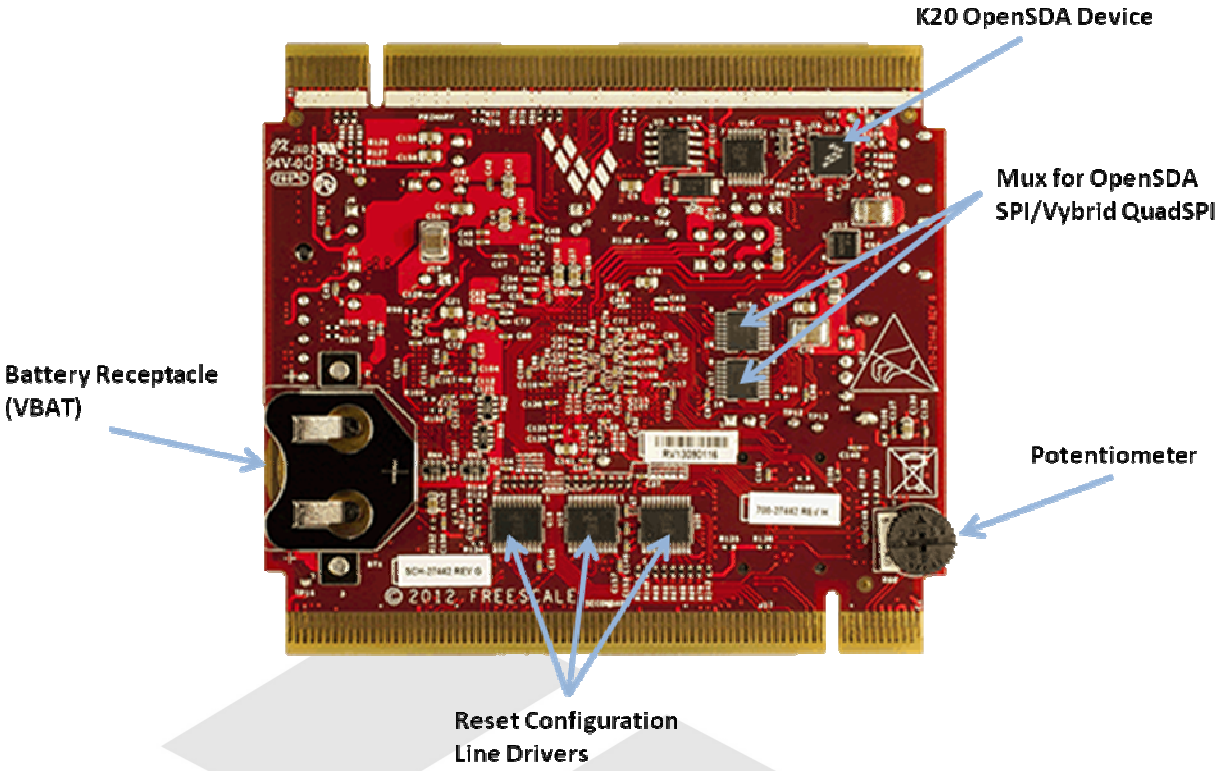


Figure 3: Back side of TWR-VF65GS10

1.3 Getting Started

Follow the Quick Start Guide found printed in the TWR-VF65GS10 for the list of recommended steps for getting started. There are also lab walk-through guides available on the tool support page for the TWR-VF65GS10: http://www.freescale.com/TWR-VF65GS10.

1.4 Reference Documents

The documents listed below should be referenced for more information on the Vybrid family, Tower System, and Peripheral Modules. These can be found in the documentation section of www.freescale.com/TWR-VF65GS10 or www.freescale.com/Vybrid.

- *TWR-VF65GS10-QSG: Quick Start Guide*
- *TWR- VF65GS10-SCH: Schematics*
- *TWR- VF65GS10-PWB: Design Package*
- *Vybrid Family Product Brief*
- *Vybrid Family Reference Manual*

2 Hardware Description

The TWR-VF65GS10 is a Tower Controller Module featuring the VF61NS151CMK50 dual core ARM Cortex-A5 + ARM Cortex-M4 microprocessor with dual TFT display, dual USB OTG with on-chip HS PHY and on-chip HS/FS/LS PHY, dual 10/100 Ethernet with on-chip L2 switch, advanced security, communication peripherals, advanced digital audio support, and tamper detect in a 364 BGA package. Maximum operating frequency of the CA5 core is 500 MHz and the CM4 core is 167 MHz. The module is intended for use in the Freescale Tower System but can operate stand-alone. An on-board circuit referred to as OpenSDA provides a JTAG debug interface and a power supply input through a single USB micro-B connector. Figure 4 shows a block diagram of the TWR-VF65GS10. The following sections describe the hardware in more detail.

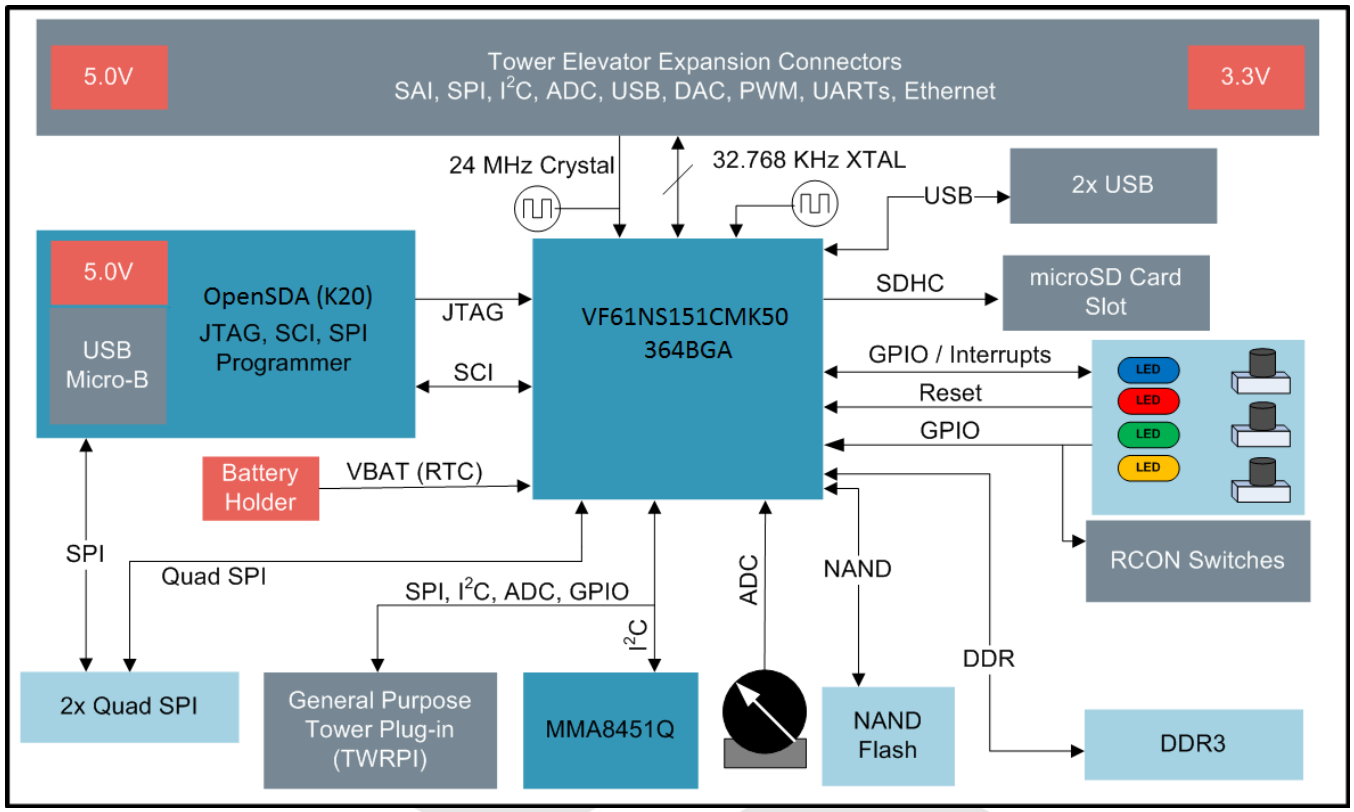


Figure 4: TWR-VF65GS10 Block Diagram

2.1 VF61NS151CMK50 Microprocessor

The VF61NS151CMK50 device highlights are listed below:

- ARM Cortex-A5 core @500MHz (1.57 DMIPS/MHz) with TrustZone with 32 KB ICache/32 KB D-Cache (L1) and 512 KB of L2 cache.

- NEON Media Processing Engine (MPE) co-processor and double precision Floating Point Unit (FPU)
- ARM Cortex-M4 @167 MHz with 16 KB I-Cache/16 KB D-Cache
- 1.0 MB on-chip SRAM, with ECC on 512 KB of the SRAM
- Support for LPDDR2/DDR3
- Dual TFT display up to WVGA
- Dual 10/100 Ethernet with on-chip L2 Switch
- Dual USB OTG with on-chip HS PHY and on-chip HS/FS/LS on-chip PHY
- NAND Flash Controller
- Power management including WAIT, STOP, LPRUN, ULPRUN, and LPSTOPx modes
- Advanced Security supporting Symmetric and Asymmetric key Cryptography with on-chip Tamper detection
- Rich set of communication peripherals and general purpose features
- Advanced digital audio support with multiple audio interfaces and hardware asynchronous sample-rate converter co-processor.
- Package options that include 176 LQFP and 364 BGA

2.2 Clocking

There are two external clock sources on the Vybrid Tower board. One is a 24 MHz XOSC, and the other is a 32.768 kHz XOSC.

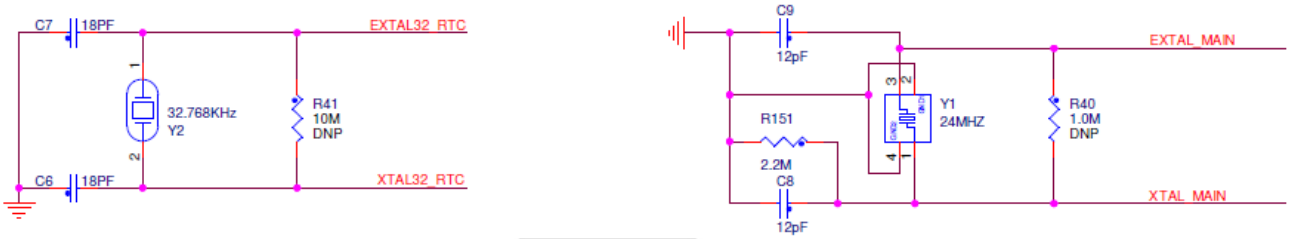
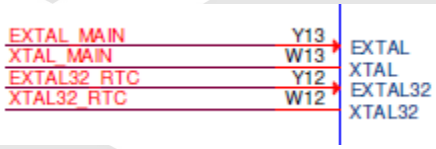


Figure 5: TWR-VF65GS10 External Clock Options

The 24 MHz XOSC connects to XTAL/EXTAL, and the 32 kHz XOSC connects to EXTAL32/XTAL32.



Internally to the Vybrid device, there is a 128 kHz internal reference clock (IRC), and a 24 MHz IRC. The 128 kHz IRC is divided by 4 by default, so it actually provides a 32 kHz clock source to the device. A high level clocking diagram of the Vybrid device is shown below for reference.

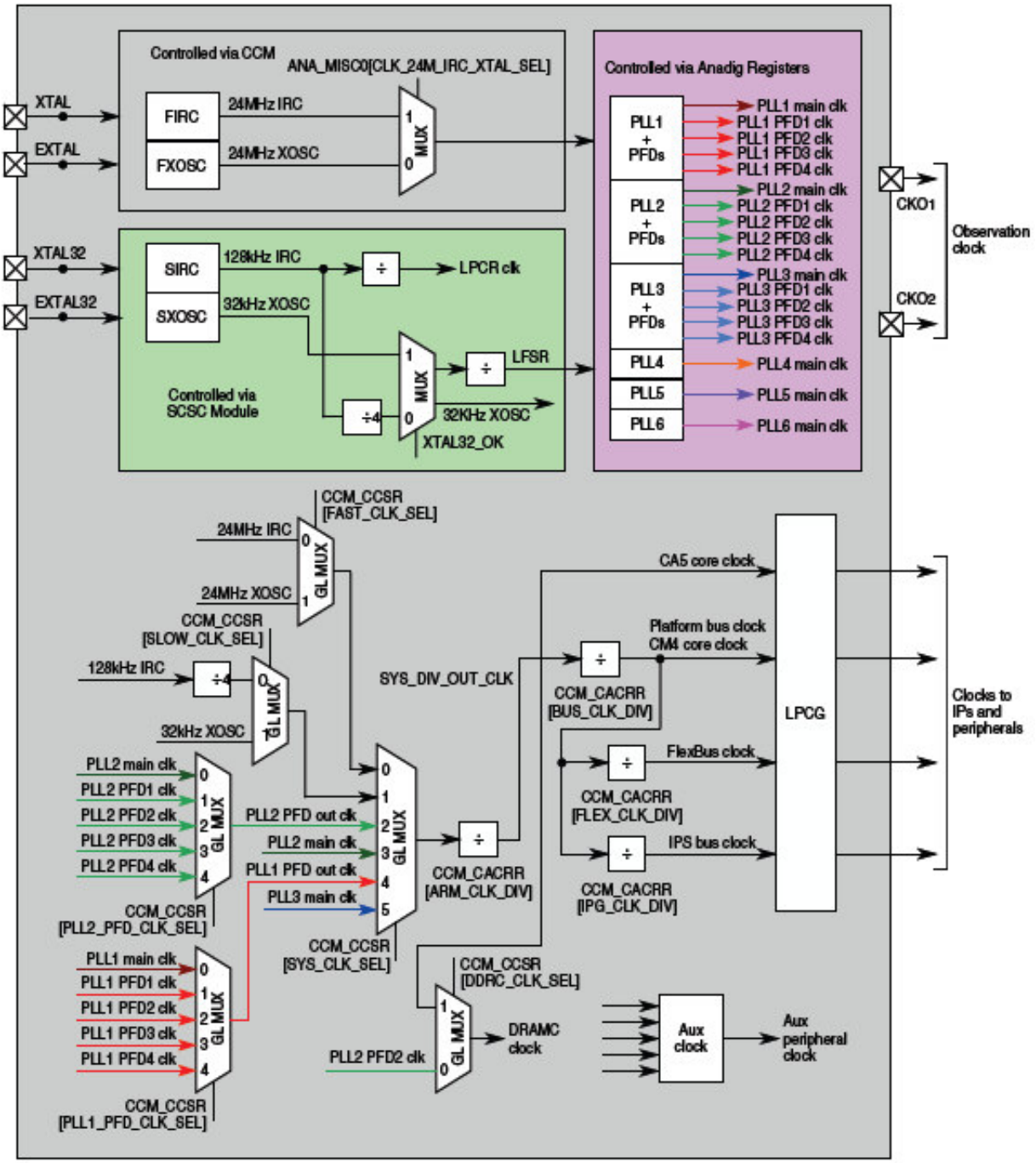


Figure 6: Vybrid Clocking Diagram

A PLL summary for the VF61NS151CMK50 device is as follows:

- PLL 1 – System PLL
- PLL 2 – PLL 528
- PLL 3 – USB0 PLL
- PLL 4 – Audio PLL
- PLL 5 – Ethernet PLL
- PLL 6 – Video PLL
- PLL 7 – USB1 PLL

For additional clocking details, please refer to the ANADIG and CCM chapters of the Vybrid Reference Manual.

2.3 System Power

In stand-alone operation, the main power source for the TWR-VF65GS10 module is derived from the 5.0V input from the USB micro-B connector, J3. A low-dropout regulator provides a 3.3V supply from the 5.0V input voltage. Refer to sheet 5 of the TWR-VF65GS10 schematics for more details.

When installed into a Tower System, the TWR-VF65GS10 can be powered from either an on-board source or from another source in the assembled Tower System. If both the on-board and off-board sources are available, the TWR-VF65GS10 will default to the off-board source.

The 3.3V power supplied to the device (P3V3) is routed through jumpers J18 and J4. TP2 is a test point that can be used to measure the main 3.3V input into the VF61NS151CMK50 device.

The core 1.2V system power is derived from a ballast transistor tied to 3.3V.

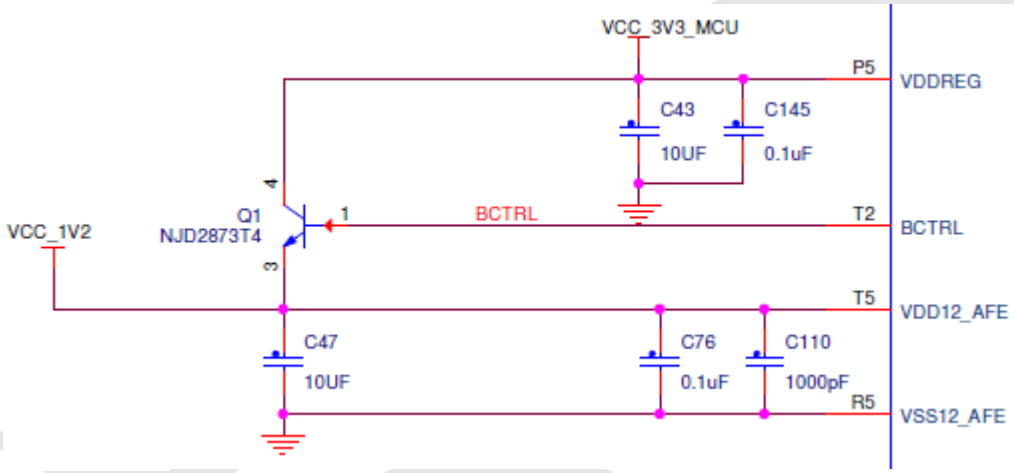


Figure 7: Core 1.2V VDD Power Configuration

The TWR-VF65GS10 board can also be powered from the TWR-ELEV USB connector. However, the TWR-ELEV should be rev F or later. Powering from the tower elevators may work with earlier revisions, but is not recommended.

2.3.1 SecureRTC VBAT

The Secure Real Time Clock (SecureRTC) module can be operational in the event there is an external power supply failure. The TWR-VF65GS10 provides a battery holder for a coin cell battery that can be used as the VBAT supply. Jumper J1 determines if VBAT is powered by the coin cell battery or the main board power. The holder can accept common 20mm diameter 3V lithium coin cell batteries (e.g. 2032, 2025). VBAT also powers the 32KHz XOSC, Tamper, and Monitors internal to the Vybrid device.

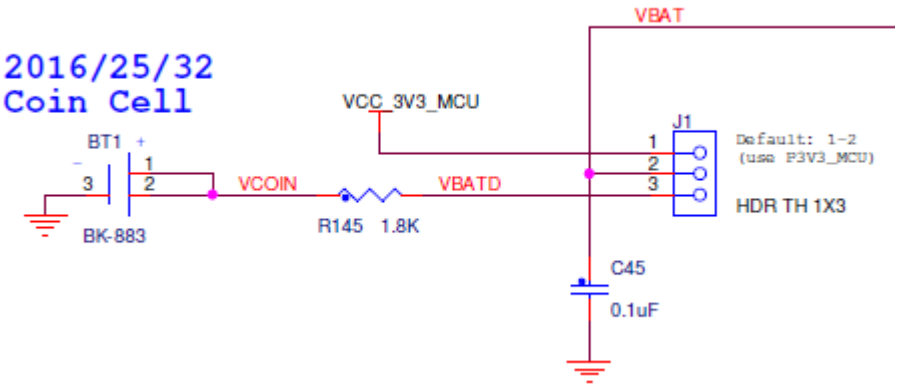


Figure 8: Coin Cell

2.4 Debug Interface

There are two physical debug ports on the TWR-VF65GS10 board, plus the OpenSDA Debug circuit. The OpenSDA circuit consists of a K20 controller connected to the micro-B USB (J3). The two physical debug ports consist of a 19-pin debug header (J5), and a 38-pin Mictor connector (J11) used for JTAG + Trace.

2.4.1 OpenSDA using CMSIS-DAP Firmware

The OpenSDA "circuit" consists of a K20 microcontroller and surrounding hardware to act as a bridge between the USB connector and the JTAG, SPI, and UART pins on the Vybrid device. The K20 firmware that ships with the Tower board is a mass storage bootloader with virtual serial port capability. This allows the demo program to output serial data through the USB from the primary (CA5) core over UART1. The CMSIS-DAP firmware (Cortex Microcontroller Software Interface Standard – Debug Access Port) allows a debug connection to be established through the micro-USB connector J3. To update the

firmware and start debugging with your TWR-VF65GS10, refer to the OpenSDA Readme document available at www.freescale.com/twr-vf65gs10.

2.4.2 Cortex JTAG Connector

Typical JTAG debugging can use the 19-pin Cortex-M debug header located at J5.

2.4.3 Cortex JTAG+Trace Connector

For more robust debugging, the 38-pin Mictor connector can be used. In addition to the normal JTAG debug pins (TDI, TDO, TMS, TCLK, RESET), several additional Trace pins are connected to the JTAG+Trace connector (J11), as shown below.

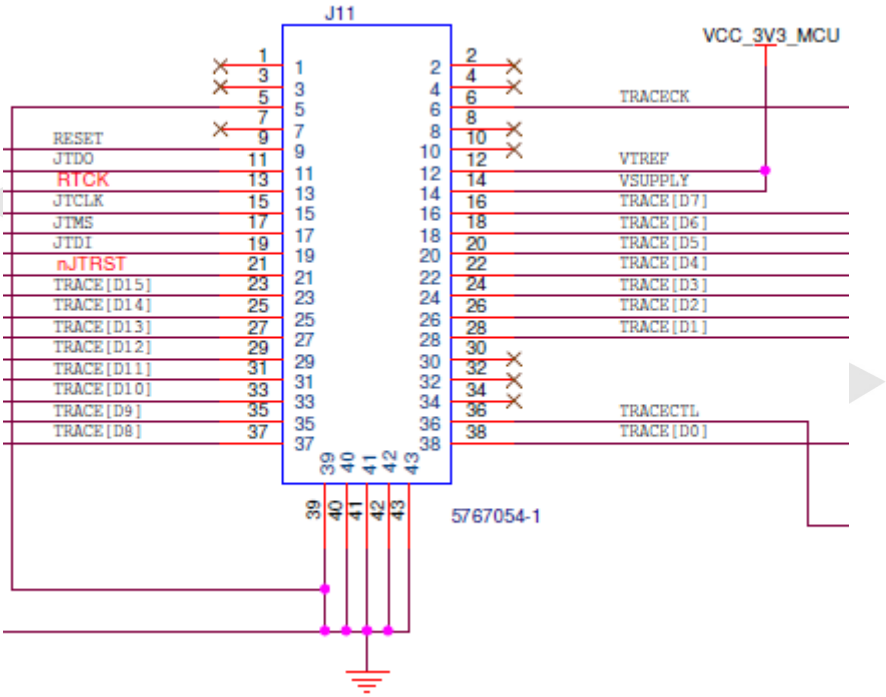


Figure 9: 38-Pin Mictor Connector

2.5 Graphical LCD Interface

The Vybrid controller includes dual on-chip Display Control Unit (DCU4) modules, DCU0 and DCU1. These can be used to drive graphical content to an TFT LCD screen, such as the TWR-LCD-RGB. On the Tower design, the DCU0 pins are connected to the Secondary elevator for this purpose. These pins include DCU0_B0-DCU0_B7, DCU0_R0-DCU_R7, DCU_G0-DCU_G7, DCU0_HSYNC, DCU0_VSYNC, and

DCU0_PCLK. The secondary DCU (DCU1) is not supported on the TWR-VF65GS10 board. Also, the original TWR-LCD, which mounts to the primary side of the elevator, cannot be used with the TWR-VF65GS10 board.

2.6 DDR3/LPDDR2 Memory

The TWR-VF65GS10 contains 1Gb (128 MB) Samsung DDR3 Memory (K4B1G1646G-BCH9). The TWR-VF65GS10 board also features individual 1.5V and 0.75V supplies for DDR3 power and termination, respectively (U2 & U5).

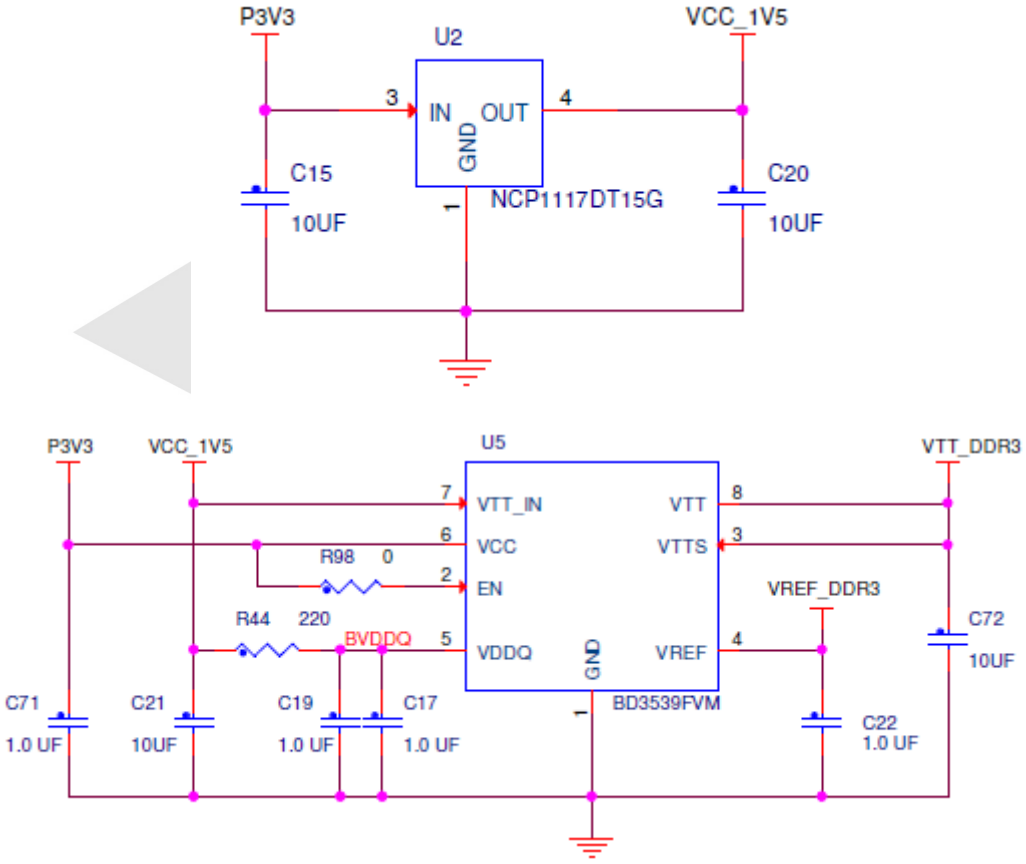


Figure 8: Vybrid DDR3 Power Supplies

2.7 NAND Flash

The TWR-VF65GS10 includes 2Gb (256MB) of SLC NAND Flash memory (Micron 29F2G16ABAEA). The data lines used for the NAND flash are shared between the NAND flash controller and the FlexBus interface. On the TWR-VF65GS10 hardware, these are dedicated specifically to NAND since there is

no mechanism to dynamically switch between the two interfaces. NAND flash does not have execute in place (XiP) capabilities, but is supported as a boot device by the internal BootROM. For more information, please refer to the Vybrid Reference manual.

2.8 QuadSPI Memory

The TWR-VF65GS10 also includes dual QuadSPI memory with execute in place (XiP) capability. The on-board QuadSPI used is Spansion FL128S, which are each 128 Mb (16MB) in size. The QuadSPI interface offers up to 104 MHz performance for Single Data Rate (SDR) and up to 80 MHz for Dual Data Rate (DDR). Parallel QuadSPI modules operating in DDR mode can achieve up to 160 MByte per second peak bandwidth. The QuadSPI can be used as a boot device by the internal Boot ROM.

2.9 Accelerometer

An MMA8451Q digital accelerometer is connected to the Vybrid device through an I2C interface and a GPIO/IRQ signal. The I2C address is 0x1C. Refer to the Vybrid TWR-VF65GS10 Schematic for connection details.

2.10 Potentiometer, Pushbuttons, LEDs

The TWR-VF65GS10 features two pushbutton switches connected to GPIO/interrupt signals, one pushbutton connected to the master reset signal, four user-controllable LEDs, and a potentiometer connected to an ADC input signal. The pushbutton labeled SW1 is connected to PTB16 which can be used as a wakeup source from low power modes. Additional connectivity detail can be referenced in the TWR-VF65GS10 Schematic.

2.11 General Purpose Tower Plug-in (TWRPI) Socket

The TWR-VF65GS10 features a socket (J15 & J16) that can accept a variety of different Tower Plug-In (TWRPI) modules featuring sensors, RF transceivers, and more. The General Purpose TWRPI socket provides access to I2C, SPI, IRQs, GPIOs, timers, analog conversion signals, TWRPI ID signals, reset, and voltage supplies. The pin out for the TWRPI Socket is defined in Table 1.

Table 1: TWRPI Connectivity

Pin	Description (J15)		Pin	Description (J16)
1	GND		1	5.0V
2	GND		2	3.3V
3	I2C0_SCL		3	GND
4	I2C0_SDA		4	3.3V
5	GND		5	GND

6	GND		6	GND
7	GND		7	GND
8	GND		8	ADC0 Input
9	DSPI0_SIN		9	ADC1 Input
10	DSPI0_SOUT		10	GND
11	DSPI0_CS1		11	GND
12	DSPI0_SCK		12	ADC2 Input
13	GND		13	GND
14	GND		14	GND
15	GPIO0/IRQ		15	GND
16	GPIO1		16	GND
17	GPIO2		17	ID0
18	GPIO3		18	ID1
19	GPIO4		19	GND
20	N/C		20	RESET_B

2.12 Ethernet

The VF61NS151CMK50 features dual 10/100 Mbps Ethernet MACs with 1588 capability, L2 Switch, and support for MII and RMII interfaces. The TWR-VF65GS10 routes the RMII signals to both the primary and secondary sides of the Elevator.

The TWR-VF65GS10 maintains compatibility with both the TWR-SER (single Ethernet) and TWR-SER2 (dual Ethernet) peripheral modules. Each should be configured for RMII mode as shown in the following table.

Table 2: Serial Card Configuration for RMII mode

TWR-SER - RMII Mode	
Jumper	Setting
J2	3-4
J3	2-3
J12	9-10

TWR-SER2 - RMII Mode (1=ON)	
Switch	Setting
SW1 - PHY A	[1:8] = 11000000
SW2 - PHY B	[1:8] = 10100000

2.13 Dual USB

The VF61NS151CMK50 has dual USB OTG with on-chip HS/FS/LS PHYs. Since both the TWR-SER and TWR-SER2 boards have on-board PHY, the USB pins are not routed to the Tower Elevators. They are

available however, on the TWR-VF65GS10 board. USB0 is available on the Micro-B connector J8, and USB1 is available on the USB-A connector J12.

2.14 SD Digital Card Slot

A micro Secure Digital (SD) card slot is available on the TWR-VF65GS10 connected to the SD Host Controller (SDHC1) signals of the VF6xx part. This slot will accept micro-SD memory cards. There are two SDHC modules on the VF61 device (SDHC0 & SDHC1). Because some pins from SDHC0 device are used for NAND Flash and Ethernet, SDHC1 module is used for the card slot. Refer to Table 4 "I/O Connections and Pin Usage Table" for the SDHC signal connection details. The SDHC can be used as a boot device by the internal Boot ROM.

2.15 External Bus Interface – FlexBus

Since the NAND device pins are muxed with the FlexBus pins, and there is on-board NAND Flash on the TWR-VF65GS10 board, the Flexbus pins are not routed to the Tower Elevator and are not available for any custom connections.

3 Jumper Table

The following table shows the available jumper options on the TWR-VF65GS10 board. The default jumper settings are shown in **bold**.

Table 3: TWR-VF65GS10 Jumper Table

Jumper	Option	Setting	Description
J1	VBAT Power Source . SecureRTC, 32kHz XOSC, Tamper, and Monitors	**1-2** 2-3	**VBAT tied to main 3.3 V (VCC_3V3_MCU)** VBAT tied to Coin Cell
J4	MCU 3.3 V Supply	**ON** OFF	**VDD33 Power to the MCU (P3V3 tied to VDD33 of device)** VDD33 Power to the MCU disconnected
J6	JTAG 5V selection	**OFF** ON	**Pin 11 & 13 of JTAG connector floating** Pin 11 & 13 of JTAG connecter tied to 5V
J7	Tamper Loopback	**ON** OFF	**EXT_WM0_TAMPER_IN tied to EXT_WM0_TAMPER_OUT** EXT_WM0_TAMPER_IN open; EXT_WM0_TAMPER_OUT open

J13	Accelerometer Interrupt	**ON** OFF	**Connect MCU PTB9 pin to INT1 of MMA8451Q accelerometer** No accelerometer interrupt connection
J18	Main board 3.3 V filtered supply derived from 5.0 V supply	**ON** OFF	**Connect 3.3V regulator output to P3V3** Disconnect P3V3 from regulator output
J19	Elevator 5V Supply	**1-2** 2-3	**P5V_ELEV tied to Elevator sense** P5V_ELEV tied to USB0_VBUS
J20	USB0 VBUS	**1-2 only** 2-3 only 1-2 & 3-4	**Device, Self powered** Device, BUS powered Host
J21	USB1 VBUS	**1-2 & 3-4** 1-2 only 2-3 only	**Host** Device, Self Powered Device, Bus Powered
J22	Boot Configuration **ON/INSTALLED-1**, OFF-0 **2 4 6 8 10 12** **1 3 5 7 9 11**	12_345 00_xxx 10_000 **10_110** 10_001 01_xxx	Switch Settings Detail Boot From Fuses QuadSPI Boot **SD Card Boot** NAND Boot UART/USB Boot
J23	SCI1_TX and SCI2_TX select	1-2 **1-3** **2-4** 3-4	SCI1_TX connected to ELEV_UART1_TX **SCI1_TX connected to OpenSDA_UART_RX** **SCI2_TX connected to ELEV_UART1_TX** SCI2_TX connected to OpenSDA_UART_RX
J24	SCI1_RX and SCI2_RX select	1-2 **1-3** **2-4** 3-4	SCI1_RX connected to ELEV_UART1_RX **SCI1_RX connected to OpenSDA_UART_TX** **SCI2_RX connected to ELEV_UART1_RX** SCI2_RX connected to OpenSDA_UART_TX
S1 – SW6	USB0 Mux Selection	0 **1**	USB0 connected to Tower elevator USB0 connected to on-board micro-B USB connector (J8)

4 Input/Output Connections and Pin Usage Table

The table below provides details on which pins are used for LEDs, switches, and other I/O interfaces onboard the TWR-VF65GS10.

Table 4: I/O Connections and Pin Usage Table

Feature	Connection	Port Pin	Pin Function
OpenSDA USB-to-serial Bridge (J3)	OpenSDA Bridge RX Data	PTB4	SCI1 TX
	OpenSDA Bridge TX Data	PTB5	SCI1 RX
TWR-ELEV serial	Elevator TX Data	PTB6	SCI2 TX
	Elevator RX Data	PTB7	SCI2 RX
SD Card Slot (J14)	SD Clock	PTA24	SDHC1_DCLK
	SD Command	PTA25	SDHC1_CMD
	SD Data0	PTA26	SDHC1_DAT0
	SD Data1	PTA27	SDHC1_DAT1
	SD Data2	PTA28	SDHC1_DAT2
	SD Data3	PTA29	SDHC1_DAT3
	SD Card Detect	PTA7	SDHC1_SW
Pushbuttons	SW1	PTB16	PTB16/Low Power Wakeup
	SW2	PTB17	PTB17
	SW3	RESET_B	RESET_B
LEDs	D1 / Blue LED	PTB0	PTB0
	D3 / Yellow LED	PTB1	PTB1
	D4 / Yellow/Green LED	PTB2	PTB2
	D6 / Orange/Red LED	PTB3	PTB3
	D7	RESET_B	RESET_B
Potentiometer (R60)	ADC Input	PTC30	ADC0SE5
Accelerometer (U10)	Accelerometer Clock	PTB14	I2C0_SCL
	Accelerometer Data	PTB15	I2C0_SDA
	Accelerometer Interrupt	PTB9	GPIO
General Purpose TWRPI Socket (J15)	TWRPI I2C0_SCL	PTB14	PTB14
	TWRPI I2C0_SDA	PTB15	PTB15
	TWRPI DSPI0_SIN	PTB20	PTB20
	TWRPI DSPI0_SOUT	PTB21	PTB21
	TWRPI DSPI0_CS1	PTB18	PTB18
	TWRPI DSPI0_SCK	PTB22	PTB22
	TWRPI GPIO0/IRQ	PTB10	PTB10
	TWRPI GPIO1	PTA20	PTA20
	TWRPI GPIO2	PTB7	PTB7
	TWRPI GPIO3	PTB6	PTB6
	TWRPI GPIO4	PTB8	PTB8
General Purpose TWRPI Socket (J16)	TWRPI ADC0 Input	ADC1SE9	ADC1SE9
	TWRPI ADC1 Input	PTC31	ADC1SE5

	TWRPI ADC2 Input	ADC1SE8	ADC1SE8
	TWRPI RESET_B	RESET_B	RESET_B
USB0 (J8) Micro-B	USB0 VBUS	USB0_VBUS	USB0_VBUS
	USB0 D-	CON_USB0_DN	CON_USB0_DN
	USB0 D+	CON_USB0_DP	CON_USB0_DP
USB1 (J12) USB-A	USB1 ATYPE_USB_VBUS	USB1_VBUS	USB1_VBUS
	USB1 D-	USB1_DN	USB1_DN
	USB1 D+	USB1_DP	USB1_DP
Boot Configuration	Boot Jumper 1	PTE0	BOOTMOD1
	Boot Jumper 3	PTE1	BOOTMOD0
	Boot Jumper 5	PTE12	RCON5 / DCU0
	Boot Jumper 7	PTE15	RCON6 / DCU0
	Boot Jumper 9	PTE16	RCON7 / DCU0
NAND Flash	NAND Flash Data	PTD16 - PTD31	NF_D[0] - NF_D[15]
	NAND Flash Write Enable	PTB24	NF_WE_b
	NAND Flash Chip Enable 0	PTB25	NF_CE0_b
	NAND Flash Chip Enable 1	PTB26	NF_CE1_b
	NAND Flash Read Enable	PTB27	NF_RE_b
	NAND Flash Read/Busy	PTC26	NF_RB_b
QuadSPI Flash	QuadSPI0 Data	PTD5	QSPI0_A_DATA0
	QuadSPI0 Data	PTD4	QSPI0_A_DATA1
	QuadSPI0 Data	PTD3	QSPI0_A_DATA2
	QuadSPI0 Data	PTD2	QSPI0_A_DATA3
	QuadSPI0 Chip Select	PTD1	QSPI0_A_CS0
	QuadSPI0 Clock	PTD0	QSPI0_A_SCK
	QuadSPI1 Data	PTD12	QSPI0_B_D0
	QuadSPI1 Data	PTD11	QSPI0_B_D1
	QuadSPI1 Data	PTD10	QSPI0_B_D2
	QuadSPI1 Data	PTD9	QSPI0_B_D3
	QuadSPI1 Chip Select	PTD8	QSPI0_B_CS0
	QuadSPI1 Clock	PTD7	QSPI0_B_SCK

5 Tower Elevator Connections

The TWR-VF65GS10 features two expansion card-edge connectors that interface to the Primary and Secondary Elevator boards in a Tower system. Please refer to the Vybrid TWR-VF65GS10 Schematics for detail on Tower board pin out connectivity.

6 Optional Low Power Configuration using DDR3

The Vybrid device has several low power options including WAIT, STOP, LPRUN, ULPRUN, LPSTOP1, LPSTOP2, and LPSTOP3. The LPSTOPx modes are the lowest power modes available. Upon entering any of the LPSTOPx modes, the I/O will not retain their state and certain parts of the device are shut down. If LPSTOPx mode is required while using DDR3, it is recommended to change the default configuration of the board. Namely:

1. Add 10k pull-up to DDR_RESET
2. Remove 47 Ohm termination resistor (R107) on DDR_CKE
3. Add 10k pull-down to DDR_CKE

The pull-up on DDR_RESET will prevent the DDR3 module from resetting (DDR_RESET is active low) when entering LPSTOPx mode on the Vybrid device. The pull-down on DDR_CKE will allow the DDR3 module to stay in self-refresh (low power) mode until it is released by the application software.