Vybrid DCUv4

Layers description registers handling

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External Use

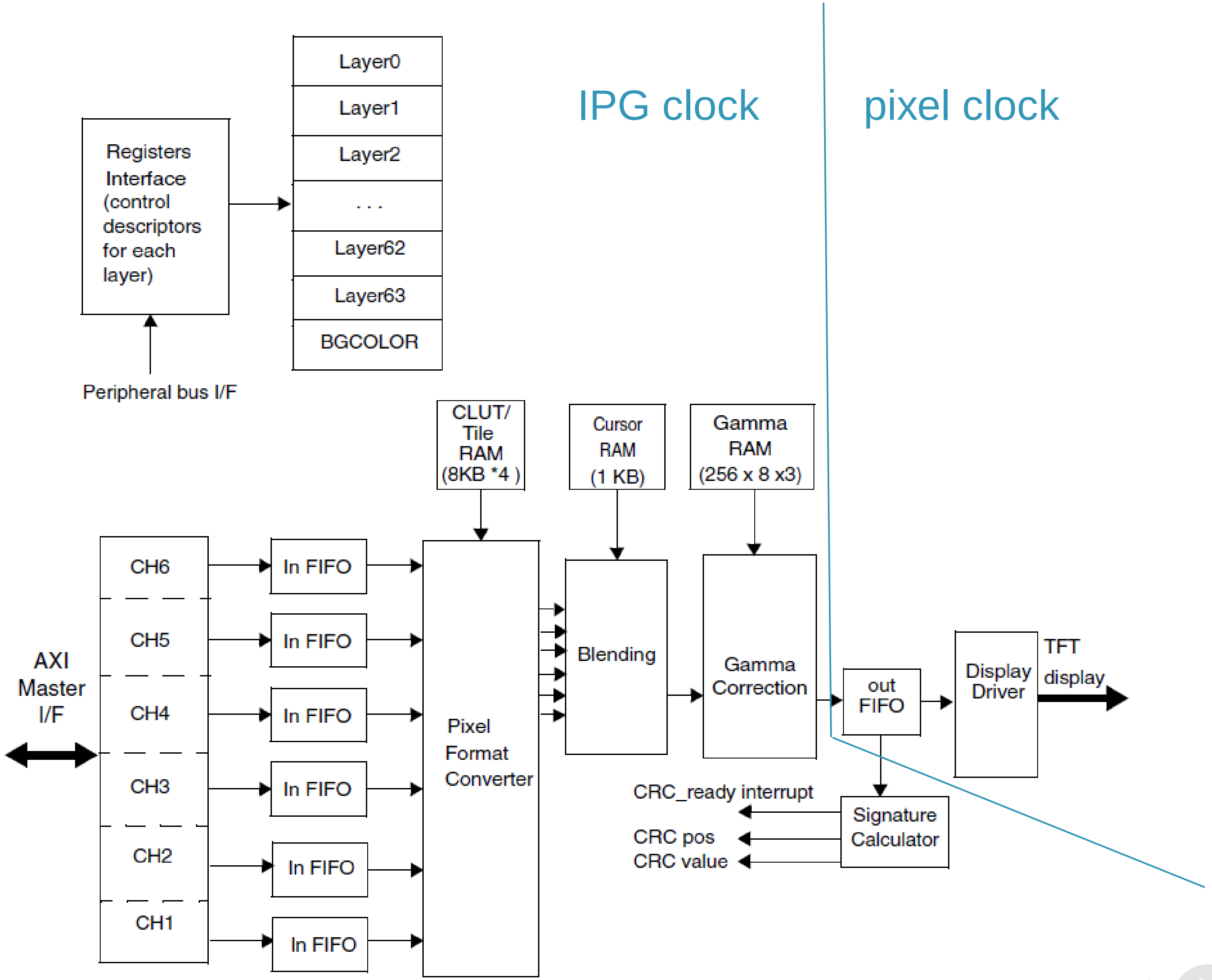
Agenda

- DCU structure
- Timing overview
- Transfer of DCU configuration
- Timing and interrupts
- Incorrect handling speculation
- Useful links

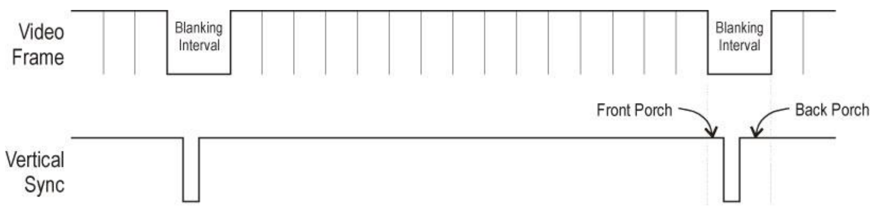
DCU structure

- Most of blocks works on IPG clock domain (precisely: DCU clock domain which is synchronous to IPG clock) .
- The rate at which these datapath blocks processes the data is dependent on the pixel clock.

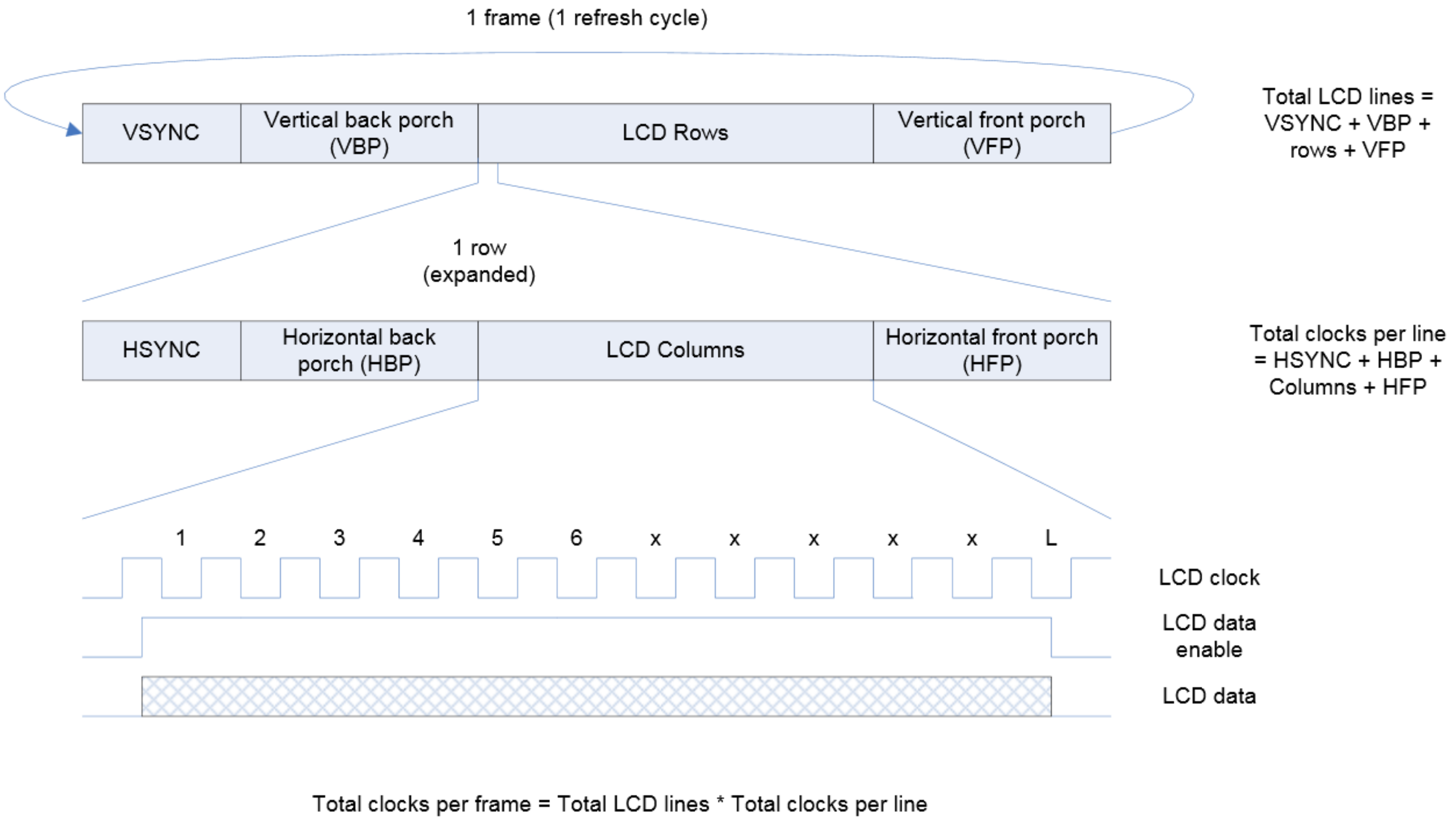
- **the user interface** through which the user configures the graphical content of the TFT LCD panel
  user control
  - IPG clock domain
- **functional blocks of the DCU4** that fetch the graphic and video content and drive the TFT LCD panel
  DCU control
  - IPG clock domain
  - pixel clock domain: Out FIFO, Display driver



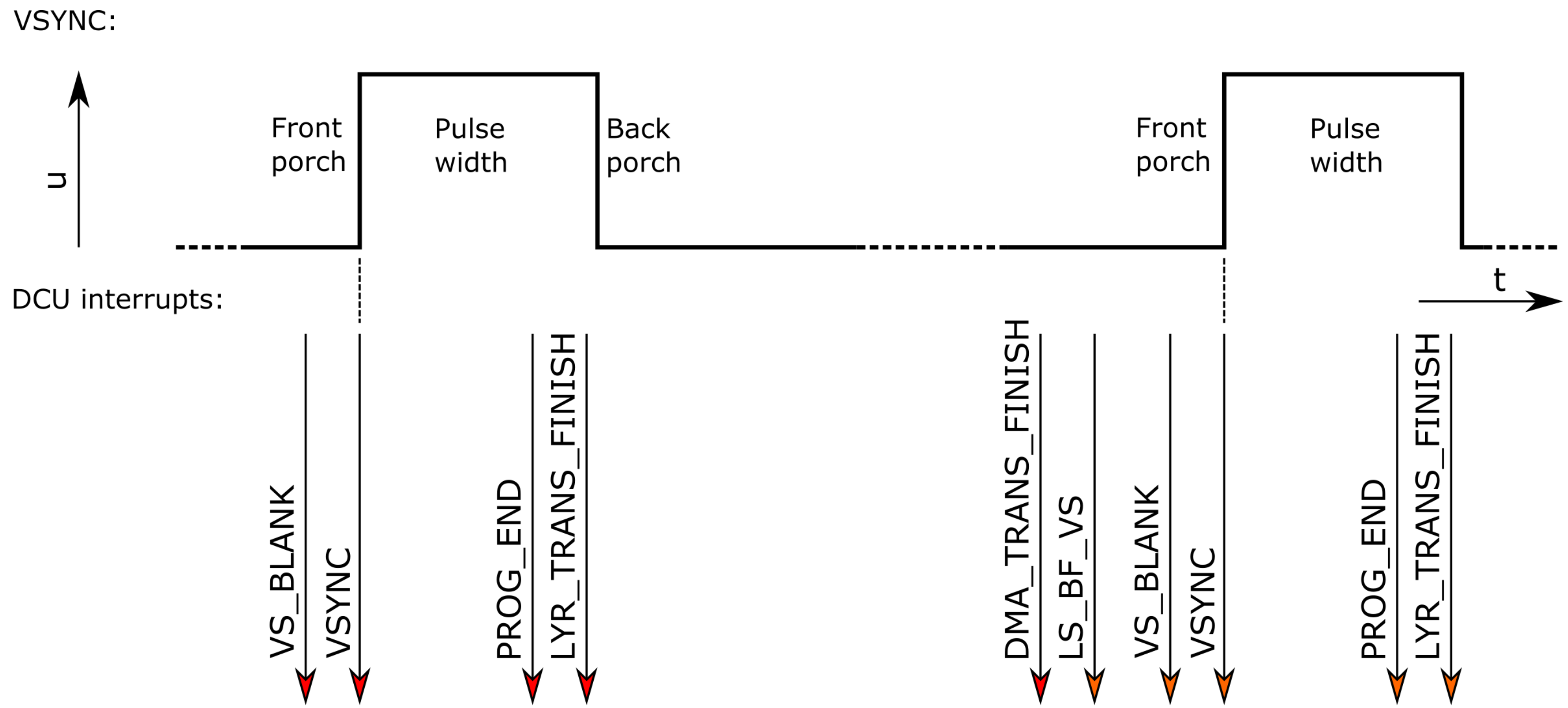
Timing overview



- Frame time = Display period + Blanking period
- Frame ~ Vsync
- Row ~ Hsync
- Pixels ~ CLK



Timing and interrupts



- Note: some interrupts might change depending on polarity. VSYNC interrupt is generated only on the positive edge of VSYNC toggle (on the picture). When negative edge is used then VSYNC to be generated after the LYR_TRANS_FINISH.

Interrupt/ flags description

- VS_BLANK: Interrupt signal to indicate vertical blanking period. This is the period in which all the registers that affect the visible state of the layers need to be latched. This is needed so that CPU writes to the register while the display is being updated does not cause any errors.
- VSYNC: Interrupt flag to indicate that the vertical synchronization phase has begun. If enabled, an interrupt is generated at the beginning of a frame.
- PROG_END: The configuration for the upcoming frame will now be locked and any update after this will lead to coherency issues (shadowing start - comes at 4 HSYNC's before the end of VS_BLANK).
- LYR_TRANS_FINISH: Interrupt flag to indicate that the transfer is complete of layer configuration from the layer control descriptor registers into the DCU4 functional block. (shadowing end - typically takes around 1024 DCU clock cycles)
- DMA_TRANS_FINISH: Interrupt flag, which indicates that the DCU4 DMA has fetched the last pixel of data from the memory.
- LS_BF_VS: Interrupt flag to indicate the Lines Before VS_BLANK event has been reached. The LS_BF_VS field in the Threshold register defines the timing of the event.

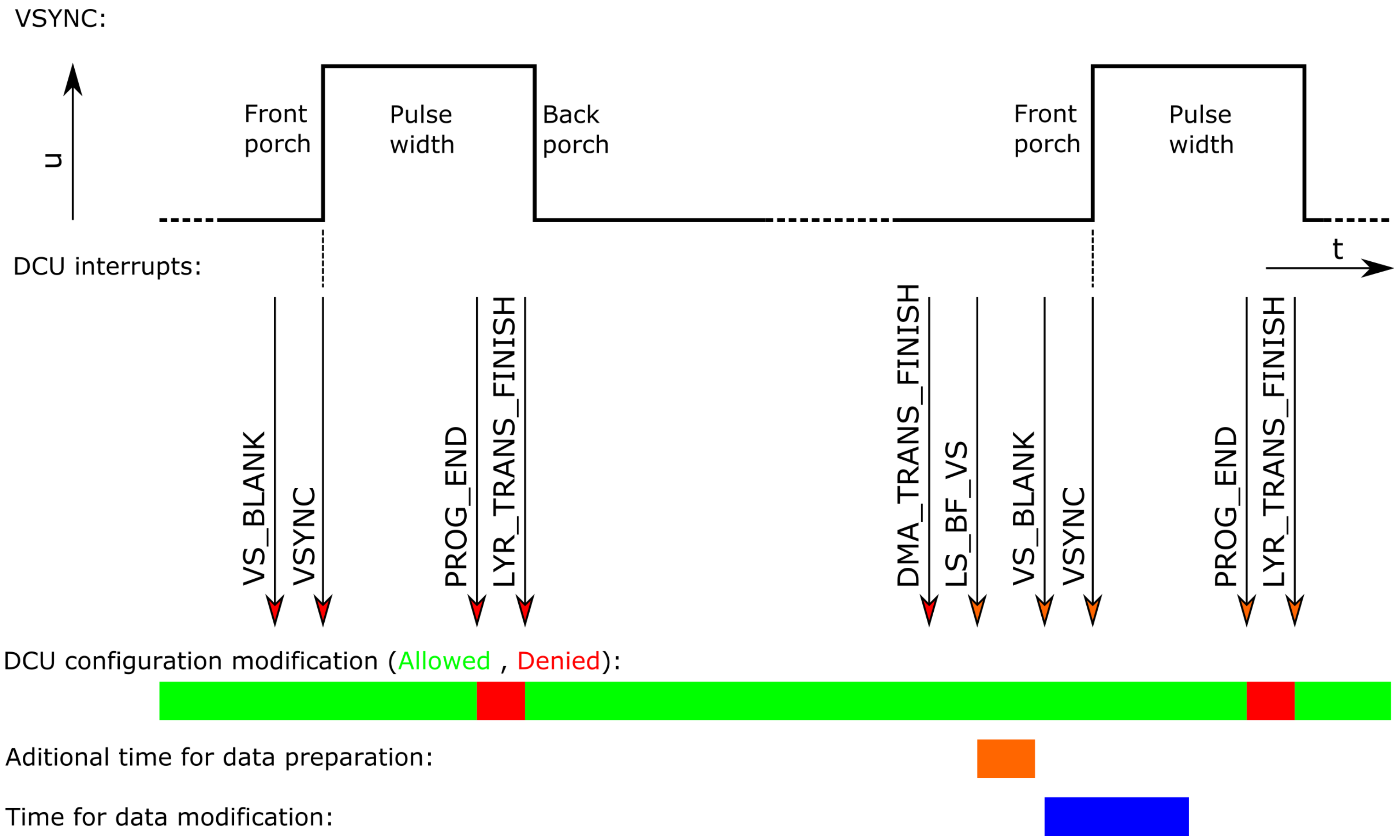
Transfer of DCU configuration

- Two steps:
  1. configuration values are written into the appropriate register by the user software
  2. values are transferred into the frame timing logic for use on the next frame refresh
- The transfer itself always occurs at a fixed time in relation to the vertical blanking period
- The time at which the control descriptors are updated and ready to transfer is under user control
- Any changes to the affected registers **must be** complete before the transfer is ready to begin (stated in Vybrid RM)
- The DCU provides a status flag called PROG_END bit in the INT_STATUS register which is asserted when the transfer is beginning and a status flag called LYR_TRANS_FINISH which indicates when the transfer is complete.

Timing and interrupts - recommend steps

1. Prepare data within LS_BF_VS ISR
2. Modify data within VS_BLANK ISR
3. Make sure that DCU configuration modification is finished prior to PROG_END

- Usage of LS_BF_VS is optional – it gives extra time for preparation of the transfer



What is happening inside

Please note that this issue has not been seen during designers simulation. Here’s what we think that happen based on what we know:

- The DCU module’s memory map has later registers that are accessible by the NIC masters (CPU, DMA or DAP) for read and write. These registers are shadow registers of the layer registers in the DCU graphics engine. The DCU engine copies the shadow registers to the graphics engine during blanking intervals. i.e. the DCU engine reads the shadow registers at that time.
- NIC masters accesses to the layer registers are clocked by the IPG clock. The Graphics Engine reads the registers influenced by the pixel clock.
- When these clocks are asynchronous, ex. using a different PLL, there is no fixed phase relation between the IPG and pixel clock.
- When now NIC master reads the layer registers during the copy process, registers are read from both NIC master and DCU at the same time. Because the read clocks are asynchronous, 2 different reads can occur at the same time, defeating the synchronization logic. In this case it can happen that the NIC master read will not be acknowledged and remain pending indefinitely. Since this pending read prevents any new bus accesses, the system will be locked-up.

Useful links

- Vybrid RM: 55.9 DCU4 Initialization
- Vybrid RM: 55.5.4.2 Transfer of DCU Configuration
- Vybrid RM: 55.6.1 Synchronizing to panel frame rate
- Vybrid RM: 55.6.2 Managing the DCU4 FIFOs and DMA activity
- Vybrid RM: 55.4.12 Interrupt Status Register (DCUx_INT_STATUS)
- Vybrid RM: Figure 55-1922. HSYNC and VSYNC timing diagram
- Vybrid RM: 55.7 Register protection

Conclusion

- Transfer of layer configuration registers have to be done at proper moment.
- Flags and interrupt sources are available and have to be used.
- It is not allowed to attempt registers during transfer of configuration into DCU logic.

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