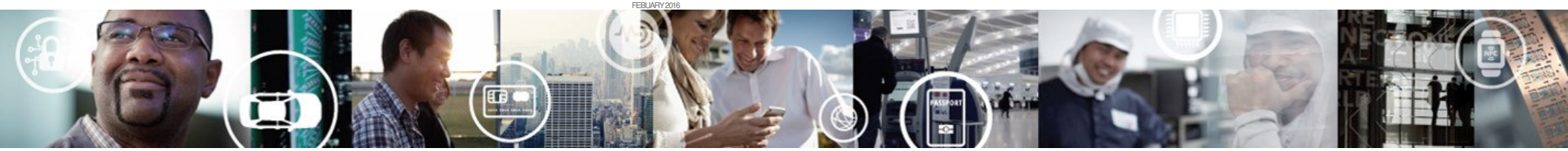
SCALABLE MULTICORE QORIQ LAYERSCAPE PROCESSORS

NXP TECHNOLOGY DAY
MARCH 2016
HAIM COHEN

FEBUARY 2016



SECURE CONNECTIONS FOR A SMARTER WORLD

ACCELERATING TECHNOLOGY TRENDS DRIVE OPPORTUNITIES FOR NXP

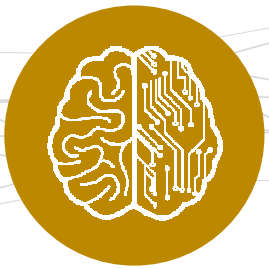
Secure Connections for a **Smarter World**

Everything **Connected**

1B+ additional consumers online, **30B+** connected devices

Connectivity

Everything **Smart**



40B+ devices with intelligence shipped in **2020**

Processing

Everything **Secure**

Potential savings to economy up to **half trillion dollars**

Security

Source: Euromonitor; Gartner; ARM Holdings; UBS; Center for Strategic and International Studies; McAfee, NXP analysis, International Telecommunications Union

EXPANDED SOLUTIONS FOR CUSTOMERS

freescale™

#1 Communications Processors
#1 RF Power Transistors
#1 Automotive Radar
#1 Automotive Safety[2]
#2 MCUs

NXP

#1 COMMUNICATIONS PROCESSORS

#1 BROAD-BASED MCUs[1]

#1 SECURE IDENTIFICATION

#1 AUTOMOTIVE

#1 RF POWER TRANSISTORS

#1 SMALL SIGNAL DISCRETES

NXP

#1 Secure Identification
#1 Car Entertainment
#1 In-Vehicle Networking
#1 Secure Car Access
#1 Smart Card MCUs
#1 Small Signal Discretes

Sources: HIS, ABI Research, Strategy Analytics, The Linley Group
(1) MCU market excluding Automotive
(2) Automotive Analog and Sensors in Airbag, Braking, Radar, and TPMS applications

NXP

A NEW POSITION OF STRENGTH[1]

freescale™

- ✓ **50+** year history
- ✓ **17,300** employees
- ✓ **$4.59b** in revenue
- ✓ **20.7%** EBIT
- ✓ **$839m** in R&D

NXP

>$10B IN ANNUAL REVENUE

~45,000 EMPLOYEES

35+ COUNTRIES

11,000+ ENGINEERS

9,000+ PATENT FAMILIES

4th Largest SEMICONDUCTOR COMPANY GLOBALLY

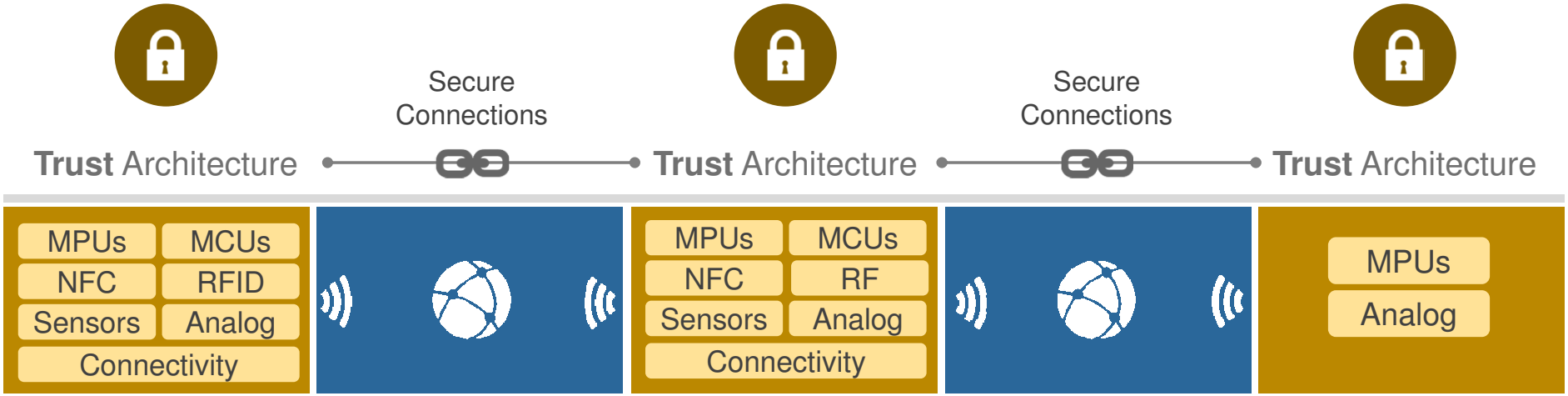
NXP

- ✓ **50+** year history
- ✓ **28,000** employees
- ✓ **$6.03b** in revenue
- ✓ **27.2%** EBIT
- ✓ **$723m** in R&D

Note:
1. All financial figures are based on trailing twelve month reported information; R&D expense and EBIT % are non-GAAP

NXP

IOT NEEDS A SECURE AND DYNAMIC NETWORK



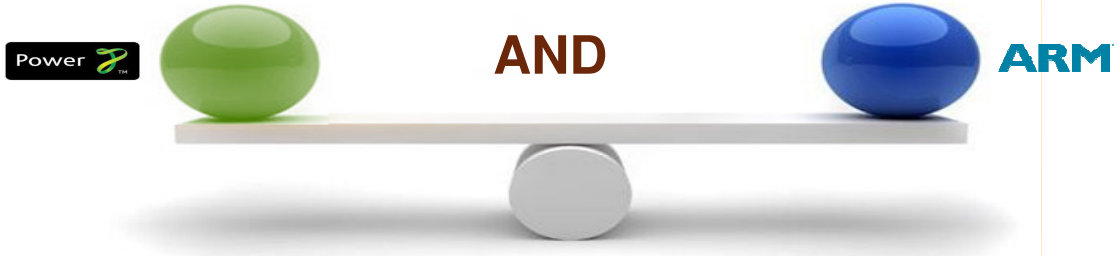
Power & ARM®: A Balanced Strategy for the Market

Continue to drive the "Core" - Power

1. #1 in wireless/wired Networking
2. 9 of top 10 WLAN vendors
3. 30+ years of R&D leadership

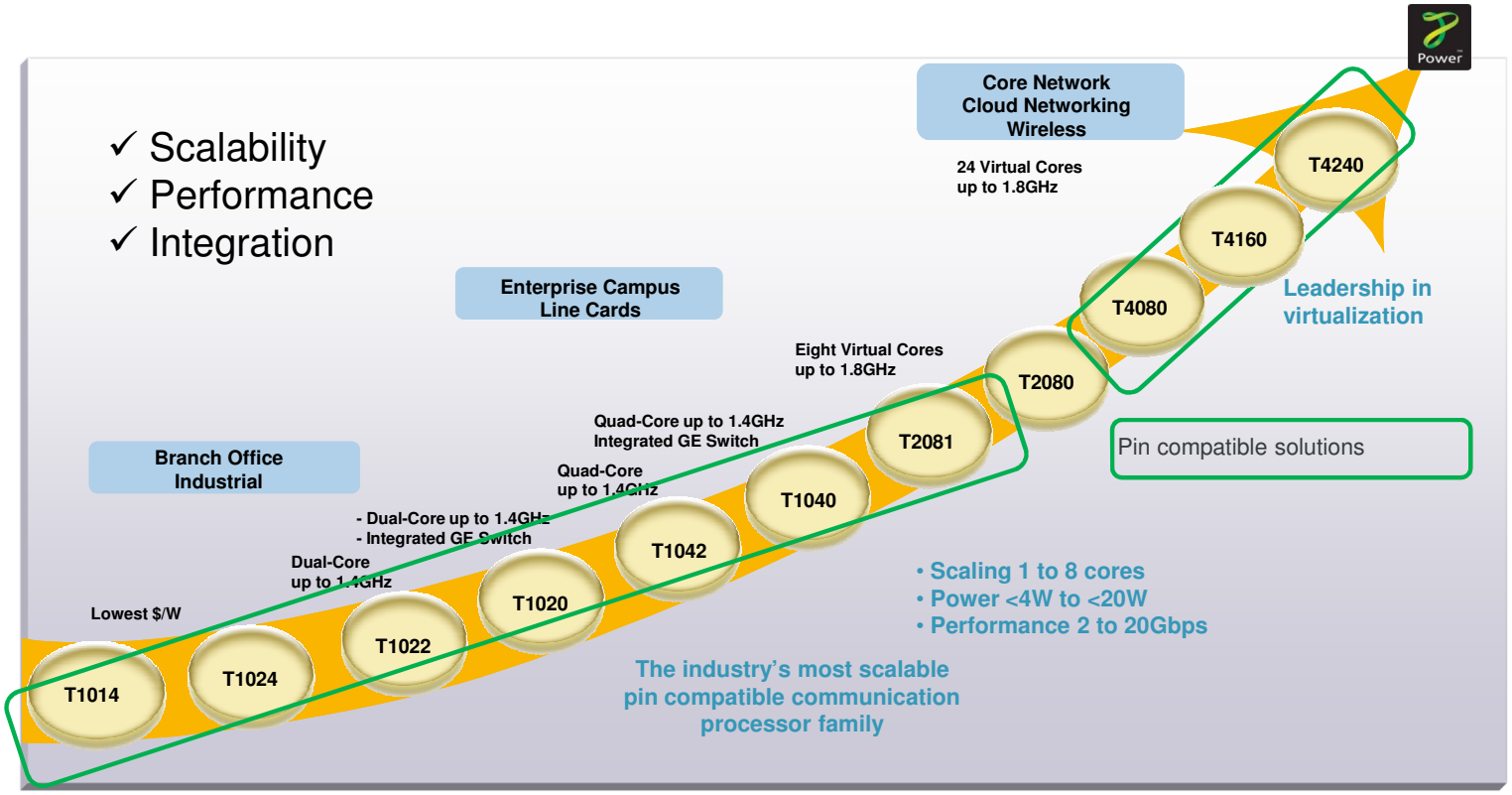
Broaden Market Reach– ARM Addition

1. First 64-bit ARM® Networking SoC
2. Largest ARM portfolio for Networking
3. Auto, Consumer and Industrial
4. Utilize our communications. expertise



NXP has infrastructure in place to support both Power and ARM

Continuing the Leadership: Power-based SoC Solutions



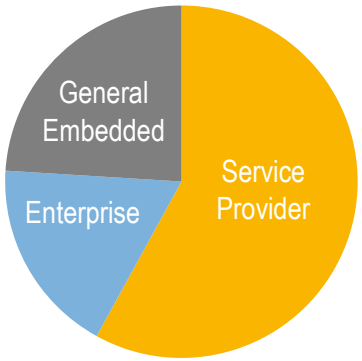
DIGITAL NETWORKING: BUSINESS EVOLUTION

TODAY

Service Provider
Wireless & Wired Equipment

Enterprise / Data Center
Network Infrastructure

General Embedded
Industrial, Mil/Aero, Printing & Imaging



FUTURE

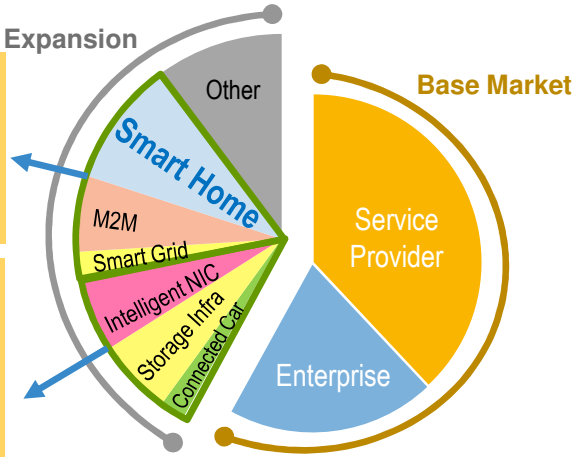
Service Provider
Wireless & Wired Equipment

Enterprise / Data Center
Network Infrastructure

Smart World Infrastructure
IoT Infrastructure, Cloud Edge

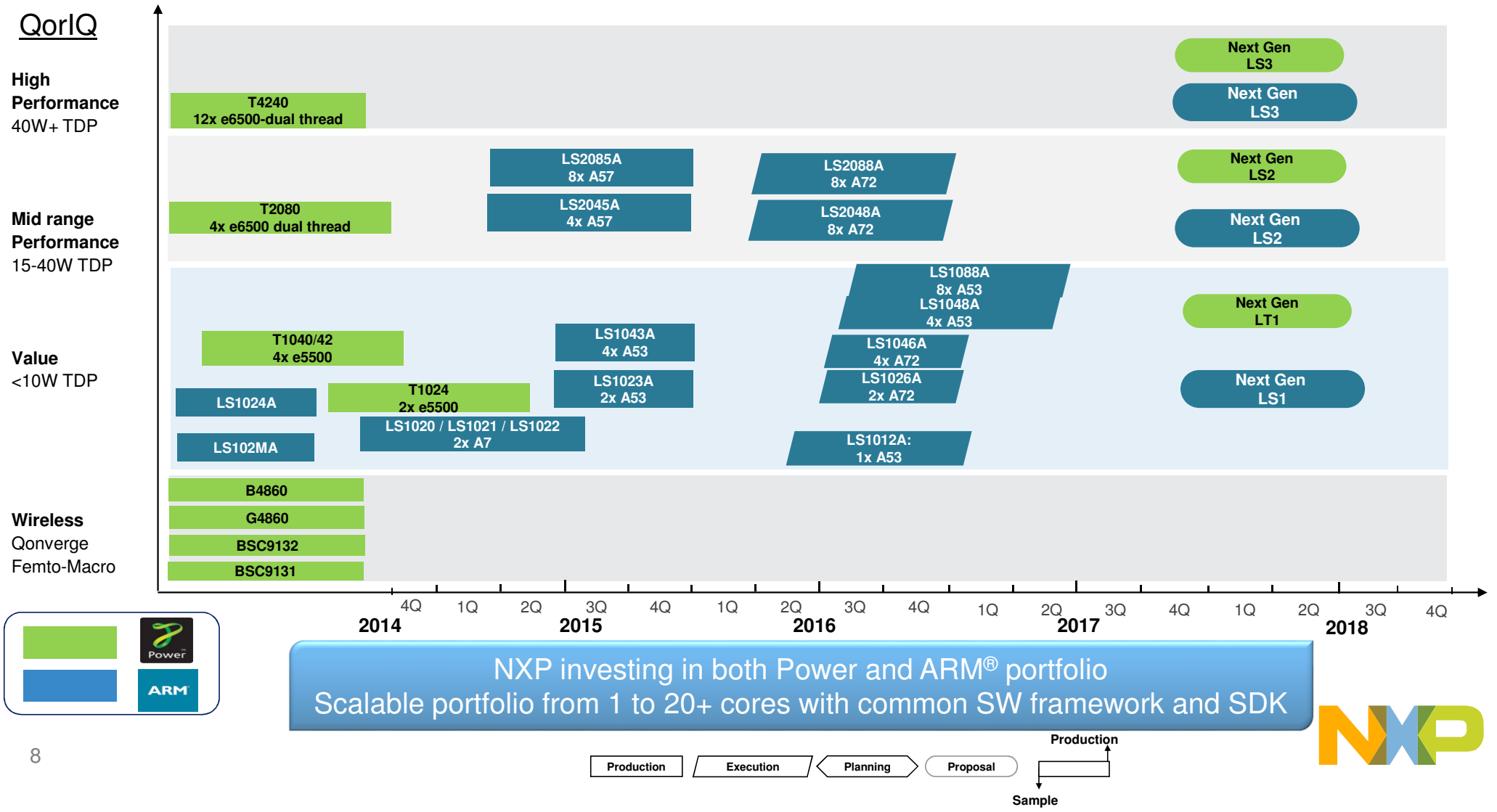
IoT Infrastructure:
- Smart Home
- M2M – Industry 4.0
- Smart Grid

Cloud Edge:
- Intelligent NIC
- Storage Infrastructure
- Connected Car Infrastructure



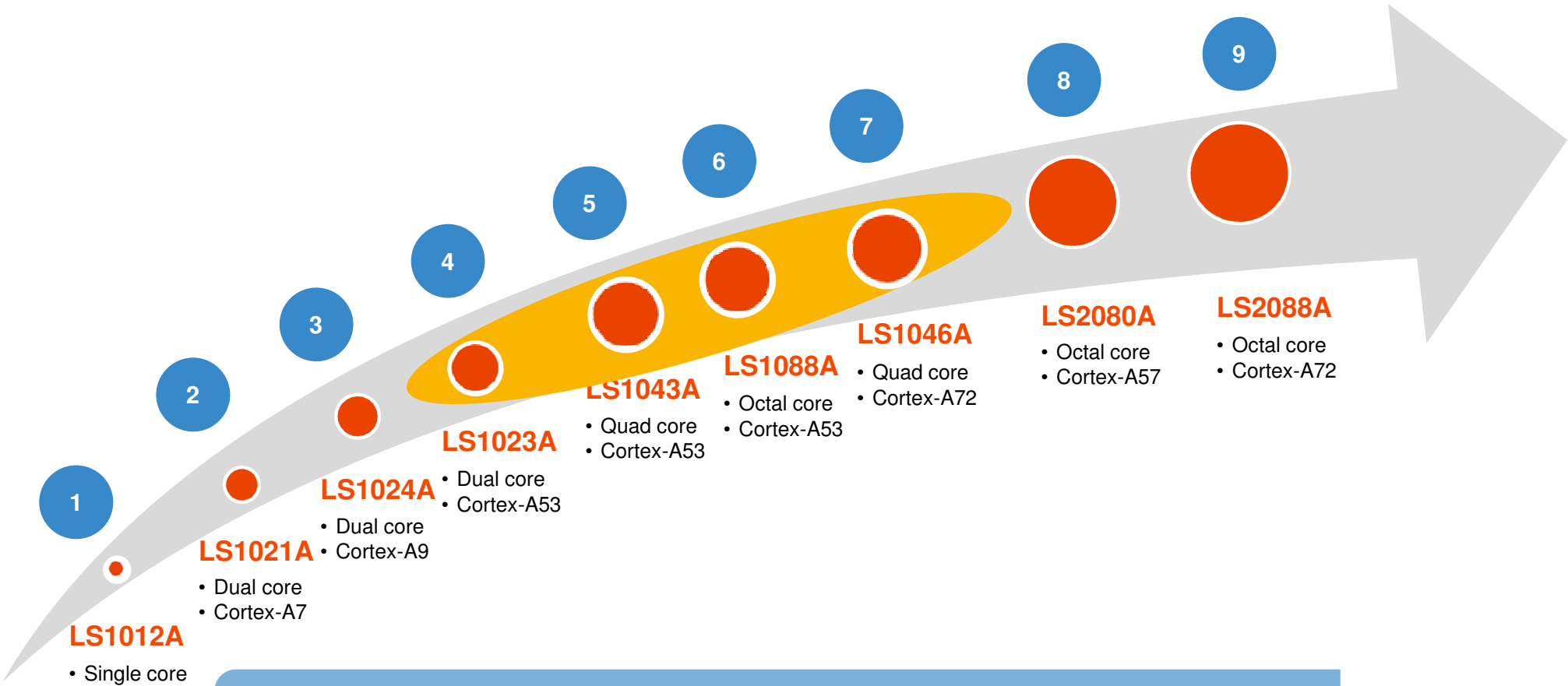
Expansion Markets Now Target Segments for Digital Networking

QorIQ Multicore Communications Processor Solution Roadmap



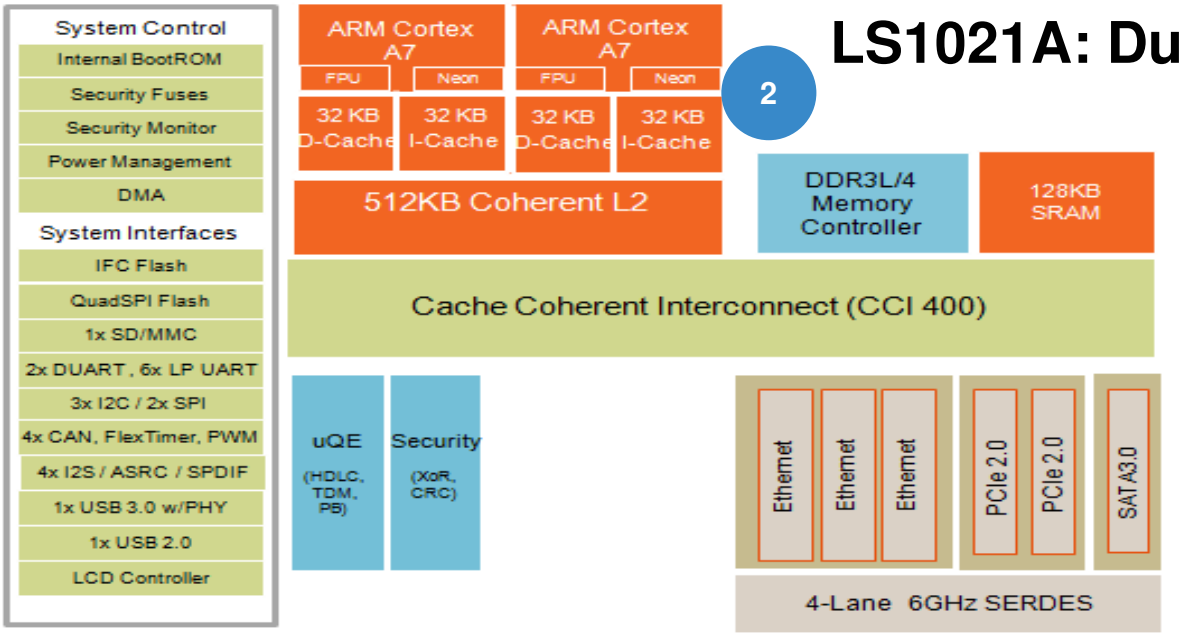
NXP investing in both Power and ARM® portfolio
Scalable portfolio from 1 to 20+ cores with common SW framework and SDK

NXP Digital Networking ARM®-based Processor Roadmap



NXP Leading ARM revolution in Networking

LS1021A: Dual ARM® Cortex® A7 Processor



- **2 x ARM Cortex A9 CPUs, up to 1.0GHz**
  - ECC protected L1/L2 caches
  - DDR3L/4 up to 1.6GHz
- **Over 5,000 Coremark at under 3.7W (TDP power)**
- **Industry best Coremark / mW ratio**
- **Outstanding security and IP forwarding**
- **High integration reduces BOM costs** for targeted applications:
  - Industrial gateways
  - Industrial Automation
  - Printing & Imaging
  - HMI
  - M2M, Smart "X"

Key Architectural Features:
- ARM AMBA4 MPCore™ Virtualization
- DDR3L/4 32-bit with ECC support
- 3-port GigE with IEEE 1588
- 2x PCI Express Gen2
- Multi-protocol 4-Lane SerDes
  - PCIe-2, SATA3, SGMII
- QUICC Engine – HDLC/TDM/ProfiBUS
- EnergyStar support with fast wakeup
- **2Gbps IP forwarding**

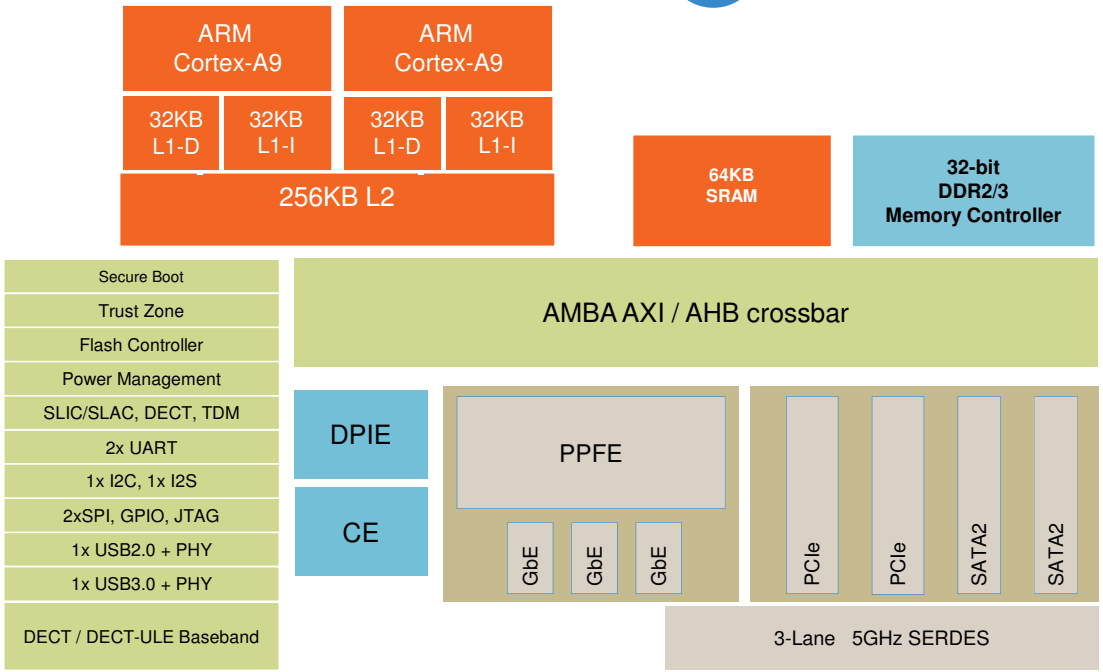
Key System Integration Features:
- Low-cost NAND/NOR flash systems
- Low-cost DRAM systems
- USB3 SuperSpeed
- Audio networking and motor control
- QorIQ processors Trust Architecture and ARM TrustZone support
- Alignment with Kinetis/Vybrid portfolio

Package & Board:

Package:	525-pin, 19x19mm, 0.8mm ball pitch
Power:	~2.8W @1.0GHz Typical
Temp:	-40C (TA) to 105C (Tj)
Boards:	Tower low-cost board NXP Linux BSPs

In production now

3 LS1024A: Dual ARM® Cortex® A9 Processor



Datapath Acceleration

- **CE** - crypto acceleration
- **PPFE** - Programmable Packet Forwarding Engine
- **DPIE** – Deep Packet Inspection Engine

General Purpose Processing

- 2 x ARM A9 CPUs, up to 1.2GHz
  - 256KB L2 cache
- Neon SIMD & FPU in all CPUs
- 16/32b DDR2/3 up to 1066MT/s

Accelerated Packet Processing

- 2Gbps PPPoE/NAT routing with 64B packets
- 2Gbps crypto acceleration
- Deep Packet Inspection Engine
  - Antivirus
  - Application-specific QoS
  - Advanced Diagnostics

DECT

- Integrated DECT and DECT-ULE baseband processor

High-speed Interfaces

- 2x PCIe 2.0 (5GHz)
- 2x SATA 2.0 with RAID 0/1/5
- 1x USB 3.0 with PHY
- 1x USB 2.0 (Host/Device) with PHY
- 3x GbE
  - 3x RGMII or 2x RGMII and 1x SGMII

In production now

QorIQ LS1043A Processors

Advanced 64b Quad Core ARM® A53 Supporting Network Edge Services

Smart Edge Access

- Leading headroom for branch router & WLAN services
- Multicore for VM services
- Hardware offload for secure edge tunneling
- Glueless HDLC & TDM support

Industrial Automation

- Industrial protocol support
- 10yr life & extended temp

Line Cards & Control

- 64bit ISA & high performance memory for fast computing
- 10G Base-KR backplane I/0

Best CPU headroom in its class for Smart Edge, virtual Branch Router & WLAN applications

Performance Leading SoCs

- Quad ARM A53 CPUs, 64b, up to 1.4 GHz
- Future Proof, Low Power Memory DDR4
- Extensive Hardware Virtualization
- Secure Boot

Advanced Packet Processing

- Packet Parse/Classify/Distribution engines
- Lossless flow control & granular traffic management
- Leading 2.5Gbps IMIX Single-pass en/decryption engine

Fast, Flexible Network Interfaces

- Up to 6x GbE with 2.5G options plus 10GbE XFI
- Integrated QUICC Engine for glueless HDLC, TDM, Industrial Protocols
- 3x USB 3.0 interfaces for highest speed LTE, Storage & Peripheral options

Highest Processing Efficiency

- Up to 15 K Coremarks at 8 watts

LS1043A: Quad ARM® Cortex® A53 Processor

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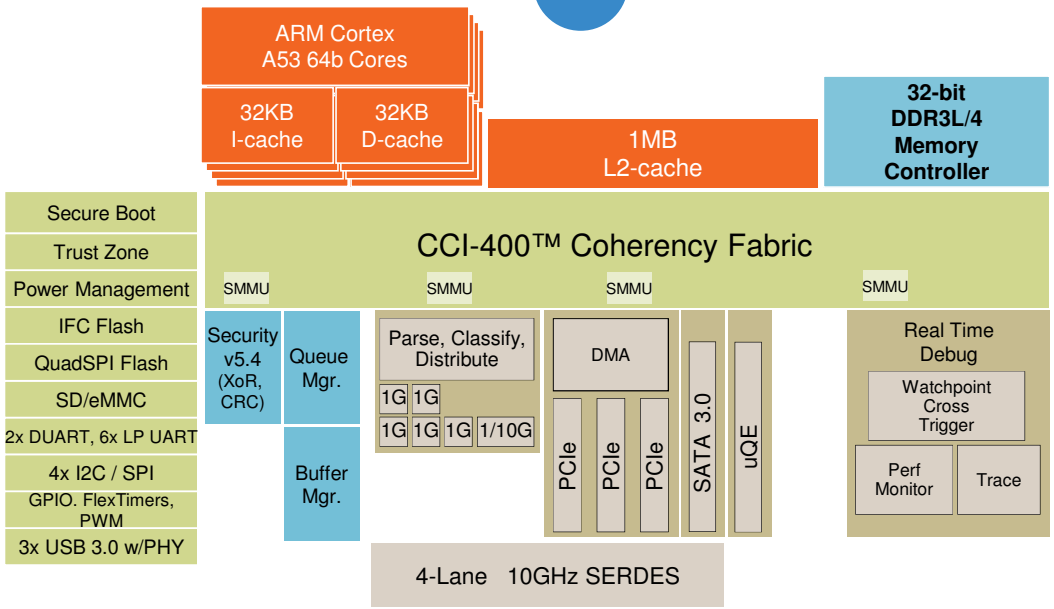


Processor
- 4x A53, 64b, up to 1.6GHz
- 1MB L2 cache shared by all cores (and platform elements)

Memory Subsystem
- 32b DDR3L/4 Controller up to 1600MHz

CCI-400 Switch Fabric
- Advanced VM hardware support

High Speed Serial IO
- 3x PCIe Gen2 Controllers
- 1x SATA 3.0, 6Gb/s
- 3x USB 3.0 with PHY

Network IO
- 1x10G + QSGMII or 3x 1/2.5G SGMII + 2x 1G RGMII
- Proven Packet Parse/Classify/Distribute
  - Up to 2.5Gbps IMIX
  - IPSec, GRE, CAPWAP, DTLS Offload
  - Lossless Flow Control

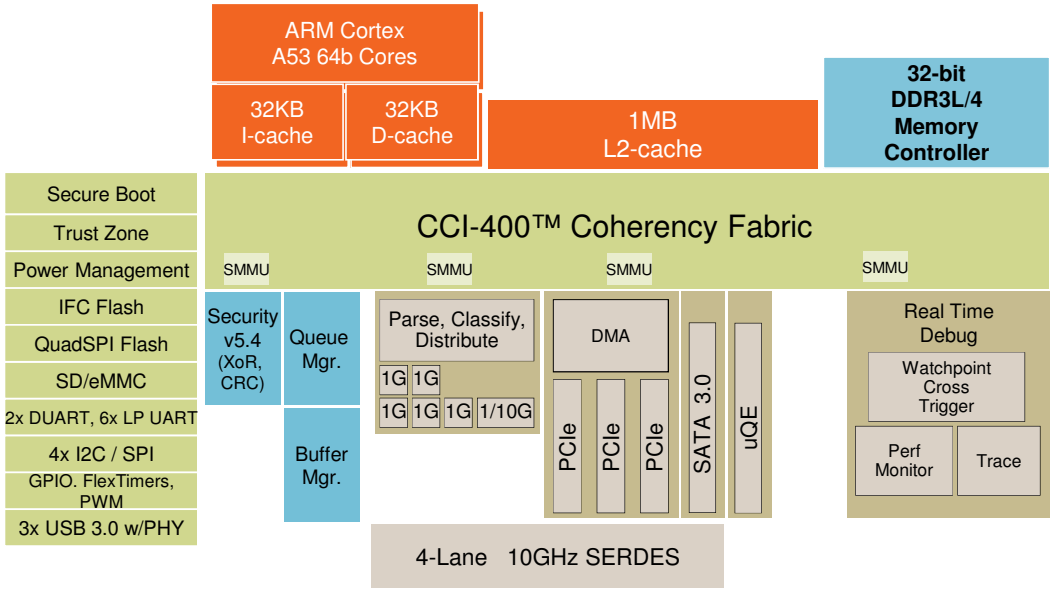
Package
- FCBPGA, 0.8mm pitch

Data path Acceleration
- SEC- crypto acceleration
- L2/3 & Custom Classification
- Tunnel Header Offload
- Reassembly
- Traffic Management & Shaping

In production now

Industry's most efficient quad core communications SoC solution

4 S1023A: Dual ARM® Cortex® A53 Processor



Package
- FCBPGA, 0.8mm pitch

Data path Acceleration
- SEC- crypto acceleration
- L2/3 & Custom Classification
- Tunnel Header Offload
- Reassembly
- Traffic Management & Shaping

Processor
- 2x A53, 64b, up to 1.6GHz
- 1MB L2 cache shared by all cores (and platform elements)

Memory Subsystem
- 32b DDR3L/4 Controller up to 1600MHz

CCI-400 Switch Fabric
- Advanced VM hardware support

High Speed Serial IO
- 3x PCIe Gen2 Controllers
- 1x SATA 3.0, 6Gb/s
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  - IPSec, GRE, CAPWAP, DTLS Offload
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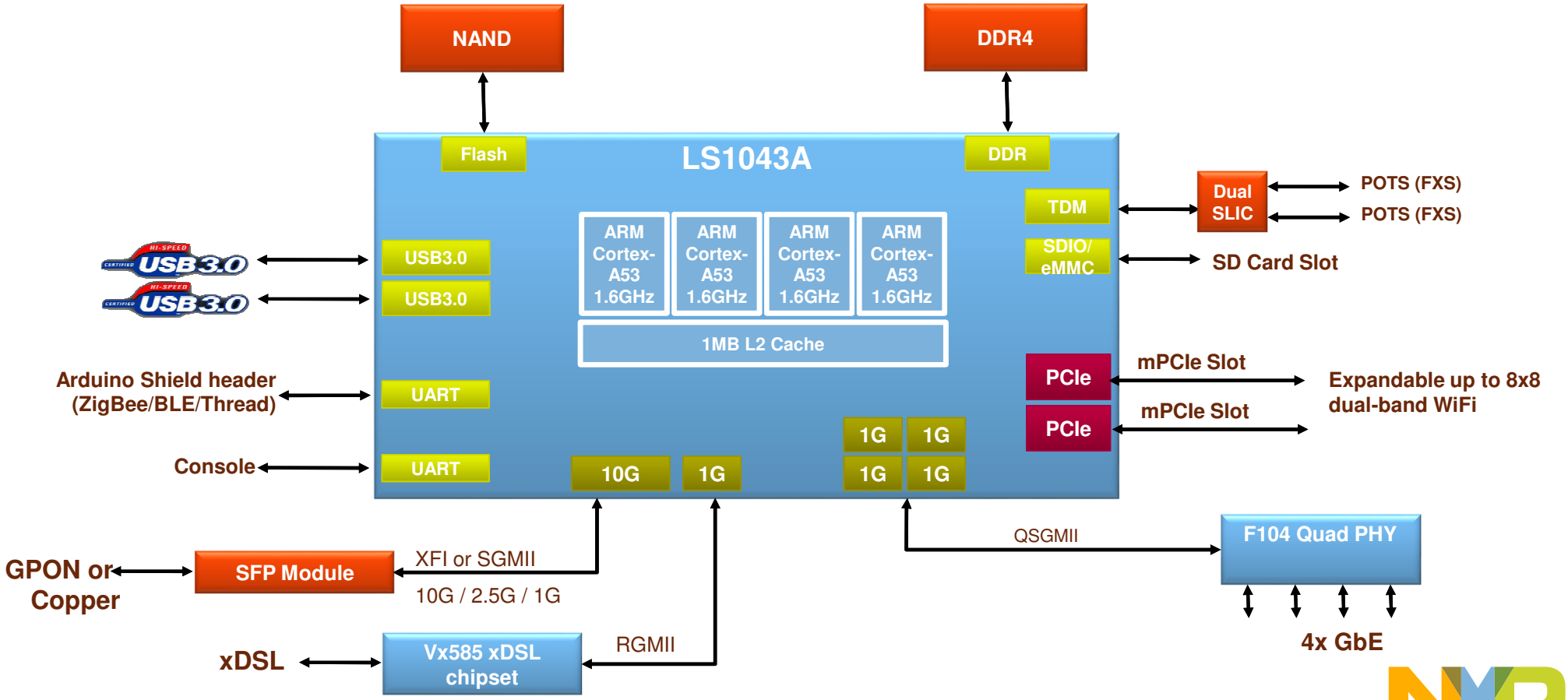
In production now

Industry's most efficient quad core communications SoC solution

LS1043A Broadband Home Gateway Reference Design (in development)



+ Software application software

Introducing the QorIQ LS1088A Processor

Bringing datapath acceleration
***to the* NETWORK EDGE**

QorIQ LS1048A and LS1088A Processors

Target Applications & Key Features

Intelligent Edge Access

NFV Solutions Virtual CPE

Industrial Control

Intelligent NIC

Performance optimized cores with leading power consciousness

- 8x ARM® Corte®x-A53 cores, 1.5 GHz, 2 MB L2 cache, w Neon SIMD
- DDR4 SDRAM support

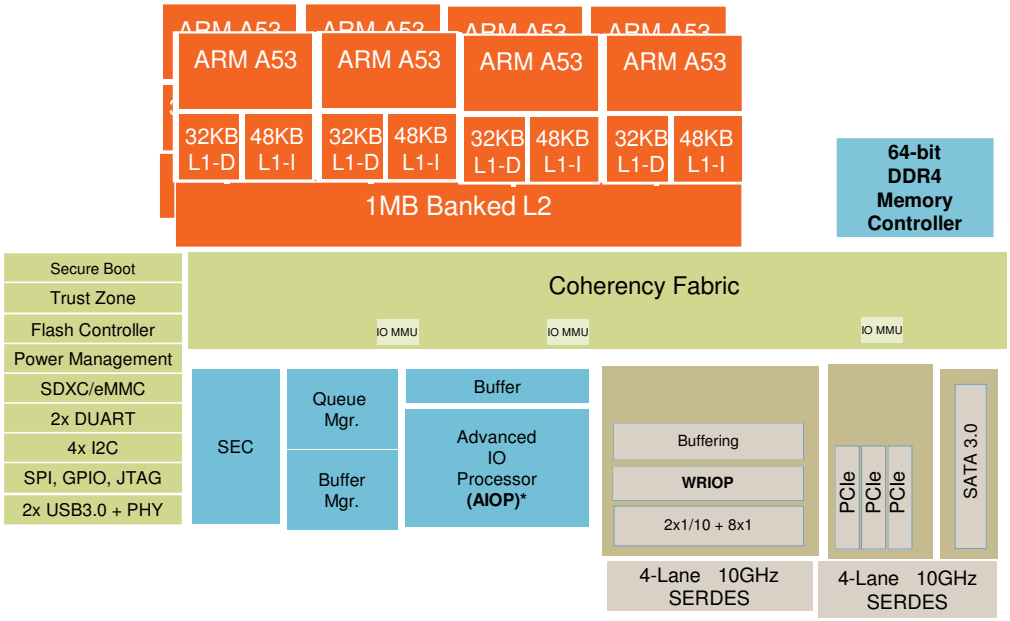
Delivers needed datapath offload with software developers in mind

- New datapath hardware and abstracted acceleration that is called via standard Linux objects
- 10Gbps Packet processing performance with security acceleration

Leading network I/O integration

- 2x10Gb Ethernet and 8x 1GB Ethernet
- PCIe Gen3, Sata3, USB3
- TDM/HDLC support

LS1088A/84A/48A



Device
- 28HPM Process
- FCBGA, 0.8mm pitch

Power target
- <18W

Schedule
- Samples: 1Q16
- Production: 4Q16

Security
- Hardware – Encryption (IPSec)
- Secure Boot
- Trust Zone & Trust Architecture
- MACSec support

Performance
- IPSec: 10 Gbps (IMIX)
- IPv4: 10 Gbps (IMIX)

General Purpose Processing Layer
- 4 or 8 x ARM® A53 CPUs, 64b, 1.5GHz
  - 1MB L2 cache / cluster
- HW L1 & L2 Prefetch Engines
- Neon SIMD in all CPUs

Memory Subsystem
- 64b DDR4 up to 2.1GT/s

CCI-400 Switch Fabric
- Advanced VM hardware support

Advanced I/O Processor
- Programmable packet handling

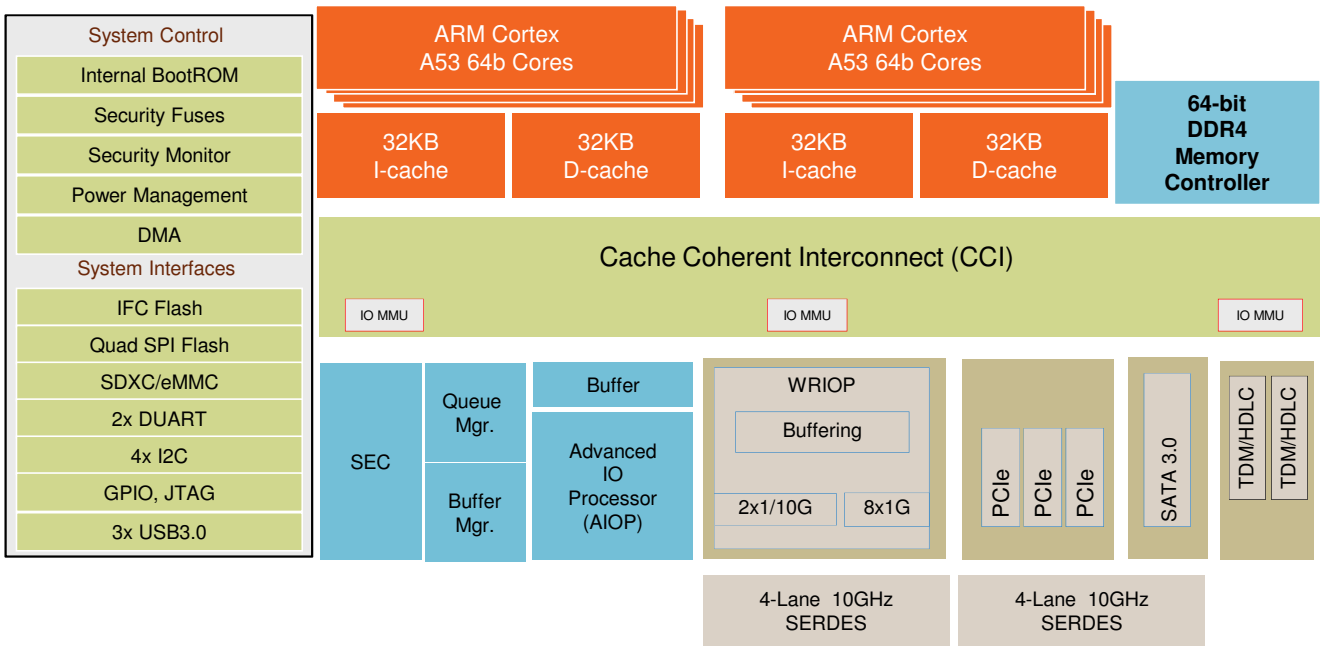
High Speed I/O
- 3x PCIe Gen3 controllers
- SATA 3.0, 2 x USB 3.0 with PHYs

Network I/O
- 2x1/10GbE + 8x1G
- XFI/KR and SGMII/KX
- MACSec on up to 4x 1GbE
- uQE for HDLC, T1/E1 support

Industrial connectivity
- Ethernet, Serial (RS485/422), uQE (for additional serial fieldbus applications)

* LS1088 only

6 LS1088A: Octal ARM Cortex A53 Processor



Samples	Production
May 2016	Dec 2016

General Purpose Processing Layer

- 8 x ARM A53 CPUs, 64b, 1.5GHz; 2MB L2 cache
- HW L1 & L2 Prefetch Engines
- Neon SIMD in all CPUs
- 1x64b DDR4 up to 2.1GT/s

Interfaces

- Supports x4,x2, x1 PCIe Gen2 controllers
- SATA 3.0, 3x USB 3.0
- SDXC/eMMC
- **Network IO**
- Wire Rate IO Processor:
  - 2x 10G and 8 x 1G; MACSEC on 4x 1G
  - XFI/KR, QSGMII, SGMII/KX, RGMII

Datapath Acceleration

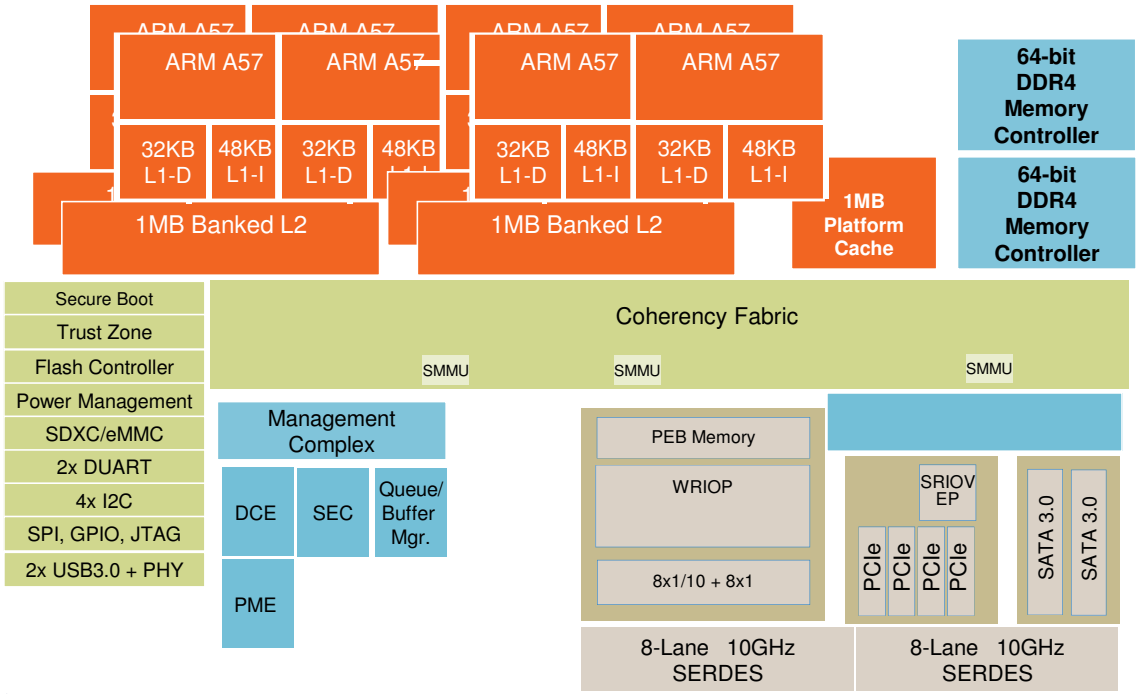
- SEC- crypto acceleration
- Packet processing engine (AIOP)
  - Protocol offload
  - Services

Other Parameters

- 25 x25mm Flipchip BGA
- 0.8mm Pitch, TBD Pins

Unprecedented performance/Watt and ease of use for smarter, more capable networks

8 LS2080A: Octal ARM® Cortex® A57 Processor



Other Parametrics

- 37.5x37.5 Flipchip
- 1mm Pitch
- 1292pins

Datapath Acceleration

- **SEC**- crypto acceleration
- **DCE** - Data Compression Engine
- **PME** – Pattern Matching Engine
- **Management Complex** – Configuration Abstraction

Samples	Production
Now	Dec 2015

General Purpose Processing

- 8x ARM A57 CPUs, 64b, 2.0GHz
  - 1MB L2 cache
- HW L1 & L2 Prefetch Engines
- Neon SIMD in all CPUs
- 1MB L3 platform cache w/ECC
- 4MB Coherent Cache
- 2x64b DDR4 up to 2.4GT/s

Accelerated Packet Processing

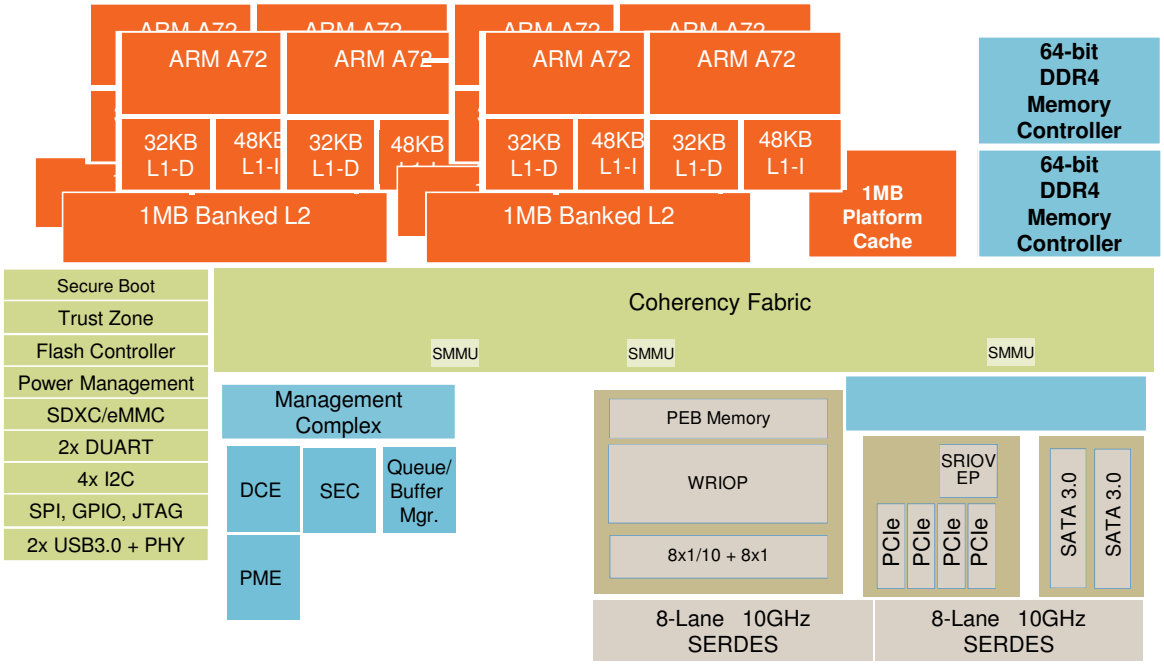
- 20Gbps SEC- crypto acceleration
- 10Gbps Pattern Match/RegEx
- 20Gbps Data Compression Engine

Express Packet IO

- Supports1x8, 4x4, 4x2, 4x1 PCIe Gen3 controllers
  - SR-IOV support, Root Complex
- 2 x SATA 3.0, 2 x USB 3.0 with PHY
- Network IO
- Wire Rate IO Processor:
  - 8x1/10GbE + 8x1G
  - XAUI/XFI/KR and SGMII
  - MACSec on up to 4x 1/10GbE

Full Featured Highly Flexible Platform: 4-8 A57 Cores

LS2084A: Octal ARM® Cortex® A72 Processor



General Purpose Processing

- **8x ARM A72** CPUs, 64b, 2.0GHz
  - 1MB L2 cache
- HW L1 & L2 Prefetch Engines
- Neon SIMD in all CPUs
- 1MB L3 platform cache w/ECC
- 4MB Coherent Cache
- 2x64b DDR4 up to 2.4GT/s

Accelerated Packet Processing

- 20Gbps SEC- crypto acceleration
- 10Gbps Pattern Match/RegEx
- 20Gbps Data Compression Engine

Express Packet IO

- Supports1x8, 4x4, 4x2, 4x1 PCIe Gen3 controllers
  - SR-IOV support, Root Complex
- 2 x SATA 3.0, 2 x USB 3.0 with PHY

Network IO

- Wire Rate IO Processor:
  - 8x1/10GbE + 8x1G
  - XAUI/XFI/KR and SGMII
  - MACSec on up to 4x 1/10GbE

Other Parametrics

- 37.5x37.5 Flipchip
- 1mm Pitch
- 1292pins

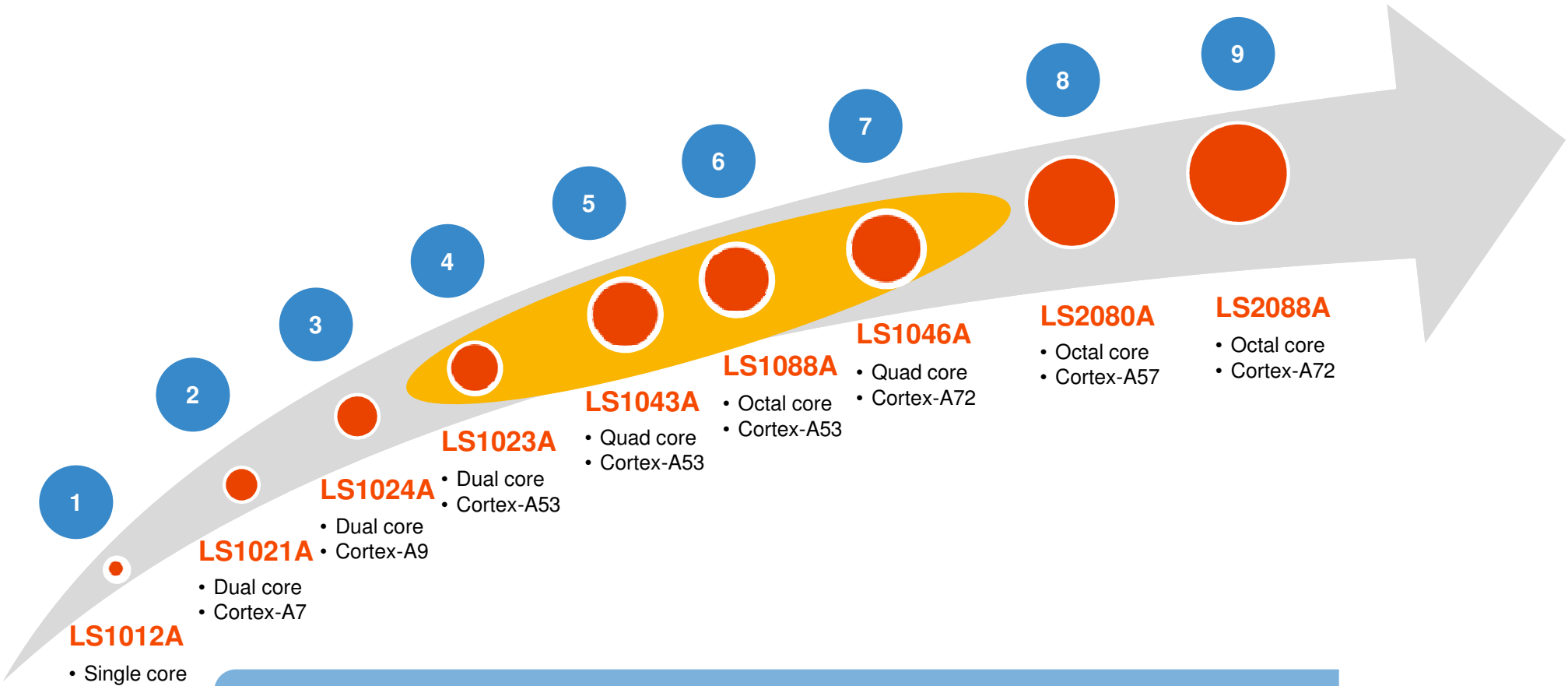
Datapath Acceleration

- **SEC**- crypto acceleration
- **DCE** - Data Compression Engine
- **PME** – Pattern Matching Engine
- **Management Complex** – Configuration Abstraction

Samples	Production
March 2016	Sep 2016

Full Featured Highly Flexible Platform
4-8 A72 Cores

NXP Digital Networking ARM®-based Processor Roadmap



NXP Leading ARM revolution in Networking

LS1046A Target Markets, Key Features

Enterprise
Routers/Switches

Industrial Computing and
Networking

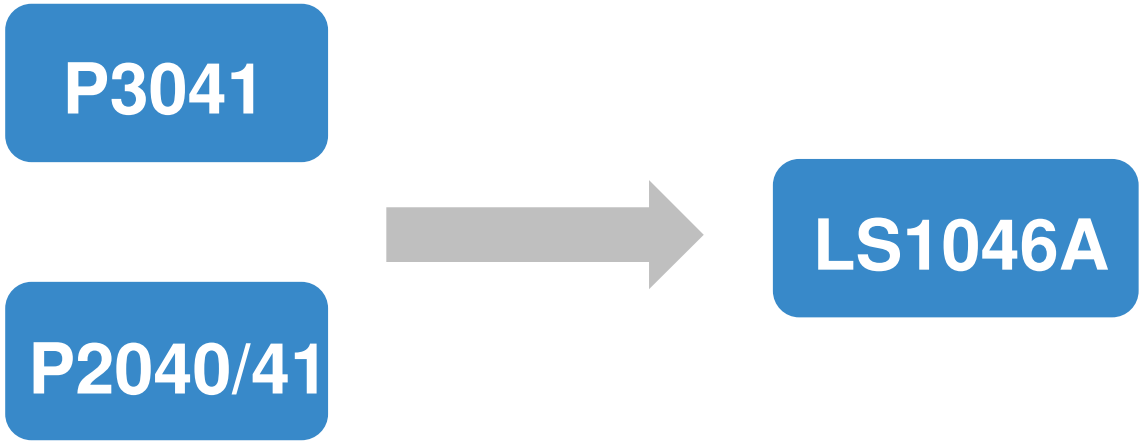
UTM Security
Appliances

The LS1 embedded processor are architected to provide maximum performance per watt

- Highest performance CPU cores in a power envelope
- Offload engines – Encryption/ Decryption for high performance security
- DPAA – for QoS and balanced networking performance
- Virtualization to support customers and 3rd party software

LS1046A: Compelling P2/ P3 upgrade path

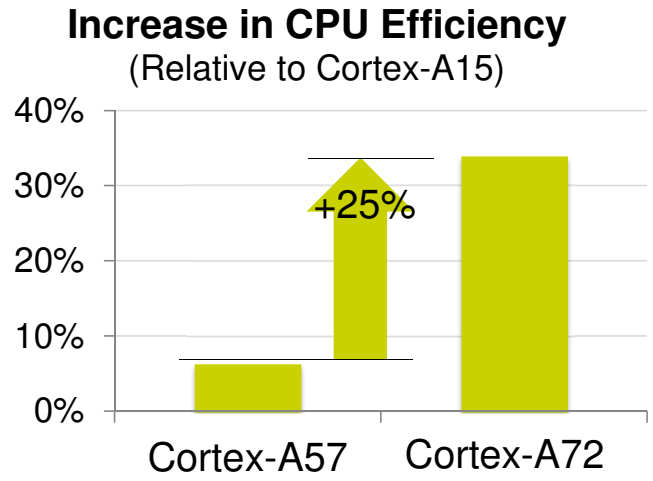
- Significant performance increase
  - Core performance increased by 75%
  - System-level performance:
    - L2 cache increased to 2MB
    - 32/64-bit DDR Controller up to 2.1GT/s
- 64-bit ARM® v8 processor cores
  - 4x A72 up to 1.6GHz
- New Networking interfaces
  - 2x 10GbE + 3x 1GbE
  - 3x PCIe 3.0
  - 3x USB 3.0
  - 1x SATA 3.0
- The same Datapath architecture
  - Datapath Acceleration Architecture 1.0 – the same as in P2040/1 and P3041
- The same power envelope as P2040/1 and P3041



Cortex®-A72 vs Cortex-A57 Benchmark Comparison

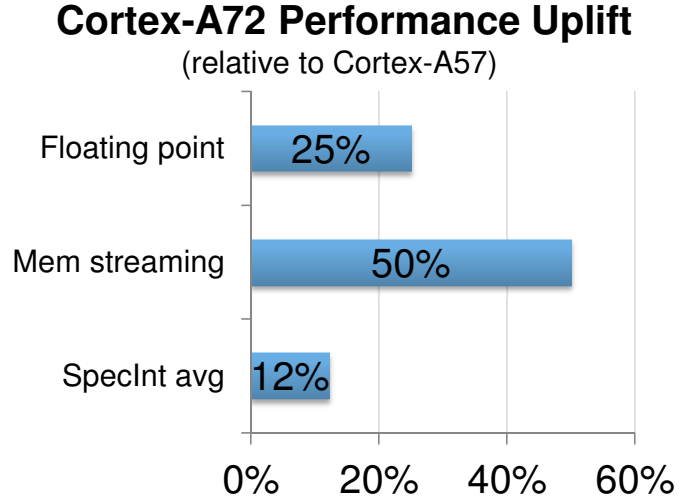
Benchmark	A57 -> A72 Improvement	Reason for Improvement
CoreMark	~ 1.14x	Improved Core Branch Prediction Unit
SpecINT2006	~ 1.12x	Improved HW Prefetcher

18% to 25% Better Energy Efficiency



More performance in constrained thermal budget

10% to 50% More Performance



Highest ARM®v8-A performance

CPU Summary

- For most workloads, Cortex®-A72 at 1.6GHz is same performance as Cortex-A57 at 1.8GHz

Cortex-A72 at 1.6GHz better performance than >2GHz Cortex-A57 for floating point or memory streaming workloads

More efficient design than Cortex-A57

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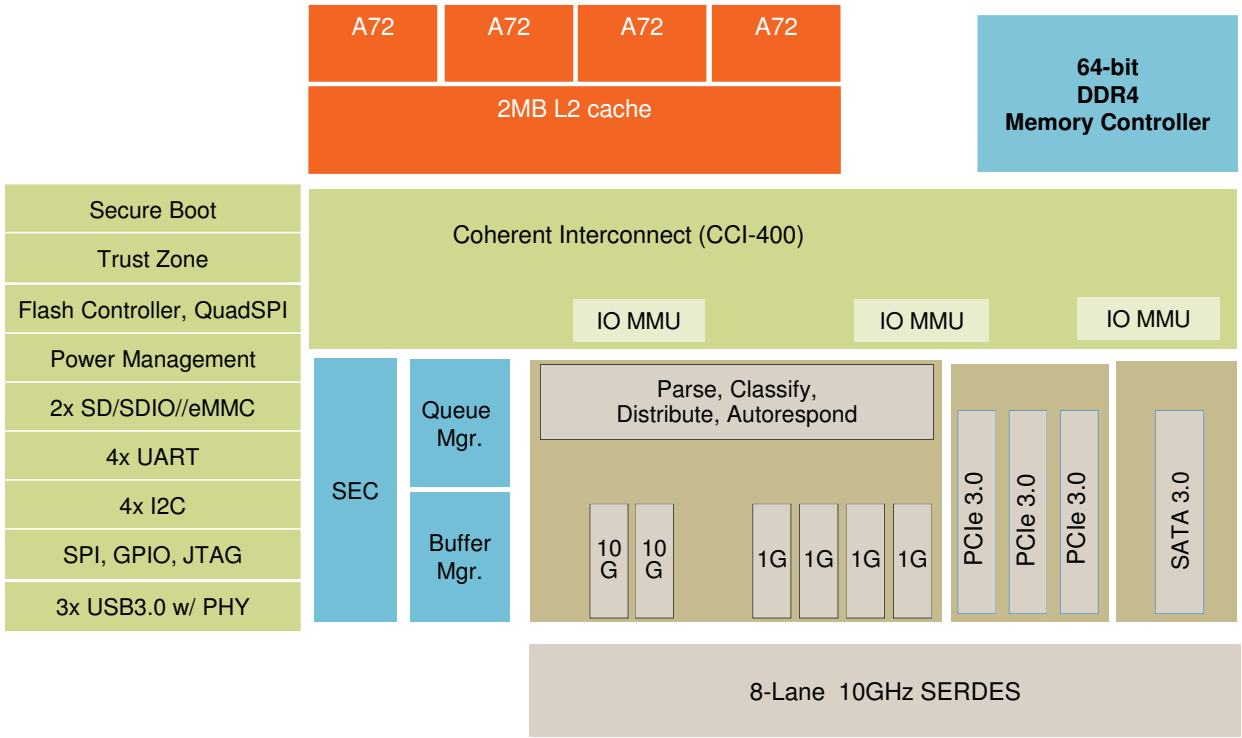
LS1046A: Quad ARM® Cortex® A72 Processor



Samples	Production
June 2016	Dec 2016

Leading Quad A72 processor with two 10GbE ports

Core & Memory Subsystem

- 4x ARM Cortex A72 up to 1.6GHz
- 2MB total L2 cache
- 64-bit DDR4 up to 2.1GT/s

Interfaces

- Three PCIe Gen3 controllers (x4, x2 and x1)
- 1x SATA 3.0
- 3x USB 3.0 with PHY
- 2x SD3.0/SDIO/eMMC 4.5

Network IO

- 2x 10GbE
- 4x 1GbE

Datapath Acceleration

- SEC- crypto acceleration
- Datapath Acceleration Architecture 1.x

Other Parameters

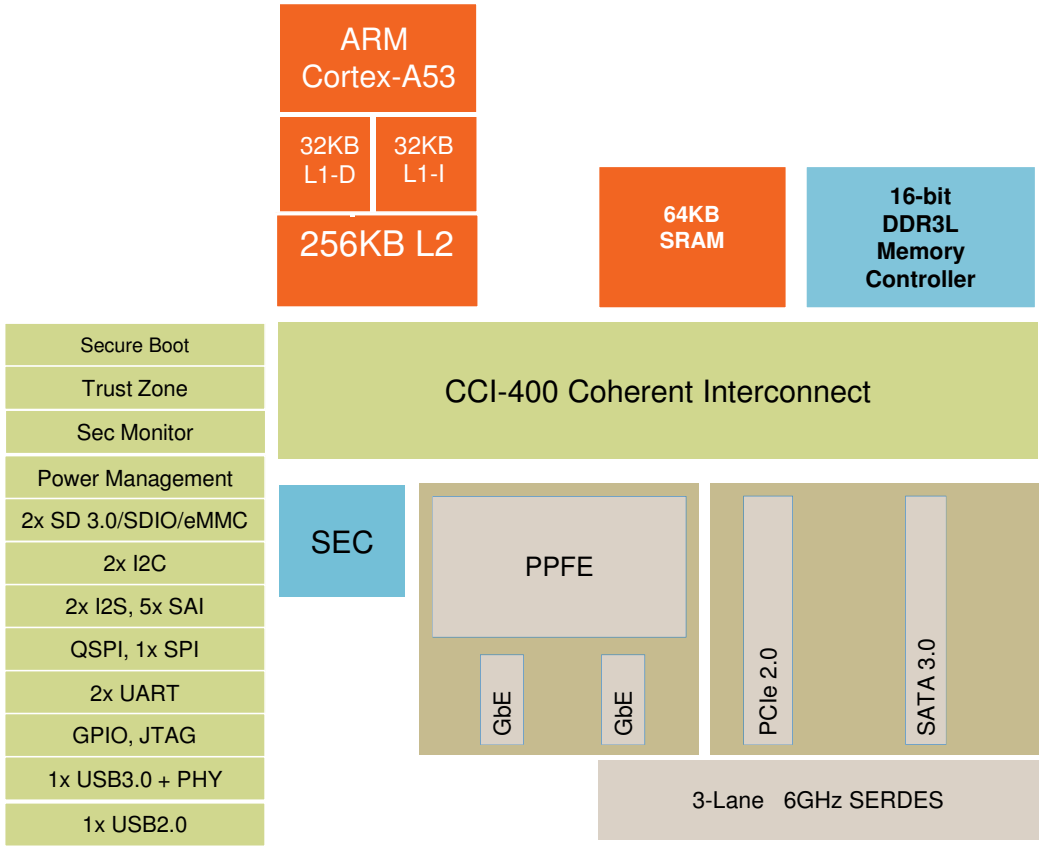
- Package:
  -23x23mm, Lidless FCBGA

INTRODUCING LS1012A…

…the world's smallest and lowest-power 64-bit processor.

1 LS1012A: Single ARM® Cortex® A53 Processor

- Single ARM Cortex-A53 processor
  - 1840 DMIPS / 2240 Coremark @ 800MHz
  - NEON Co-processor and DP FPU
  - 256 KB L2 cache with ECC
- Memory Controller
  - DDR3L up to 1000 MHz
  - 16-bit data bus, 1 chip select
- High Speed Interconnect
  - 1x PCI Express Gen2
  - 1x SATA Gen3
  - 1x USB 3.0 w/PHY
  - 1x USB 2.0 w/ULPI
- Ethernet Packet Accelerator
  - 2x GbE (2.5G or 1G)
- Datapath
  - Packet Acceleration Engine (PPFE)
  - Security acceleration engine (SEC)
- 2x SD 3.0/SDIO/eMMC
- QSPI, 1x SPI, 2x UART, 2x I2C
- 2x I2S, 5x SAI
- Secure Boot, Trust Architecture, ARM TrustZone
- Advanced Power Management
- Package: 10x10mm, routable in 4-layers



Samples	Production
June-2016	Q4-2016

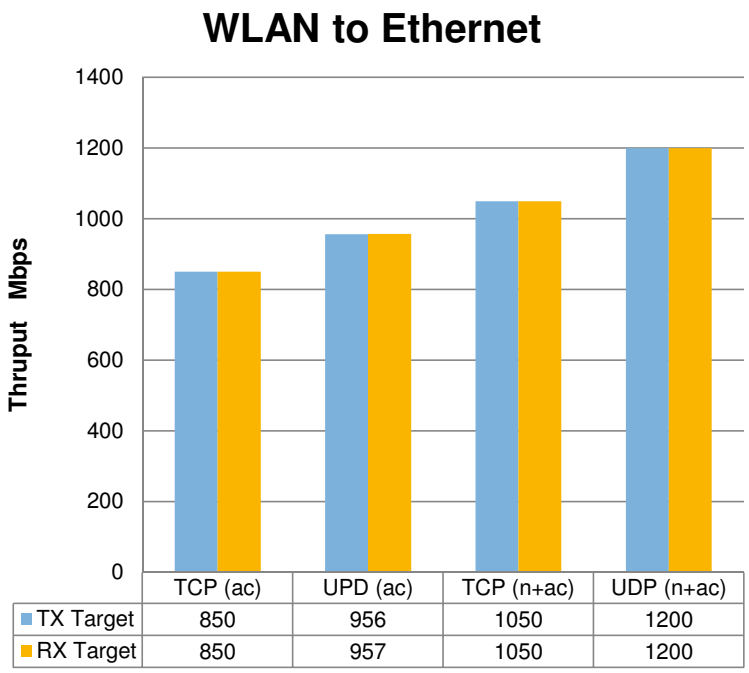
LS1012A High Level Features

- **Processor Complex**
  - 64-bit ARM® Cortex®-A53 up to 800 MHz
    - NEON SimD / DP FPU
    - 32KB/32KB L1 Parity protected Cache & 256KB L2 Cache with ECC
- **Data Interfaces (up to 2x 6GHz SerDes Lanes)**
  - 2x Gb Ethernet (2.5G/1G)
  - 1x USB3.0 w/PHY
  - 1x USB2.0 w/ULPI
  - 1x PCIe Gen2 (5 GHz) (x1)
  - 1x SATA-3 (6 GHz)
- **Memory Interfaces**
  - QSPI (NOR flash)
  - 1x SPI
  - 2x SDIO 3.0
  - DDR3L-1066 MHz (16b)
- **Control I/Os**
  - 2x I2C, 1x SPI
  - 2x UARTs
  - 2x I2S, 5x SAI
  - Watchdog/Timers
  - 16 dedicated GPIOs, 6 PWM Capable
- **Boot**
  - SPI FLASH

- **Packet Acceleration**
  - **Packet Acceleration Engine**
    - 2Gbps of PPPoE/NAT routing with 390B packets
    - RSO/LRO offload
  - **Hardware Security Engine**
    - 400 MB/s block mode encryption
    - AES256 CBC, ECB, XTS
    - XOR
- **Hardware/Silicon Security**
  - Secure Boot, JTAG Blocking, 8Kb OTP Memory
  - ARM TrustZone + Trust Architecture
  - DRM compliance
- **Battery Operation**
  - Dynamic Frequency Scaling (DFS) with integrated power management
  - USB charging

LS1012A Packet Forwarding Engine - Performance Estimates

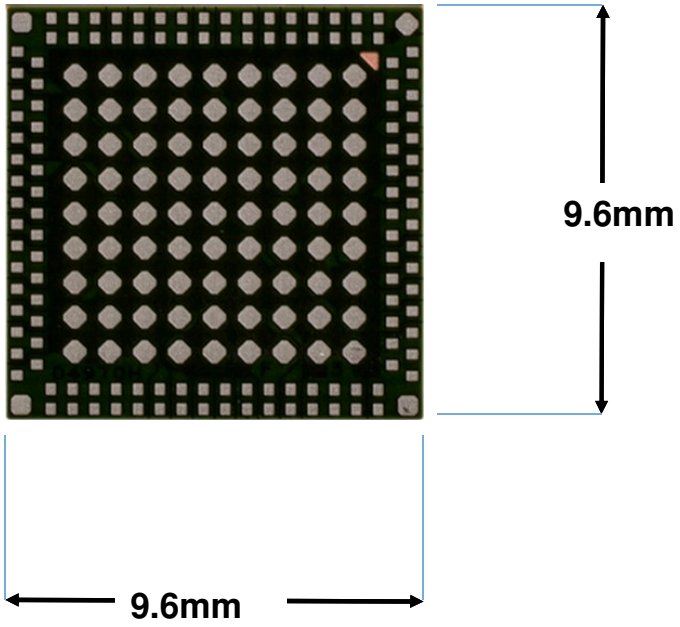
Ethernet to Ethernet: NAT Routing			
Frame Size	Bi-dir thruput (IPV4) – Mbps	Bi-dir thruput (IPV6) - Mbps	CPU utilization target
64	2000	2000	<5%
128	2000	2000	<5%
256	2000	2000	<5%
512	2000	2000	<5%
1024	2000	2000	<5%
1280	2000	2000	<5%
1518	2000	2000	<5%



- NAT routing targets should be achieved with minimal CPU impact for IPV4/6 acceleration

LS1012A Ultra-low form-factor package

- Innovative Laminate BGA Technology
  - Signal pins in outer two pad rows with 0.5mm pitch
  - Inner balls with 0.8mm pitch used only for power and ground
- Supports cost-effective 4-layer PCB
- Enables designs with severe space constraints

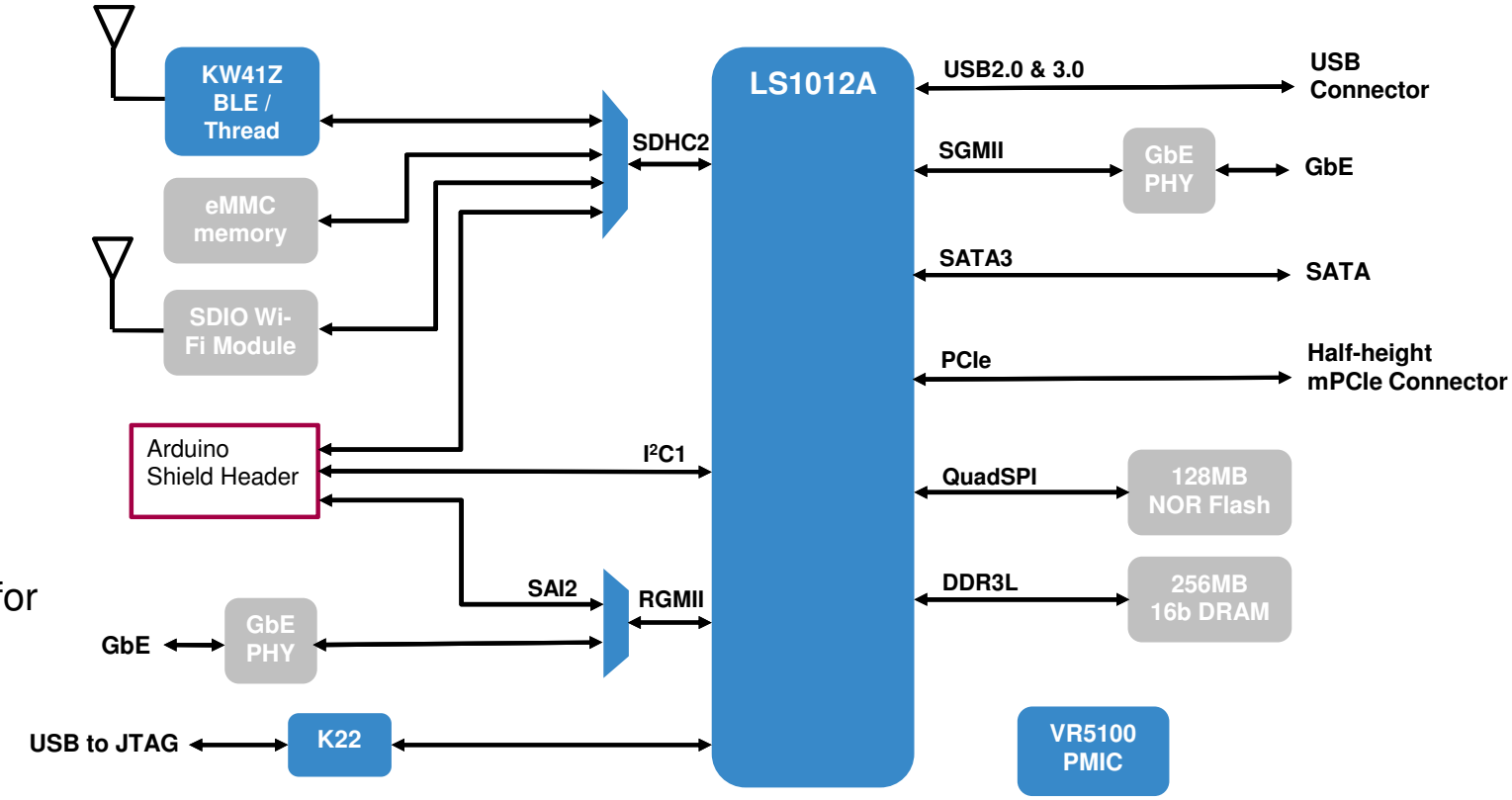


LS1012A ENABLEMENT

LS1012A-RDB board

Features

- 128MB NOR Flash
- 256MB DDR3L DRAM
- 2x GbE
- 1x mPCIe
- 1x SATA
- USB3.0
- USB2.0
- KW41Z 2.4GHz radio supports Thread & Bluetooth Low Energy
- Arduino Shield header for expansion



MC34VR5100: PMIC Solution for LS1012A

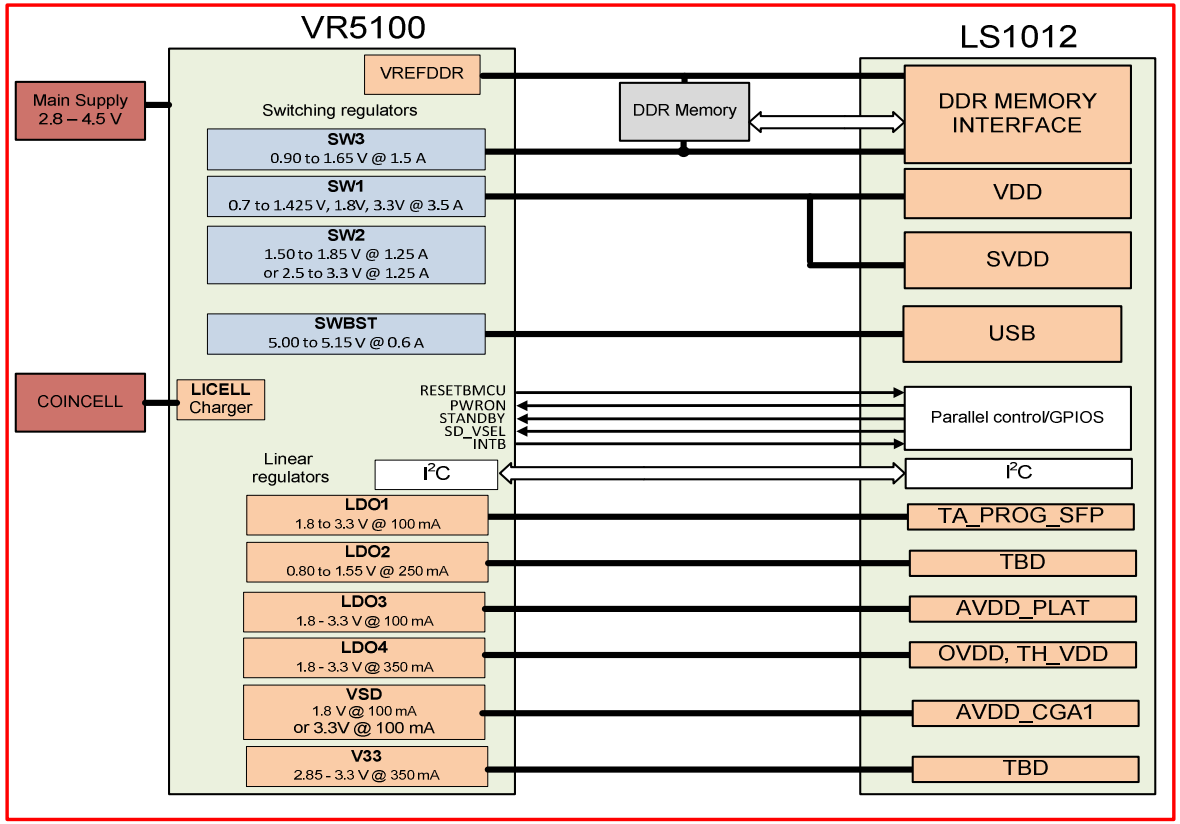
High Efficiency, Multi-output buck regulator with up to 3.8A output and six user-programmable LDOs

Differentiating Points

- Optimized to work with single or dual core LS1, T1 network processor systems
- >90% peak, >80% light-load efficiency to meet low power mode specs for LS1012
- Pre-programmed output voltages, sequencing, and timing to meet LS1012 applications need
- Dynamic regulator control via I2C
  - Voltage, Current Limit, Frequency

Product Features

- Vin = 3.3Vbus Supply (2.8V to 4.5V)
- Three independent buck converters
- Six user programmable LDOs
- Forced PWM/PFM or APS operation
- DDR reference, LiCell Charger, USB-5V Boost
- -40 to +105°C Operating Temp Range
- High power 7x7 mm QFN package



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TARGET MARKETS & DIFFERENTIATED FEATURES

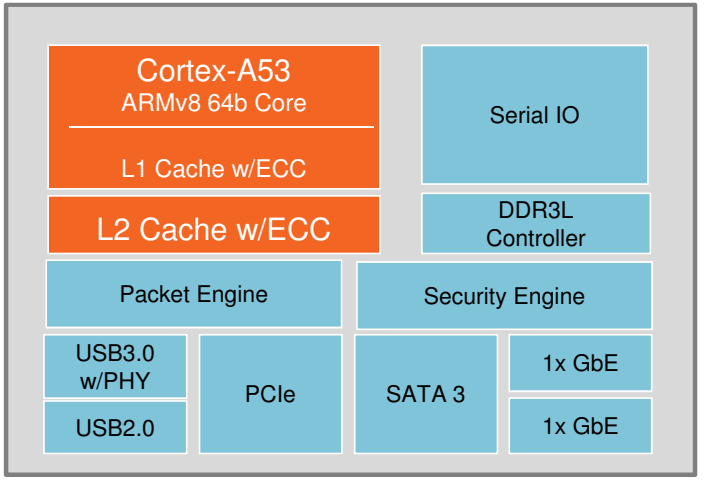
LS1012A Differentiated Features & Target Applications

Performance starts with the core

- First 64-bit ARM® Corte®x-A53 core to be offered in a sub- 10x10 mm package, delivering over **2,000 CoreMark®** of performance at **1W (typical)** for outstanding performance at exceptionally low power utilization
- **Best in class** 2.5 CoreMark / mW ratio

Broadest range of peripheral and I/O features in the sub-$10 ASP price range

- Only product in its class to offer **Packet Acceleration** for **IP forwarding and NAS,** delivering ourstanding packet throughput for this power/package envelope
- **Trust and Security acceleration** enables root of trust and high performance encryption consistent with much higher cost microprocessors
- **First in its class** to offer 64-bit support for **battery powered** mobile applications and **performance efficiency**
- Only 1W 64-bit processor to combine **USB 3.0 with integrated PHY, PCIe, 2.5 Gigabit Ethernet and SATA3 on a single SoC** to enable lower system-level costs
- Enables **low-cost, 4-layer board** level designs together with **high system level integration** to support ultra-small form factor systems

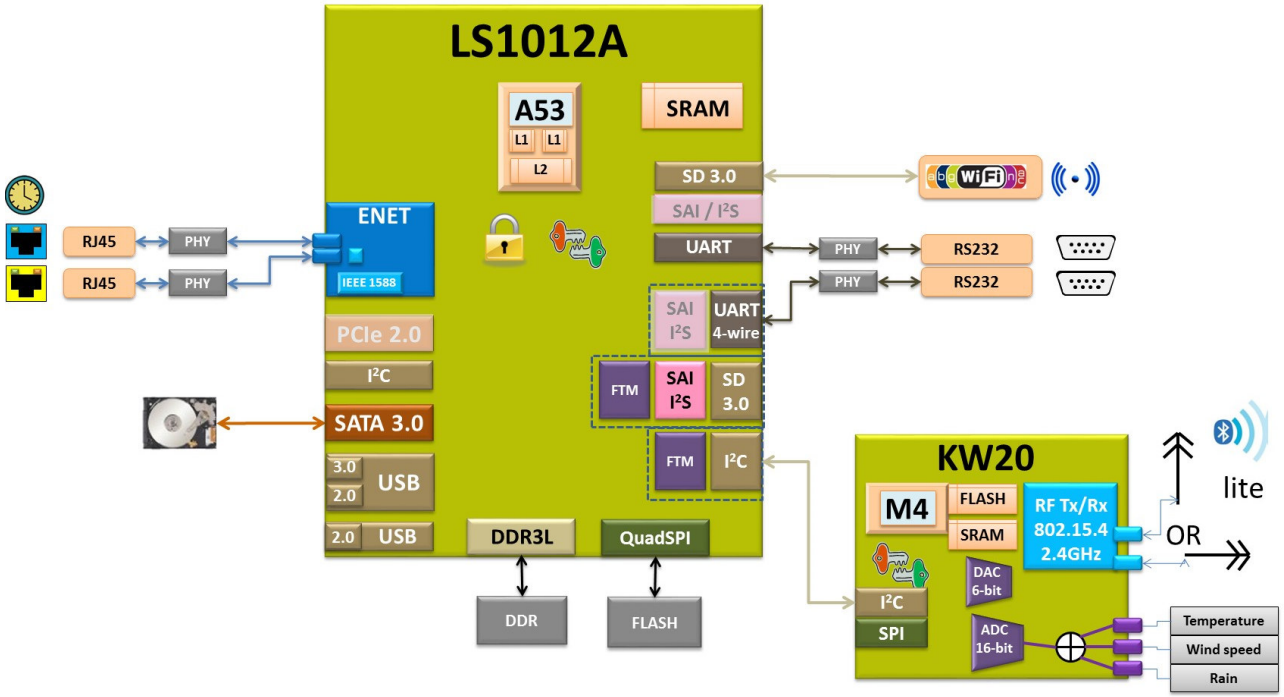


LS1012A Target Applications
Consumer NAS
Value tier IOT gateway
Battery Powered Mobile NAS
Entry BB Ethernet Gateway
Trusted Gateway
Industrial Automation & Control
Building Control systems
Ethernet Drives
Networked Audio

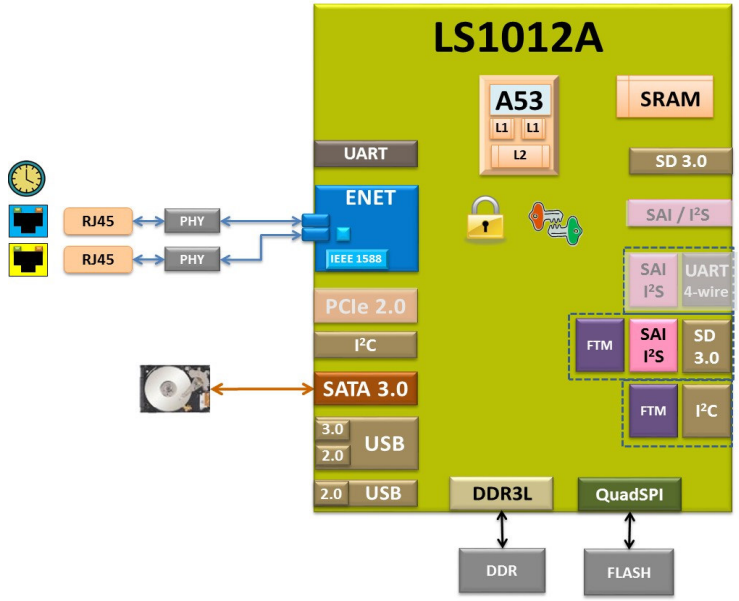
Use Case Examples

IOT Gateway Use Case

Value IOT Gateway

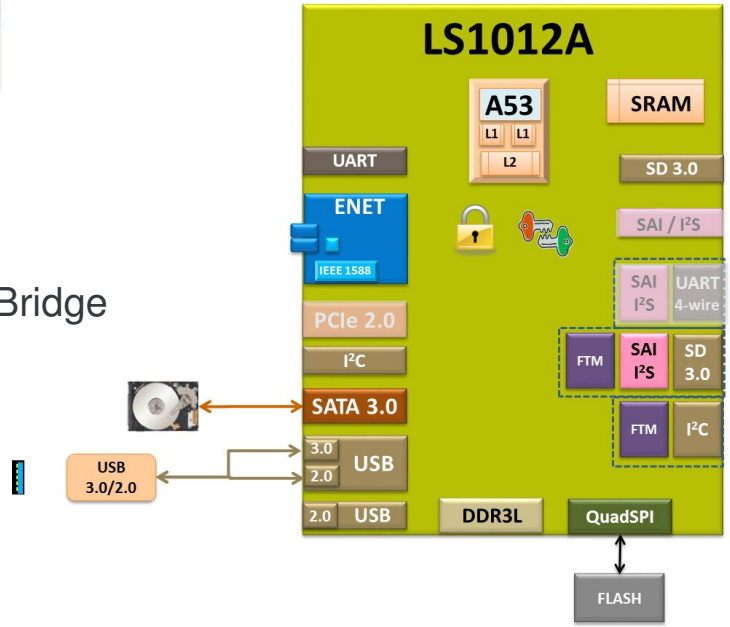


Ethernet Drive and USB to SATA DAS Use Cases

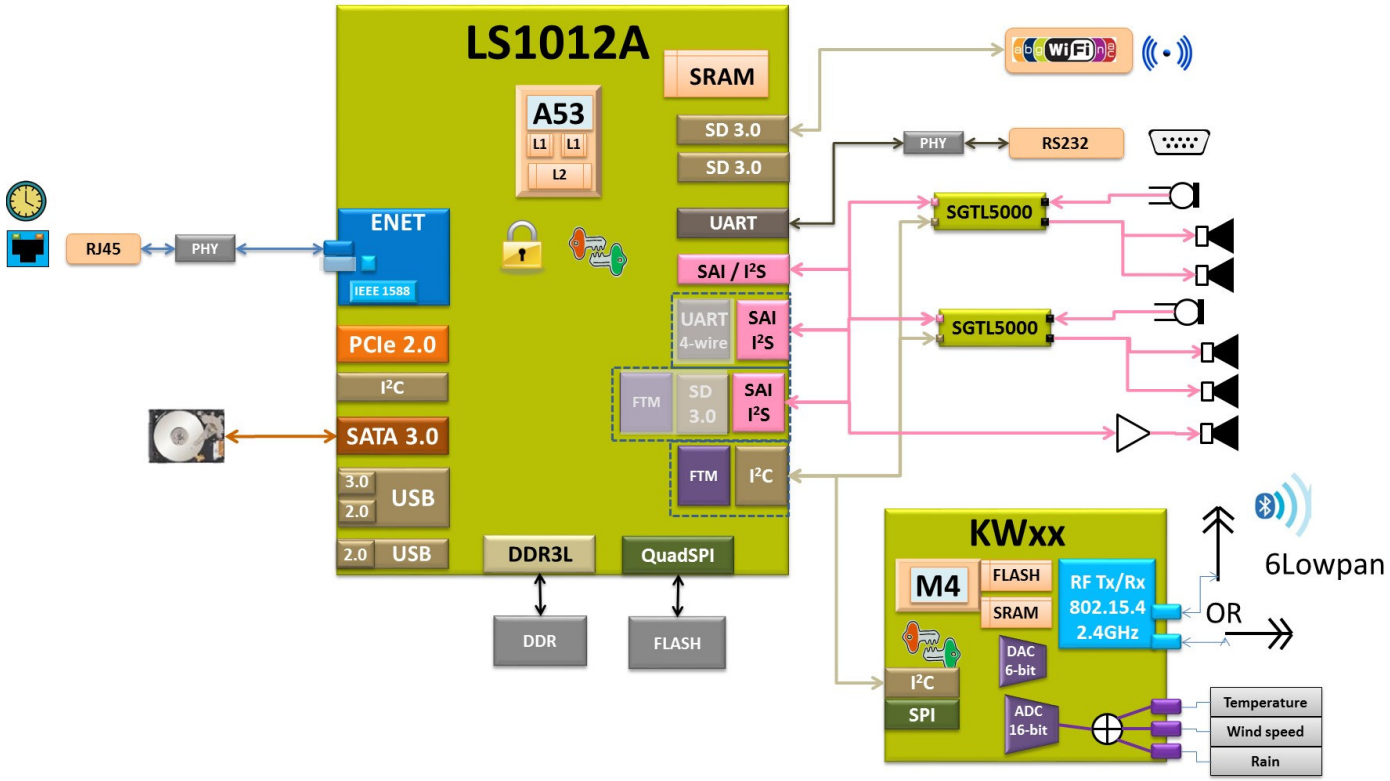


Ethernet Drive

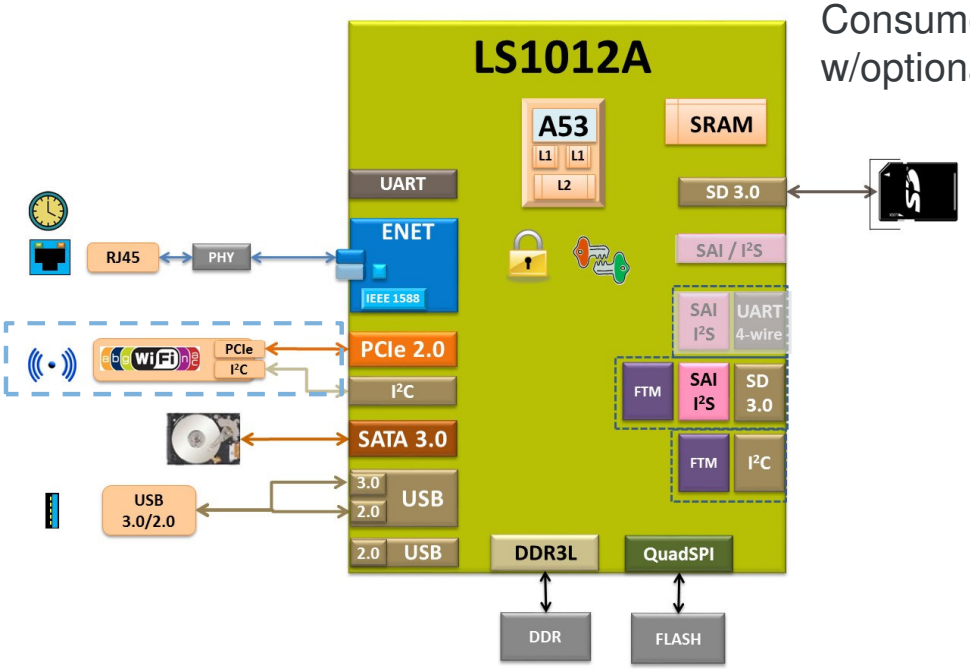
USB to SATA Bridge



Value IoT Gateway with Audio Networking

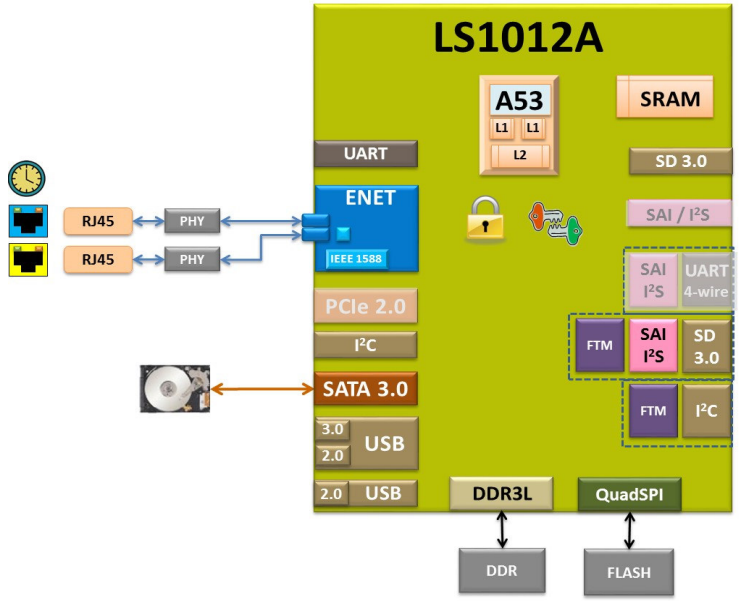


Consumer NAS/DAS Use Case



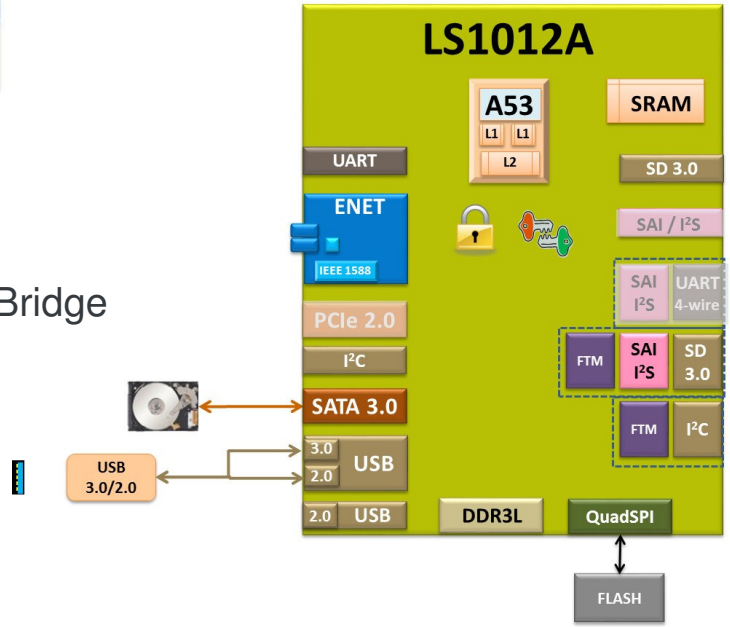
Consumer NAS/DAS
w/optional Wi-Fi

Ethernet Drive and USB to SATA DAS Use Cases

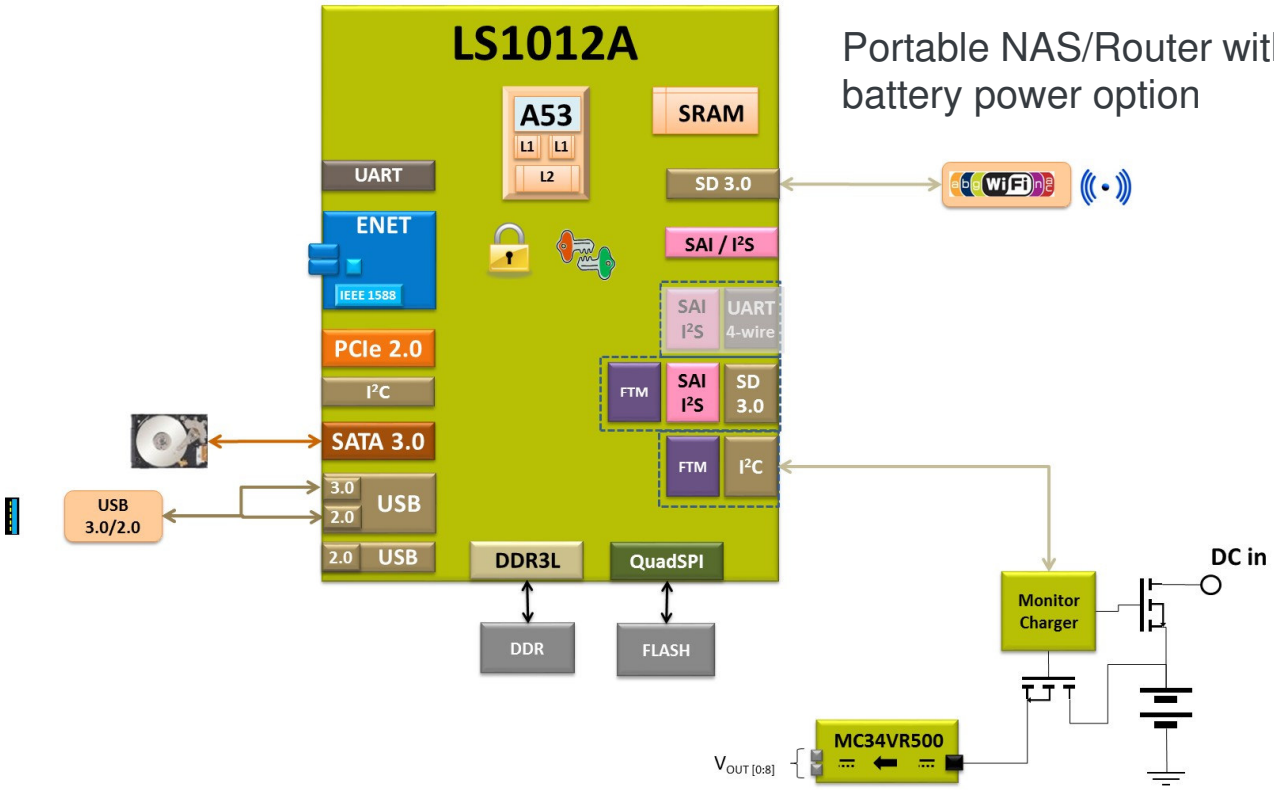


Ethernet Drive

USB to SATA Bridge

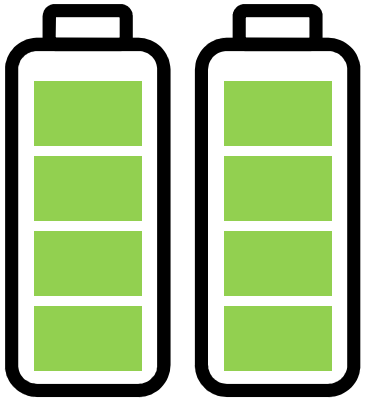


Battery Powered Portable NAS Use Case



LS1012A Power Management Features

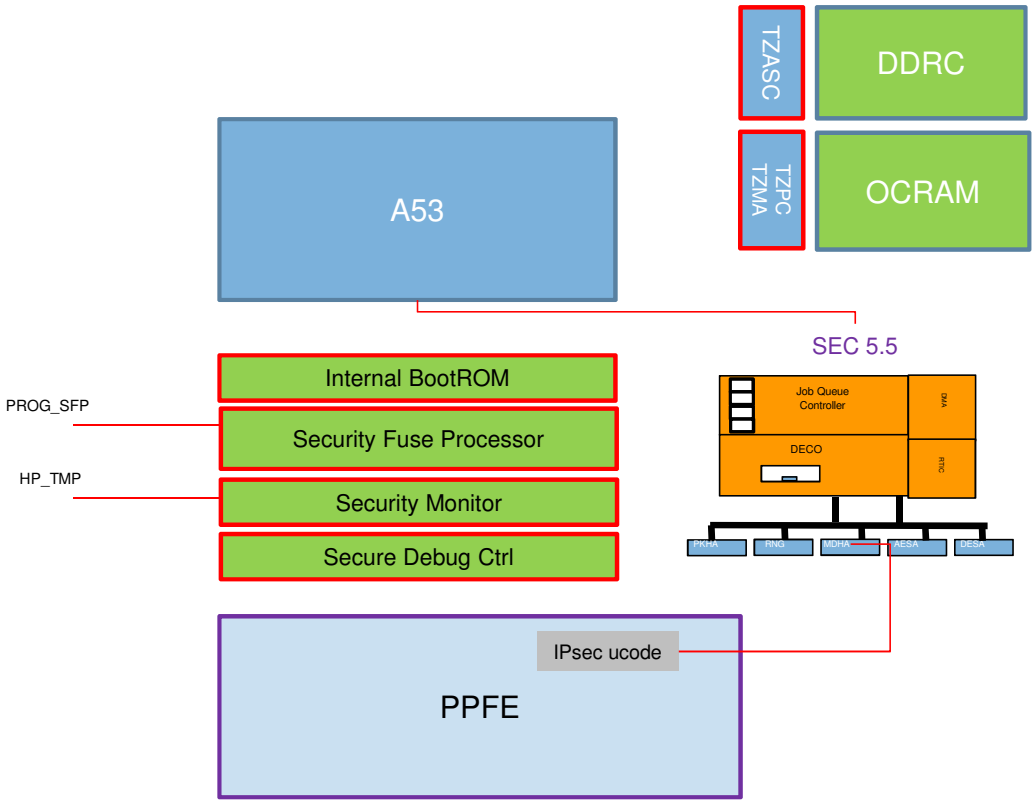
- Packet-forwarding engine offloads CPU and reduces power consumption
- Typical 1W power consumption when active
- Dynamic Frequency Scaling
- On-chip temperature monitor
- Clock-gating of major functional blocks



LS1012A Security & Trust Architecture Features

Security Capabilities Supported

- Secure boot – hardware root of trust
- Secure key handling
- Tamper detection
- Secure manufacturing
- Secure debug
- ARM® TrustZone
- Cryptographic acceleration



LS1012A Cryptographic Acceleration features

(1) Public Key Hardware Accelerator (PKHA)
- •RSA and Diffie-Hellman (to 4096b)
- •Elliptic curve cryptography (1024b)
- •Supports Run Time Equalization

(1) Random Number Generator (RNG)
- •NIST Certified
- •RNGB in P1010, RNG4 in PSC9131

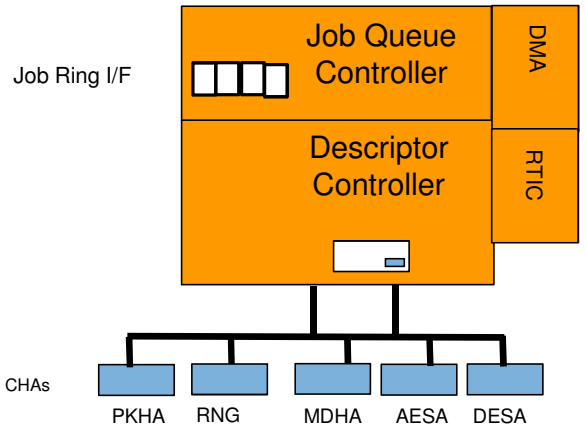
(1) Message Digest Hardware Accelerators (MDHA)
- •SHA-1, SHA-2 256,384,512-bit digests
- • MD5 128-bit digest
- •HMAC with all algorithms

(1) Advanced Encryption Standard Accelerators (AESA)
- •Key lengths of 128-, 192-, and 256-bit
- •ECB, CBC, CTR, CCM, GCM, CMAC, OFB, CFB, and XTS

(1) Data Encryption Standard Accelerators (DESA)
- •DES, 3DES (2K, 3K)
- •ECB, CBC, OFB modes

(1) CRC Unit
- •CRC32, CRC32C, 802.16e OFDMA CRC

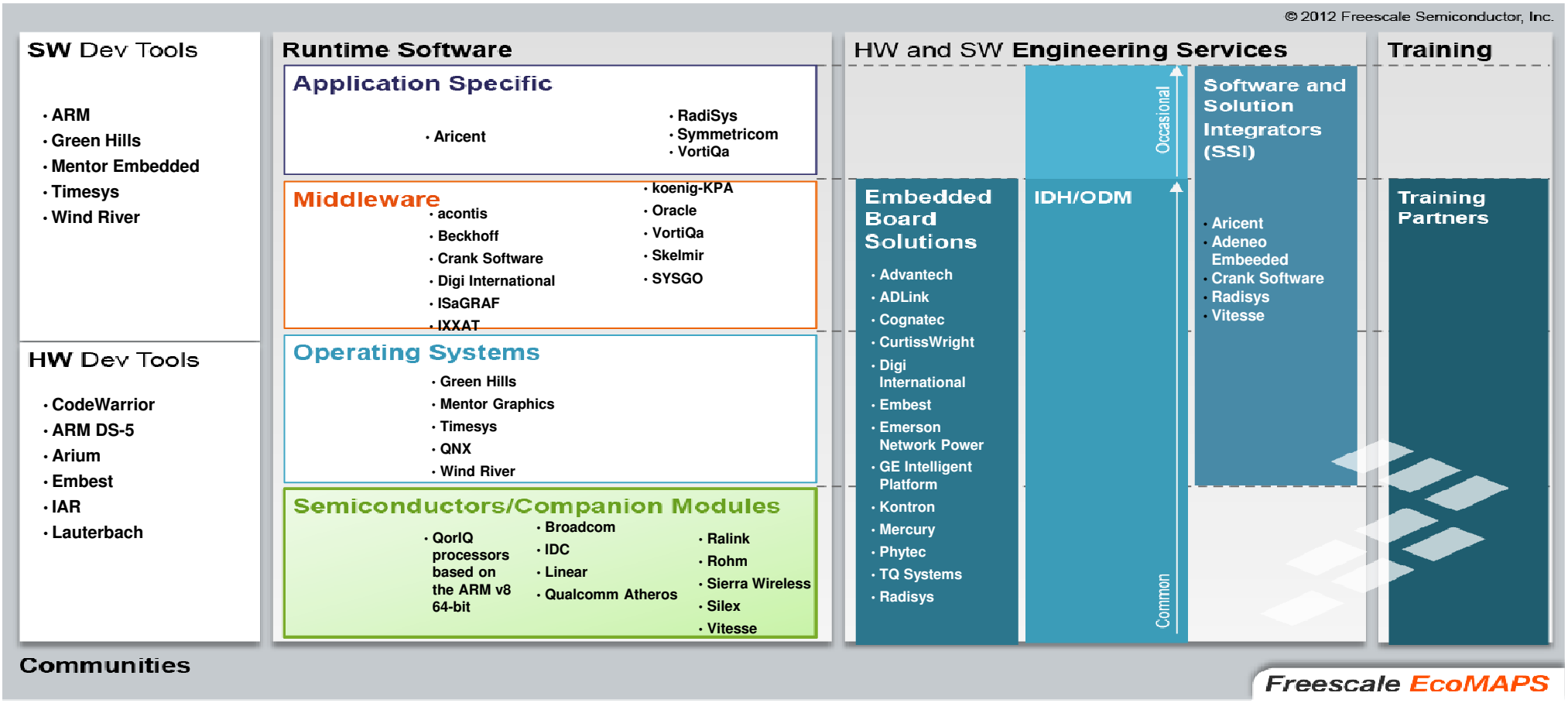
Header & Trailer off-load for the following Security Protocols:
- •IPSec, SSL/TLS, 3G RLC, PDCP, SRTP, 802.11i, 802.16e, 802.1ae



Function	Rate (Gbps)
AES	1.6
3DES	1.4
SHA-256	1.9
RSA	(TBD)
IPSec	1.6
IPSec @ (IMIX)	1.1

EcoMAP: QorIQ LS1012A

For more partner options, visit freescale.com/partners



SECURE CONNECTIONS
FOR A SMARTER WORLD