Time Sensitive Networking (TSN) and Precision Time Protocol (PTP): Challenges, Opportunities and Solutions

Jeff Steinheider

Product Marketing Manager – Industrial Applications
Digital Networking

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SECURE CONNECTIONS FOR A SMARTER WORLD

Agenda

- Why do we need PTP?
- Why do we need TSN?
- PTP Solutions
- TSN Solutions
- Questions

Why do we need PTP?

Synchronization

Synchronization

Many applications require synchronization with:

Wireless Systems	Industrial Control	Distributed Computing
• Frequency accuracy • Timing for transmission alignment	• Coordination of multiple machines • Synchronized communication	• Accurate time of day for distributed transactions

Options for Synchronization

	GPS	Shared Clock and Periodic Signal	TI/EI
Pros	• Available anywhere	• Low cost	• Covers medium distances
Cons	• Not effective inside buildings	• Limited to board level systems • Requires extra out of band signals	• Not useful in smaller systems • Less common due to increasing bandwidth requirements

The Answer: Precision Time Protocol

- Usable over multiple physical mediums – Ethernet, Wireless, etc.
- Covers metro and in-building
- Shares data networks and cabling
- Provides timing synchronization under 1 usec

Why Do We Need Time-Sensitive Networking (TSN)?

Determinism

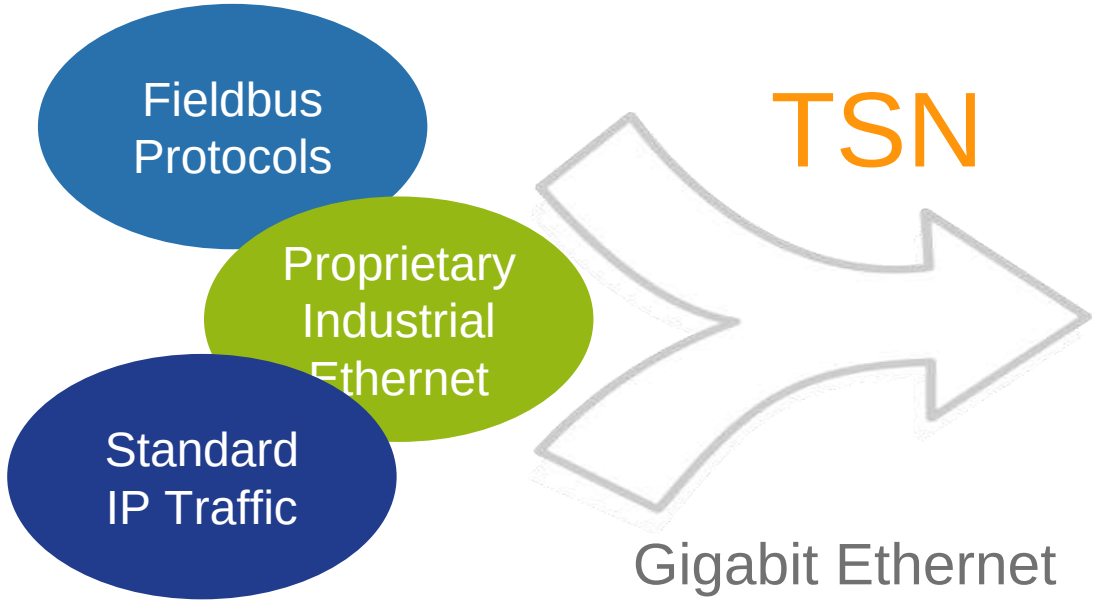
Ethernet is Great, But….

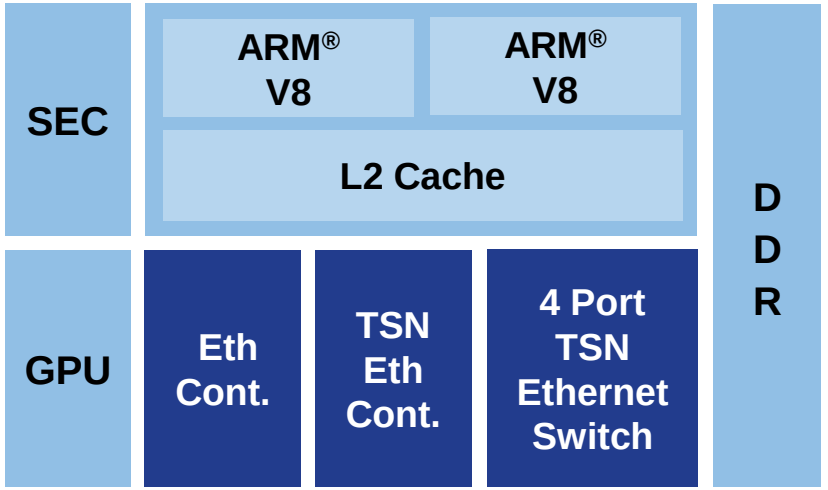
- Ethernet is ubiquitous for embedded systems
  - Standardized
  - Backward compatible – Auto-negotiation between 10/100/1G
  - Increasing bandwidth 1G -> 2.5G -> 10G -> 25G -> 100G

- But Ethernet only provides best-effort delivery

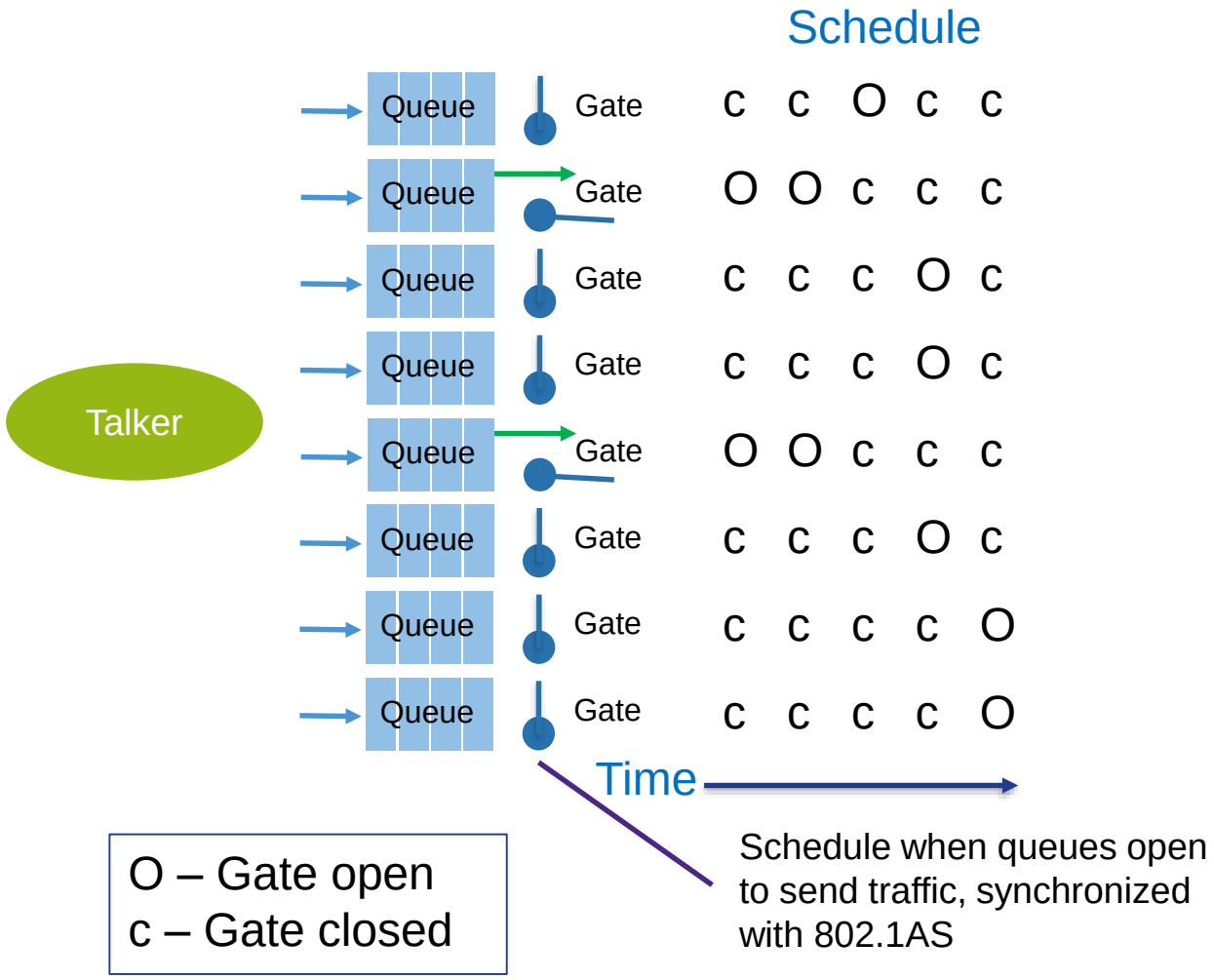
Embedded Time-Sensitive Networking (TSN)

- Converge OT and IT traffic in a single network
- Determinist Ethernet at gigabit speeds
- Reduce network delays, improve robustness
- Embedded in Multi-processor SoCs



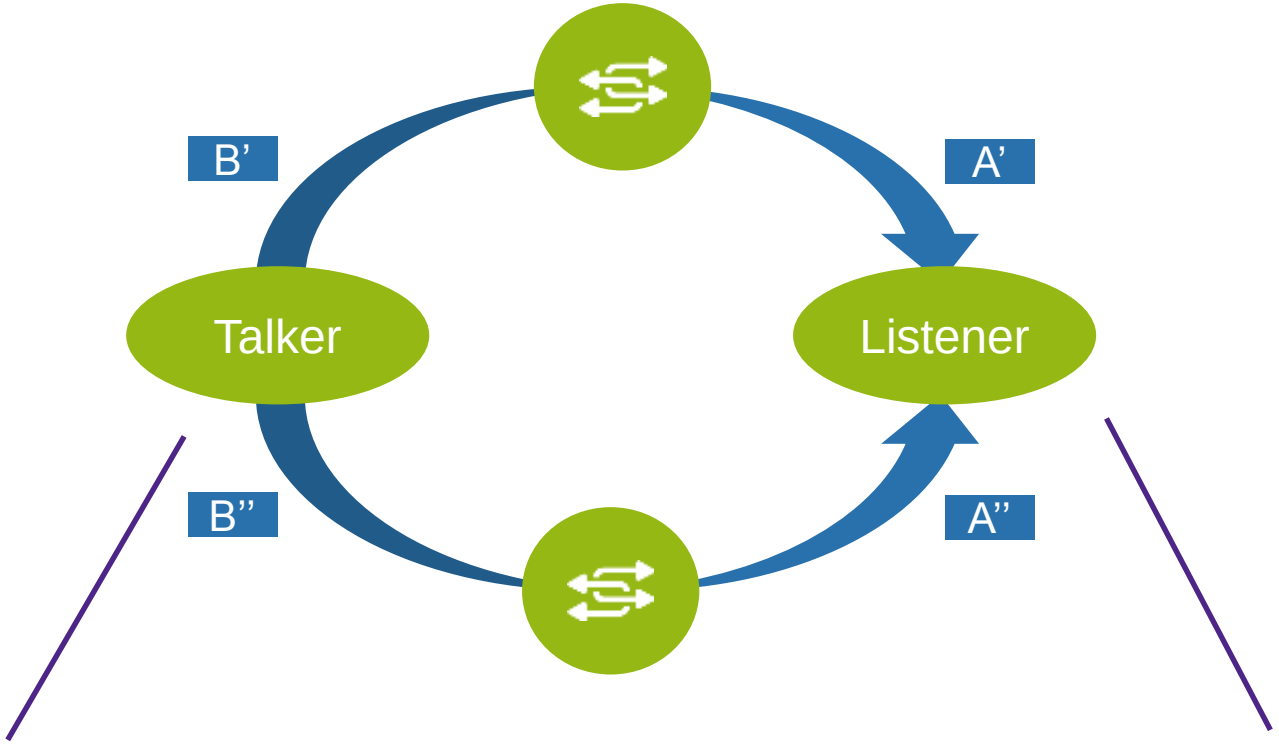


802.1.Qbv – Time Aware Shaping



- Different priority traffic allocated for each queue
- Queue gate schedule synchronized to global time
- 8 Queues available

802.1CB – Frame Replication and Elimination for Reliability



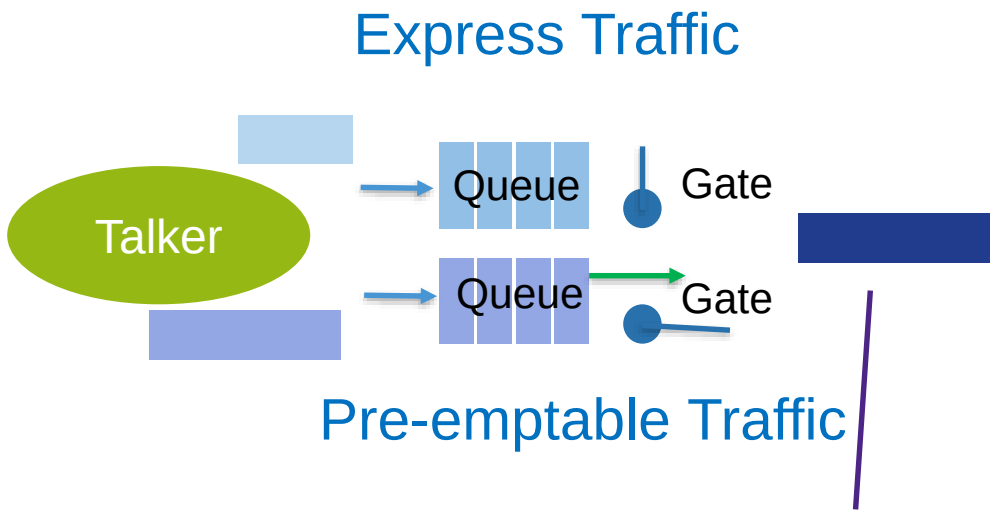
- TSN hardware performs replication/elimination
- Zero time failover if 1 path fails
- No need for upper level retry mechanisms
- Simpler code base with reliability

Talker replicates Ethernet frames and sends over multiple paths to Listener

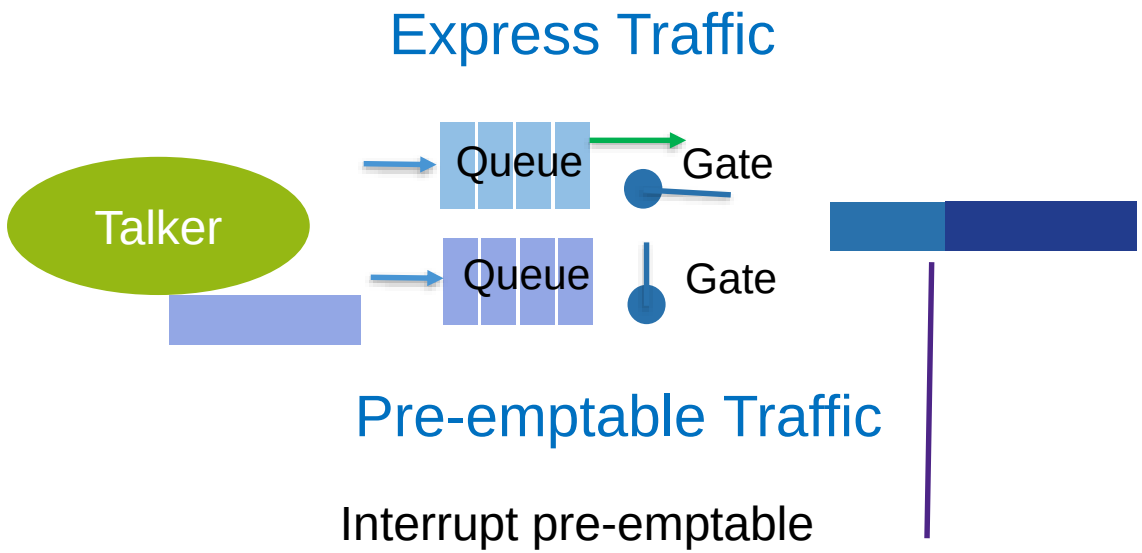
- Listener provides first Ethernet frame that arrives to application
- Listener removes duplicates

802.1Qbu – Frame Pre-emption

- Ensure zero delay for express traffic
- Efficient use of bandwidth for pre-emptable traffic
- Used with TAS, or stand-alone



Start to transmit frame of pre-emptable traffic



Interrupt pre-emptable frame with express frame. Will transmit remaining pre-emptable frame once express frame complete

PTP Solutions

Layerscape Arm® MPUs With IEEE 1588 Hardware

LS1046A
- Cortex-A72
- 2-4 cores
- 1.8GHz
- 1/10 G Ethernet, USB, PCI
- 10-12W

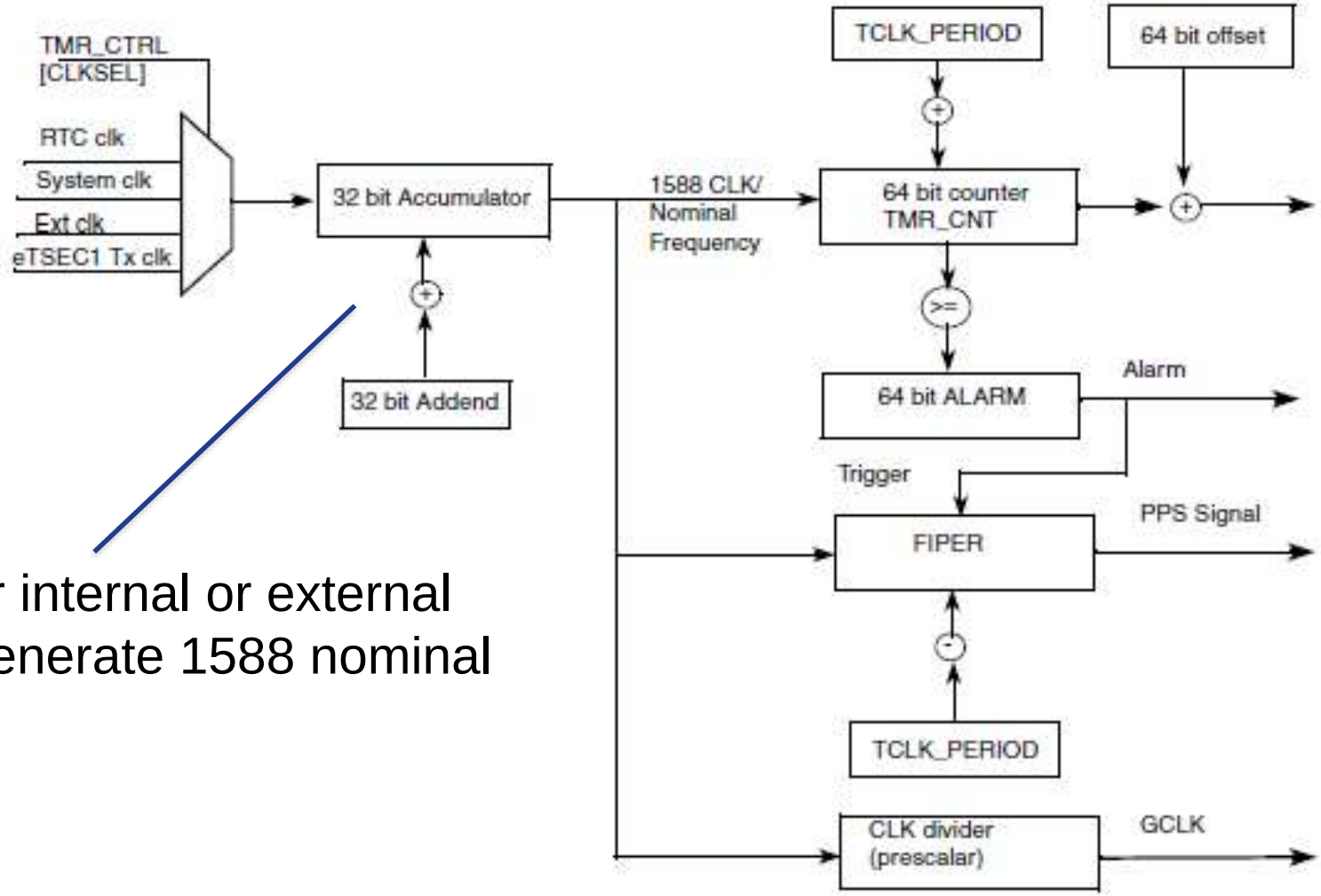
LS1028A
- Cortex-A72
- 2 cores
- 1.6GHz
- 4-9W
- *Integrated TSN switch*

LS1043A
- Cortex-A53
- 2-4 cores
- 1.6GHz
- 1/10G Ethernet, USB, PCI
- 5-10W

LS1021A
- Cortex-A7
- 2 cores
- 1.2GHz
- 2W
- Ethernet, USB, PCI

- Scalable family of ARM SoCs
- IEEE 1588 Hardware Time Stamping
  - Hardware 2-Step supported in all devices
  - 1-Step supported in LS1028 Family
- IEEE 1588 Timing Logic
  - Use internal or external clock source
  - Generate periodic phase aligned pulse signals for external devices

1588 Clock Circuits Available in Layerscape SoCs

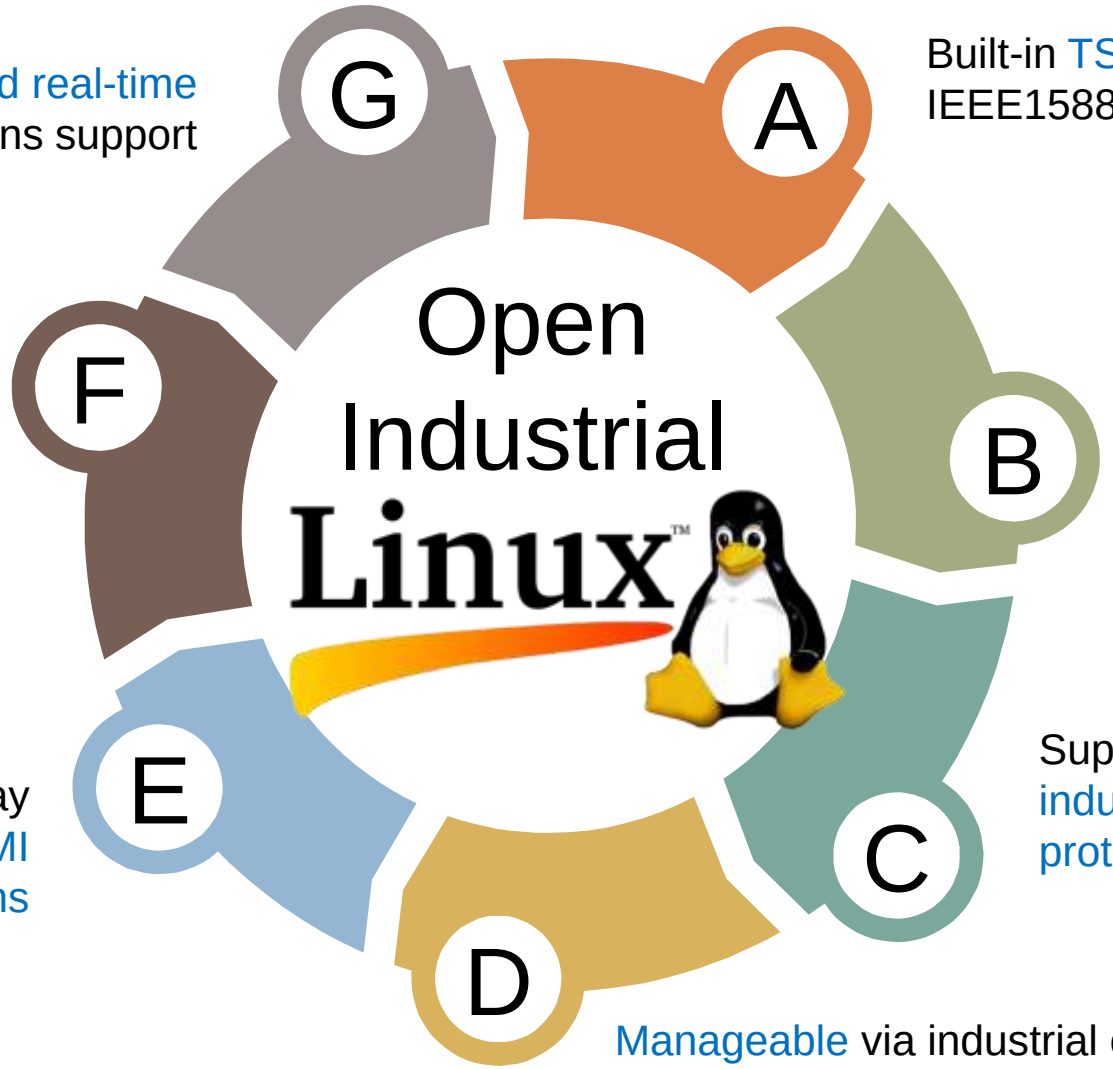


Use either internal or external clock to generate 1588 nominal frequency

Timestamping value used for Tx and Rx packets

Generate phase aligned periodic pulses

OpenIL.org



Hard real-time applications support

Built-in TSN and IEEE1588 Support

Open Software Repository and Community

Built-in industrial-grade security

Built-in graphic display support for HMI Applications

Support for various industrial networking protocols

Manageable via industrial control and networking protocols

IEEE 1588 for Timing Synchronization

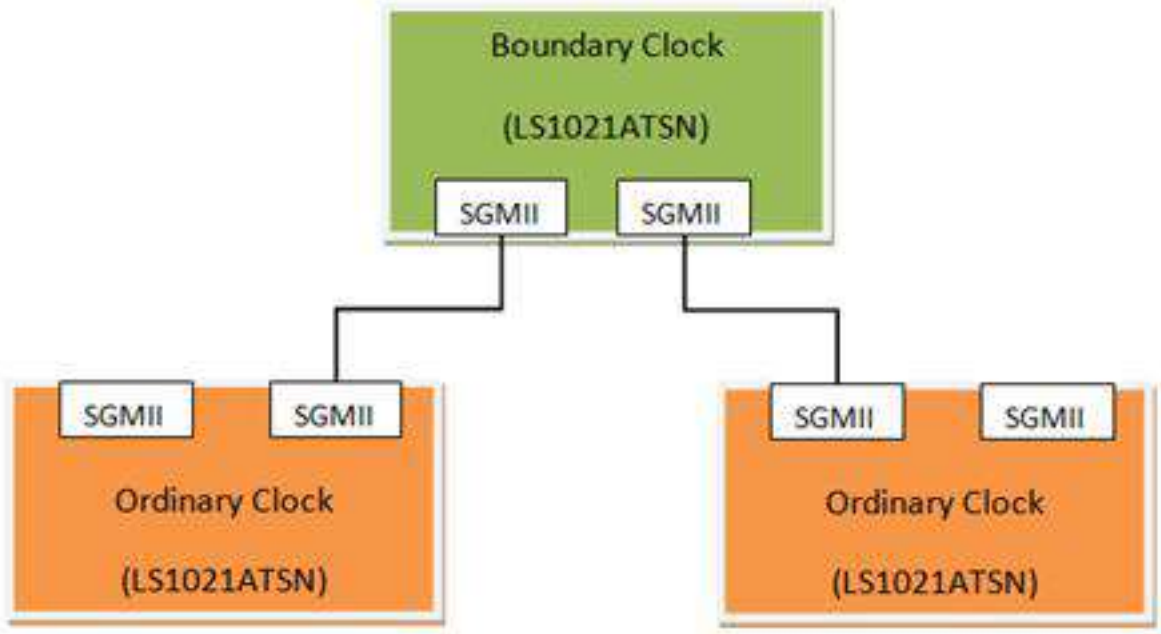
linuxptp support

LS1021A
LS1043A
LS1046A

Boundary Clock Mode

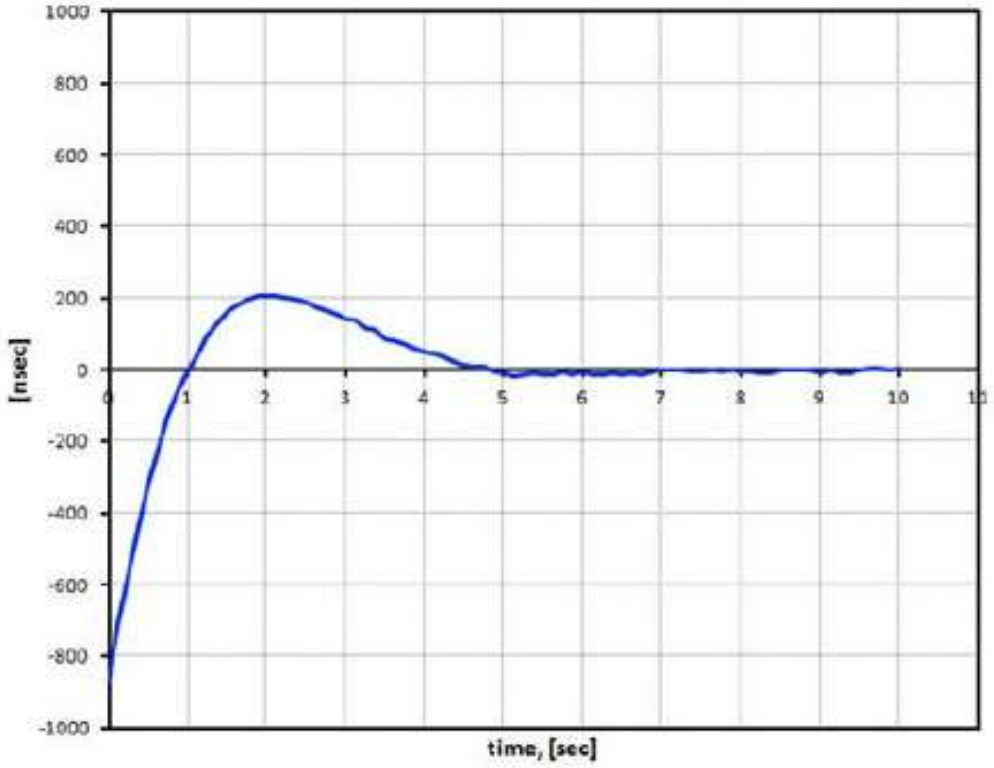
Synchronization within +/- 23 nsec for back to back boards

Example configurations and test results



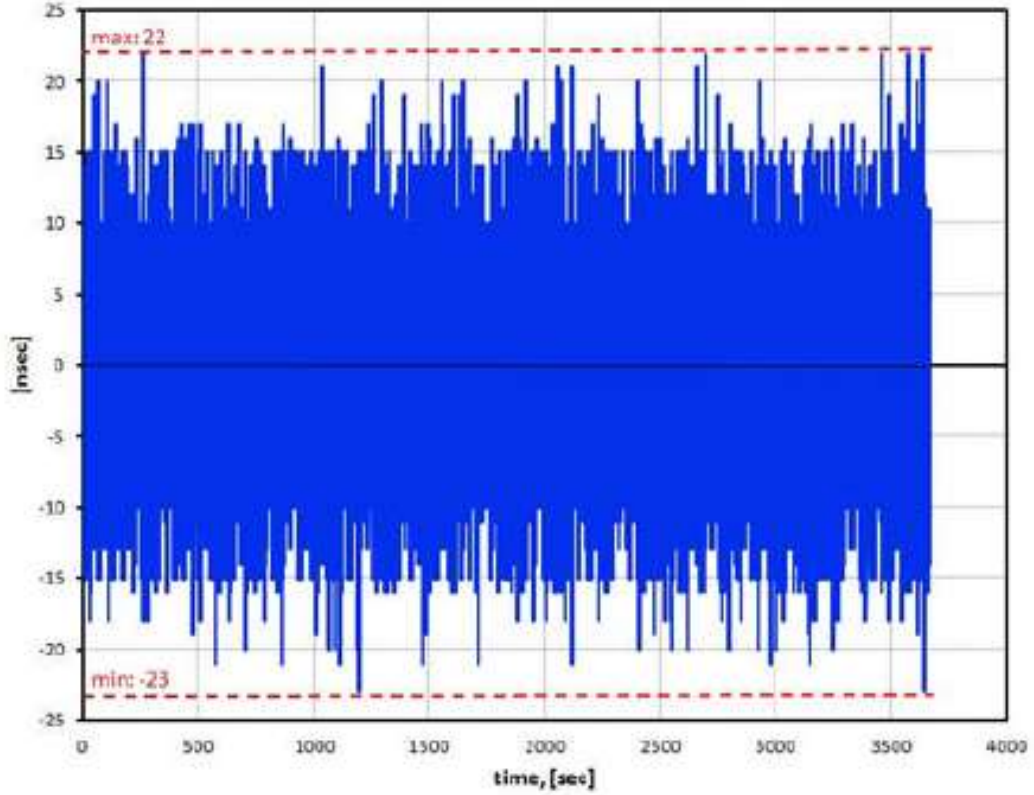
1588 Performance

Offset from Master, Startup



Timing settles within 5 seconds

Offset from Master, Stable State



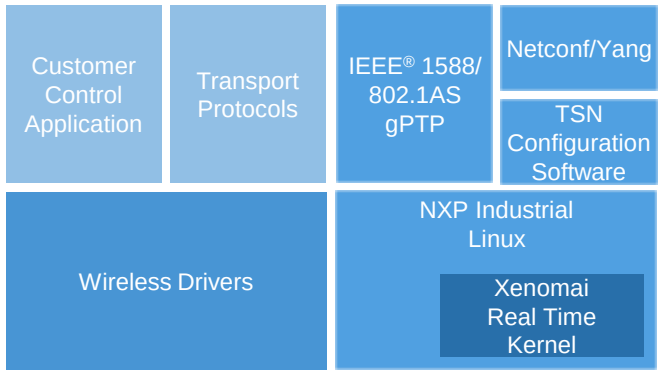
Accuracy within ±23 nsec

TSN Solutions

LS1021ATSN – TSN Solution Reference Design

- Synchronization with IEEE® 1588
- 4 Switched Gigabit Ethernet TSN interfaces
  - Time Aware Shaping
  - Per-Stream Filtering and Policing
- Arduino Shield for IoT Wireless Integration
- Expandable IO – mini PCIe, SATA, USB 3.0, SD Card, GPIO

TSN Solution



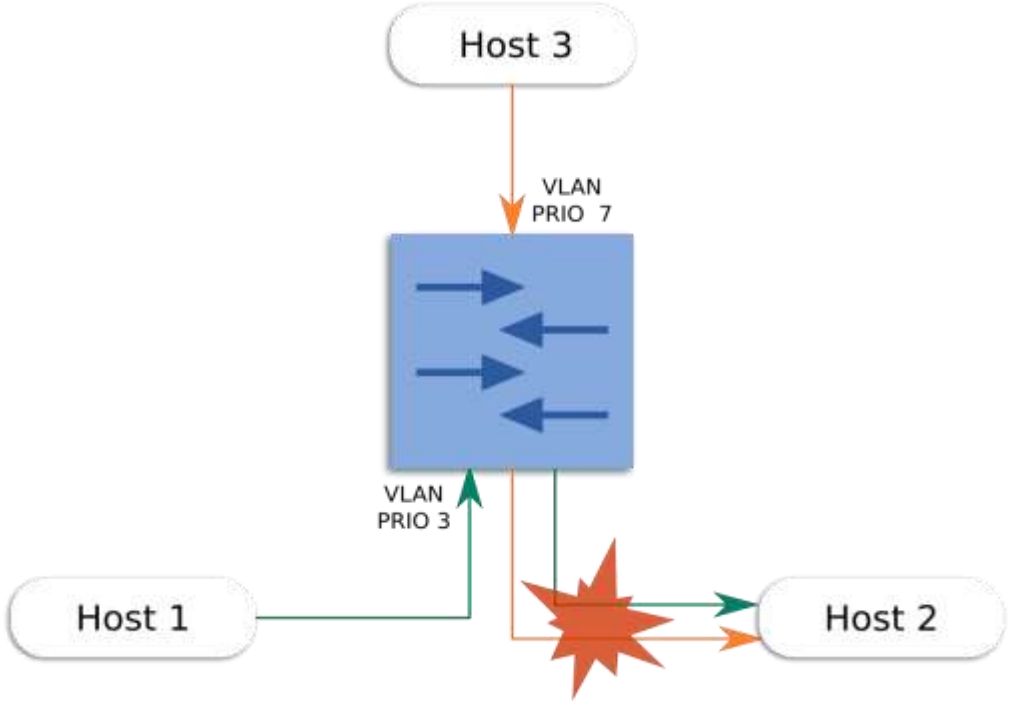
Industrial Linux SDK

LS1021ATSN Reference Design

Available Now – $829

Single Board TSN Demonstration

- 3 host Linux machines connected through a switch
- 2 TCP flows competing for bandwidth
- Flows bottlenecked because they are sharing the same link towards Host 2
- Combined throughput cannot exceed 1000Mbps
- Utilize TSN features to isolate flows
  - *Ingress Policing*: rate-limit traffic coming from Host 3
  - *Time Gating*: schedule the 2 flows on different time slots



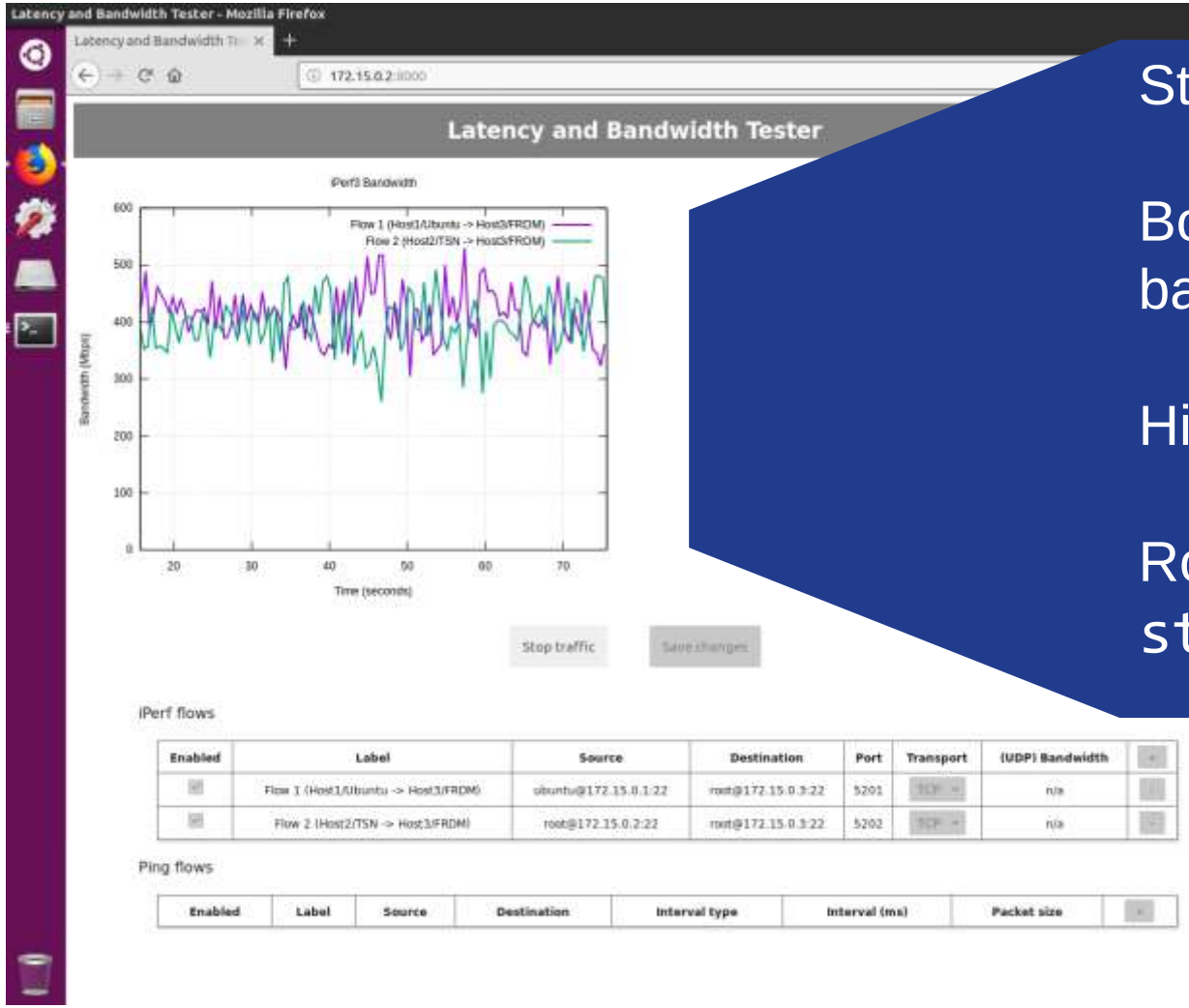
Demonstration Setup

LS1012A-FRDM

LS1021ATSN

ubuntu

Standard Ethernet Switch Settings



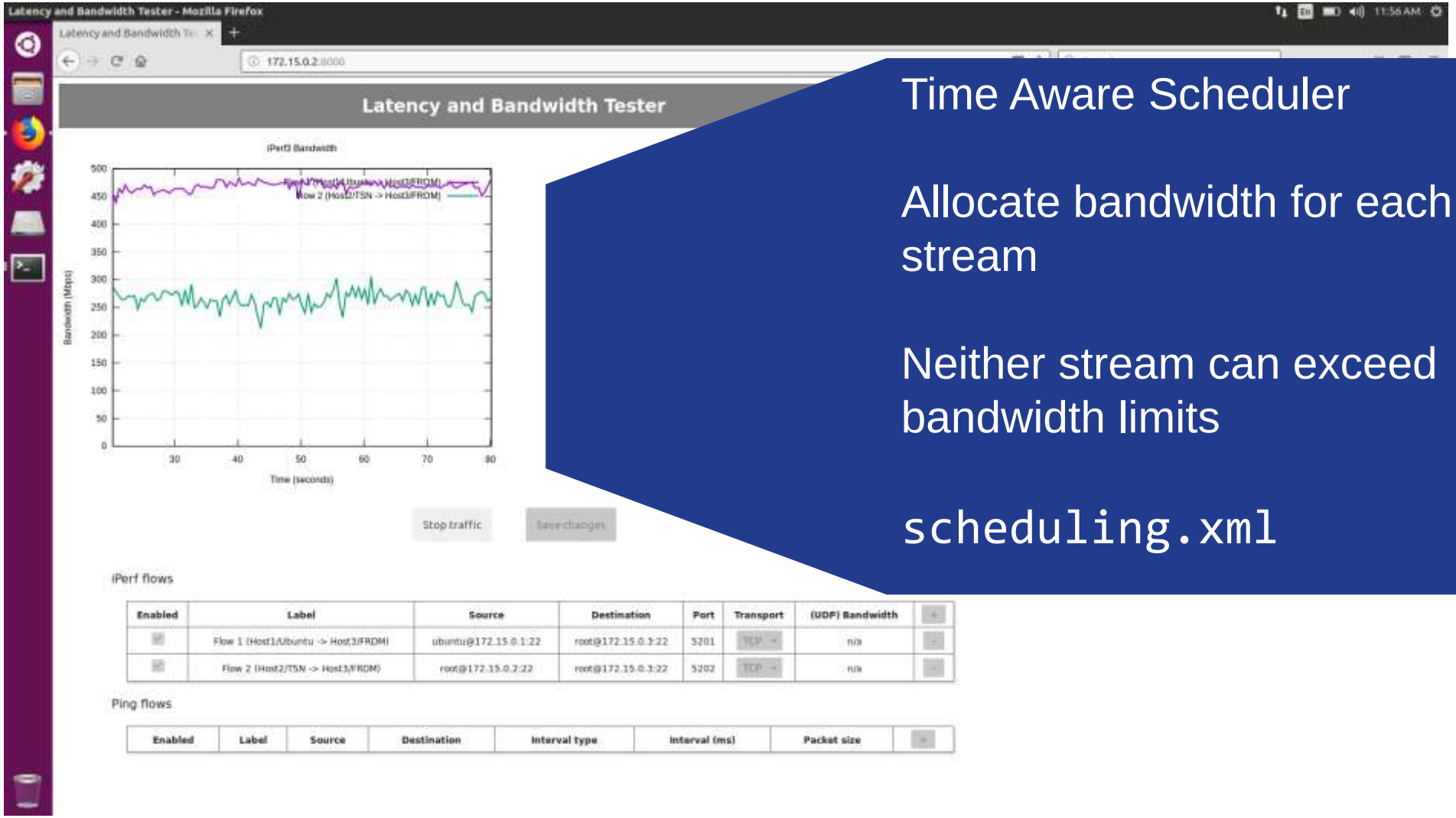
Standard Switch Settings

Both streams compete for bandwidth

High variation

Roughly equal distribution `standard.xml`

Time Aware Shaper



Time Aware Scheduler

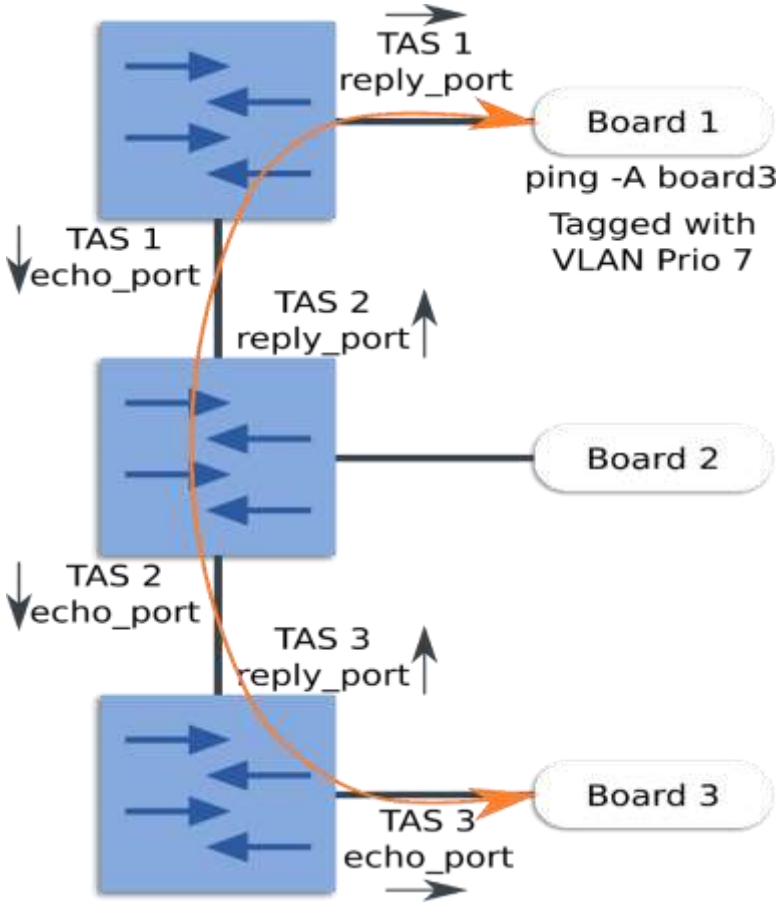
Allocate bandwidth for each stream

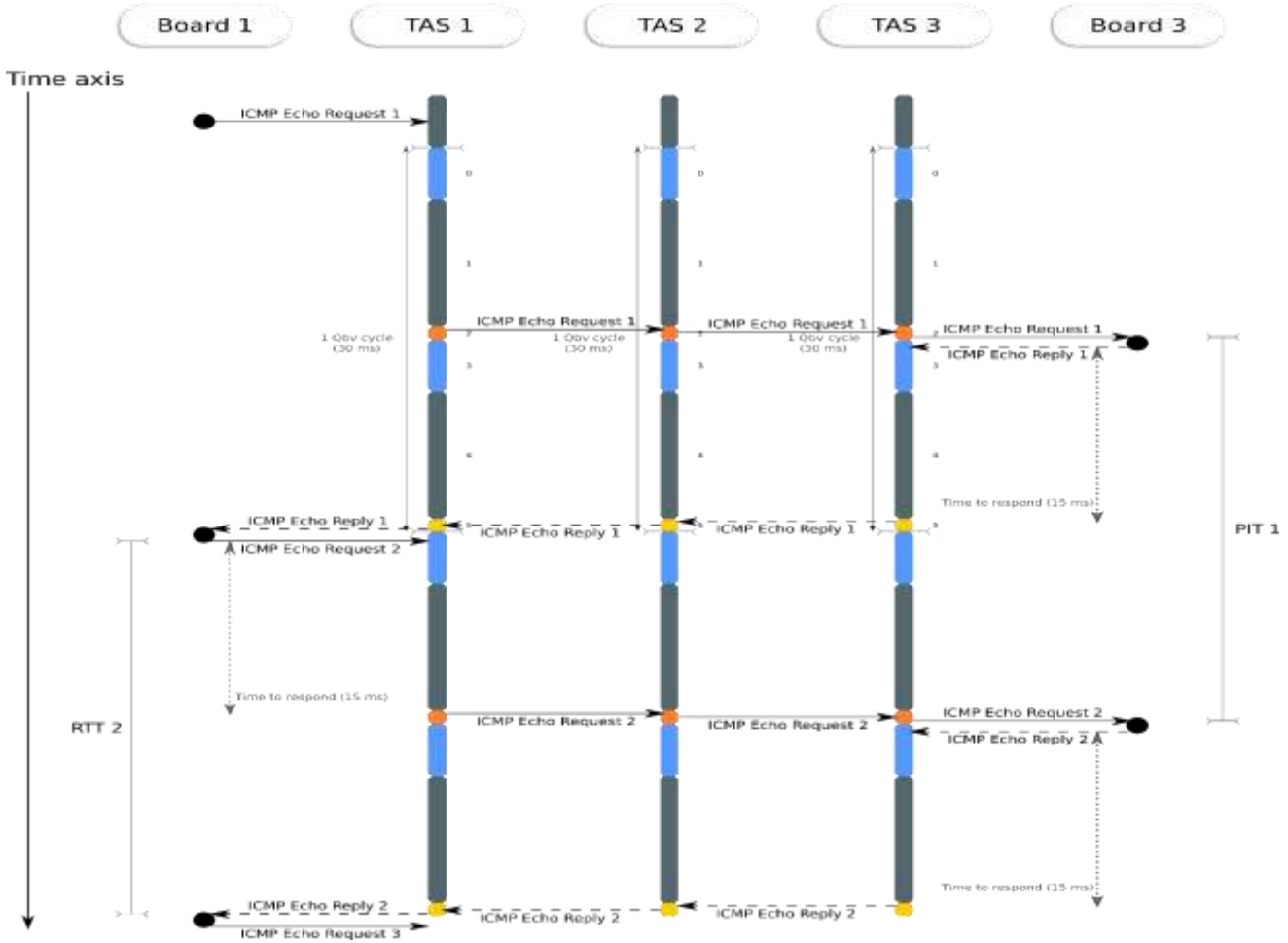
Neither stream can exceed bandwidth limits

`scheduling.xml`

Synchronizing Multiple Time Aware Shapers

Traffic goes through 3 TAS

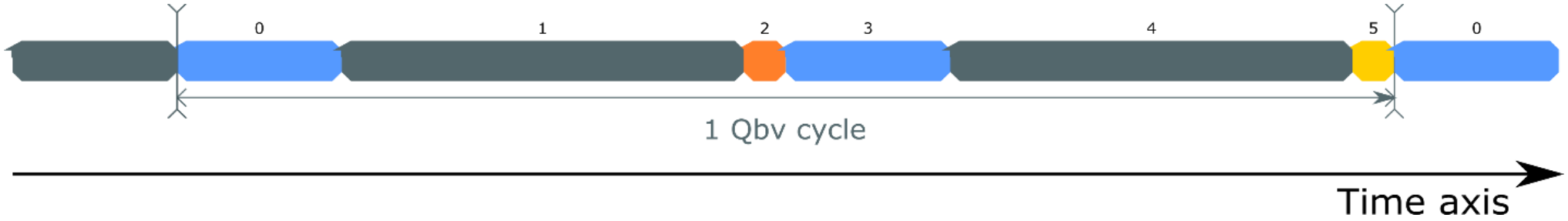




Synchronized Qbv – Configuration

Configuration found in *src/helpers/configs/synchronized-qbv/qbv-ptp.sh*

- Time slots 2, 5 – only gate 7 open for ICMP request / reply
  - 0 (4ms), 1(10ms), 2(1ms), 3(4ms), 4(10ms), 5(1ms)

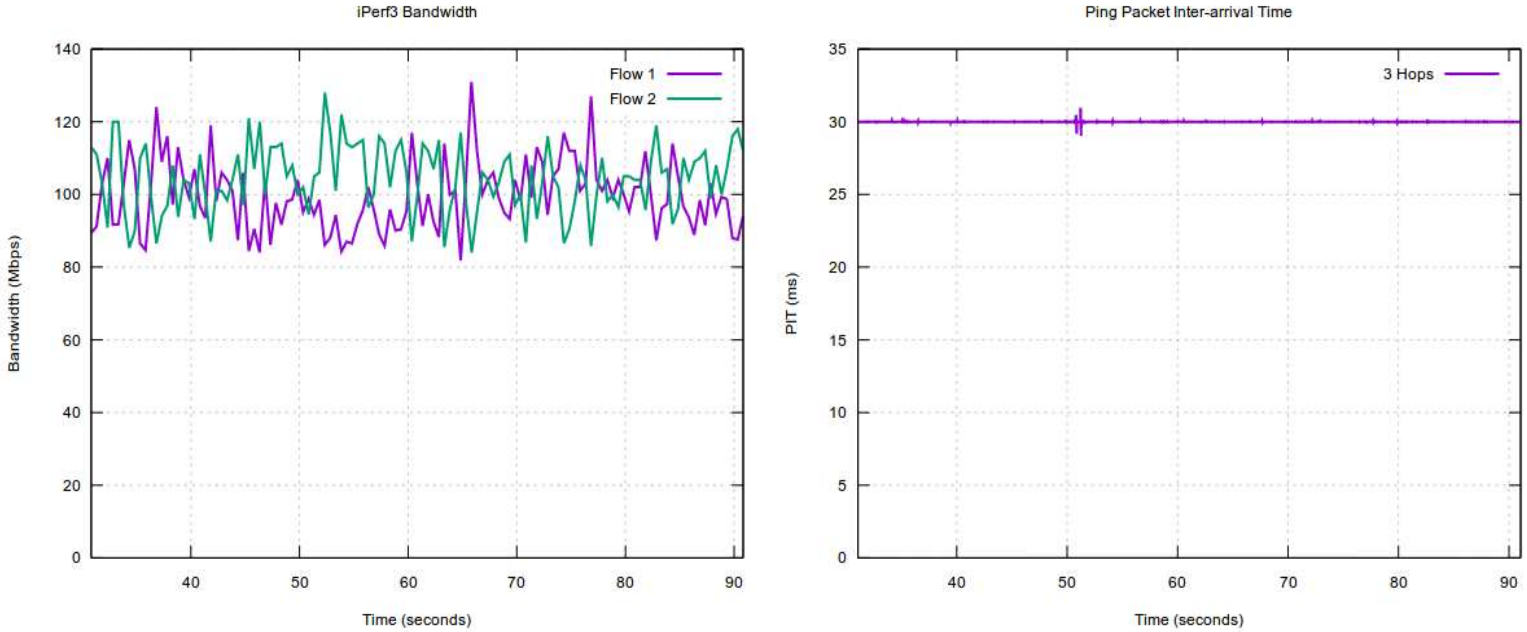


- Using adaptive ping
  - Sending interval of ping will adapt to the RTT of the TSN network
- Guard band roles
  - Reduce jitter while forwarding ping(ensure no other packets are enqueued on egress port; its an alternative to 802.1Qbu Frame preemption)
  - Let the SoC cores finish process the packets signaled by the Rx interrupts. (e.g if it will not process a ping request until subschedule 5, an entire cycle will be lost and the PIT will change)

Synchronized Qbv – Multiple TAS

Traffic flows

- Flow 1 (iPerf)
- Flow 2 (iPerf)
- 1 Hop (Ping)



Adaptive Ping from Board 1 to Board 3 (over VLAN-tagged TSN network)

Start TSN on LS1021A-TSN – Enhance with LS1028A

LS1021A-TSN

TSN Features

- Time Aware Shaper (802.1Qbv)
- Per-Stream Filtering & Policing (802.1Qci)
- Credit Based Shaper (802.1Qav)
- Time Synchronization (802.1AS)

LS1028A

New TSN Features

- Frame Pre-emption (802.1Qbu)
- Frame Replication and Elimination (802.1CB)
- Cut-through Switching
- Cyclic Queuing and Forwarding (802.1Qch)
- 802.1AS-Rev

Supported by one SDK – Open Industrial Linux

LS1028 Reference Design with TSN

LS1028A SoC

- 2x A72 cores running at 1.3 GHz
- 4 GB DDR4 w/ ECC at 1600 MTPS

Boot Sources and Storage:

- 2x 256MB QSPI NOR FLASH for alternating boot sources
- SD Card for fast firmware and demonstration updates
- 8 GB eMMC for Filesystem Storage

General availability Q4 2018

LS1028A Reference Design

Front Panel

2x CAN FD Interfaces

2x UART

Back Panel

Full Size SD Card Slot

Up to 4K Display via DisplayPort

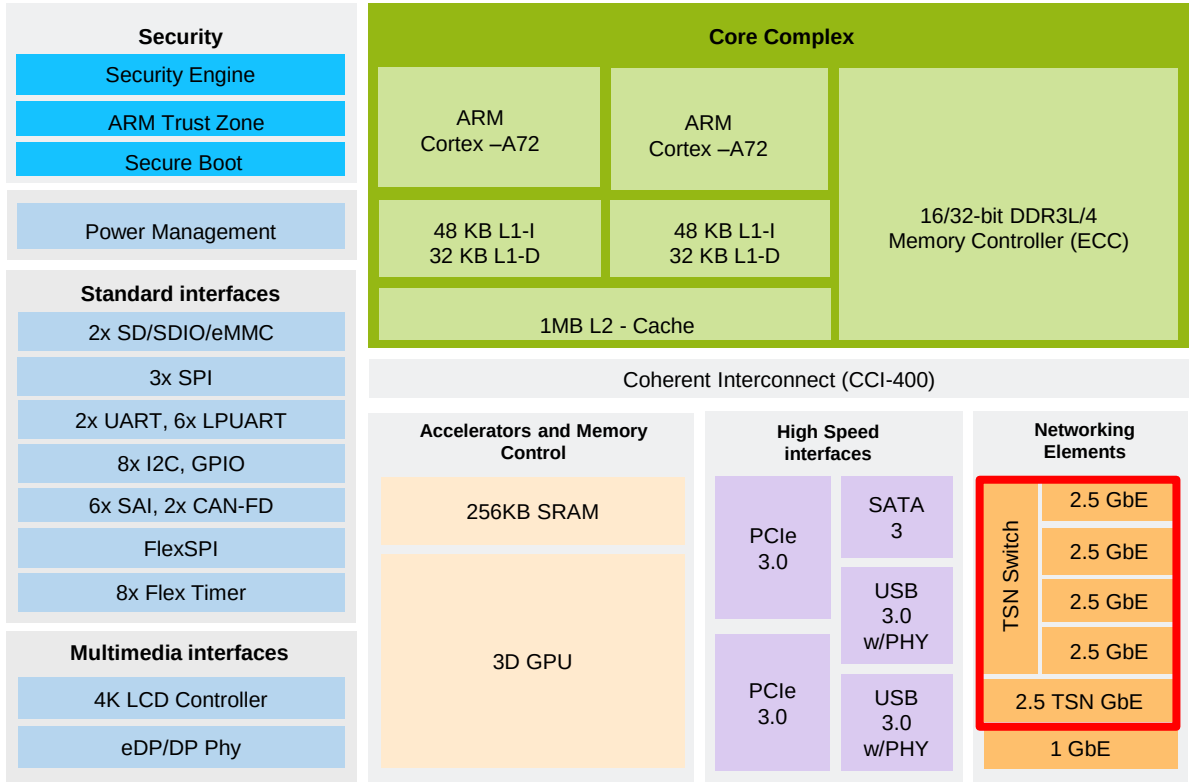
USB 3.0 Type C and Type A

1G/100M/10M TSN Ethernet Controller

4 Switched 1G/100M/10M TSN Ethernet Ports

Compelling Combination of IO, Computing and TSN

LS1028A: Dual ARM Cortex A72 Processor



Target Applications:

- Industrial Control, PLCs, Gateways
- Automotive
- Professional Audio/Video
- IoT Gateways
- Human Machine Interface

Package

- 17x17mm, 0.75mm pitch FC-PBGA

Core complex

- 2x 64-bit Cortex-A72 with Neon SIMD engine
- Speed up to 1300 MHz
- Parity and ECC protected 48 KB L1 instruction and 32 KB L1 data cache
- 1 MB L2 cache with ECC protection

Basic peripheral and Interconnect

- 2x USB 3.0 OTG controllers with integrated PHY
- 2x eSDHC controllers supporting SD/SDIO 4.0
- 2x CAN-FD controllers
- 8x UART serial ports

Networking elements

- Four Port TSN Ethernet Switch up to 2.5 Gbps on each port
- Up to four SGMII supporting 1 Gbps
- Up to one USXGMII supporting 2.5 Gbps
- Up to one QSGMII
- Up to one RGMII
- 2x PCI Express Gen 3 controllers
- 1x SATA Gen 3.0 controller

Accelerators and Memory Control

- 1x 16/32-bit DDR3L/4 Controller with ECC support up to 1.6 GT/s
- Time Sensitive Networking (TSN) Ethernet Switch
- Security Engine (SEC)
- QorIQ Trust architecture: Secure boot, ARM Trust zone and security monitor

Qualification

- Commercial and extended temperature (support for 125C Tj)

Power

- 5W TDP

Precision Time Protocol and Time-Sensitive Networking

- Achieve synchronization accuracy within 10s of nanoseconds
- 1588 hardware timestamping and time logic available in Layerscape processors
- TSN provides many features for reliable, guaranteed delivery of packets
- New LS1028A SoC will offer integrated TSN and features for Industrial Automation, Audio/Video, and IoT applications

References and Additional Information

- Open Industrial Linux User Guide
- Application Note: AN3423 – Support for IEEE™ 1588 Protocol in PowerQUICC and QorIQ Processors
- LS1021ATSN Reference Design Board
- LS1028A Layerscape SoC with integrated TSN

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