GNU Tools for e200 processors

Release Notes

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1 Release description

This release of gcc for e200-VLE supports the "Power Architecture® 32-bit Application Binary Interface Supplement 1.0 - Embedded". It is based on gcc 4.9.2, binutils 2.24 and gdb 7.8.2.

The current release supports VLE codegen for

- e200z0
- e200z2
- e200z3
- e200z4
- e200z6
- e200z7

It has built-in MULTILIB support for the e200 with soft-float or the Embedded FPU, libraries also support single precisiom double folding (`-fshort-double`) and the SPE.

This distribution provides support for newlib, newlib-nano and Freescale EWL2. Since distinct libraries are provided, the tools require setting explicitly `--sysroot` to perform MULTILIB resolution:

–sysroot=INSTALL/powerpc-eabivle/newlib for newlib

–sysroot=INSTALL/ewl2 for EWL2

2 What's new

This version 1.1.3 contains critical fixes for issues found in 1.1.2

Fixed:

- [ENGR00382613] Typo in extendqisi2 in md causes wrong codegen with se_extsb

3 New features

3.1 Mixed BookE and VLE code assembly and linking

Use `-mno-vle` key to force BookE codegen, even if `-mvle` key is used. For mixed VLE & BookE code corresponding linker script shall be provided.

For example:

```
.text_booke :  INPUT_SECTION_FLAGS (!SHF_PPC_VLE) *(.text*)  > text_e
.text_vle :   INPUT_SECTION_FLAGS (SHF_PPC_VLE) *(.text*)  > m_text
```

First line will force pick non-VLE .text sections. Second line will force pick VLE .text sections.

3.2 BookE to VLE translation

Use `-Wa,-ppc_asm_to_vle` option to enable translation for assembler file. Option requires `-mvle` option. Following BookE instructions can be translated:

> addi addic addic. addis andi. andis. b bc bcl bctr bctrl bdnz bdnzl bdz bdzl beq beql bf bfl bge bgel bgt bgtl bl ble blel blr blt bltl bne bnel bng bngl bnl bnll bns bnsl bnu bnul bso bsol bt btl bun bunl clrlslwi clrlwi clrrwi cmpi cmpli cmplwi cmpwi crand crandc crclr creqv crmove crnand crnor crnot cror crorc crset crxor extlwi extrwi inslwi insrwi isync lbz lbzu lha lhau lhz lhzu li lis lmw lwz lwzu mcrf mfdec mtdec mulli nop ori oris rfi rlwimi rlwinm rlwnm rotlw rotlw. rotlwi rotrwi sc slwi srwi stb stbu sth sthu stmw stw stwu subfic subi subic subic. subis xnop xori

Follwoing VLE-compatible instructions can be translated to shorter form:

> mr or

3.3 SPE v2 instruction support

Use `-mspe2` option to enable SPE2 insrtuctions support in assembler. SPE2 instructions can be used by assembler inline syntax or pure assembler. For example:

```
__asm("evdotpwcssi 0, 1, 2");
```

List of supported SPE2 instructions can be found in Freescale SPE2PIM Rev.2 08/2011 document.

See current GCC limitations for SPE2 in Chapter 4 [Known issues], page 5

3.4 Generate error for e200z425 errata

There's a problem with the e200z425 cores.

The problem occurs at any page with offset 16K + 2 when a long branch with a target displacement of 0x3ffe is preceded by a 32 bit instruction. The code needs to be relinked to be located at another address.

If you want just to disable this error use option `-Wl,-no-e200z425-rel-error`

4 Known issues

SPE2 limitations:

- SPE2 intrinsic functions are not implemented.
- Disassembler doesn't show SPE2 instructions mnemonics.

5 Release history

Version	Date	Description
1.0	27 November 2015	See Section 5.1 [1.0], page 7
1.1	8 June 2016	See Section 5.2 [1.1], page 7
1.1.1	23 June 2016	See Section 5.3 [1.1.1], page 8
1.1.2	10 August 2016	See Section 5.4 [1.1.2], page 8
1.1.3	7 September 2016	See Chapter 2 [What's new], page 2

5.1 Version 1.0

5.2 Version 1.1

Fixed:

- [ENGR00377284] Compiler uses stswi/lswi instructions even if they are not supported by e200 when -Os -O3 switches are enabled.
- [ENGR00377271] Decorated storage instructions should be supported
- [ENGR00374776] Bitfield write access could be optimized to shorter data type write instr
- [ENGR00373844] Incorrect code generation for the C expression with optimization level 0.
- [ENGR00373558] Support /dev/null on Windows for Ecos config tool

Changes:

• Following instructions marked as VLE according to PowerISA 2.07b:

evlddepx evstddepx e_sc se_rfgi sld sld. srad srad. srd srd. stbcx. stbdx stddx stfddx sthcx. sthdx stvebx stvehx stvepx stvepxl stvewx stwdx vcmpbfp. subfo subfo. subfmeo subfmeo.

• Changes in accordance with EFP2_rev1.4_spec.pdf:

  – Moved opcodes for

    efdcfsid efdcfuid efdctsidz efdctuidz

  – Added missed instructions

    evfssqrt evfscfh evfscth evfsmax evfsmin evfsaddsub evfssubadd evfssum evfsdiff evfssumdiff evfsdiffsum evfsaddx evfssubx evfsaddsubx evfssubaddx evfsmulx evfsmule evfsmulo efsmax efsmin efdmadd efdmsub efdnmadd efdnmsub efssqrt efscfh efscth efdmax efdmin efdsqrt efdcfh efdcth

• Added mapping for SPE2 instructions in accordance with SPE2PIM Rev.1.0-2:

evdotphsssi evdotphsssia evdotpwsssi evdotpwsssia

• Added instructions from Engineering Bulletin EB689 Rev. 0, 2/2008 for e200z3 and e200z6 cores:

evfsmadd evfsmsub evfsnmadd evfsnmsub efsmadd efsmsub efsnmadd efsnmsub

5.3 Version 1.1.1

This version contains critical fixes for version 1.1

Fixed:

- [ENGR00379772] Compiler may generate the instruction e_subfic with invalid immediate value when size optimization is enabled.
- [ENGR00379484] Compiler assigns a wrong register (r9) when extended inline asm statement with se_bclri %0,%1 instruction is used.
  Note: User should manually set correct constraints for short VLE instructions. Added VLE constraints in documentation.

5.4 Version 1.1.2

Fixed:

- [ENGR00381415] GDB incorrectly prints full expression that this variable object represents
  Note: Utilized patch from this message in GDB mailing list.
- [ENGR00381558] GCC codegen emits illegal 'stwu' instruction in VLE mode