Getting Started with Pins Tool User's Guide

Document Number: PINSGS
Rev. 0, 05/2016

Contents

Section number **Title** **Page**

Chapter 1
Introduction

Chapter 2
Example Usage

Chapter 3
Configuration

Chapter 4
Pins Tool

Section number Title Page

Chapter 5 Advanced Features

Chapter 6 Support

Chapter 1
Introduction

The Pins tool is a part of the NXP Configuration Tools, a suite of evaluation and configuration tools that helps users from first evaluation to production software development. The Pins tool is an easy-to-use way to configure the pins of the device. The Pins tool software enables you to create, inspect, change, and modify any aspect of the pin configuration and muxing of the device. This document introduces you to the Pins tool. It describes the basic components of the tool and lists the steps to configure and use the tool to configure the pins.

NOTE

The Pins tool software is available in Web and desktop versions. For i.MX processors currently only the desktop version is available.

1.1 Features

The Pins tool is designed for:

- Configuration of pin routing/muxing
- Managing different functions used for routing initialization
- Configuration of pin functional/electrical properties
- Generation of code for routing and functional/electrical properties

The Pins tool can be used to define routing of pins for target device/board. The tool configuration may be shared using the stored configuration or by using the generated C file (via Import/ Export or via copy-paste of the generated source). The following sections describe the parts of the Pins tool.

NOTE

> The tool generates code for routing pin to peripheral, but not for the configuration of the peripheral. Some peripherals might need additional configuration of the pin to assign function or channel. For example, for some ADC - the routing provide connection between pin and the ADC peripheral. You can then assign the ADC channel from within the ADC peripheral.

1.2 Conventions

The following conventions are used in this document.

Table 1-1. Conventions used in the document

Icon	Description
🖥	Indicates that the content is related to the desktop version of the tool.
🕸	Indicates that the content is related to the Web version of the tool.
💬	Indicates useful tips.

1.3 Versions

The suite of these tools is called NXP Configuration Tools. These tools are provided as an online Web application or as a desktop application.

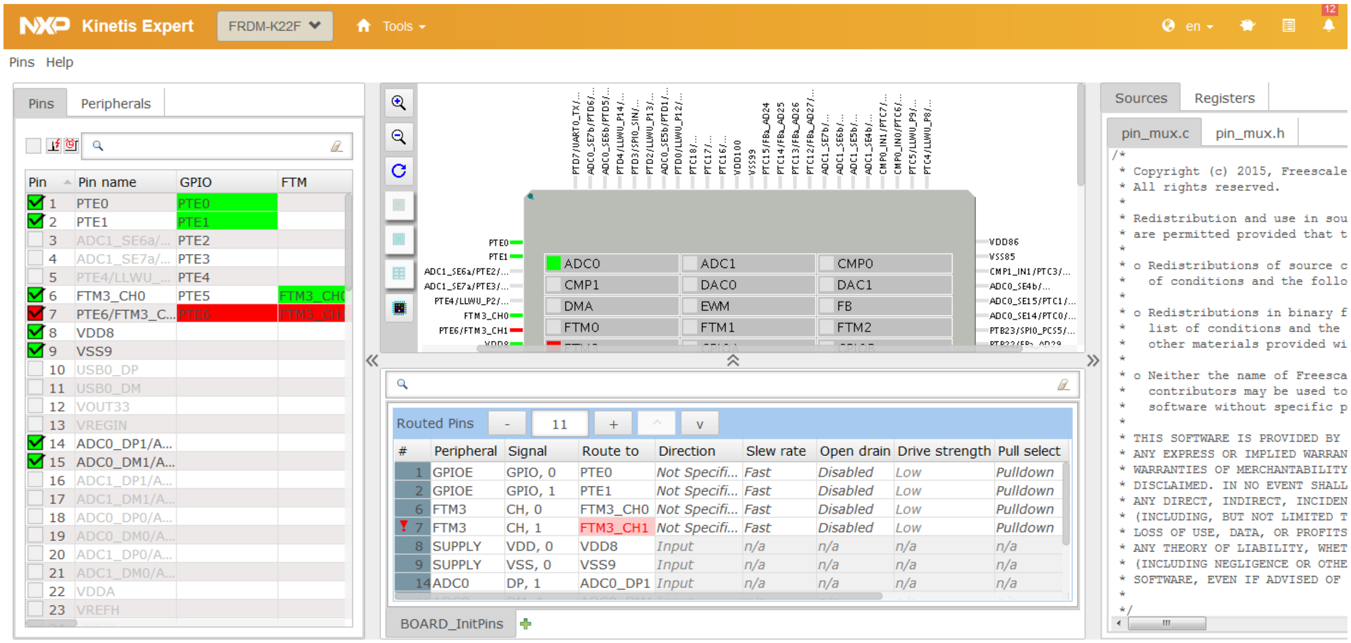
For Kinetis, the tools are referred as Kinetis Expert Tools and they are available both as Web and desktop applications.

For i.MX, the tool is referred as Pins Tool for i.MX Processors and is available as a desktop application only.

NOTE

> The desktop version of the tool contacts the NXP server and fetches the list of the available processors. Once used, the processors data is retrieved on demand.

💬	To use the desktop tool in the offline mode, create a configuration for the given processor while online. The tool will then store the processors locally in the user folder and enable faster access and offline use.



Pin	Pin name	GPIO	FTM
☑ 1	PTE0	PTE0	
☑ 2	PTE1	PTE1	
□ 3	ADC1_SE6a/...	PTE2	
□ 4	ADC1_SE7a/...	PTE3	
□ 5	PTE4/LLWU_...	PTE4	
☑ 6	FTM3_CH0	PTE5	FTM3_CH0
☑ 7	PTE6/FTM3_C...	PTE6	FTM3_CH1
☑ 8	VDD8		
☑ 9	VSS9		
□ 10	USB0_DP		
□ 11	USB0_DM		
□ 12	VOUT33		
□ 13	VREGIN		
☑ 14	ADC0_DP1/A...		
☑ 15	ADC0_DM1/A...		
□ 16	ADC1_DP1/A...		
□ 17	ADC1_DM1/A...		
□ 18	ADC0_DP0/A...		
□ 19	ADC0_DM0/A...		
□ 20	ADC1_DP0/A...		
□ 21	ADC1_DM0/A...		
□ 22	VDDA		
□ 23	VREFH		

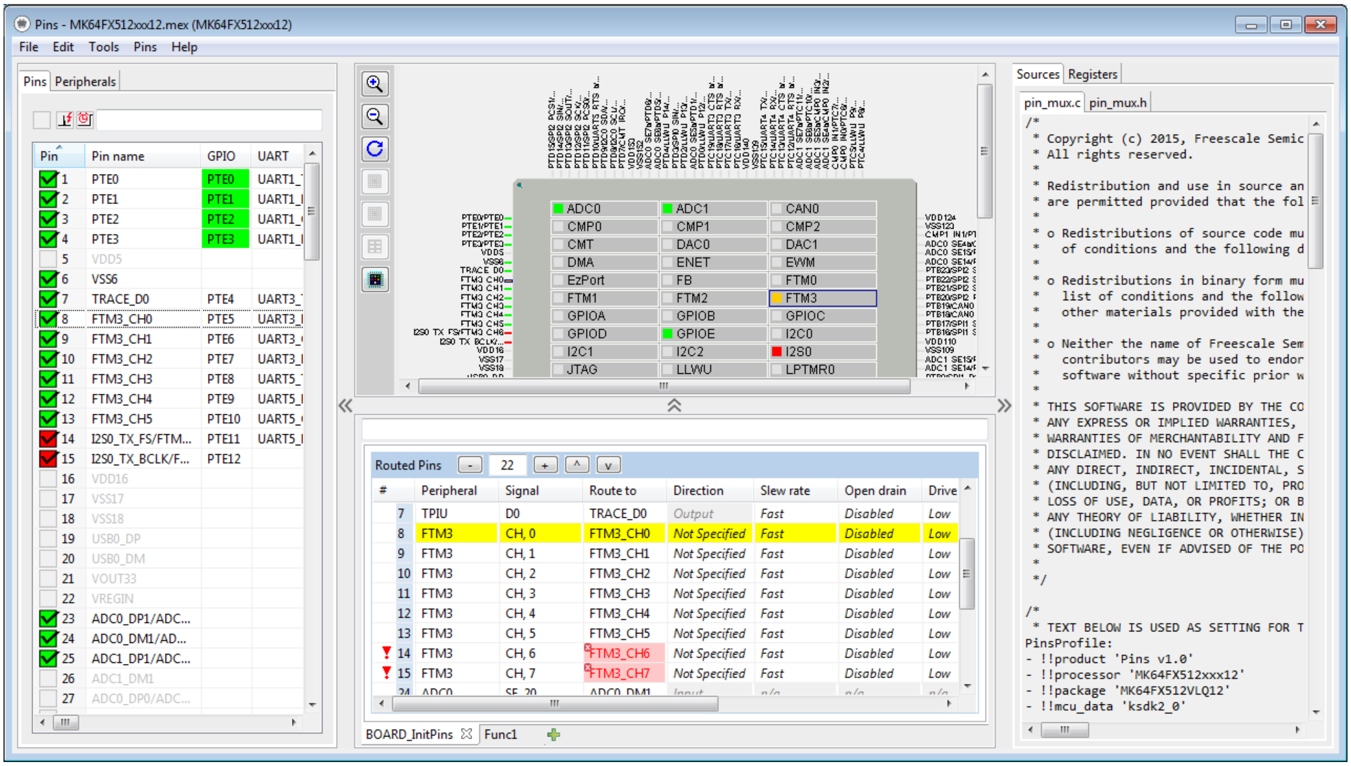
Routed Pins - 11 + ^ v

#	Peripheral	Signal	Route to	Direction	Slew rate	Open drain	Drive strength	Pull select
1	GPIOE	GPIO, 0	PTE0	Not Specifi...	Fast	Disabled	Low	Pulldown
2	GPIOE	GPIO, 1	PTE1	Not Specifi...	Fast	Disabled	Low	Pulldown
6	FTM3	CH, 0	FTM3_CH0	Not Specifi...	Fast	Disabled	Low	Pulldown
7	FTM3	CH, 1	FTM3_CH1	Not Specifi...	Fast	Disabled	Low	Pulldown
8	SUPPLY	VDD, 0	VDD8	Input	n/a	n/a	n/a	n/a
9	SUPPLY	VSS, 0	VSS9	Input	n/a	n/a	n/a	n/a
14	ADC0	DP, 1	ADC0_DP1	Input	n/a	n/a	n/a	n/a

```
/*
 * Copyright (c) 2015, Freescale
 * All rights reserved.
 *
 * Redistribution and use in sou
 * are permitted provided that t
 *
 * o Redistributions of source c
 *   of conditions and the follo
 *
 * o Redistributions in binary f
 *   list of conditions and the
 *   other materials provided wi
 *
 * o Neither the name of Freesca
 *   contributors may be used to
 *   software without specific p
 *
 * THIS SOFTWARE IS PROVIDED BY
 * ANY EXPRESS OR IMPLIED WARRAN
 * WARRANTIES OF MERCHANTABILITY
 * DISCLAIMED. IN NO EVENT SHALL
 * ANY DIRECT, INDIRECT, INCIDEN
 * (INCLUDING, BUT NOT LIMITED T
 * LOSS OF USE, DATA, OR PROFITS
 * ANY THEORY OF LIABILITY, WHET
 * (INCLUDING NEGLIGENCE OR OTHE
 * SOFTWARE, EVEN IF ADVISED OF
 *
 */
```

Figure 1-1. Web version

🖥	Pins tool for i.MX Processors is available as desktop application only.



Pin	Pin name	GPIO	UART
☑ 1	PTE0	PTE0	UART1_
☑ 2	PTE1	PTE1	UART1_I
☑ 3	PTE2	PTE2	UART1_
☑ 4	PTE3	PTE3	UART1_I
□ 5	VDD5		
☑ 6	VSS6		
☑ 7	TRACE_D0	PTE4	UART3_
☑ 8	FTM3_CH0	PTE5	UART3_I
☑ 9	FTM3_CH1	PTE6	UART3_
☑ 10	FTM3_CH2	PTE7	UART3_I
☑ 11	FTM3_CH3	PTE8	UART5_
☑ 12	FTM3_CH4	PTE9	UART5_I
☑ 13	FTM3_CH5	PTE10	UART5_
☑ 14	I2S0_TX_FS/FTM...	PTE11	UART5_I
☑ 15	I2S0_TX_BCLK/F...	PTE12	
□ 16	VDD16		
□ 17	VSS17		
□ 18	VSS18		
□ 19	USB0_DP		
□ 20	USB0_DM		
□ 21	VOUT33		
□ 22	VREGIN		
☑ 23	ADC0_DP1/ADC...		
☑ 24	ADC0_DM1/AD...		
☑ 25	ADC1_DP1/ADC...		
□ 26	ADC1_DM1		
□ 27	ADC0_DP0/ADC...		

ADC0	ADC1	CAN0
CMP0	CMP1	CMP2
CMT	DAC0	DAC1
DMA	ENET	EWM
EzPort	FB	FTM0
FTM1	FTM2	FTM3
GPIOA	GPIOB	GPIOC
GPIOD	GPIOE	I2C0
I2C1	I2C2	I2S0
JTAG	LLWU	LPTMR0

Routed Pins - 22 + ^ v

#	Peripheral	Signal	Route to	Direction	Slew rate	Open drain	Drive
7	TPIU	D0	TRACE_D0	Output	Fast	Disabled	Low
8	FTM3	CH, 0	FTM3_CH0	Not Specified	Fast	Disabled	Low
9	FTM3	CH, 1	FTM3_CH1	Not Specified	Fast	Disabled	Low
10	FTM3	CH, 2	FTM3_CH2	Not Specified	Fast	Disabled	Low
11	FTM3	CH, 3	FTM3_CH3	Not Specified	Fast	Disabled	Low
12	FTM3	CH, 4	FTM3_CH4	Not Specified	Fast	Disabled	Low
13	FTM3	CH, 5	FTM3_CH5	Not Specified	Fast	Disabled	Low
! 14	FTM3	CH, 6	FTM3_CH6	Not Specified	Fast	Disabled	Low
! 15	FTM3	CH, 7	FTM3_CH7	Not Specified	Fast	Disabled	Low
24	ADC0	SE, 20	ADC0_DM1	Input	n/a	n/a	n/a

```
/*
 * Copyright (c) 2015, Freescale Semic
 * All rights reserved.
 *
 * Redistribution and use in source an
 * are permitted provided that the fol
 *
 * o Redistributions of source code mu
 *   of conditions and the following d
 *
 * o Redistributions in binary form mu
 *   list of conditions and the follow
 *   other materials provided with the
 *
 * o Neither the name of Freescale Sem
 *   contributors may be used to endor
 *   software without specific prior w
 *
 * THIS SOFTWARE IS PROVIDED BY THE CO
 * ANY EXPRESS OR IMPLIED WARRANTIES,
 * WARRANTIES OF MERCHANTABILITY AND F
 * DISCLAIMED. IN NO EVENT SHALL THE C
 * ANY DIRECT, INDIRECT, INCIDENTAL, S
 * (INCLUDING, BUT NOT LIMITED TO, PRO
 * LOSS OF USE, DATA, OR PROFITS; OR B
 * ANY THEORY OF LIABILITY, WHETHER IN
 * (INCLUDING NEGLIGENCE OR OTHERWISE)
 * SOFTWARE, EVEN IF ADVISED OF THE PO
 *
 */

/*
 * TEXT BELOW IS USED AS SETTING FOR T
PinsProfile:
- !!product 'Pins v1.0'
- !!processor 'MK64FX512xxx12'
- !!package 'MK64FX512VLQ12'
- !!mcu_data 'ksdk2_0'
```

Figure 1-2. Desktop version

1.4 Tool localization

The Pins Tool supports English and Chinese languages, based on your locale settings.

To manually set the locale, add the following parameter to the command line:

```
tools.exe -nl zh
```

It is possible to set the locale in the tools.ini file by adding the following line:

```
-Duser.language=zh
```

The supported languages are:

- en - English
- zh – Chinese

NOTE

Setting your system locale to Chinese will automatically launch the tool with localized Chinese menu items, tool tips, and help.

Chapter 2
Example Usage

This section lists the steps to create an example pin configuration, which then can be used in a project.

In this example, three pins (UART0_RX, UART0_TX and PTB21) on a board are configured.

The steps are listed both for the desktop and the Web version.

NOTE

The Web version exists only for the Kinetis devices.

You can the use the generated files with the application code.

1. For the **desktop** version, launch the tool with the shortcut present in the installation folder.
2. For the **Web** version visit http://kex.nxp.com and select the Pins tool.

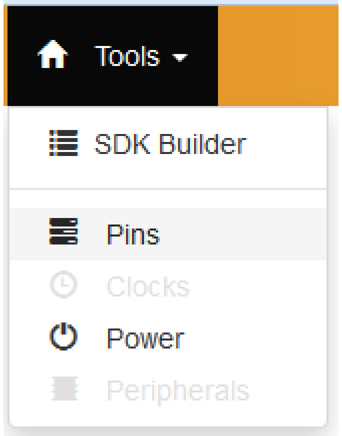
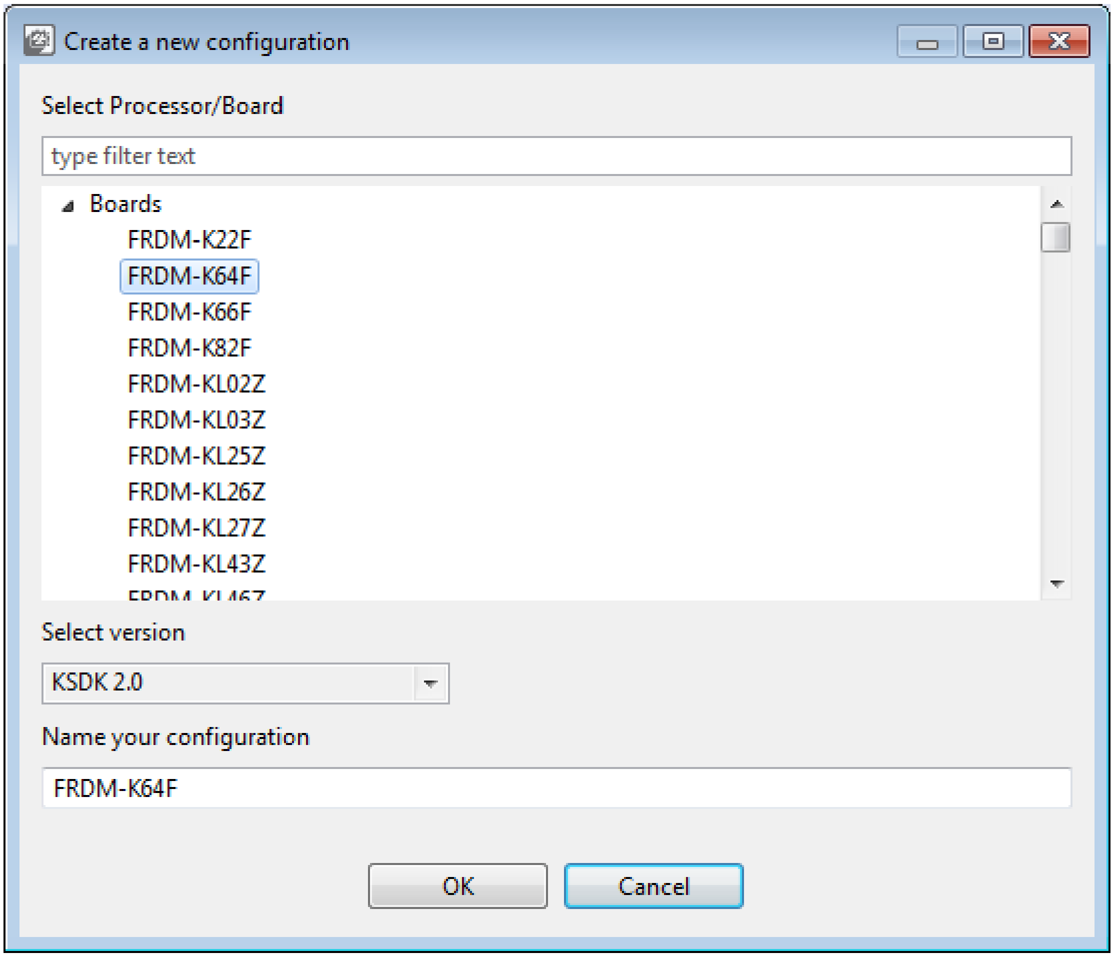


Figure 2-1. Select the Pins tool

3. In the **desktop** version, create a new configuration with the menu **File > New** and select the processor/board you want to use.



Create a new configuration

Select Processor/Board

type filter text

Boards

FRDM-K22F

FRDM-K64F

FRDM-K66F

FRDM-K82F

FRDM-KL02Z

FRDM-KL03Z

FRDM-KL25Z

FRDM-KL26Z

FRDM-KL27Z

FRDM-KL43Z

Select version

KSDK 2.0

Name your configuration

FRDM-K64F

Figure 2-2. Create a new configuration

Optionally, name the configuration to match your project.

4. In the Web version:
   a. Select an existing configuration or create a new configuration.

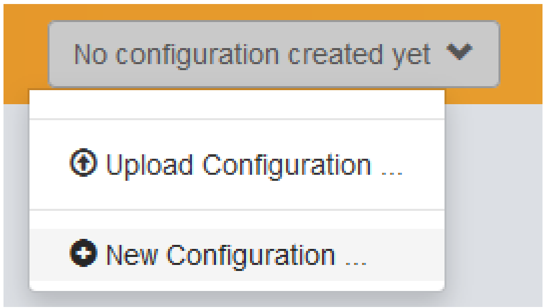
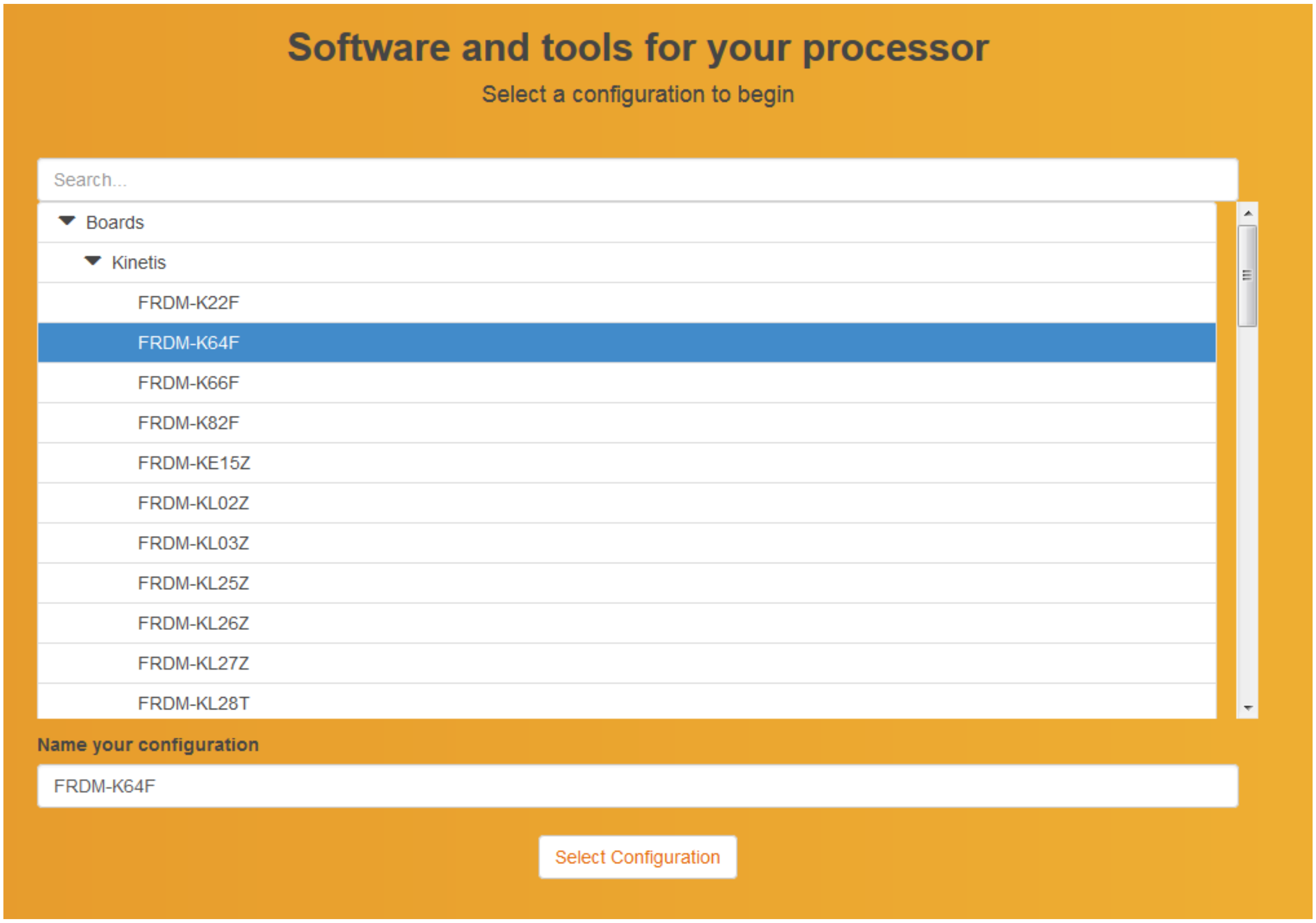


Figure 2-3. New Configuration

   b. For a new configuration, select the board and the configuration.



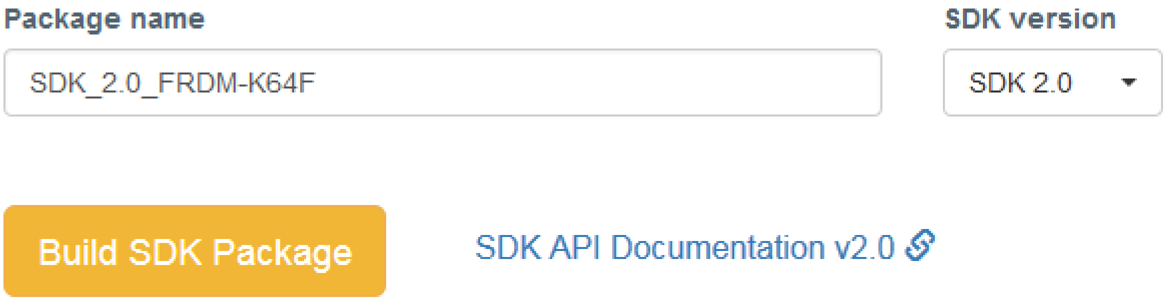
Software and tools for your processor

Select a configuration to begin

Name your configuration: FRDM-K64F

Figure 2-4. Select a configuration to begin

c. Create the SDK package for the configuration.



Package name: SDK_2.0_FRDM-K64F

SDK version: SDK 2.0

Figure 2-5. Build SDK Package

d. After creating a new configuration, switch to the Pins tool.

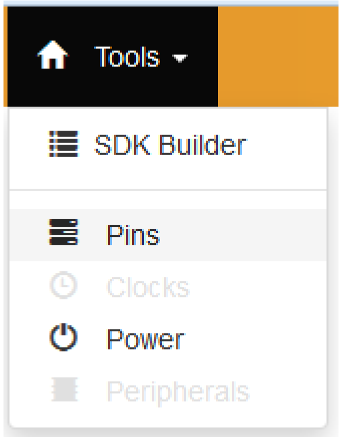
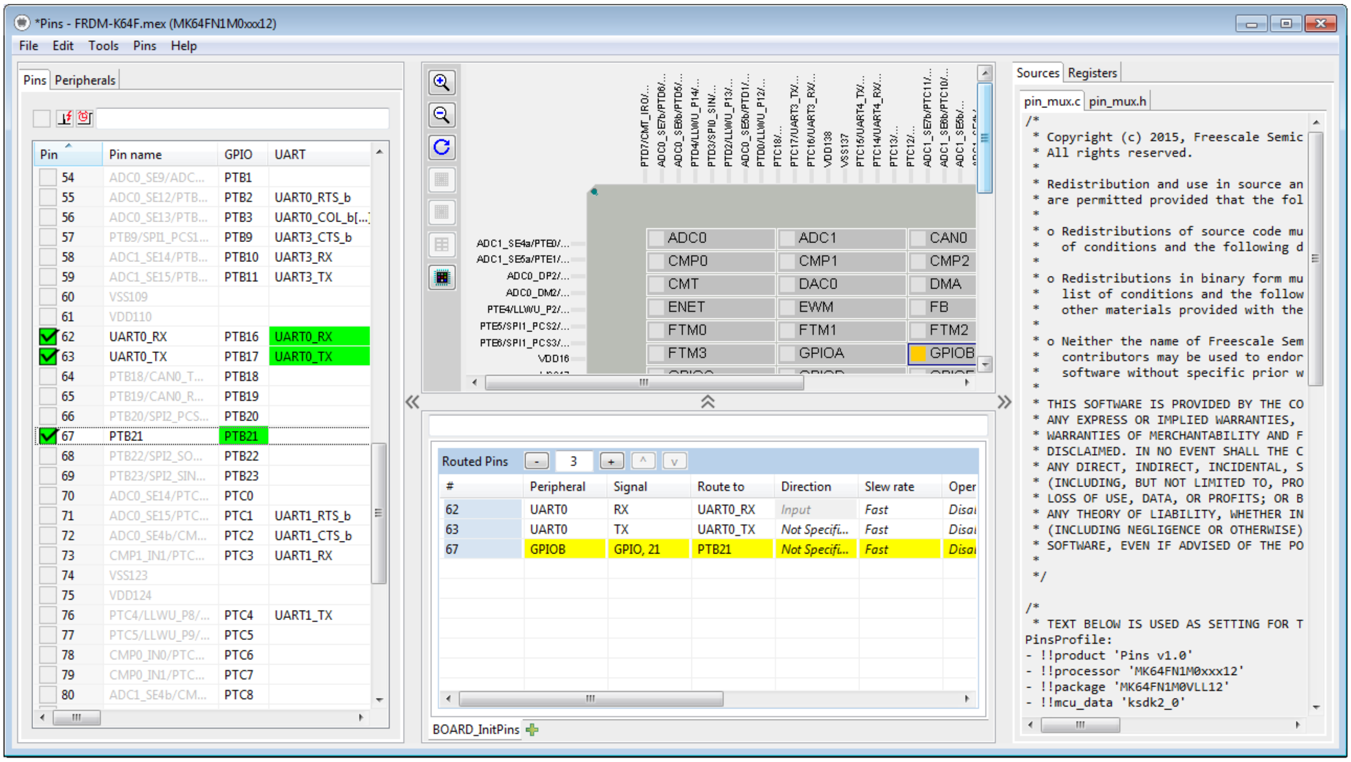


Figure 2-6. Switch to Pins tool

5. In the **Pins** view on the left, select the UART0_RX and TX signals and the PTB21 GPIO. For this, you can click into the cells to make them ‘green’.



Pin	Pin name	GPIO	UART
□ 54	ADC0_SE9/ADC...	PTB1	
□ 55	ADC0_SE12/PTB...	PTB2	UART0_RTS_b
□ 56	ADC0_SE13/PTB...	PTB3	UART0_COL_b[...]
□ 57	PTB9/SPI1_PCS1...	PTB9	UART3_CTS_b
□ 58	ADC1_SE14/PTB...	PTB10	UART3_RX
□ 59	ADC1_SE15/PTB...	PTB11	UART3_TX
□ 60	VSS109		
□ 61	VDD110		
☑ 62	UART0_RX	PTB16	UART0_RX
☑ 63	UART0_TX	PTB17	UART0_TX
□ 64	PTB18/CAN0_T...	PTB18	
□ 65	PTB19/CAN0_R...	PTB19	
□ 66	PTB20/SPI2_PCS...	PTB20	
☑ 67	PTB21	PTB21	
□ 68	PTB22/SPI2_SO...	PTB22	
□ 69	PTB23/SPI2_SIN...	PTB23	
□ 70	ADC0_SE14/PTC...	PTC0	
□ 71	ADC0_SE15/PTC...	PTC1	UART1_RTS_b
□ 72	ADC0_SE4b/CM...	PTC2	UART1_CTS_b
□ 73	CMP1_IN1/PTC...	PTC3	UART1_RX
□ 74	VSS123		
□ 75	VDD124		
□ 76	PTC4/LLWU_P8/...	PTC4	UART1_TX
□ 77	PTC5/LLWU_P9/...	PTC5	
□ 78	CMP0_IN0/PTC...	PTC6	
□ 79	CMP0_IN1/PTC...	PTC7	
□ 80	ADC1_SE4b/CM...	PTC8	

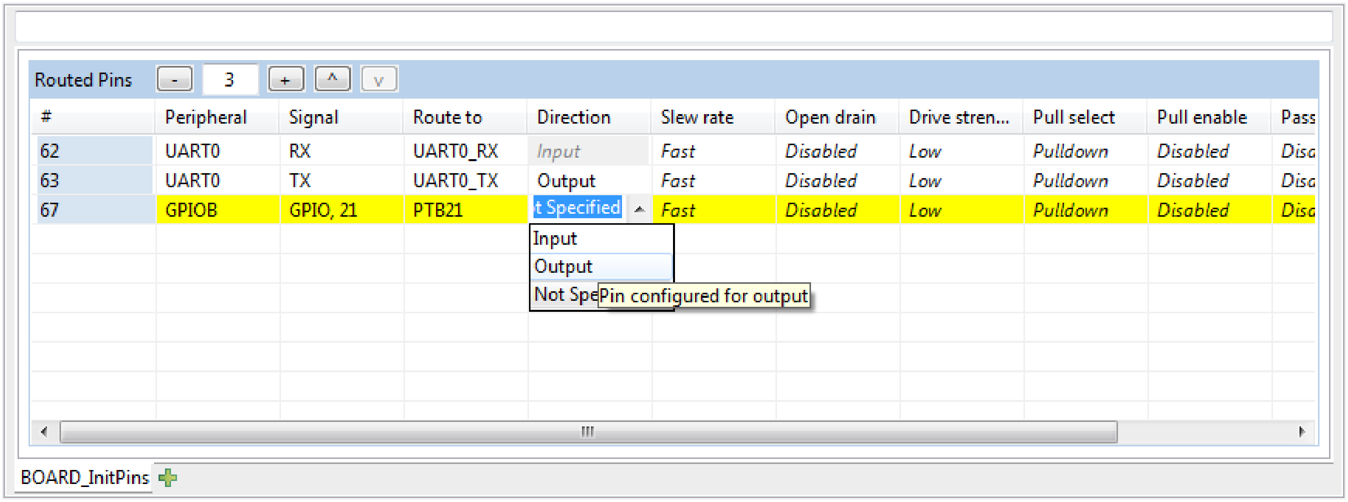
Routed Pins 3

#	Peripheral	Signal	Route to	Direction	Slew rate	Oper
62	UART0	RX	UART0_RX	*Input*	*Fast*	*Disal*
63	UART0	TX	UART0_TX	*Not Specifi...*	*Fast*	*Disal*
67	GPIOB	GPIO, 21	PTB21	*Not Specifi...*	*Fast*	*Disal*

```
/*
 * Copyright (c) 2015, Freescale Semic
 * All rights reserved.
 *
 * Redistribution and use in source an
 * are permitted provided that the fol
 *
 * o Redistributions of source code mu
 *   of conditions and the following d
 *
 * o Redistributions in binary form mu
 *   list of conditions and the follow
 *   other materials provided with the
 *
 * o Neither the name of Freescale Sem
 *   contributors may be used to endor
 *   software without specific prior w
 *
 * THIS SOFTWARE IS PROVIDED BY THE CO
 * ANY EXPRESS OR IMPLIED WARRANTIES,
 * WARRANTIES OF MERCHANTABILITY AND F
 * DISCLAIMED. IN NO EVENT SHALL THE C
 * ANY DIRECT, INDIRECT, INCIDENTAL, S
 * (INCLUDING, BUT NOT LIMITED TO, PRO
 * LOSS OF USE, DATA, OR PROFITS; OR B
 * ANY THEORY OF LIABILITY, WHETHER IN
 * (INCLUDING NEGLIGENCE OR OTHERWISE)
 * SOFTWARE, EVEN IF ADVISED OF THE PO
 *
 */

/*
 * TEXT BELOW IS USED AS SETTING FOR T
PinsProfile:
- !!product 'Pins v1.0'
- !!processor 'MK64FN1M0xxx12'
- !!package 'MK64FN1M0VLL12'
- !!mcu_data 'ksdk2_0'
```

Figure 2-7. Switch to Pins tool

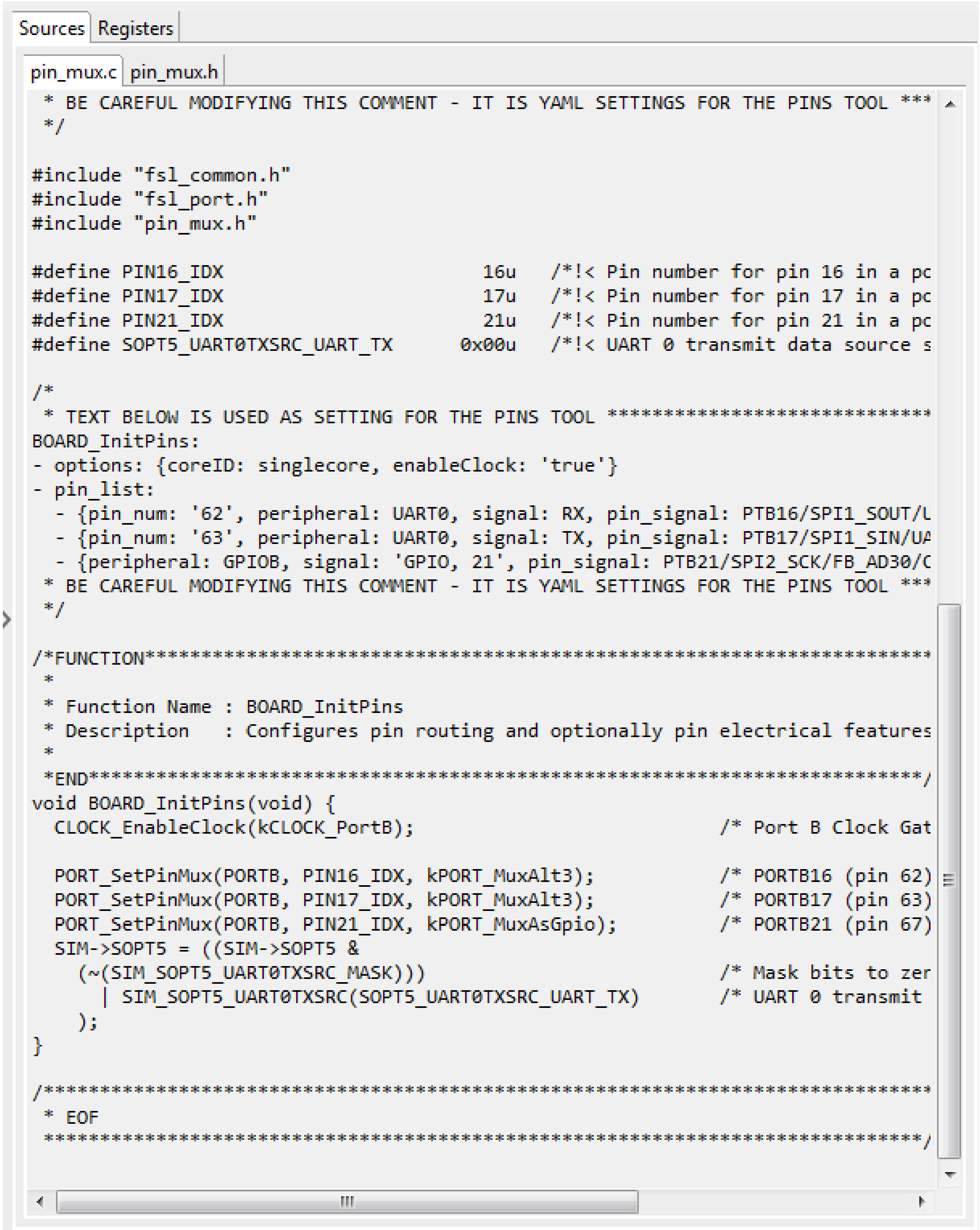
6. In the middle view, called the Routed Pins table, select **Output** for the TX and PTB21 signals.



#	Peripheral	Signal	Route to	Direction	Slew rate	Open drain	Drive stren...	Pull select	Pull enable	Pass
62	UART0	RX	UART0_RX	Input	Fast	Disabled	Low	Pulldown	Disabled	Disa
63	UART0	TX	UART0_TX	Output	Fast	Disabled	Low	Pulldown	Disabled	Disa
67	GPIOB	GPIO, 21	PTB21	t Specified	Fast	Disabled	Low	Pulldown	Disabled	Disa

Figure 2-8. Select output

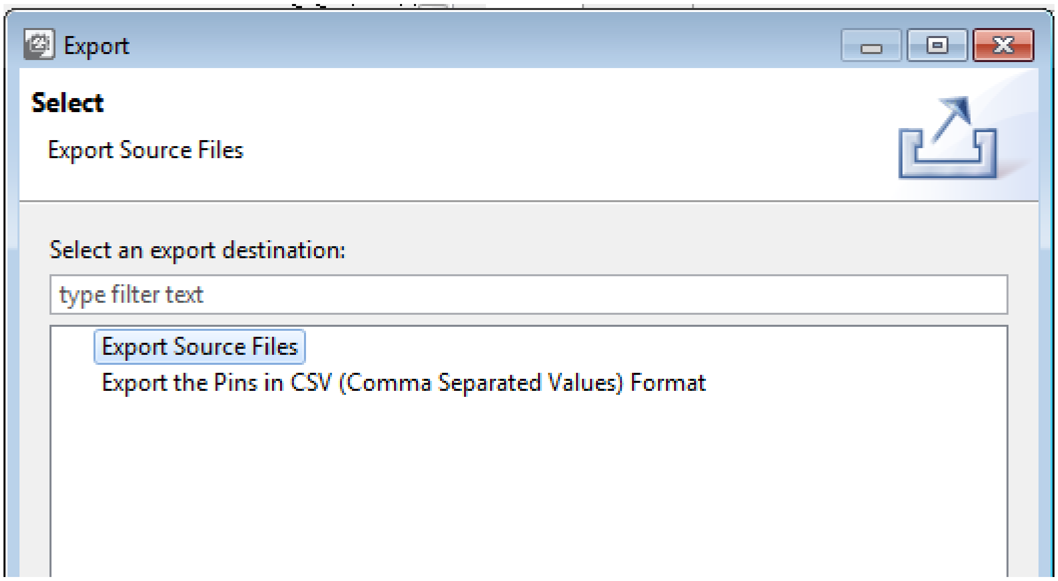
7. The Pins tool automatically generates the source code for `pin_mux.c` and `pin_mux.h` on the right panel.



```
 * BE CAREFUL MODIFYING THIS COMMENT - IT IS YAML SETTINGS FOR THE PINS TOOL ***
 */

#include "fsl_common.h"
#include "fsl_port.h"
#include "pin_mux.h"

#define PIN16_IDX                        16u   /*!< Pin number for pin 16 in a pc
#define PIN17_IDX                        17u   /*!< Pin number for pin 17 in a pc
#define PIN21_IDX                        21u   /*!< Pin number for pin 21 in a pc
#define SOPT5_UART0TXSRC_UART_TX       0x00u   /*!< UART 0 transmit data source s

/*
 * TEXT BELOW IS USED AS SETTING FOR THE PINS TOOL *****************************
BOARD_InitPins:
- options: {coreID: singlecore, enableClock: 'true'}
- pin_list:
  - {pin_num: '62', peripheral: UART0, signal: RX, pin_signal: PTB16/SPI1_SOUT/L
  - {pin_num: '63', peripheral: UART0, signal: TX, pin_signal: PTB17/SPI1_SIN/UA
  - {peripheral: GPIOB, signal: 'GPIO, 21', pin_signal: PTB21/SPI2_SCK/FB_AD30/C
 * BE CAREFUL MODIFYING THIS COMMENT - IT IS YAML SETTINGS FOR THE PINS TOOL ***
 */

/*FUNCTION**********************************************************************
 *
 * Function Name : BOARD_InitPins
 * Description   : Configures pin routing and optionally pin electrical features
 *
 *END**************************************************************************/
void BOARD_InitPins(void) {
  CLOCK_EnableClock(kCLOCK_PortB);                           /* Port B Clock Gat

  PORT_SetPinMux(PORTB, PIN16_IDX, kPORT_MuxAlt3);           /* PORTB16 (pin 62)
  PORT_SetPinMux(PORTB, PIN17_IDX, kPORT_MuxAlt3);           /* PORTB17 (pin 63)
  PORT_SetPinMux(PORTB, PIN21_IDX, kPORT_MuxAsGpio);         /* PORTB21 (pin 67)
  SIM->SOPT5 = ((SIM->SOPT5 &
    (~(SIM_SOPT5_UART0TXSRC_MASK)))                          /* Mask bits to zer
      | SIM_SOPT5_UART0TXSRC(SOPT5_UART0TXSRC_UART_TX)       /* UART 0 transmit
    );
}

/*******************************************************************************
 * EOF
 ******************************************************************************/
```

Figure 2-9. Generated code

8. You can now copy-paste the content of the source(s) to your application and IDE. Alternatively, you can export the generated files. To export the files: select the menu **File > Export** (in the desktop version) or select the menu **Pins > Export** menu (in the Web version). In the **Export** dialog, select the **Export Source Files** option.



Export

Select

Export Source Files

Select an export destination:

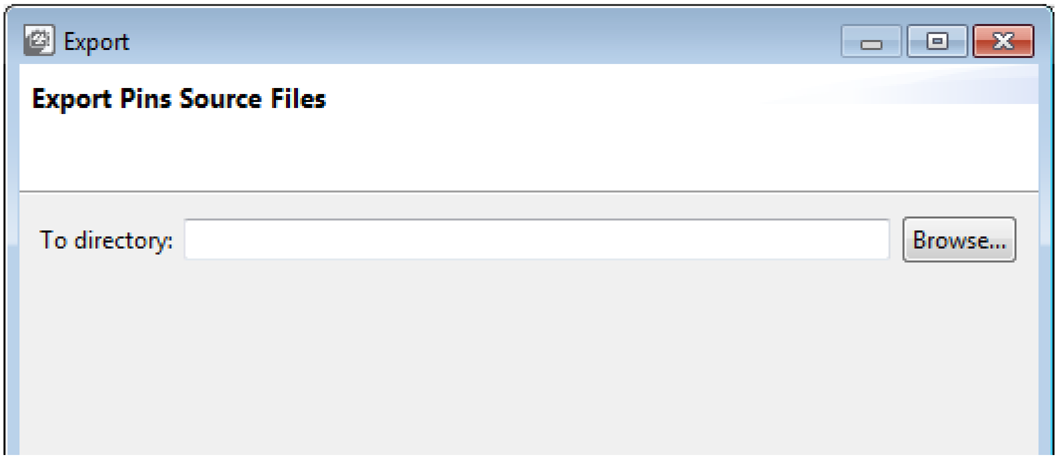
type filter text

Export Source Files

Export the Pins in CSV (Comma Separated Values) Format

Figure 2-10. Export Source Files

9. Click **Next** and specify the directory where you want to store the files.



Export

Export Pins Source Files

To directory:

Figure 2-11. Exported Pins Source Files

10. Click **Finish** to export the files.
11. Integrate and use the exported files in your application as source files.

Congratulations, you have created the configuration for your pins!

The following sections in this User’s Guide describe the features of the tool in detail.

Chapter 3
Configuration

Configuration stands for common tools settings stored in .mex file. This file contains settings of all available tools and can be used in both web and desktop versions.

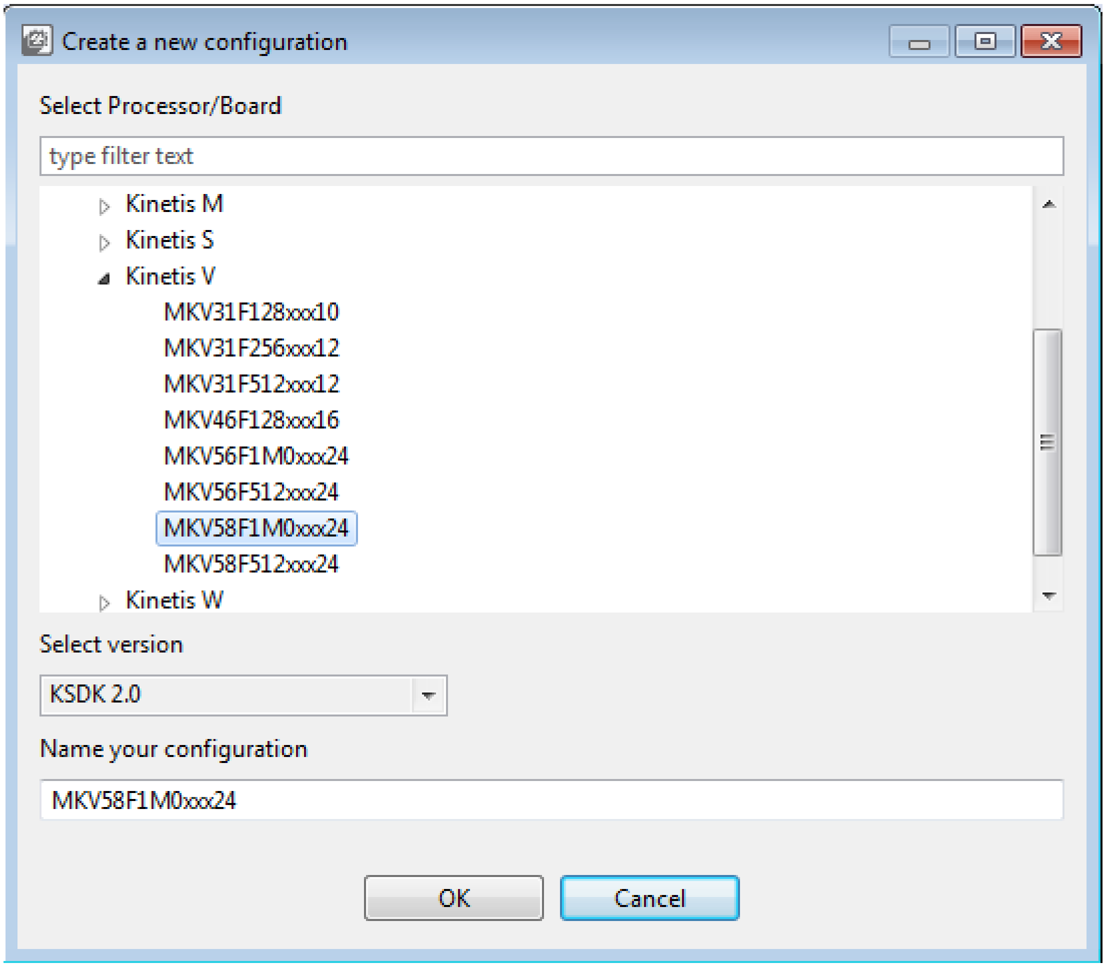
3.1 Creating a new configuration

To create a new configuration:

1. If the Pins tool is already open, select the **File > New** command.

   The Select a configuration to begin dialog box appears.

2. Expand the list of family and select the desired processor.



Create a new configuration

Select Processor/Board

type filter text

- Kinetis M
- Kinetis S
- Kinetis V
  - MKV31F128xxx10
  - MKV31F256xxx12
  - MKV31F512xxx12
  - MKV46F128xxx16
  - MKV56F1M0xxx24
  - MKV56F512xxx24
  - MKV58F1M0xxx24
  - MKV58F512xxx24
- Kinetis W

Select version: KSDK 2.0

Name your configuration: MKV58F1M0xxx24

Figure 3-1. Select a processor

Alternatively, type the name of the processor in the Search Processor text box and select the processor from the filtered results.

3. To specify a different name for your configuration, edit the text in the Name your configuration dialog box.
4. Click the OK button.

   The selected configuration appears in the Pins tool. You can now configure the device.

5. You can now add the peripheral, package, and pins you want to configure and assigns/configure the muxing for the selected pins.

NOTE

You can create a new configuration from the drop-down menu on the top of the Web page.

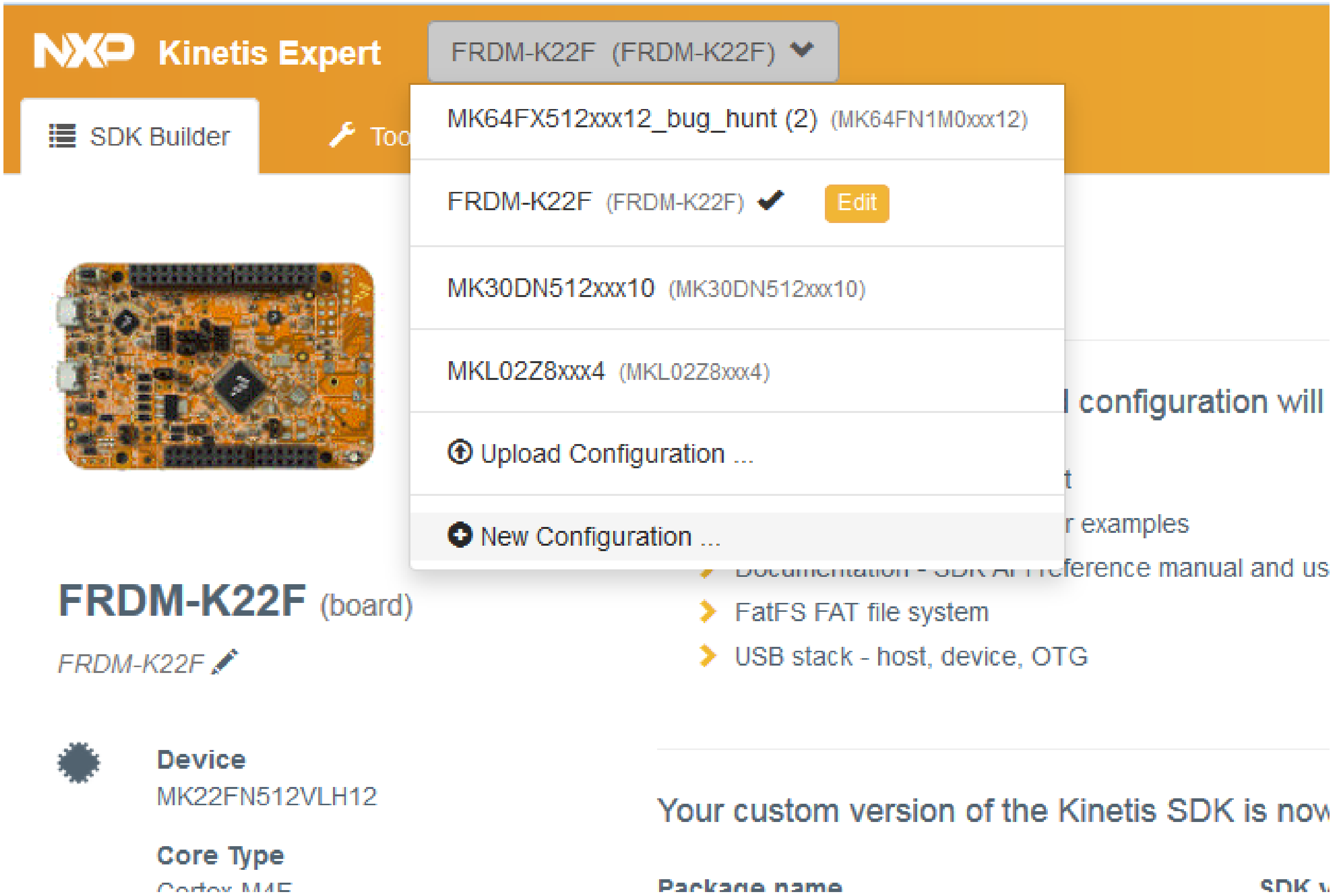
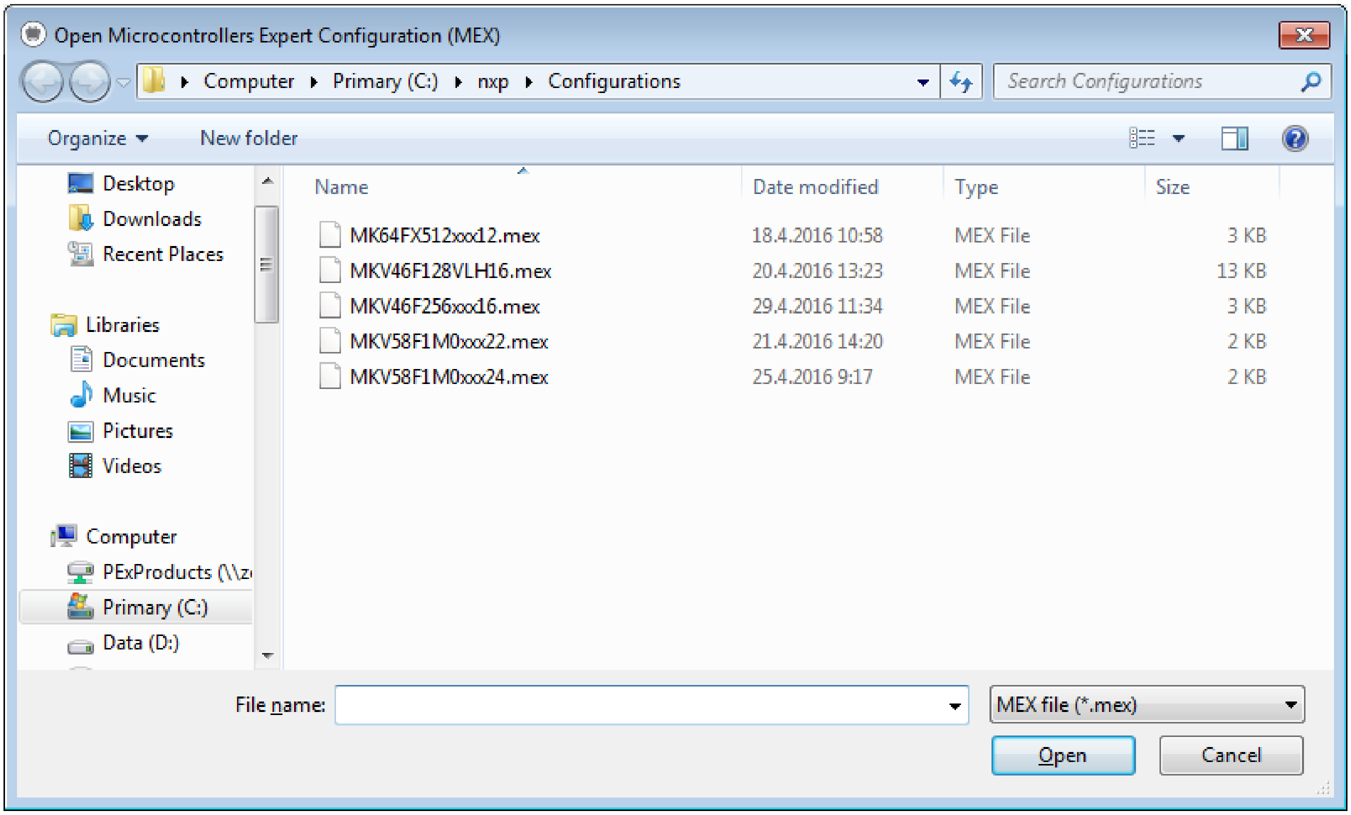


Figure 3-2. Drop-down menu on the Web page

3.2 Saving a configuration

To save a configuration or a profile, select **File > Save As**.



Name	Date modified	Type	Size
MK64FX512xxx12.mex	18.4.2016 10:58	MEX File	3 KB
MKV46F128VLH16.mex	20.4.2016 13:23	MEX File	13 KB
MKV46F256xxx16.mex	29.4.2016 11:34	MEX File	3 KB
MKV58F1M0xxx22.mex	21.4.2016 14:20	MEX File	2 KB
MKV58F1M0xxx24.mex	25.4.2016 9:17	MEX File	2 KB

File name:

Figure 3-3. Save configuration

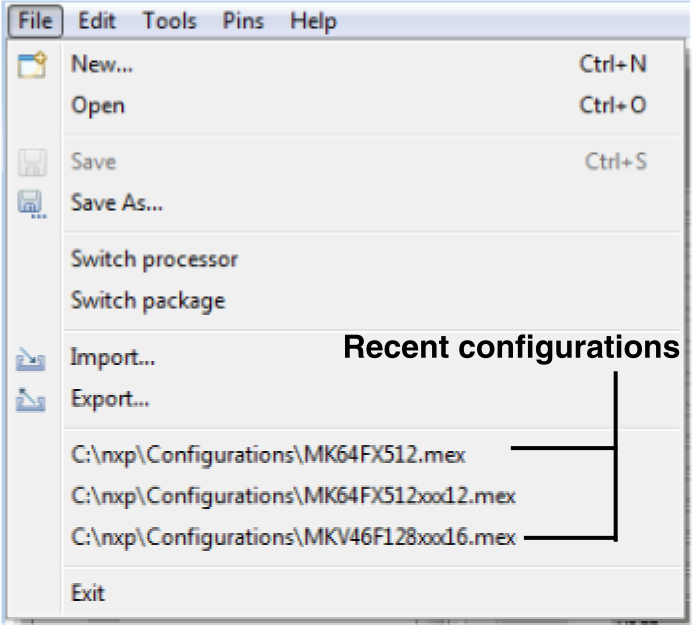
NOTE

In the desktop version, the configuration gets stored with a .mex file extension.

3.3 Opening an existing configuration

To open a previously saved profile:

1. Select **File > Open**.

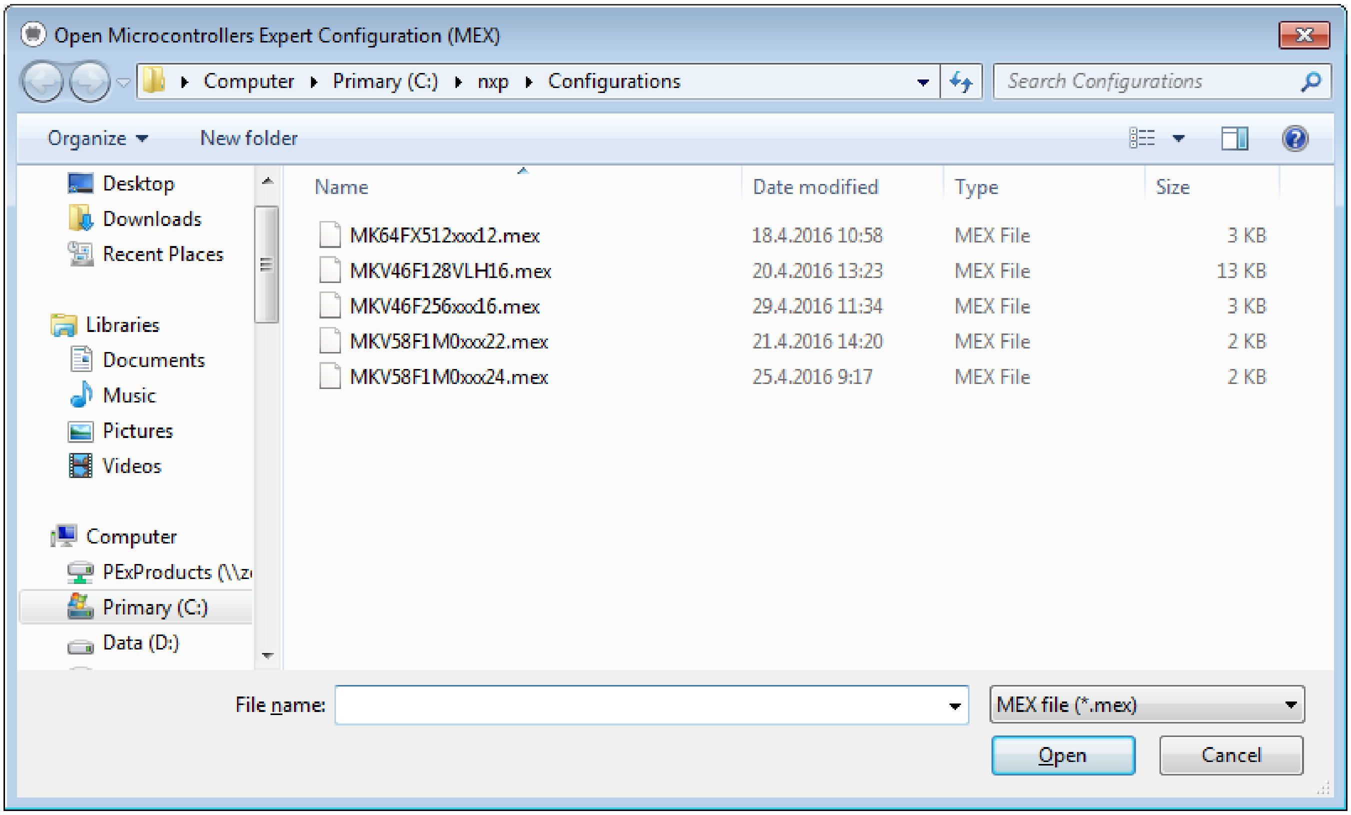


Recent configurations

Figure 3-4. Open profile

The Open profile dialog box appears.

2. Navigate to the folder where the previous profile has been saved.



Name	Date modified	Type	Size
MK64FX512xxx12.mex	18.4.2016 10:58	MEX File	3 KB
MKV46F128VLH16.mex	20.4.2016 13:23	MEX File	13 KB
MKV46F256xxx16.mex	29.4.2016 11:34	MEX File	3 KB
MKV58F1M0xxx22.mex	21.4.2016 14:20	MEX File	2 KB
MKV58F1M0xxx24.mex	25.4.2016 9:17	MEX File	2 KB

Figure 3-5. Open dialog box

3. Select the profile and click Open.

The existing profile appears in the Pins tool.

Chapter 4
Pins Tool

This chapter describes the Pins tool principle and its use to generate the routing and muxing for pins.

4.1 Selecting Pins tool

Select the Pins tool either via menu or by using shortcut installed on the desktop version.

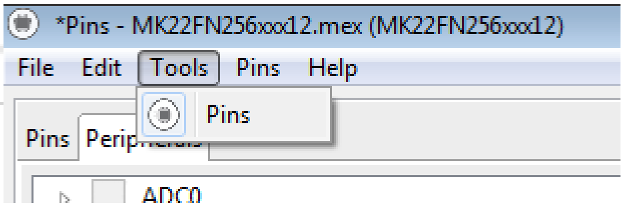


Figure 4-1. Selecting Pins Tool - Desktop

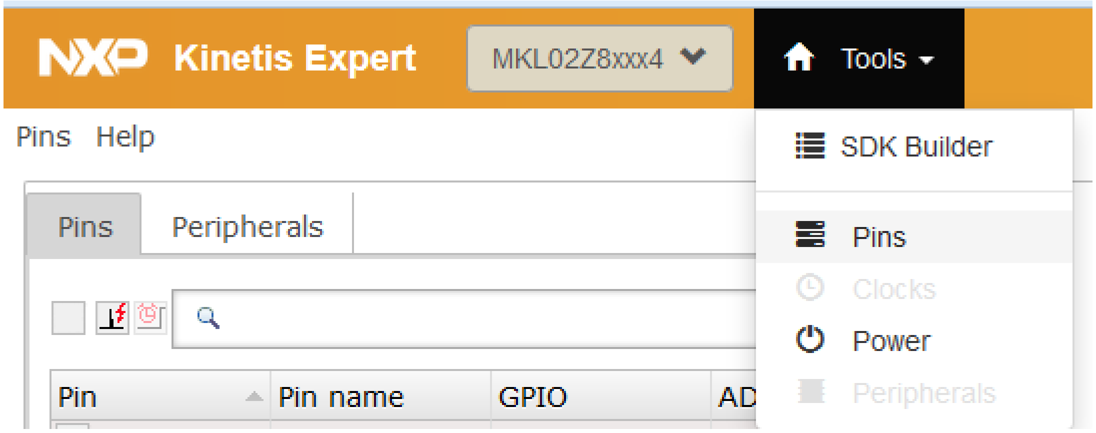


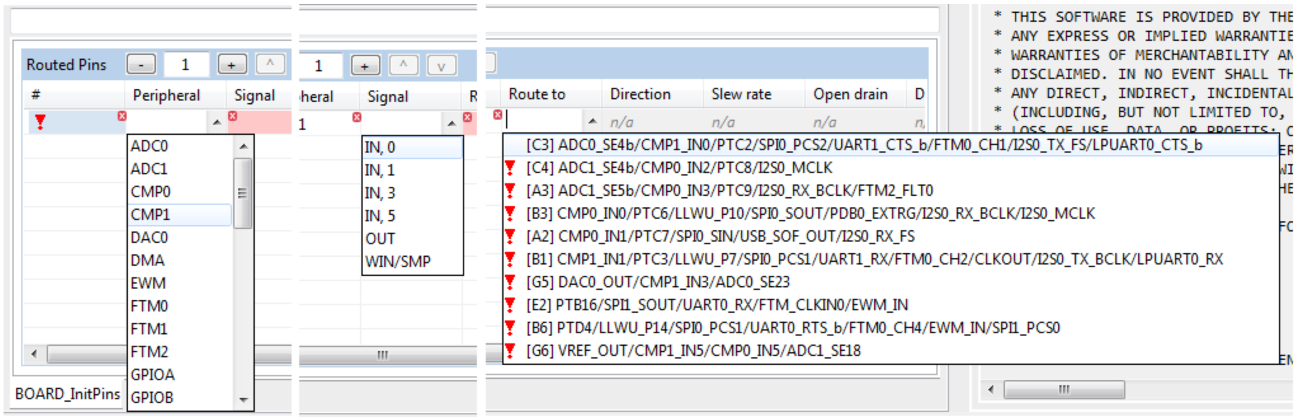
Figure 4-2. Selecting Pins Tool - Web

4.2 Pins routing principle

The Pins tool is designed to configure routing of signals from peripherals either to pins or to internal signals.

To define routing path, select:

1. Peripheral
2. Signal
3. Pin


Routed Pins
-
1
+
^
v
#
Peripheral
Signal
heral
R
Route to
Direction
Slew rate
Open drain
D
n/a
n/a
n/a
ADC0
ADC1
CMP0
CMP1
DAC0
DMA
EWM
FTM0
FTM1
FTM2
GPIOA
GPIOB
IN, 0
IN, 1
IN, 3
IN, 5
OUT
WIN/SMP
[C3] ADC0_SE4b/CMP1_IN0/PTC2/SPI0_PCS2/UART1_CTS_b/FTM0_CH1/I2S0_TX_FS/LPUART0_CTS_b
[C4] ADC1_SE4b/CMP0_IN2/PTC8/I2S0_MCLK
[A3] ADC1_SE5b/CMP0_IN3/PTC9/I2S0_RX_BCLK/FTM2_FLT0
[B3] CMP0_IN0/PTC6/LLWU_P10/SPI0_SOUT/PDB0_EXTRG/I2S0_RX_BCLK/I2S0_MCLK
[A2] CMP0_IN1/PTC7/SPI0_SIN/USB_SOF_OUT/I2S0_RX_FS
[B1] CMP1_IN1/PTC3/LLWU_P7/SPI0_PCS1/UART1_RX/FTM0_CH2/CLKOUT/I2S0_TX_BCLK/LPUART0_RX
[G5] DAC0_OUT/CMP1_IN3/ADC0_SE23
[E2] PTB16/SPI1_SOUT/UART0_RX/FTM_CLKIN0/EWM_IN
[B6] PTD4/LLWU_P14/SPI0_PCS1/UART0_RTS_b/FTM0_CH4/EWM_IN/SPI1_PCS0
[G6] VREF_OUT/CMP1_IN5/CMP0_IN5/ADC1_SE18
BOARD_InitPins

```
 * THIS SOFTWARE IS PROVIDED BY THE
 * ANY EXPRESS OR IMPLIED WARRANTIE
 * WARRANTIES OF MERCHANTABILITY AN
 * DISCLAIMED. IN NO EVENT SHALL TH
 * ANY DIRECT, INDIRECT, INCIDENTAL
 * (INCLUDING, BUT NOT LIMITED TO,
```

Figure 4-3. Defining routing path

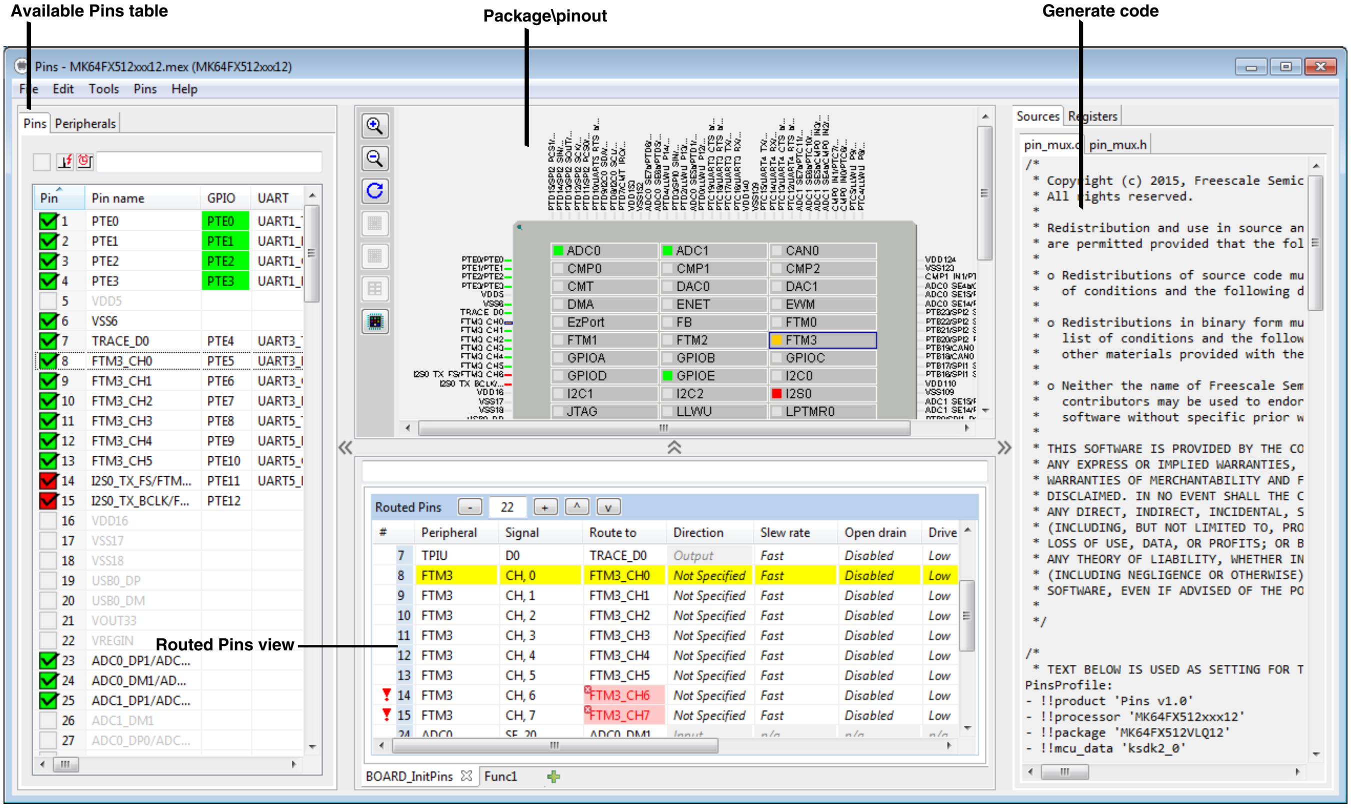
For the selected **Peripheral**, select one of the available signals.

Route the selected **Signal** to the desired pin.

Select one of non-conflicting/available pins. Once you have selected **Peripheral**, **Signal**, and **Route to**, the pin configuration is done. Later, it is also possible to configure the pin electrical features.

4.3 User interface

The Pins tool consists of several views.



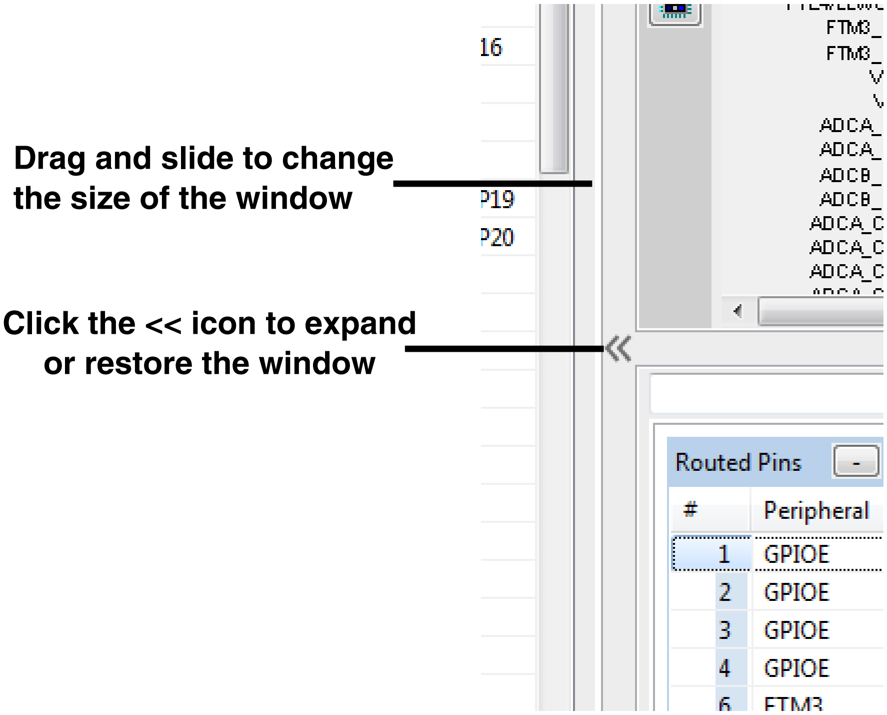
Pin	Pin name	GPIO	UART
☑ 1	PTE0	PTE0	UART1_
☑ 2	PTE1	PTE1	UART1_
☑ 3	PTE2	PTE2	UART1_
☑ 4	PTE3	PTE3	UART1_
□ 5	VDD5		
☑ 6	VSS6		
☑ 7	TRACE_D0	PTE4	UART3_
☑ 8	FTM3_CH0	PTE5	UART3_
☑ 9	FTM3_CH1	PTE6	UART3_
☑ 10	FTM3_CH2	PTE7	UART3_
☑ 11	FTM3_CH3	PTE8	UART5_
☑ 12	FTM3_CH4	PTE9	UART5_
☑ 13	FTM3_CH5	PTE10	UART5_
☑ 14	I2S0_TX_FS/FTM...	PTE11	UART5_
☑ 15	I2S0_TX_BCLK/F...	PTE12	
□ 16	VDD16		
□ 17	VSS17		
□ 18	VSS18		
□ 19	USB0_DP		
□ 20	USB0_DM		
□ 21	VOUT33		
□ 22	VREGIN		
☑ 23	ADC0_DP1/ADC...		
☑ 24	ADC0_DM1/AD...		
☑ 25	ADC1_DP1/ADC...		
□ 26	ADC1_DM1		
□ 27	ADC0_DP0/ADC...		

Routed Pins - 22 + ^ v

#	Peripheral	Signal	Route to	Direction	Slew rate	Open drain	Drive
7	TPIU	D0	TRACE_D0	Output	Fast	Disabled	Low
8	FTM3	CH, 0	FTM3_CH0	Not Specified	Fast	Disabled	Low
9	FTM3	CH, 1	FTM3_CH1	Not Specified	Fast	Disabled	Low
10	FTM3	CH, 2	FTM3_CH2	Not Specified	Fast	Disabled	Low
11	FTM3	CH, 3	FTM3_CH3	Not Specified	Fast	Disabled	Low
12	FTM3	CH, 4	FTM3_CH4	Not Specified	Fast	Disabled	Low
13	FTM3	CH, 5	FTM3_CH5	Not Specified	Fast	Disabled	Low
! 14	FTM3	CH, 6	FTM3_CH6	Not Specified	Fast	Disabled	Low
! 15	FTM3	CH, 7	FTM3_CH7	Not Specified	Fast	Disabled	Low
24	ADC0	SE, 20	ADC0_DM1	Input	n/a	n/a	n/a

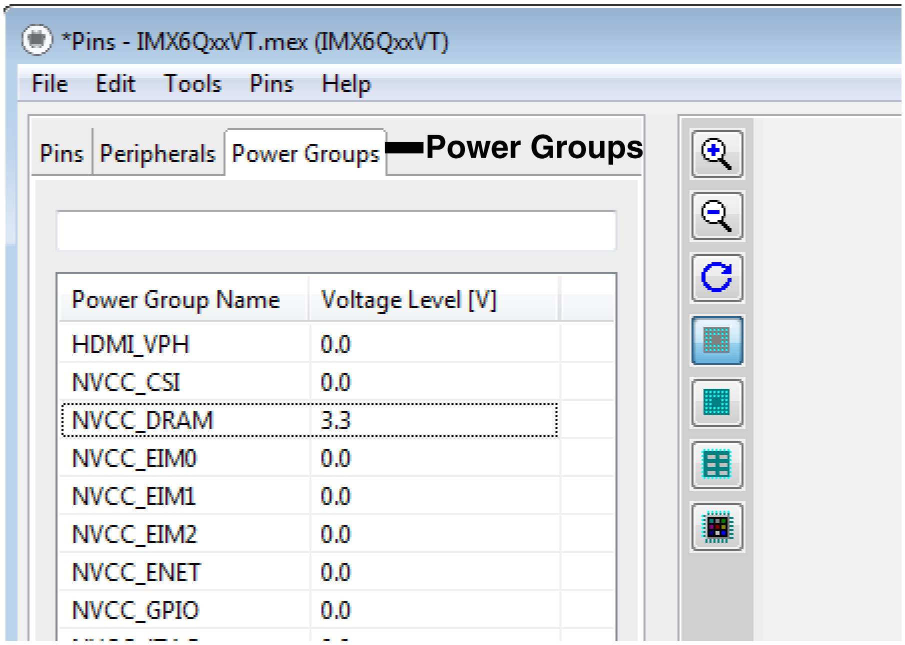
```
/*
 * Copyright (c) 2015, Freescale Semic
 * All rights reserved.
 *
 * Redistribution and use in source an
 * are permitted provided that the fol
 *
 * o Redistributions of source code mu
 *   of conditions and the following d
 *
 * o Redistributions in binary form mu
 *   list of conditions and the follow
 *   other materials provided with the
 *
 * o Neither the name of Freescale Sem
 *   contributors may be used to endor
 *   software without specific prior w
 *
 * THIS SOFTWARE IS PROVIDED BY THE CO
 * ANY EXPRESS OR IMPLIED WARRANTIES,
 * WARRANTIES OF MERCHANTABILITY AND F
 * DISCLAIMED. IN NO EVENT SHALL THE C
 * ANY DIRECT, INDIRECT, INCIDENTAL, S
 * (INCLUDING, BUT NOT LIMITED TO, PRO
 * LOSS OF USE, DATA, OR PROFITS; OR B
 * ANY THEORY OF LIABILITY, WHETHER IN
 * (INCLUDING NEGLIGENCE OR OTHERWISE)
 * SOFTWARE, EVEN IF ADVISED OF THE PO
 *
 */

/*
 * TEXT BELOW IS USED AS SETTING FOR T
PinsProfile:
- !!product 'Pins v1.0'
- !!processor 'MK64FX512xxx12'
- !!package 'MK64FX512VLQ12'
- !!mcu_data 'ksdk2_0'
```

Figure 4-4. Pins tool user interface


Drag and slide to change the size of the window
Click the << icon to expand or restore the window
16
P19
P20
FTM3_
FTM3_
ADCA_
ADCA_
ADCB_
ADCB_
ADCA_C
ADCA_C
ADCA_C
Routed Pins -

#	Peripheral
1	GPIOE
2	GPIOE
3	GPIOE
4	GPIOE
6	FTM3

Figure 4-5. Resizing/restoring window



Power Group Name	Voltage Level [V]
HDMI_VPH	0.0
NVCC_CSI	0.0
NVCC_DRAM	3.3
NVCC_EIM0	0.0
NVCC_EIM1	0.0
NVCC_EIM2	0.0
NVCC_ENET	0.0
NVCC_GPIO	0.0

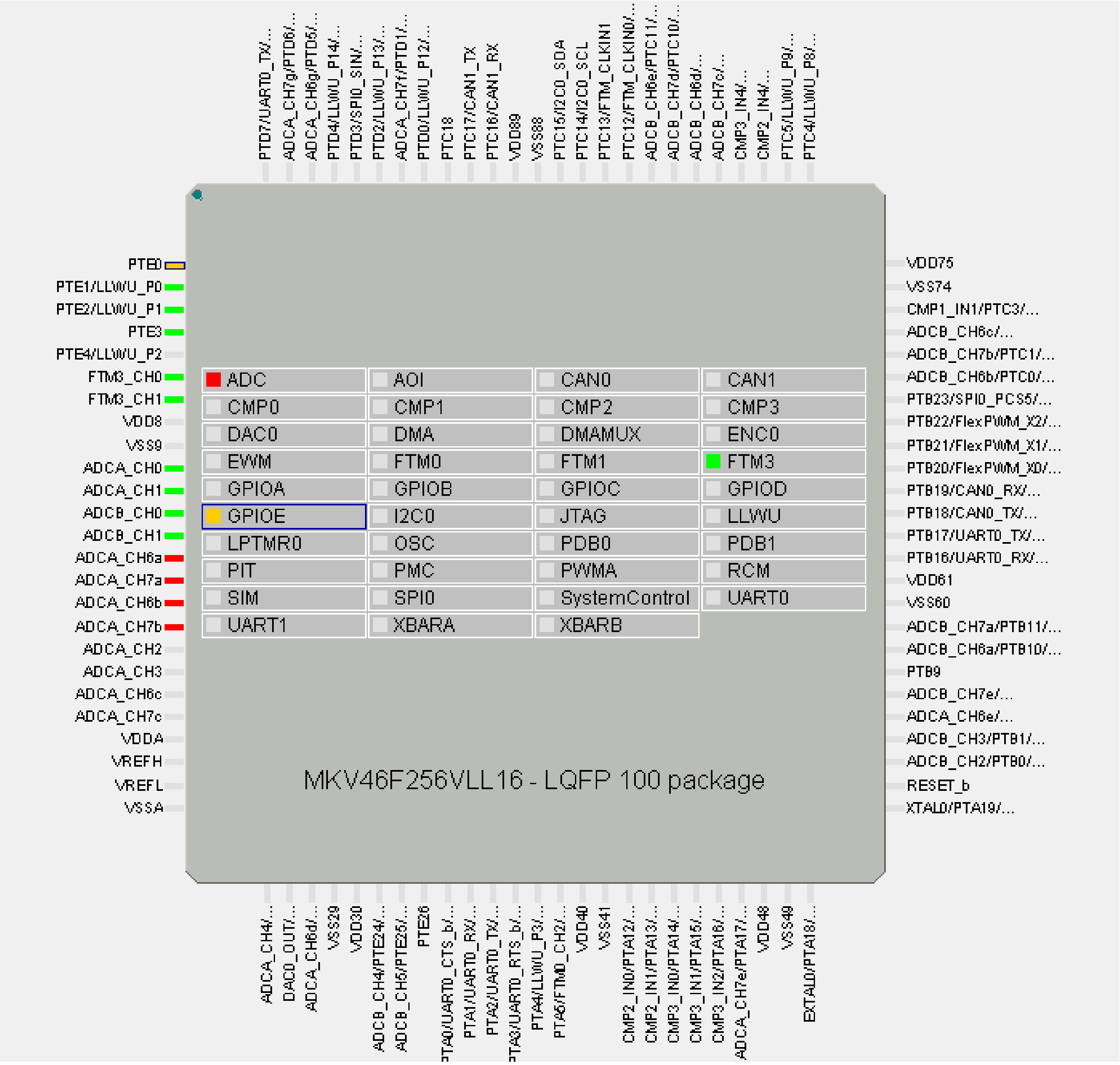
Figure 4-6. Selecting power group

NOTE

Power Groups are not supported for all processors.

4.3.1 Package

The processor package appears in the middle of the Pins tool window. The processor package shows an overall overview of the package including the resources allocation.



This view shows Package overview with pins location. In the middle there are peripherals.

For BGA packages, use the **Show Peripherals** icon to see it.

Green color indicates the routed pins/peripherals.

Gray color indicates that the pin/peripheral is not routed.

The view also shows the package variant and the description (type and number of pins).

The following icons are available in the toolbar:

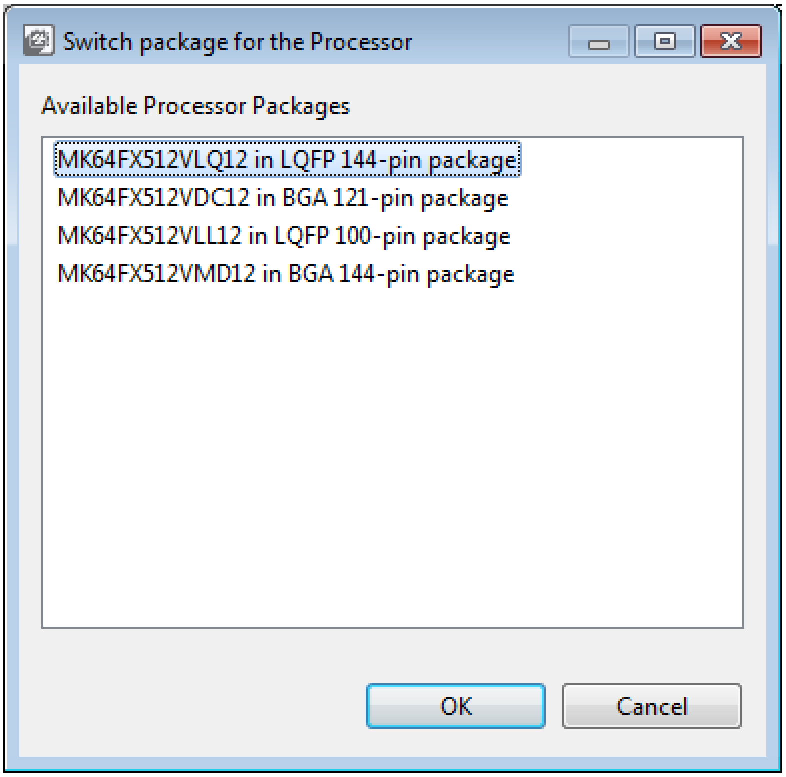
Table 4-1. Toolbar options

Icon	Description
⊕	Zoom in package image.
⊖	Zoom out package image.
↻	Rotate package image.
▦	Show pins as you can see it from the bottom. This option is available on BGA packages only.
▦	Show pins as you can see it from the top. This option is available on BGA packages only.
⊞	Show peripherals. This option is available on BGA packages only.
▣	Switch package.

NOTE

Depending on the processor package selected, not all views are available.

The **Switch package** icon launches the **Select package for the Processor** dialog box.



Switch package for the Processor
Available Processor Packages
OK
Cancel

MK64FX512VLQ12 in LQFP 144-pin package
MK64FX512VDC12 in BGA 121-pin package
MK64FX512VLL12 in LQFP 100-pin package
MK64FX512VMD12 in BGA 144-pin package

Figure 4-7. Switch package

The **Switch package for the Processor** dialog shows list of available processor packages, showing package type and number of pins.

4.3.2 Routed Pins view

This **Routed Pins** view shows a list of routed pins and allows configuriation. This view also allows the configuration of the electrical properties of pins and displays all the pins. It displays the pad configuration available in a configuration where each pin is associated with the signal name and the function.

NOTE

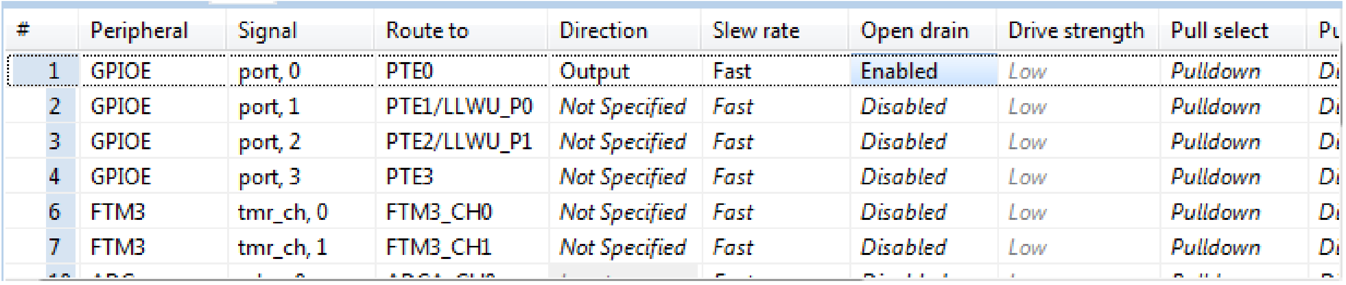
> The electrical features are configured only for pins in the table. For example, the routed pins.

The table is empty when the new project is created, which means no pin configured. Each row represents configuration of one pin and if there are no conflicts, the code is immediately updated.

Use the table drop down menu to configure the pin. To configure pins, start from left to right – select the peripheral first, then select required signal, and finally select the routed pin.

See the right part of the table to configure the electrical features.

If the feature is not supported, n/a is shown.



#	Peripheral	Signal	Route to	Direction	Slew rate	Open drain	Drive strength	Pull select	Pu
1	GPIOE	port, 0	PTE0	Output	Fast	Enabled	*Low*	*Pulldown*	*Di*
2	GPIOE	port, 1	PTE1/LLWU_P0	*Not Specified*	*Fast*	*Disabled*	*Low*	*Pulldown*	*Di*
3	GPIOE	port, 2	PTE2/LLWU_P1	*Not Specified*	*Fast*	*Disabled*	*Low*	*Pulldown*	*Di*
4	GPIOE	port, 3	PTE3	*Not Specified*	*Fast*	*Disabled*	*Low*	*Pulldown*	*Di*
6	FTM3	tmr_ch, 0	FTM3_CH0	*Not Specified*	*Fast*	*Disabled*	*Low*	*Pulldown*	*Di*
7	FTM3	tmr_ch, 1	FTM3_CH1	*Not Specified*	*Fast*	*Disabled*	*Low*	*Pulldown*	*Di*

Figure 4-8. Routed Pins view

The gray background indicates the read-only items.

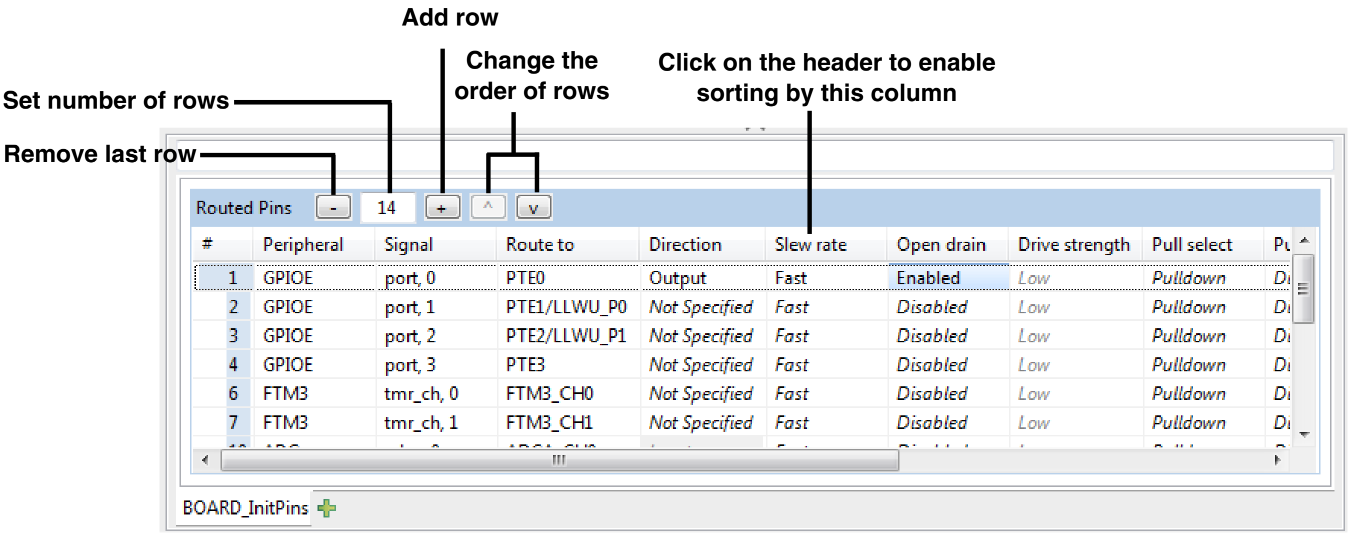
The italic value indicates that the value is not configured and it shows the after-reset value and no code is generated, so the configuration relies on the after reset value.

💬	The value shown using italic indicates the after-reset value. The real value may be different from the after reset value, if configured in other functions.
Use the drop down menu to select the required value.	
💬	If you select a similiar value as the after-reset value, the tool will always generate code to set this feature.
Use the drop-down menu to reset the value to its after-reset state.	
💬	If an item doesn't support reset to after reset value, or current value already represents after reset state, the **Reset** menu is not available.

The first row shows pin number or coordinate on BGA package.

4.3.3 View controls

The following figure illustrated the Routed pins view controls.



#	Peripheral	Signal	Route to	Direction	Slew rate	Open drain	Drive strength	Pull select	Pu
1	GPIOE	port, 0	PTE0	Output	Fast	Enabled	Low	Pulldown	Di
2	GPIOE	port, 1	PTE1/LLWU_P0	Not Specified	Fast	Disabled	Low	Pulldown	Di
3	GPIOE	port, 2	PTE2/LLWU_P1	Not Specified	Fast	Disabled	Low	Pulldown	Di
4	GPIOE	port, 3	PTE3	Not Specified	Fast	Disabled	Low	Pulldown	Di
6	FTM3	tmr_ch, 0	FTM3_CH0	Not Specified	Fast	Disabled	Low	Pulldown	Di
7	FTM3	tmr_ch, 1	FTM3_CH1	Not Specified	Fast	Disabled	Low	Pulldown	Di

Figure 4-9. View controls

Add / remove rows:

- To add a new row to the end of table, click on the [+] icon.
- To remove the last row, click on the [-] icon.
- To delete a specific row or insert a new row at a given position, right-click and use the pop-up menu commands.

Add a specific number of rows or clear the table:

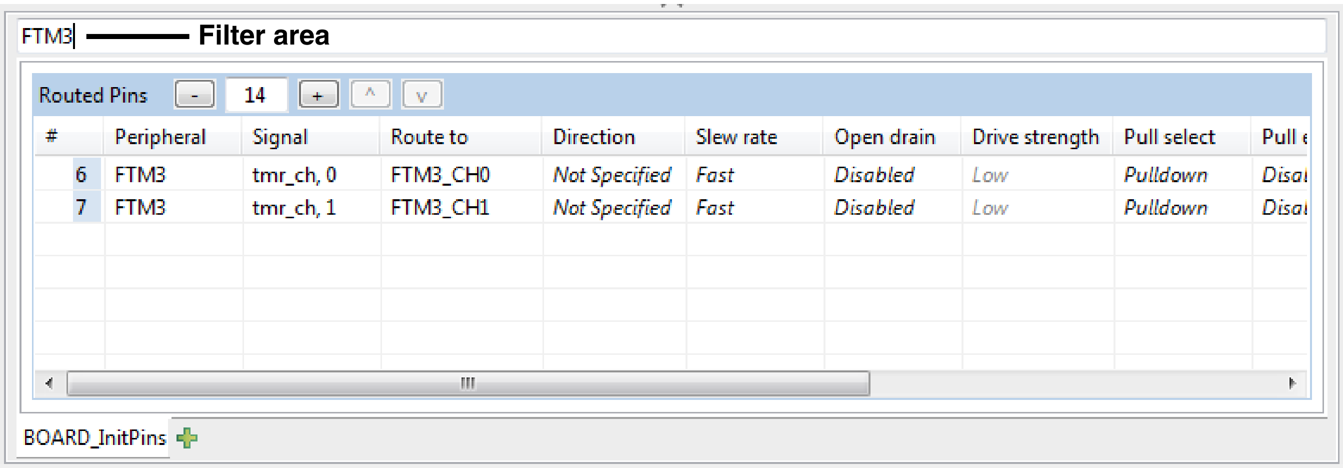
- To add a specific number of rows, specify the exact number of rows.
- To clear the table, type 0.

Change the order of the rows:

To change the order of the rows, use the arrow icons to move one row up or down.

4.3.4 Filtering routed pins

The following image illustrated the filter are of the **Routed Pins** view.



#	Peripheral	Signal	Route to	Direction	Slew rate	Open drain	Drive strength	Pull select	Pull e
6	FTM3	tmr_ch, 0	FTM3_CH0	*Not Specified*	*Fast*	*Disabled*	*Low*	*Pulldown*	*Disa*
7	FTM3	tmr_ch, 1	FTM3_CH1	*Not Specified*	*Fast*	*Disabled*	*Low*	*Pulldown*	*Disa*

Figure 4-10. Filter area

To instantly filter rows, type the text or the search phrase in the filter area.

NOTE

When you enter the search text, it also searches the text in the full pin names displays rows that contain the search text.

4.3.5 Highlighting and color coding

It is possible to easily identify routed pins/peripherals on the package using highlighting. By default, the current selection (pin/peripheral) is highlighted in the package view.

- Error (red) indicates that the pin has an error.
- Used (green) indicates that the pin is muxed.
- Not used (light grey) indicates that the pin is available for mux, but is not muxed.
- Selected (yellow border around the pin such that the other color is still visible) indicates that the pin is selected. For example, by peripheral or by pin.

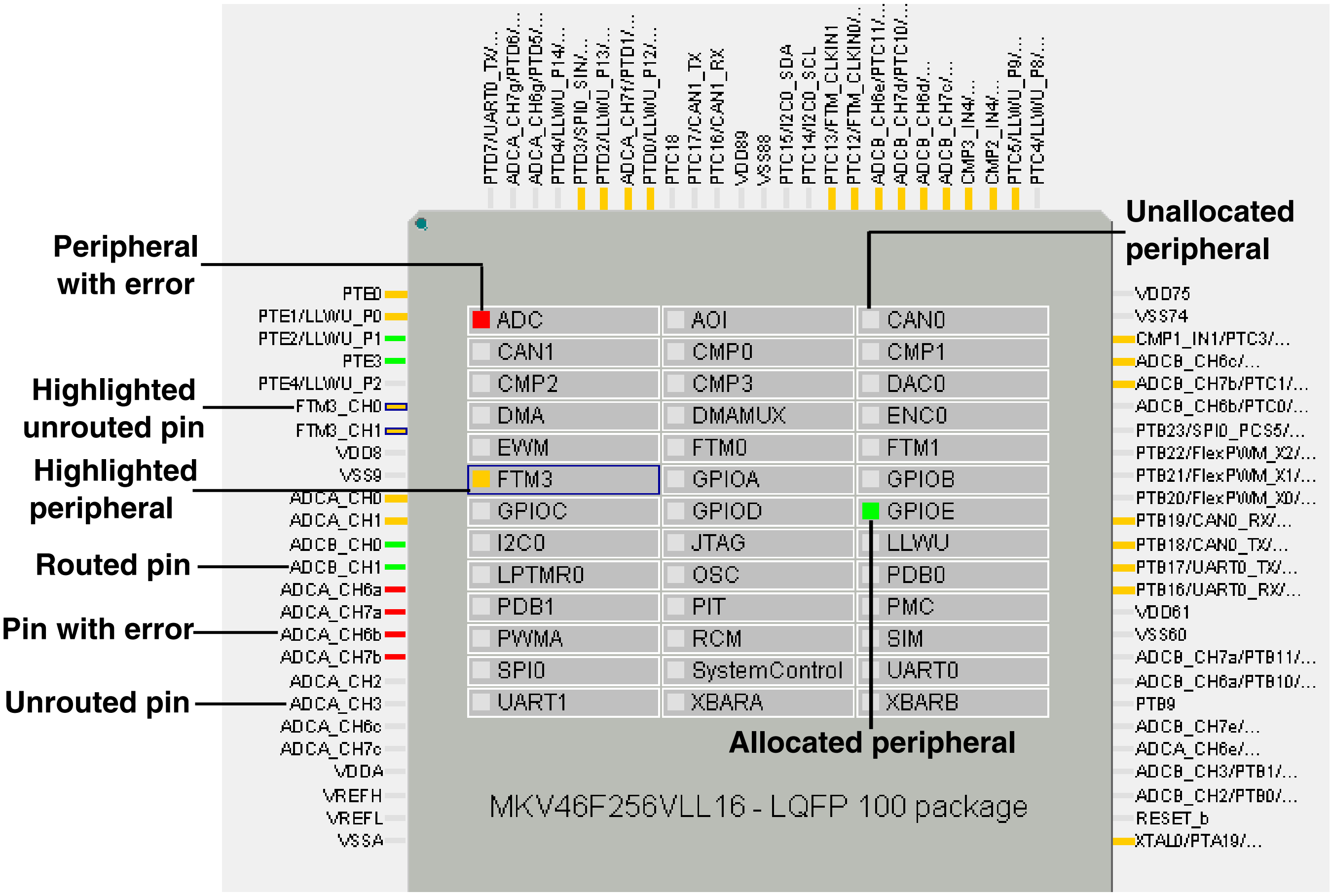
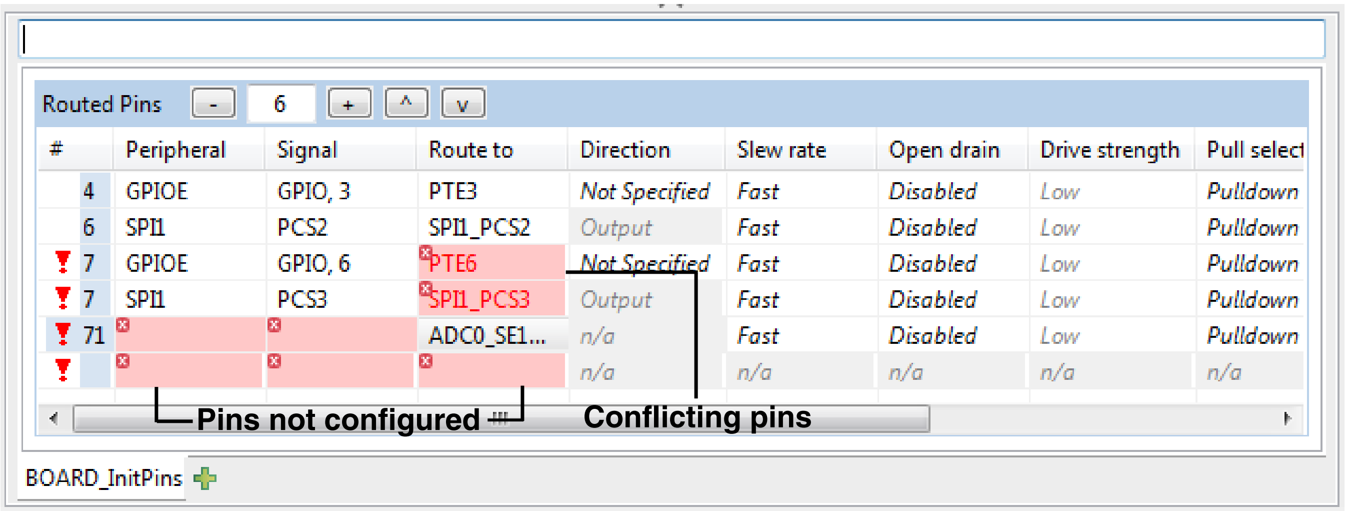
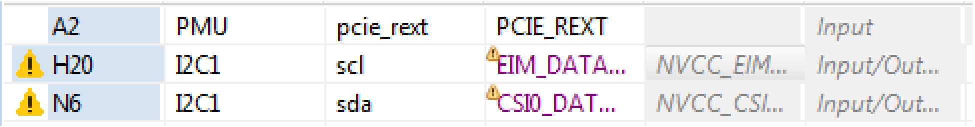


Figure 4-11. Highlighting and color coding



#		Peripheral	Signal	Route to	Direction	Slew rate	Open drain	Drive strength	Pull select
	4	GPIOE	GPIO, 3	PTE3	Not Specified	Fast	Disabled	Low	Pulldown
	6	SPI1	PCS2	SPI1_PCS2	Output	Fast	Disabled	Low	Pulldown
❗	7	GPIOE	GPIO, 6	☒PTE6	Not Specified	Fast	Disabled	Low	Pulldown
❗	7	SPI1	PCS3	☒SPI1_PCS3	Output	Fast	Disabled	Low	Pulldown
❗	71	☒	☒	ADC0_SE1...	n/a	Fast	Disabled	Low	Pulldown
❗		☒	☒	☒	n/a	n/a	n/a	n/a	n/a

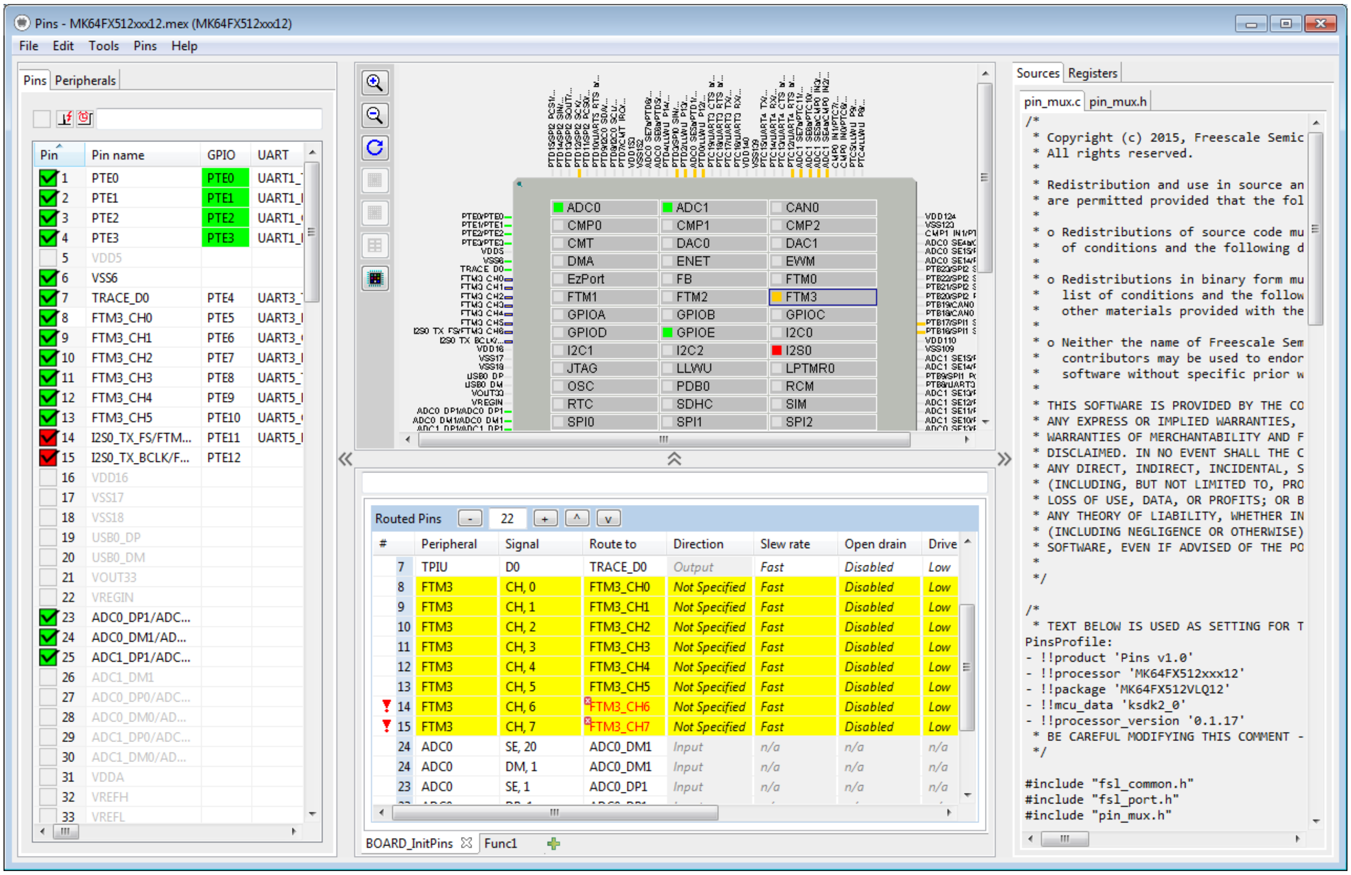
Figure 4-12. Pins conflicts



	A2	PMU	pcie_rext	PCIE_REXT		Input
⚠	H20	I2C1	scl	⚠EIM_DATA...	NVCC_EIM...	Input/Out...
⚠	N6	I2C1	sda	⚠CSI0_DAT...	NVCC_CSI...	Input/Out...

Figure 4-13. Warnings

- Package view
  - Click on the peripheral or use the pop-up menu to highlight peripherals:
    - and all allocated pins (to selected peripheral)
    - or all available pins if nothing is allocated yet
  - Click on the pin or use the pop-up menu to highlight the pin and the peripherals.
  - Click outside the package to cancel the highlight.
- Peripherals/pins view
  - Peripheral and pin behaves as described above image
  - Keyboard can be used for (multiple) selection. This works only for Desktop version.



Pin	Pin name	GPIO	UART
☑ 1	PTE0	PTE0	UART1_
☑ 2	PTE1	PTE1	UART1_
☑ 3	PTE2	PTE2	UART1_
☑ 4	PTE3	PTE3	UART1_
□ 5	VDD5		
☑ 6	VSS6		
☑ 7	TRACE_D0	PTE4	UART3_
☑ 8	FTM3_CH0	PTE5	UART3_
☑ 9	FTM3_CH1	PTE6	UART3_
☑ 10	FTM3_CH2	PTE7	UART3_
☑ 11	FTM3_CH3	PTE8	UART5_
☑ 12	FTM3_CH4	PTE9	UART5_
☑ 13	FTM3_CH5	PTE10	UART5_
☑ 14	I2S0_TX_FS/FTM...	PTE11	UART5_
☑ 15	I2S0_TX_BCLK/F...	PTE12	
□ 16	VDD16		
□ 17	VSS17		
□ 18	VSS18		
□ 19	USB0_DP		
□ 20	USB0_DM		
□ 21	VOUT33		
□ 22	VREGIN		
☑ 23	ADC0_DP1/ADC...		
☑ 24	ADC0_DM1/AD...		
☑ 25	ADC1_DP1/ADC...		
□ 26	ADC1_DM1		
□ 27	ADC0_DP0/ADC...		
□ 28	ADC0_DM0/AD...		
□ 29	ADC1_DP0/ADC...		
□ 30	ADC1_DM0/AD...		
□ 31	VDDA		
□ 32	VREFH		
□ 33	VREFL		

Routed Pins [-] 22 [+] [^] [v]

#	Peripheral	Signal	Route to	Direction	Slew rate	Open drain	Drive
7	TPIU	D0	TRACE_D0	Output	Fast	Disabled	Low
8	FTM3	CH, 0	FTM3_CH0	Not Specified	Fast	Disabled	Low
9	FTM3	CH, 1	FTM3_CH1	Not Specified	Fast	Disabled	Low
10	FTM3	CH, 2	FTM3_CH2	Not Specified	Fast	Disabled	Low
11	FTM3	CH, 3	FTM3_CH3	Not Specified	Fast	Disabled	Low
12	FTM3	CH, 4	FTM3_CH4	Not Specified	Fast	Disabled	Low
13	FTM3	CH, 5	FTM3_CH5	Not Specified	Fast	Disabled	Low
! 14	FTM3	CH, 6	FTM3_CH6	Not Specified	Fast	Disabled	Low
! 15	FTM3	CH, 7	FTM3_CH7	Not Specified	Fast	Disabled	Low
24	ADC0	SE, 20	ADC0_DM1	Input	n/a	n/a	n/a
24	ADC0	DM, 1	ADC0_DM1	Input	n/a	n/a	n/a
23	ADC0	SE, 1	ADC0_DP1	Input	n/a	n/a	n/a

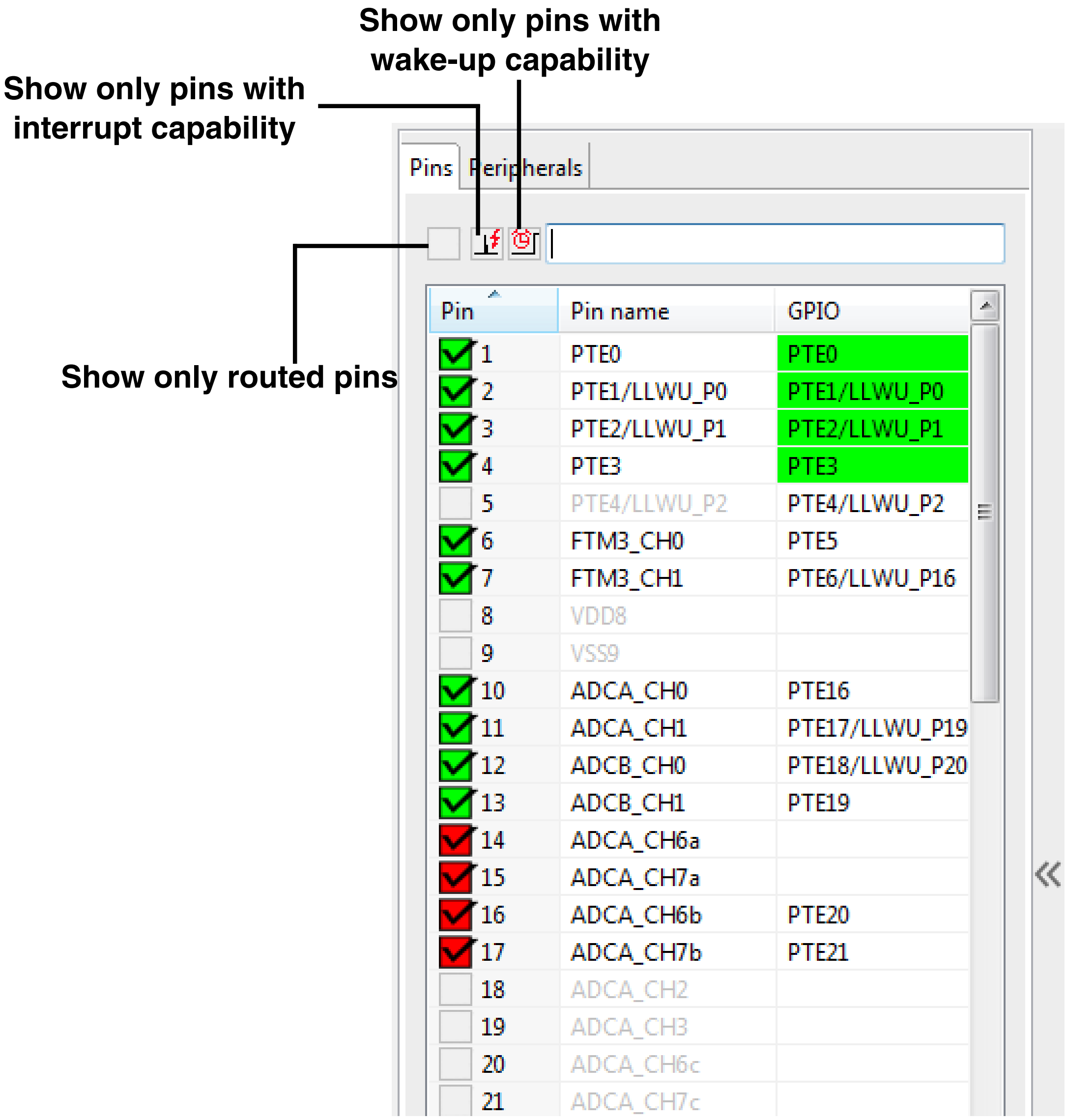
```
/*
 * Copyright (c) 2015, Freescale Semic
 * All rights reserved.
 *
 * Redistribution and use in source an
 * are permitted provided that the fol
 *
 * o Redistributions of source code mu
 *   of conditions and the following d
 *
 * o Redistributions in binary form mu
 *   list of conditions and the follow
 *   other materials provided with the
 *
 * o Neither the name of Freescale Sem
 *   contributors may be used to endor
 *   software without specific prior w
 *
 * THIS SOFTWARE IS PROVIDED BY THE CO
 * ANY EXPRESS OR IMPLIED WARRANTIES,
 * WARRANTIES OF MERCHANTABILITY AND F
 * DISCLAIMED. IN NO EVENT SHALL THE C
 * ANY DIRECT, INDIRECT, INCIDENTAL, S
 * (INCLUDING, BUT NOT LIMITED TO, PRO
 * LOSS OF USE, DATA, OR PROFITS; OR B
 * ANY THEORY OF LIABILITY, WHETHER IN
 * (INCLUDING NEGLIGENCE OR OTHERWISE)
 * SOFTWARE, EVEN IF ADVISED OF THE PO
 *
 */

/*
 * TEXT BELOW IS USED AS SETTING FOR T
PinsProfile:
- !!product 'Pins v1.0'
- !!processor 'MK64FX512xxx12'
- !!package 'MK64FX512VLQ12'
- !!mcu_data 'ksdk2_0'
- !!processor_version '0.1.17'
 * BE CAREFUL MODIFYING THIS COMMENT -
 */

#include "fsl_common.h"
#include "fsl_port.h"
#include "pin_mux.h"
```

Figure 4-14. Pins tool interface

🖥	Desktop version of the too highlights pins during the drop-down menu traversal on pins

4.3.6 Filtering in the Pins view

The following image illustrates the filtering controls in the Pins view.



Show only pins with wake-up capability

Show only pins with interrupt capability

Show only routed pins

Pin	Pin name	GPIO
🟩✓ 1	PTE0	🟩 PTE0
🟩✓ 2	PTE1/LLWU_P0	🟩 PTE1/LLWU_P0
🟩✓ 3	PTE2/LLWU_P1	🟩 PTE2/LLWU_P1
🟩✓ 4	PTE3	🟩 PTE3
☐ 5	PTE4/LLWU_P2	PTE4/LLWU_P2
🟩✓ 6	FTM3_CH0	PTE5
🟩✓ 7	FTM3_CH1	PTE6/LLWU_P16
☐ 8	VDD8	
☐ 9	VSS9	
🟩✓ 10	ADCA_CH0	PTE16
🟩✓ 11	ADCA_CH1	PTE17/LLWU_P19
🟩✓ 12	ADCB_CH0	PTE18/LLWU_P20
🟩✓ 13	ADCB_CH1	PTE19
🟥✓ 14	ADCA_CH6a	
🟥✓ 15	ADCA_CH7a	
🟥✓ 16	ADCA_CH6b	PTE20
🟥✓ 17	ADCA_CH7b	PTE21
☐ 18	ADCA_CH2	
☐ 19	ADCA_CH3	
☐ 20	ADCA_CH6c	
☐ 21	ADCA_CH7c	

Figure 4-15. Filtering Controls

Type any text to search across the table. It will search for the pins features, like wake-up feature, or the low-power feature.

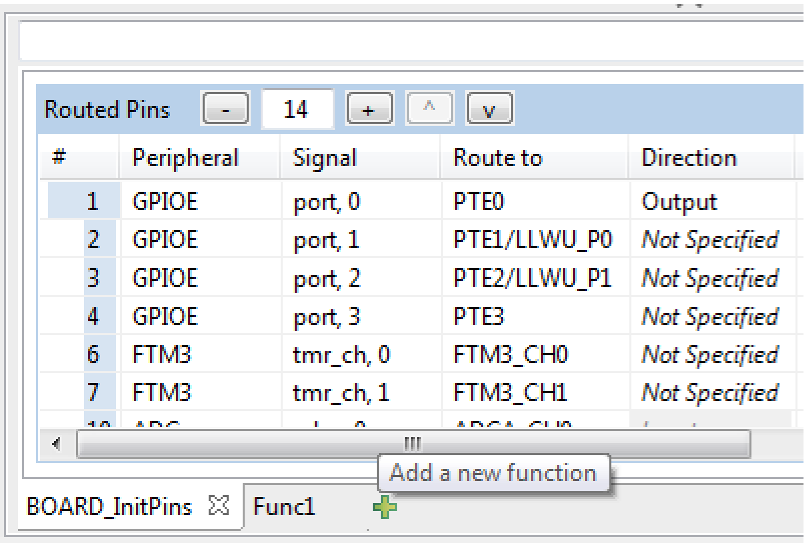
To see only pins on the selected peripheral, click on the header to sort pins for given peripheral by name.

Click on the first checkbox icon to see all or the routed pins only.

4.3.7 Functions

'Functions' are used to group a set of routed pins, and it will create code for the configuration in a function which then can be called by the application.

The tool creates multiple functions that can be used to configure pin muxing.

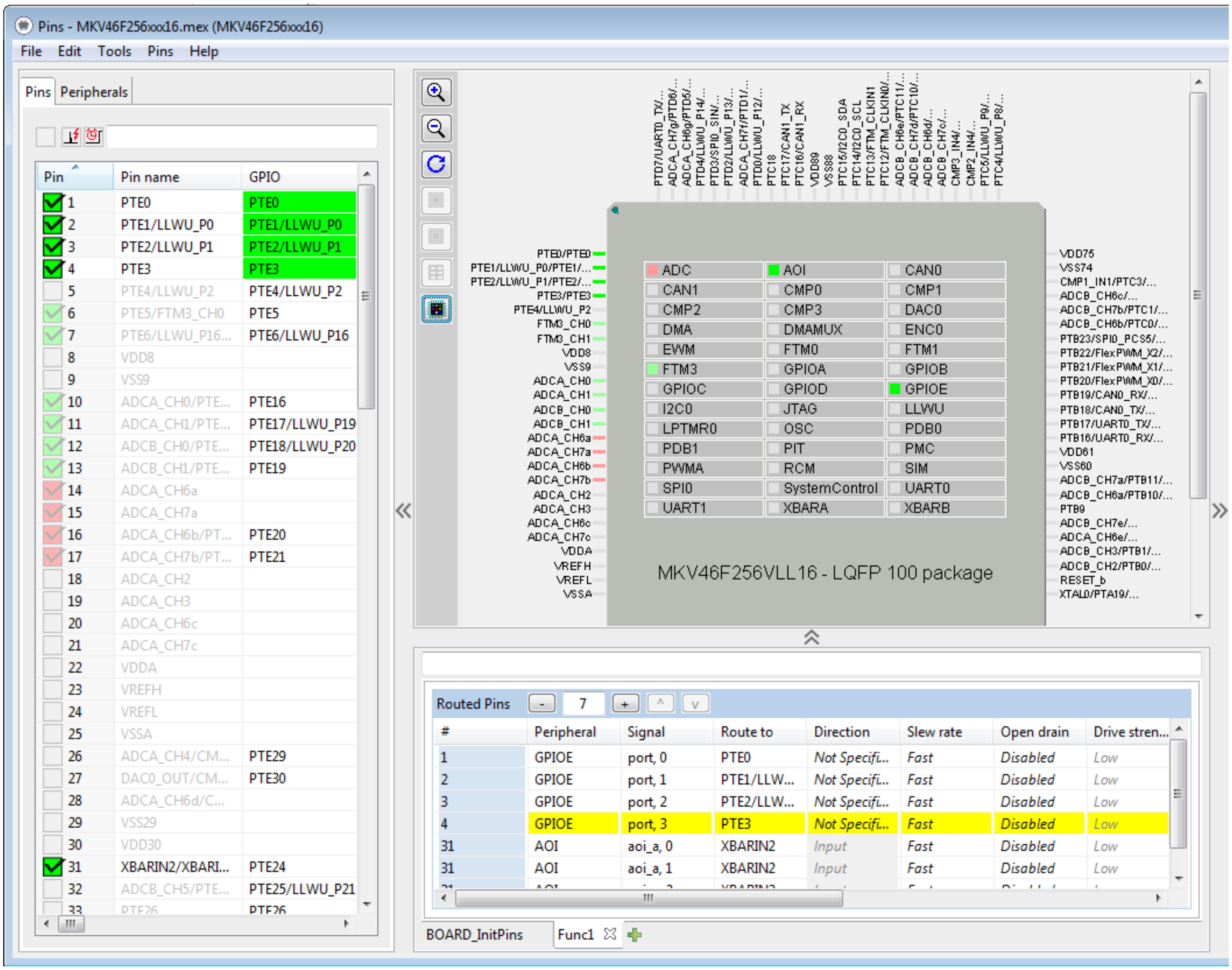


#	Peripheral	Signal	Route to	Direction
1	GPIOE	port, 0	PTE0	Output
2	GPIOE	port, 1	PTE1/LLWU_P0	*Not Specified*
3	GPIOE	port, 2	PTE2/LLWU_P1	*Not Specified*
4	GPIOE	port, 3	PTE3	*Not Specified*
6	FTM3	tmr_ch, 0	FTM3_CH0	*Not Specified*
7	FTM3	tmr_ch, 1	FTM3_CH1	*Not Specified*

Figure 4-16. Routed pins

The tool does not limit nor indicate the usage of pins in each function. Each function can define a set of routed pins or re-configure already routed pins.

When multiple functions are specified in the configuration, the package view primarily shows the pins and the peripherals for the selected function. Pins and peripherals for different functions are shown with light transparency and cannot be configured, until switched to this function.



Pin	Pin name	GPIO
✓ 1	PTE0	PTE0
✓ 2	PTE1/LLWU_P0	PTE1/LLWU_P0
✓ 3	PTE2/LLWU_P1	PTE2/LLWU_P1
✓ 4	PTE3	PTE3
□ 5	PTE4/LLWU_P2	PTE4/LLWU_P2
✓ 6	PTE5/FTM3_CH0	PTE5
✓ 7	PTE6/LLWU_P16...	PTE6/LLWU_P16
□ 8	VDD8	
□ 9	VSS9	
✓ 10	ADCA_CH0/PTE...	PTE16
✓ 11	ADCA_CH1/PTE...	PTE17/LLWU_P19
✓ 12	ADCB_CH0/PTE...	PTE18/LLWU_P20
✓ 13	ADCB_CH1/PTE...	PTE19
✓ 14	ADCA_CH6a	
✓ 15	ADCA_CH7a	
✓ 16	ADCA_CH6b/PT...	PTE20
✓ 17	ADCA_CH7b/PT...	PTE21
□ 18	ADCA_CH2	
□ 19	ADCA_CH3	
□ 20	ADCA_CH6c	
□ 21	ADCA_CH7c	
□ 22	VDDA	
□ 23	VREFH	
□ 24	VREFL	
□ 25	VSSA	
□ 26	ADCA_CH4/CM...	PTE29
□ 27	DAC0_OUT/CM...	PTE30
□ 28	ADCA_CH6d/C...	
□ 29	VSS29	
□ 30	VDD30	
✓ 31	XBARIN2/XBARI...	PTE24
□ 32	ADCB_CH5/PTE...	PTE25/LLWU_P21
□ 33	PTE26	PTE26

🟥 ADC	🟩 AOI	CAN0
CAN1	CMP0	CMP1
CMP2	CMP3	DAC0
DMA	DMAMUX	ENC0
EWM	FTM0	FTM1
🟩 FTM3	GPIOA	GPIOB
GPIOC	GPIOD	🟩 GPIOE
I2C0	JTAG	LLWU
LPTMR0	OSC	PDB0
PDB1	PIT	PMC
PWMA	RCM	SIM
SPI0	SystemControl	UART0
UART1	XBARA	XBARB

Routed Pins - 7 + ^ v

#	Peripheral	Signal	Route to	Direction	Slew rate	Open drain	Drive stren...
1	GPIOE	port, 0	PTE0	*Not Specifi...*	*Fast*	*Disabled*	*Low*
2	GPIOE	port, 1	PTE1/LLW...	*Not Specifi...*	*Fast*	*Disabled*	*Low*
3	GPIOE	port, 2	PTE2/LLW...	*Not Specifi...*	*Fast*	*Disabled*	*Low*
4	GPIOE	port, 3	PTE3	*Not Specifi...*	*Fast*	*Disabled*	*Low*
31	AOI	aoi_a, 0	XBARIN2	*Input*	*Fast*	*Disabled*	*Low*
31	AOI	aoi_a, 1	XBARIN2	*Input*	*Fast*	*Disabled*	*Low*

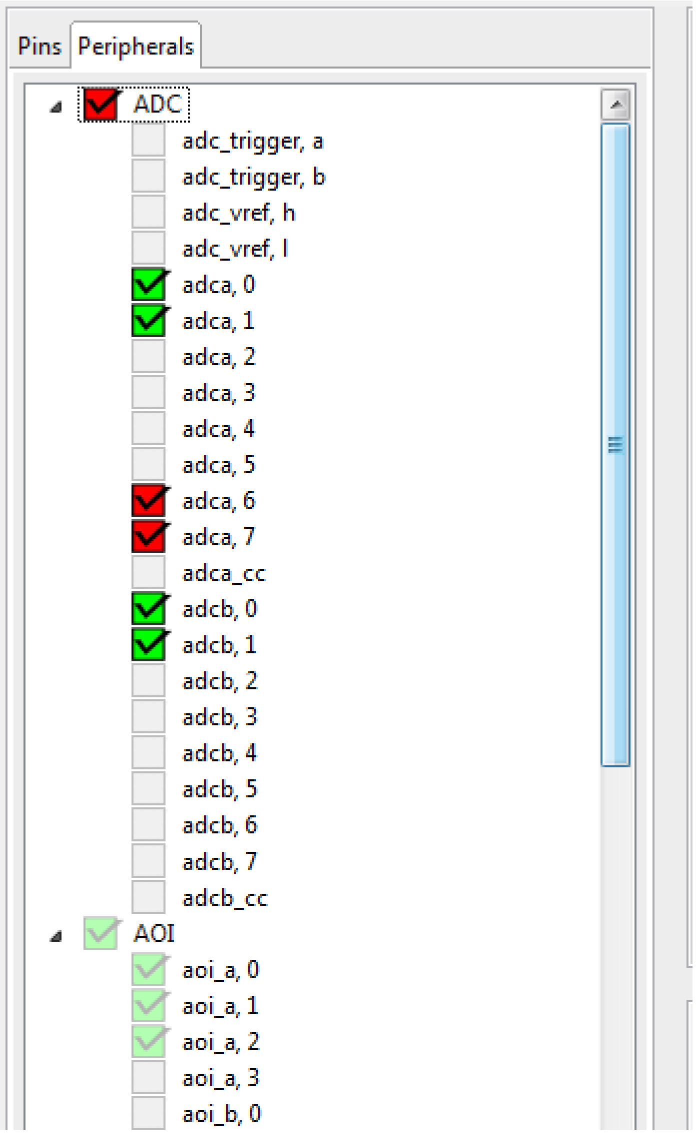
Figure 4-17. Pins and peripherals

4.3.8 Peripherals view

The **Peripherals** view shows a list of peripheral and its signals. Only the **Peripherals** and **Pins** view shows the checkbox (allocated) with status.

Table 4-2. Status codes

Color code	Status
✓ port, 1	Error
✓ port, 2	Allocated
□ port, 3	Available
✓ port, 16	Warning

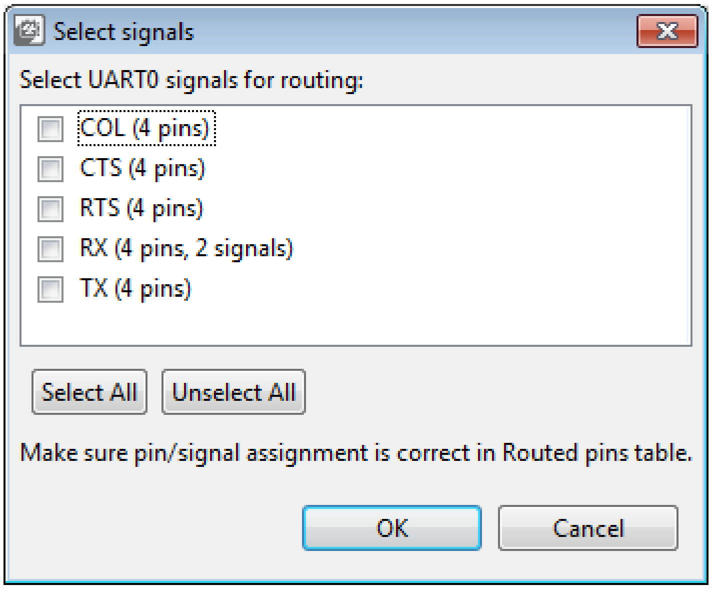


- ☑ ADC
  - □ adc_trigger, a
  - □ adc_trigger, b
  - □ adc_vref, h
  - □ adc_vref, l
  - ☑ adca, 0
  - ☑ adca, 1
  - □ adca, 2
  - □ adca, 3
  - □ adca, 4
  - □ adca, 5
  - ☑ adca, 6
  - ☑ adca, 7
  - □ adca_cc
  - ☑ adcb, 0
  - ☑ adcb, 1
  - □ adcb, 2
  - □ adcb, 3
  - □ adcb, 4
  - □ adcb, 5
  - □ adcb, 6
  - □ adcb, 7
  - □ adcb_cc
- ☑ AOI
  - ☑ aoi_a, 0
  - ☑ aoi_a, 1
  - ☑ aoi_a, 2
  - □ aoi_a, 3
  - □ aoi_b, 0

Figure 4-18. Peripherals tab

Use the checkbox to route/unroute the selected pins.

To route/unroute multiple pins, click on the peripheral and select the options in the Select signals dialog box.



Select signals

Select UART0 signals for routing:

□ COL (4 pins)
□ CTS (4 pins)
□ RTS (4 pins)
□ RX (4 pins, 2 signals)
□ TX (4 pins)

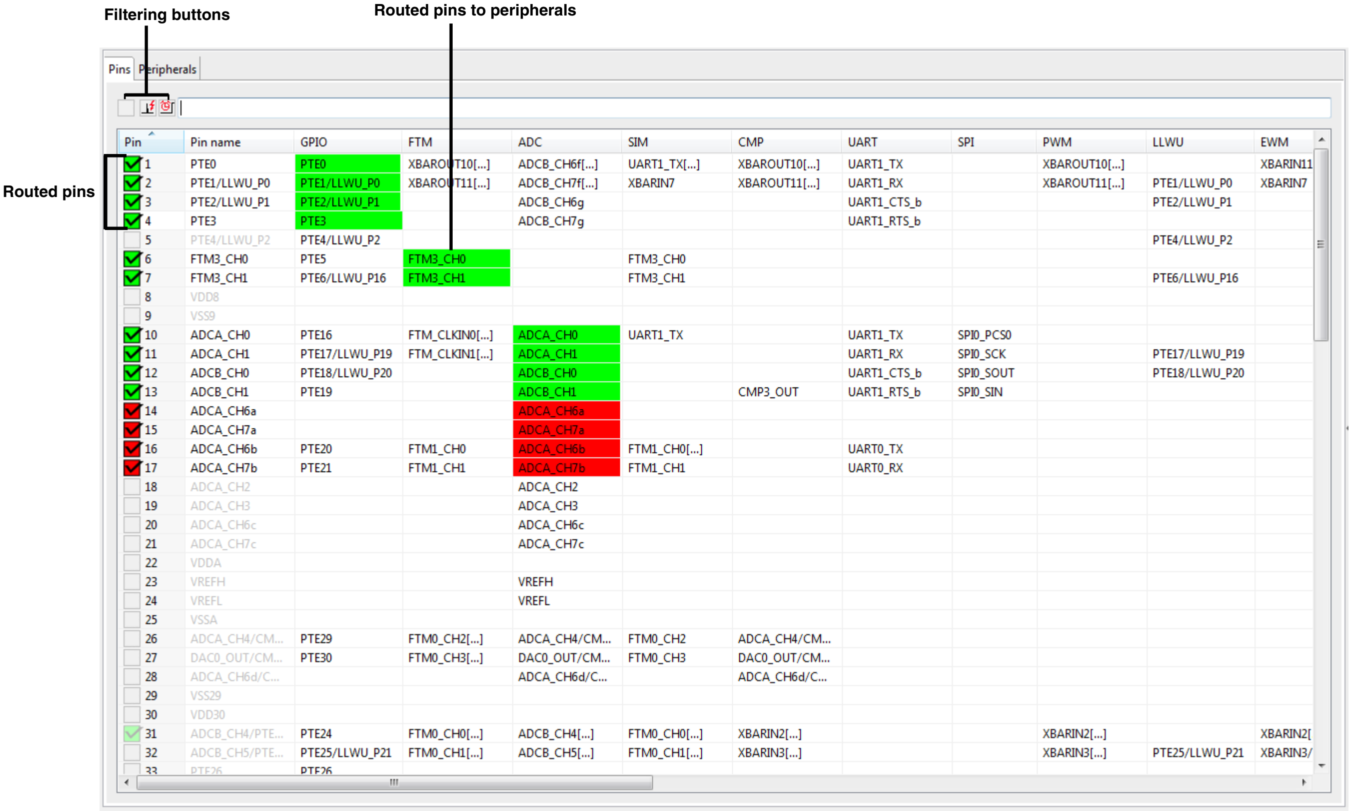
Make sure pin/signal assignment is correct in Routed pins table.

Figure 4-19. Select signals dialog box

💬	If more signals can be routed to one pin, it is indicated by […]. Multiple signals configuration dialog appears, if clicked.

4.3.9 Pins table

The **Pins** table view shows all the pins in a tabular format.



Pin	Pin name	GPIO	FTM	ADC	SIM	CMP	UART	SPI	PWM	LLWU	EWM
☑ 1	PTE0	PTE0	XBAROUT10[...]	ADCB_CH6f[...]	UART1_TX[...]	XBAROUT10[...]	UART1_TX		XBAROUT10[...]		XBARIN11
☑ 2	PTE1/LLWU_P0	PTE1/LLWU_P0	XBAROUT11[...]	ADCB_CH7f[...]	XBARIN7	XBAROUT11[...]	UART1_RX		XBAROUT11[...]	PTE1/LLWU_P0	XBARIN7
☑ 3	PTE2/LLWU_P1	PTE2/LLWU_P1		ADCB_CH6g			UART1_CTS_b			PTE2/LLWU_P1	
☑ 4	PTE3	PTE3		ADCB_CH7g			UART1_RTS_b				
□ 5	PTE4/LLWU_P2	PTE4/LLWU_P2								PTE4/LLWU_P2	
☑ 6	FTM3_CH0	PTE5	FTM3_CH0		FTM3_CH0						
☑ 7	FTM3_CH1	PTE6/LLWU_P16	FTM3_CH1		FTM3_CH1					PTE6/LLWU_P16	
□ 8	VDD8										
□ 9	VSS9										
☑ 10	ADCA_CH0	PTE16	FTM_CLKIN0[...]	ADCA_CH0	UART1_TX		UART1_TX	SPI0_PCS0			
☑ 11	ADCA_CH1	PTE17/LLWU_P19	FTM_CLKIN1[...]	ADCA_CH1			UART1_RX	SPI0_SCK		PTE17/LLWU_P19	
☑ 12	ADCB_CH0	PTE18/LLWU_P20		ADCB_CH0			UART1_CTS_b	SPI0_SOUT		PTE18/LLWU_P20	
☑ 13	ADCB_CH1	PTE19		ADCB_CH1		CMP3_OUT	UART1_RTS_b	SPI0_SIN			
☑ 14	ADCA_CH6a			ADCA_CH6a							
☑ 15	ADCA_CH7a			ADCA_CH7a							
☑ 16	ADCA_CH6b	PTE20	FTM1_CH0	ADCA_CH6b	FTM1_CH0[...]		UART0_TX				
☑ 17	ADCA_CH7b	PTE21	FTM1_CH1	ADCA_CH7b	FTM1_CH1		UART0_RX				
□ 18	ADCA_CH2			ADCA_CH2							
□ 19	ADCA_CH3			ADCA_CH3							
□ 20	ADCA_CH6c			ADCA_CH6c							
□ 21	ADCA_CH7c			ADCA_CH7c							
□ 22	VDDA										
□ 23	VREFH			VREFH							
□ 24	VREFL			VREFL							
□ 25	VSSA										
□ 26	ADCA_CH4/CM...	PTE29	FTM0_CH2[...]	ADCA_CH4/CM...	FTM0_CH2	ADCA_CH4/CM...					
□ 27	DAC0_OUT/CM...	PTE30	FTM0_CH3[...]	DAC0_OUT/CM...	FTM0_CH3	DAC0_OUT/CM...					
□ 28	ADCA_CH6d/C...			ADCA_CH6d/C...		ADCA_CH6d/C...					
□ 29	VSS29										
□ 30	VDD30										
☑ 31	ADCB_CH4/PTE...	PTE24	FTM0_CH0[...]	ADCB_CH4[...]	FTM0_CH0[...]	XBARIN2[...]			XBARIN2[...]		XBARIN2[
□ 32	ADCB_CH5/PTE...	PTE25/LLWU_P21	FTM0_CH1[...]	ADCB_CH5[...]	FTM0_CH1[...]	XBARIN3[...]			XBARIN3[...]	PTE25/LLWU_P21	XBARIN3/
□ 33	PTE26	PTE26									

Figure 4-20. Pins table view

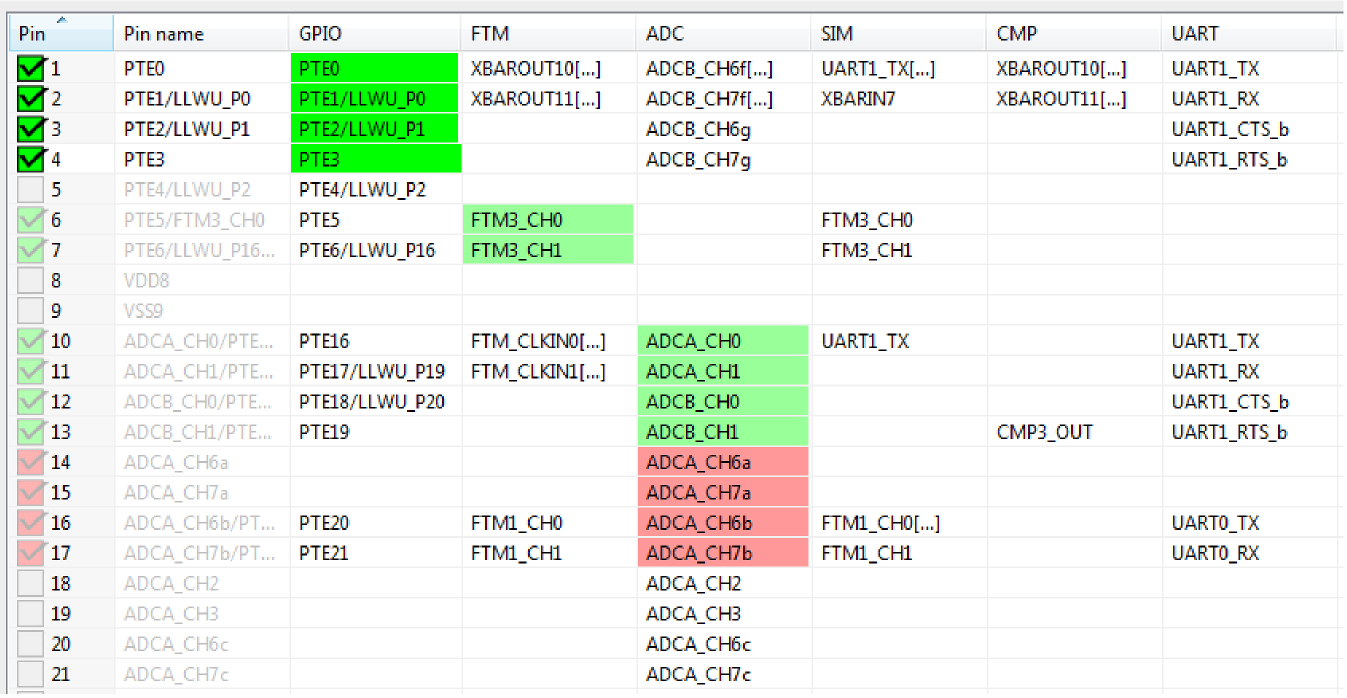
This view shows the list of all the pins available on a given device. The **Pin name** column shows the default name of the pin, or if the pin is routed. The pin name is changed to show appropriate function for selected peripheral if routed. The next columns of the table shows peripherals and pin name(s) on given peripheral. Peripheral with few items is cumulated in the last column.

To route/un-route pin to the given peripheral, click in the cell of the table. Routed pins are marked with checkbox and green color. Colored cells indicates pin is routed to given peripherals. If there is conflict in routing, red color is used.

Unroute is possible by clicking on given cell, or by checkbox in the first column.

Every routed pin appears in the Routed pins table.

When multiple functions specified in the configuration, the pins table view shows pins for selected function primarily. Pins for different functions are shown with light transparency and can't be configured, until switched to this function.



Pin	Pin name	GPIO	FTM	ADC	SIM	CMP	UART
☑ 1	PTE0	PTE0	XBAROUT10[…]	ADCB_CH6f[…]	UART1_TX[…]	XBAROUT10[…]	UART1_TX
☑ 2	PTE1/LLWU_P0	PTE1/LLWU_P0	XBAROUT11[…]	ADCB_CH7f[…]	XBARIN7	XBAROUT11[…]	UART1_RX
☑ 3	PTE2/LLWU_P1	PTE2/LLWU_P1		ADCB_CH6g			UART1_CTS_b
☑ 4	PTE3	PTE3		ADCB_CH7g			UART1_RTS_b
☐ 5	PTE4/LLWU_P2	PTE4/LLWU_P2					
☑ 6	PTE5/FTM3_CH0	PTE5	FTM3_CH0		FTM3_CH0		
☑ 7	PTE6/LLWU_P16…	PTE6/LLWU_P16	FTM3_CH1		FTM3_CH1		
☐ 8	VDD8						
☐ 9	VSS9						
☑ 10	ADCA_CH0/PTE…	PTE16	FTM_CLKIN0[…]	ADCA_CH0	UART1_TX		UART1_TX
☑ 11	ADCA_CH1/PTE…	PTE17/LLWU_P19	FTM_CLKIN1[…]	ADCA_CH1			UART1_RX
☑ 12	ADCB_CH0/PTE…	PTE18/LLWU_P20		ADCB_CH0			UART1_CTS_b
☑ 13	ADCB_CH1/PTE…	PTE19		ADCB_CH1		CMP3_OUT	UART1_RTS_b
☑ 14	ADCA_CH6a			ADCA_CH6a			
☑ 15	ADCA_CH7a			ADCA_CH7a			
☑ 16	ADCA_CH6b/PT…	PTE20	FTM1_CH0	ADCA_CH6b	FTM1_CH0[…]		UART0_TX
☑ 17	ADCA_CH7b/PT…	PTE21	FTM1_CH1	ADCA_CH7b	FTM1_CH1		UART0_RX
☐ 18	ADCA_CH2			ADCA_CH2			
☐ 19	ADCA_CH3			ADCA_CH3			
☐ 20	ADCA_CH6c			ADCA_CH6c			
☐ 21	ADCA_CH7c			ADCA_CH7c			

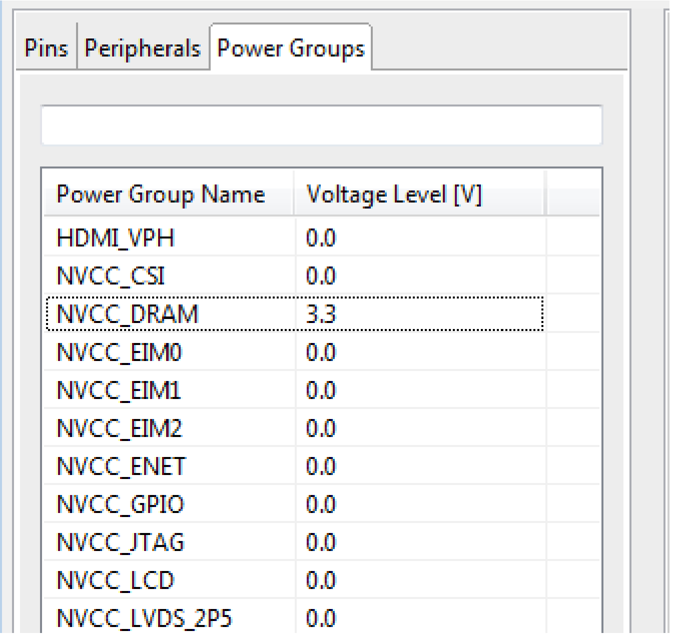
Figure 4-21. Example of routing mutiple functions

4.3.10 Power groups

If processor supports power groups, an additional tab will appear next to Pins and Peripherals allowing configuration of it.

NOTE

This feature is not supported for all the devices.

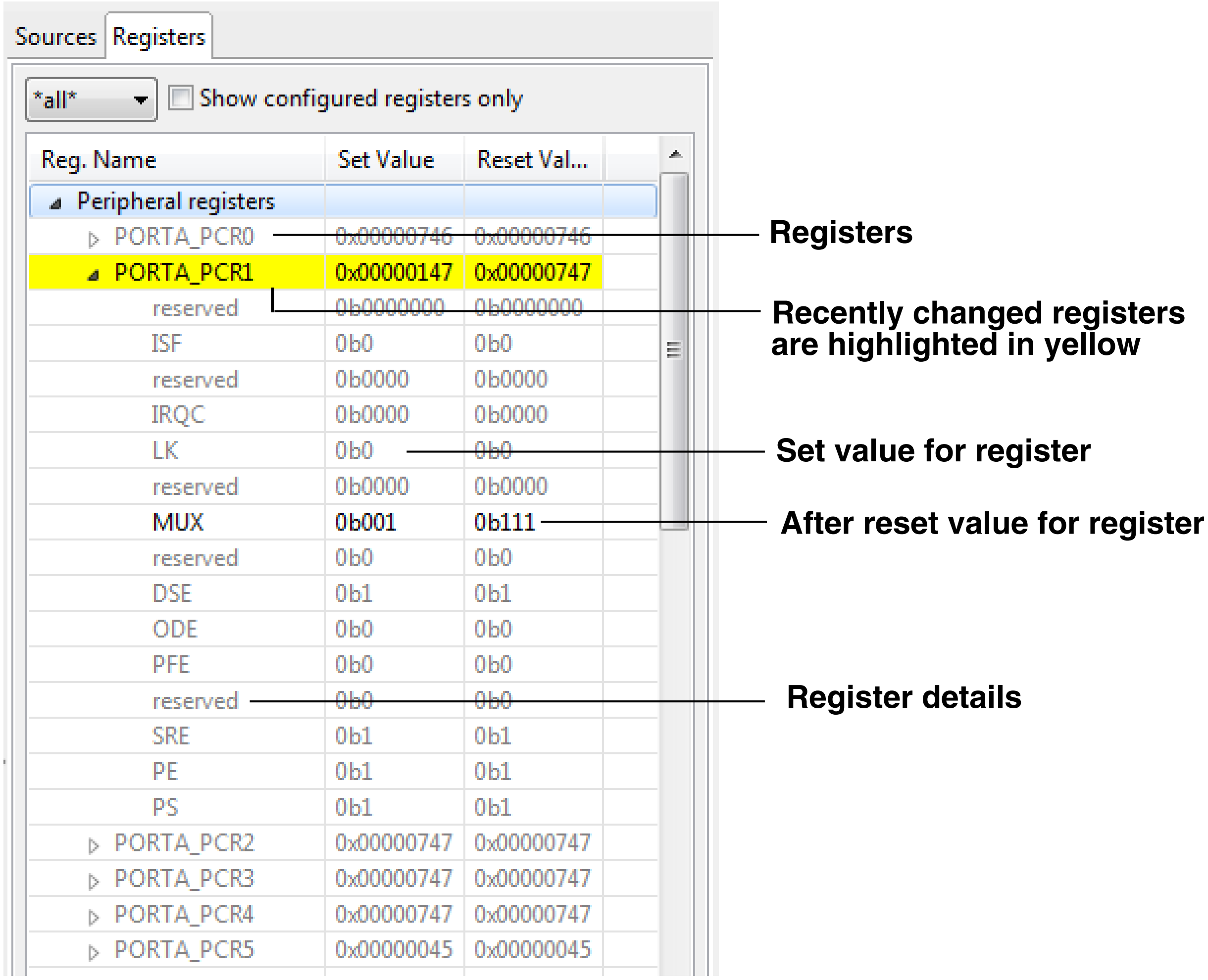


Power Group Name	Voltage Level [V]
HDMI_VPH	0.0
NVCC_CSI	0.0
NVCC_DRAM	3.3
NVCC_EIM0	0.0
NVCC_EIM1	0.0
NVCC_EIM2	0.0
NVCC_ENET	0.0
NVCC_GPIO	0.0
NVCC_JTAG	0.0
NVCC_LCD	0.0
NVCC_LVDS_2P5	0.0

Figure 4-22. Selecting power group

4.3.11 Registers view

The **Registers** view shows the list of registers of a given peripheral. The view shows the register name, the value used for routing configuration, and the after-reset values. This value is written into the register or bit by the generated code during the initialization process of the application. It is the last value that is written by the routing function to the register. The reset column contains the value that is in the register by default after the reset. The values of the registers are displayed in the hexadecimal and binary form. If the value of the register (or bit) is not defined, an interrogation mark "?" is displayed instead of the value.



all □ Show configured registers only

Reg. Name	Set Value	Reset Val...
Peripheral registers		
PORTA_PCR0	0x00000746	0x00000746
PORTA_PCR1	0x00000147	0x00000747
reserved	0b0000000	0b0000000
ISF	0b0	0b0
reserved	0b0000	0b0000
IRQC	0b0000	0b0000
LK	0b0	0b0
reserved	0b0000	0b0000
MUX	0b001	0b111
reserved	0b0	0b0
DSE	0b1	0b1
ODE	0b0	0b0
PFE	0b0	0b0
reserved	0b0	0b0
SRE	0b1	0b1
PE	0b1	0b1
PS	0b1	0b1
PORTA_PCR2	0x00000747	0x00000747
PORTA_PCR3	0x00000747	0x00000747
PORTA_PCR4	0x00000747	0x00000747
PORTA_PCR5	0x00000045	0x00000045

Registers

Recently changed registers are highlighted in yellow

Set value for register

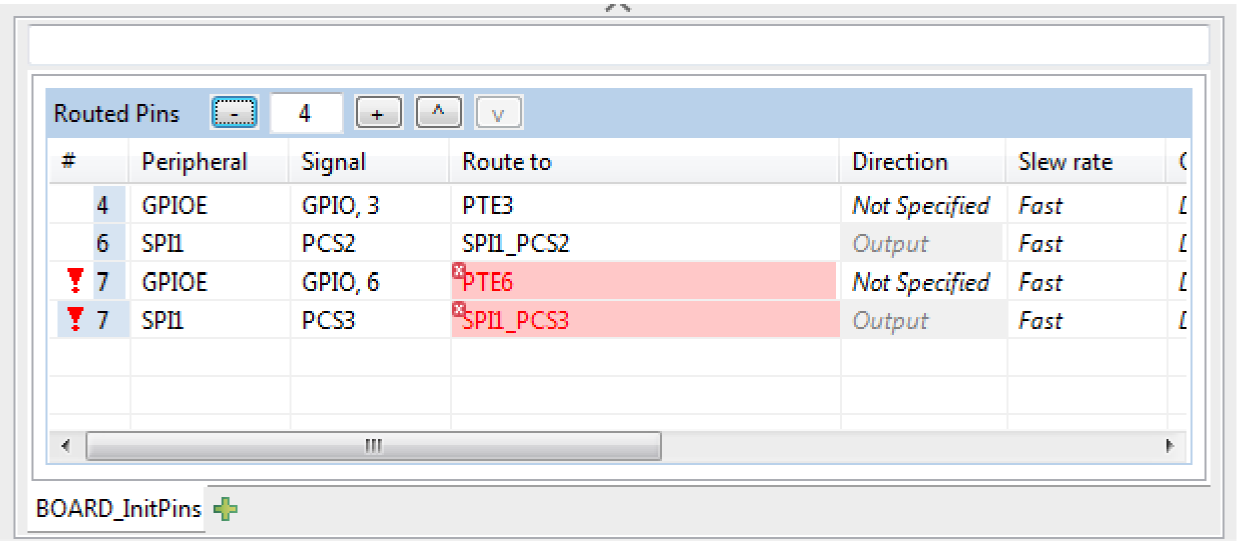
After reset value for register

Register details

Figure 4-23. Registers view

4.4 Errors and warnings

The pins tool checks for any conflict in the routing and also for errors in the configuration. Routing conflicts are checked only for the selected function. It is possible to configure different routing of one pin in different functions to allow dynamic pins routing re-configuration.



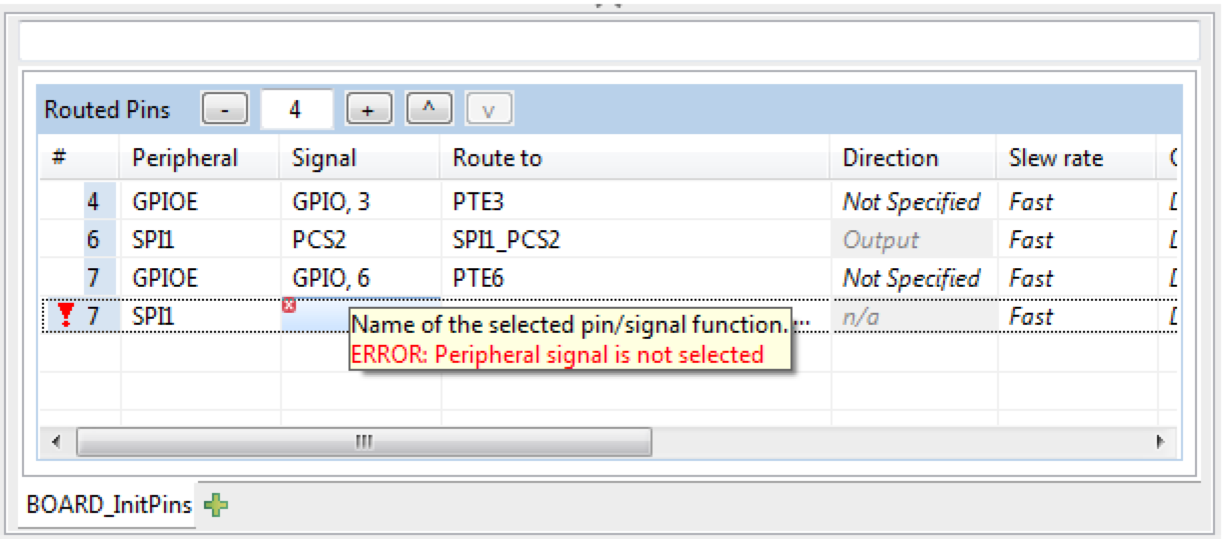
#	Peripheral	Signal	Route to	Direction	Slew rate
4	GPIOE	GPIO, 3	PTE3	*Not Specified*	*Fast*
6	SPI1	PCS2	SPI1_PCS2	*Output*	*Fast*
! 7	GPIOE	GPIO, 6	PTE6	*Not Specified*	*Fast*
! 7	SPI1	PCS3	SPI1_PCS3	*Output*	*Fast*

Figure 4-24. Error and warnings

If an error is encountered, the conflict is represented in the first column of the row and the error is indicated in the cell, where the conflict was created. The figure above shows the peripheral/ signal where the erroneous configuration occurs. The detailed error message appears as a tooltip.

4.4.1 Incomplete routing

Cell with incomplete routing is indicated by a red background. To generate proper pin routing, click on the drop down arrow and select the suitable value. Red decorator on a cell indicates an error condition.



#	Peripheral	Signal	Route to	Direction	Slew rate
4	GPIOE	GPIO, 3	PTE3	*Not Specified*	*Fast*
6	SPI1	PCS2	SPI1_PCS2	*Output*	*Fast*
7	GPIOE	GPIO, 6	PTE6	*Not Specified*	*Fast*
! 7	SPI1			*n/a*	*Fast*

Name of the selected pin/signal function.
ERROR: Peripheral signal is not selected

Figure 4-25. Incomplete routing

The tooltip of the cell shows more details about the conflict or the error, typically it lists the lines where conflict occurs.

4.5 Code generation

The tool generates source code that can be incorporated into an application to initialize pins routing. The source code is generated automatically on change or can be invoked explicitly by selecting the main menu **Pins > Generate Now**.

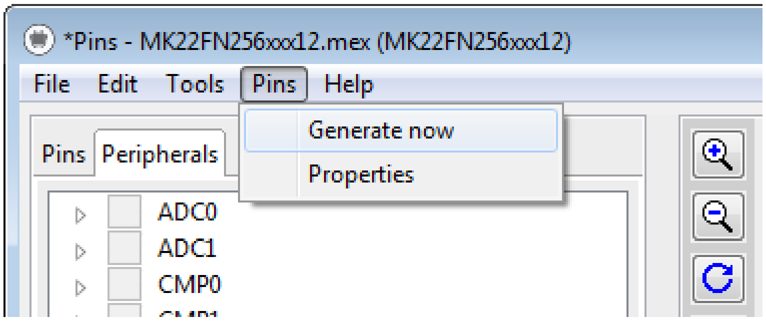
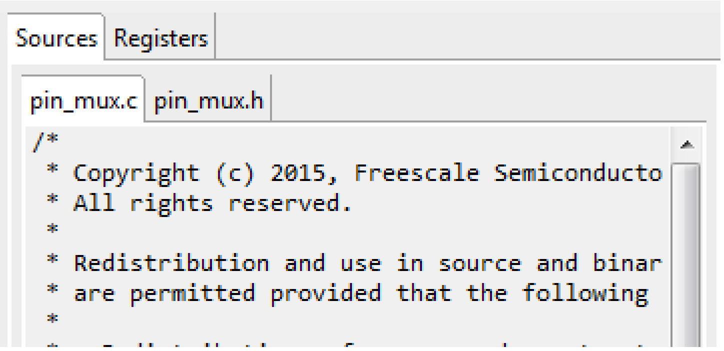


Figure 4-26. Generate code

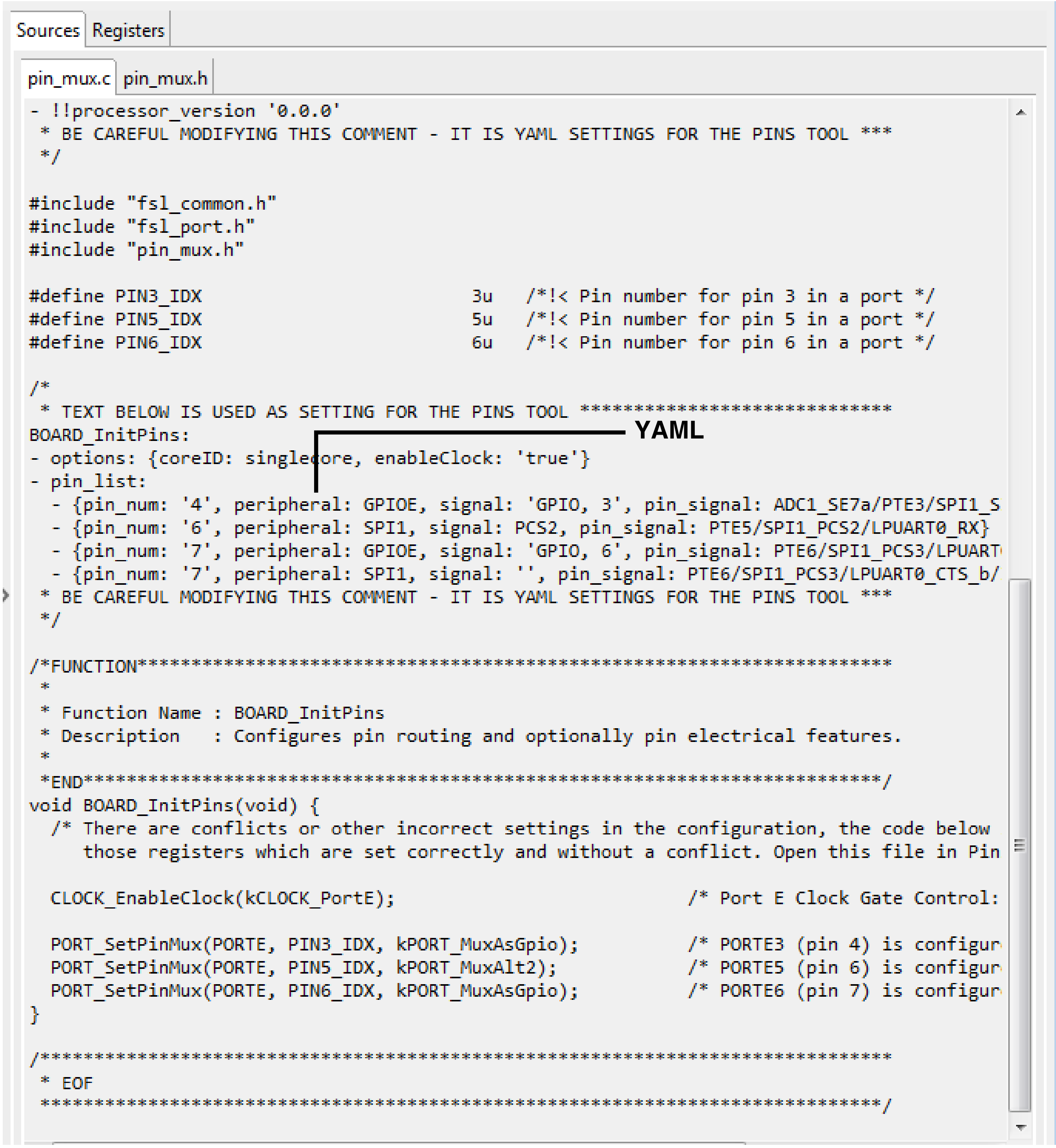
The generated code is shown in the **Sources** tab on the right window. It shows all generated files and each file has its own tab.



```
/*
 * Copyright (c) 2015, Freescale Semiconducto
 * All rights reserved.
 *
 * Redistribution and use in source and binar
 * are permitted provided that the following
 *
```

Figure 4-27. Sources view

It is also possible to copy and paste the generated code into the source files. The view generates code for each function. In addition to the function comments, the tool configuration is stored in YAML format. This comment is not intended for direct editing and can be used later to re-store the pins configuration.



```
- !!processor_version '0.0.0'
 * BE CAREFUL MODIFYING THIS COMMENT - IT IS YAML SETTINGS FOR THE PINS TOOL ***
 */

#include "fsl_common.h"
#include "fsl_port.h"
#include "pin_mux.h"

#define PIN3_IDX                         3u   /*!< Pin number for pin 3 in a port */
#define PIN5_IDX                         5u   /*!< Pin number for pin 5 in a port */
#define PIN6_IDX                         6u   /*!< Pin number for pin 6 in a port */

/*
 * TEXT BELOW IS USED AS SETTING FOR THE PINS TOOL *****************************
BOARD_InitPins:
- options: {coreID: singlecore, enableClock: 'true'}
- pin_list:
  - {pin_num: '4', peripheral: GPIOE, signal: 'GPIO, 3', pin_signal: ADC1_SE7a/PTE3/SPI1_S
  - {pin_num: '6', peripheral: SPI1, signal: PCS2, pin_signal: PTE5/SPI1_PCS2/LPUART0_RX}
  - {pin_num: '7', peripheral: GPIOE, signal: 'GPIO, 6', pin_signal: PTE6/SPI1_PCS3/LPUART
  - {pin_num: '7', peripheral: SPI1, signal: '', pin_signal: PTE6/SPI1_PCS3/LPUART0_CTS_b/
 * BE CAREFUL MODIFYING THIS COMMENT - IT IS YAML SETTINGS FOR THE PINS TOOL ***
 */

/*FUNCTION**********************************************************************
 *
 * Function Name : BOARD_InitPins
 * Description   : Configures pin routing and optionally pin electrical features.
 *
 *END**************************************************************************/
void BOARD_InitPins(void) {
  /* There are conflicts or other incorrect settings in the configuration, the code below
     those registers which are set correctly and without a conflict. Open this file in Pin

  CLOCK_EnableClock(kCLOCK_PortE);                          /* Port E Clock Gate Control:

  PORT_SetPinMux(PORTE, PIN3_IDX, kPORT_MuxAsGpio);         /* PORTE3 (pin 4) is configur
  PORT_SetPinMux(PORTE, PIN5_IDX, kPORT_MuxAlt2);           /* PORTE5 (pin 6) is configur
  PORT_SetPinMux(PORTE, PIN6_IDX, kPORT_MuxAsGpio);         /* PORTE6 (pin 7) is configur
}

/*******************************************************************************
 * EOF
 ******************************************************************************/
```

Figure 4-28. Generated code

YAML configuration contains configuration of each pin. It stores only non-default values.

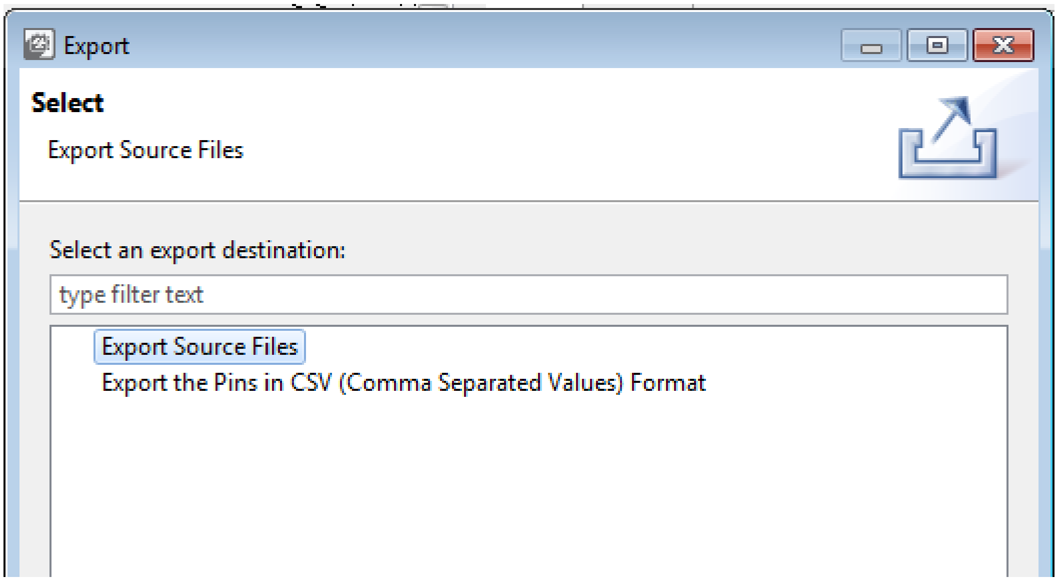
💬	For multicore processors there is source file per each core generated.

4.5.1 Exporting source code

It is possible to export generate source using the Export wizard.

To launch the Export wizard:

1. Select **File > Export** from the main menu.
2. Select the **Export Source Files** option.



Export

Select

Export Source Files

Select an export destination:

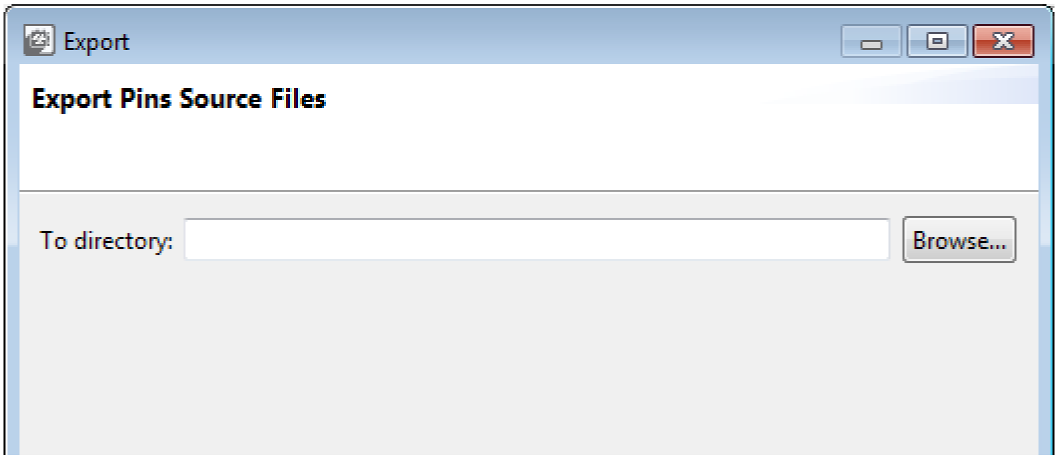
type filter text

Export Source Files

Export the Pins in CSV (Comma Separated Values) Format

Figure 4-29. Export wizard

3. Click **Next**.
4. Select the target folder where you want to store the generated files.



Export

Export Pins Source Files

To directory:

Figure 4-30. Select target folder

5. Click **Finish**.

-	Web version offers download zip file containing all generated files.

4.5.2 Importing source code

To import source code files:

1. Select **File > Import** from the main menu.

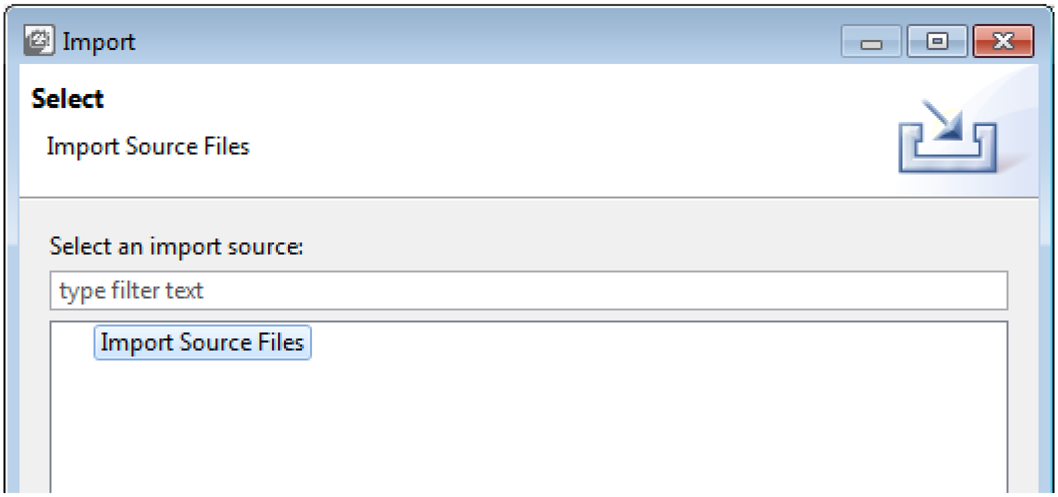
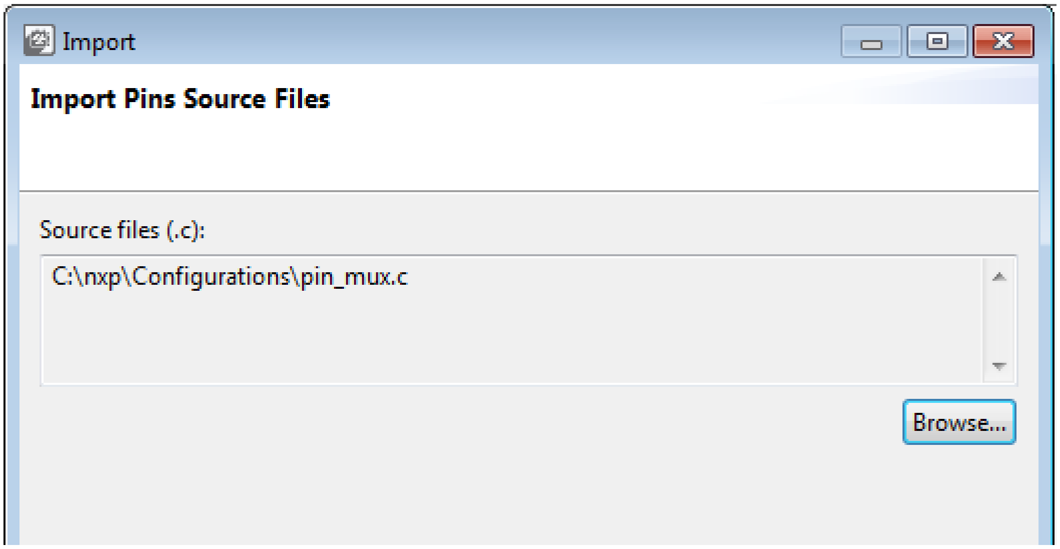


Figure 4-31. Import wizard

2. Select the **Import Source Files** option.
3. Click **Next**.
4. It is possible to select one or more C files to import using the **Browse** button in the **Import Pins Source Files** dialog box.



C:\nxp\Configurations\pin_mux.c

Figure 4-32. Import Pins Source Files

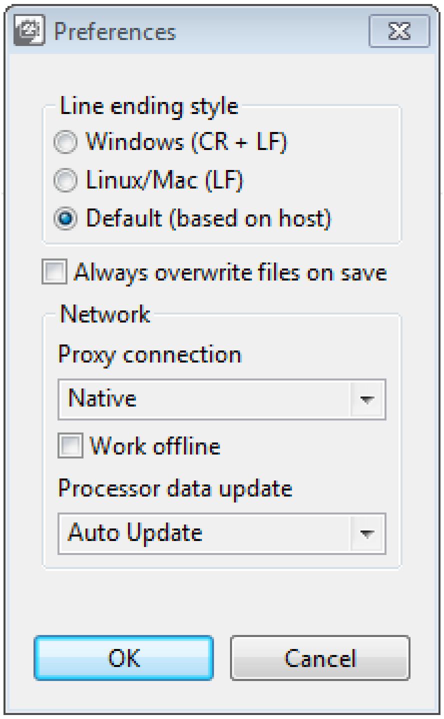
5. Click **Finish**.
   All files are merged into current configuration. It imports all the functions only. If imported function has the same name as in the existing configuration, it is automatically renamed to the indexed one. For example, if BOARD_InitPins already exists in the configuration then the imported function is renamed to BOARD_InitPins1.

	Only C files with valid Yaml configuration can be imported. It imports the configuration only, then the whole C file is re-created based on this setting (the rest of the C file is ignored).

4.6 Options

4.6.1 Configuration preferences

To configure preferences, select **Edit > Preferences** from the main menu. The configuration Preferences dialog box appears.



Preferences

Line ending style
○ Windows (CR + LF)
○ Linux/Mac (LF)
● Default (based on host)

□ Always overwrite files on save

Network
Proxy connection: Native
□ Work offline
Processor data update: Auto Update

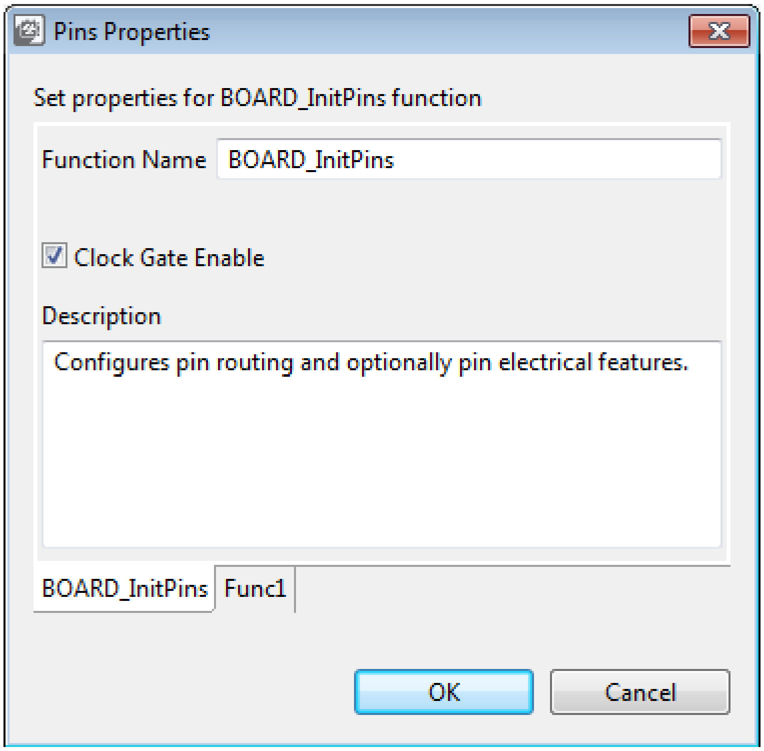
Figure 4-33. Preferences dialog box

In this dialog it is possible to set:

- Line ending style (Windows, Linux or default based on host)
- Auto overwrite files on save behavior
- Proxy connection
  - Direct – direct network connection without any proxy.
  - Native – uses system proxy configuration for network connection.
- Work offline to enable this mode
  - It will not download/update new data from NXP cloud, at it will not show all possible processors available for download if this feature is enabled.
- Processor data update options
  - Update will be proceeded either automatically or manually (user has to confirm it when requested) or disabled at all.

4.6.2 Pins properties

To set pins properties, select **Pins > Properties** from the main menu. The **Pins Properties** dialog box appears.


Pins Properties

Set properties for BOARD_InitPins function

Function Name: BOARD_InitPins

☑ Clock Gate Enable

Description

Configures pin routing and optionally pin electrical features.

Figure 4-34. Pins Properties

In this option it is possible to configure several options for functions and code generation. Each settings is applicable for selected function, which can be specified by selecting appropriate tab. It is possible to specify generated function name, selected core*, option to enable clock gate* in source code, or write function description (this description will be generated in the C file). [1]

4.6.3 Updates

To perform a check for updates select **Help > Check** for the updates menu. It contacts the server and checks whether there is a new version available.

NOTE

To check updates, internet connection is required.

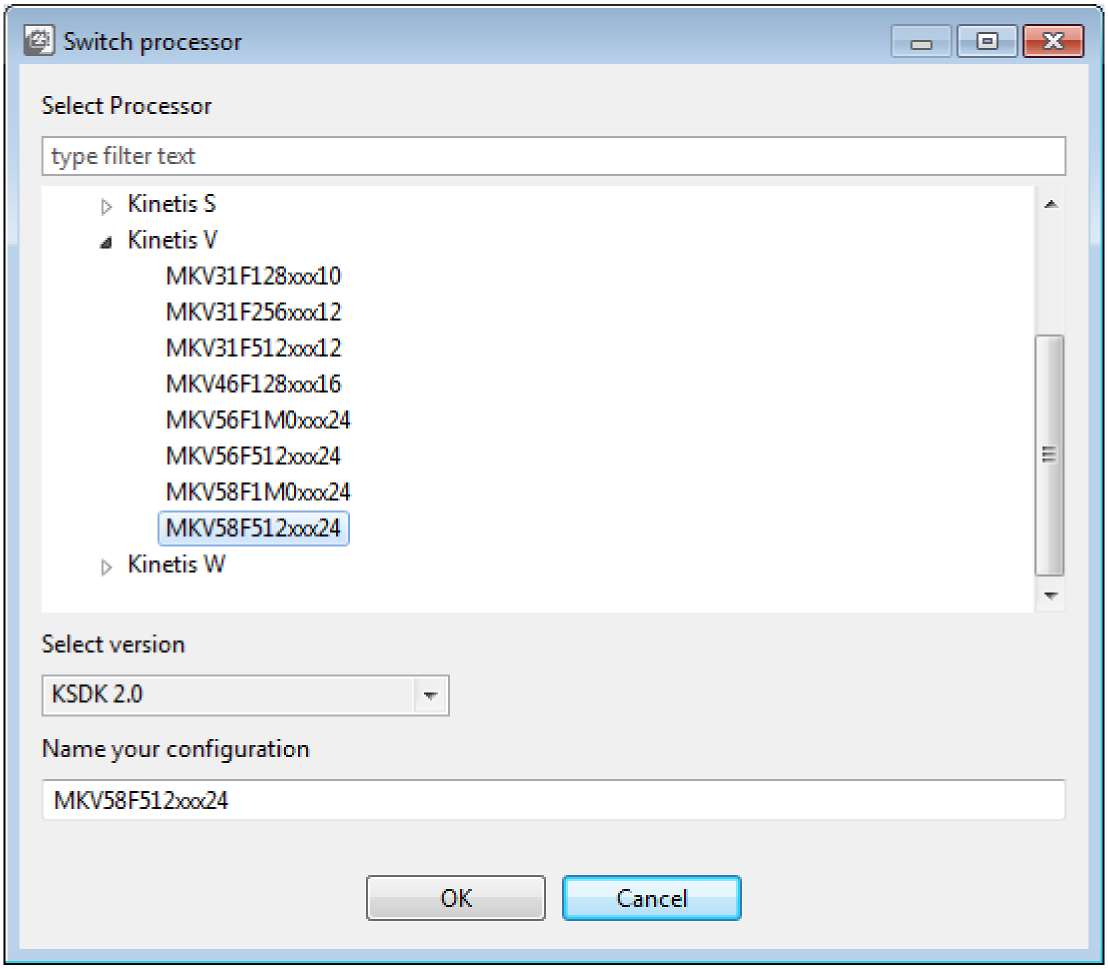
[1] *if supported by processor

Chapter 5
Advanced Features

5.1 Switching processor

It is possible to switch processor or package of the current configuration to different one. If the processor or package is switched, all functions and configured routing of pins remains same, only applied on different processor. This is typically useful to change to similar packages. If switched to completely different processor, it may lead in many conflict or inaccessible pin routing. In this case, it is necessary go to Pins Routing table and re-configure all pins, which reports an error or conflicts.

Select **File > Switch processor** menu to change the processor in the selected configuration.

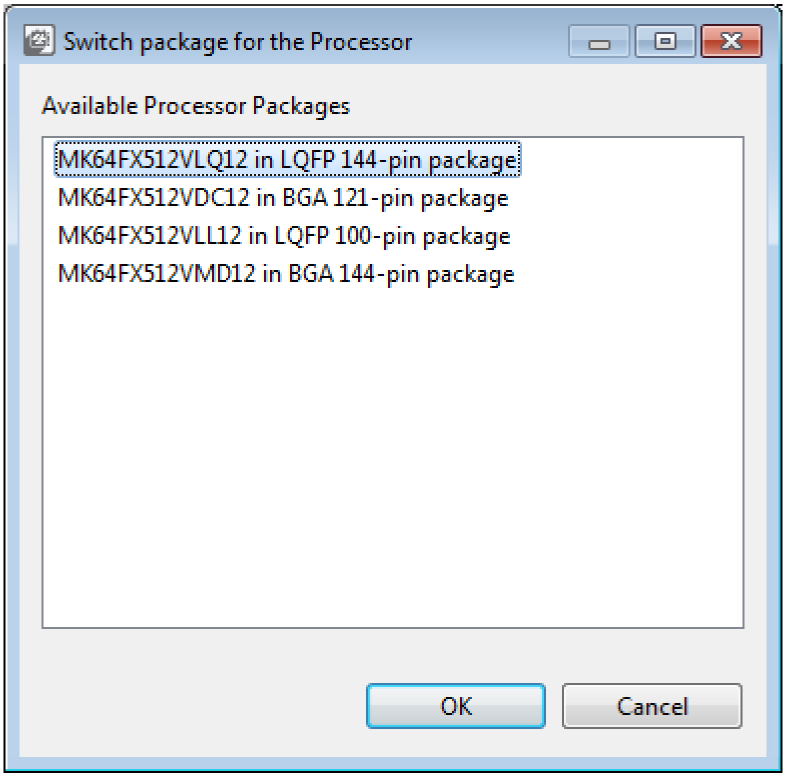


Select version: KSDK 2.0

Name your configuration: MKV58F512xxx24

Figure 5-1. Switch configuration

Select **File > Switch package** menu to change package of current processor.


Switch package for the Processor
Available Processor Packages
OK
Cancel

MK64FX512VLQ12 in LQFP 144-pin package
MK64FX512VDC12 in BGA 121-pin package
MK64FX512VLL12 in LQFP 100-pin package
MK64FX512VMD12 in BGA 144-pin package

Figure 5-2. Switch package

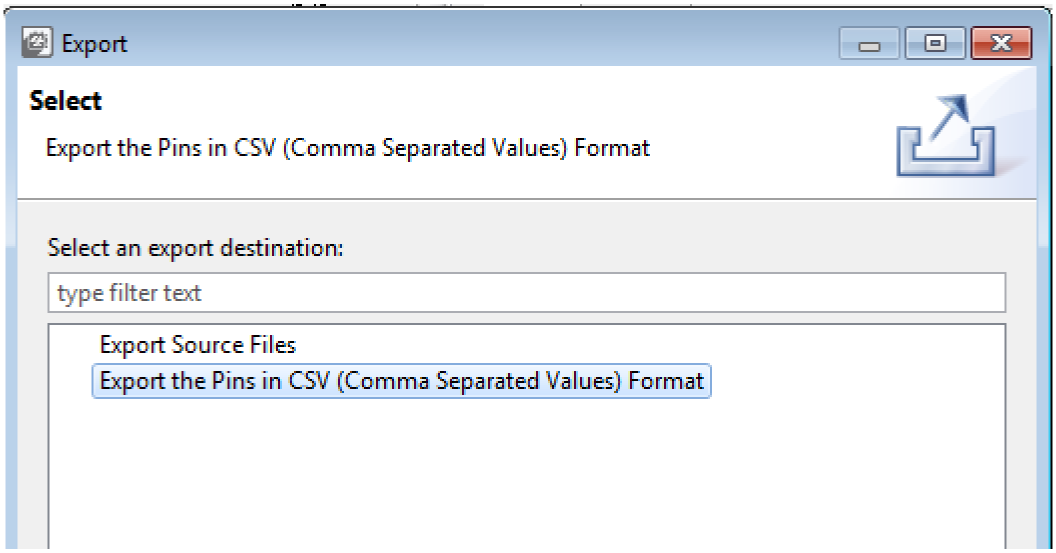
NOTE

In order to switch processor in Web version, it is required to select top configuration menu and then change it.

5.2 Exporting pins table

To export Pins table:

1. Select **File > Export** from the main menu.
2. In the **Export** dialog box, select the **Export the Pins in CSV (Comma Separated Values) Format** option.



Export

Select

Export the Pins in CSV (Comma Separated Values) Format

Select an export destination:

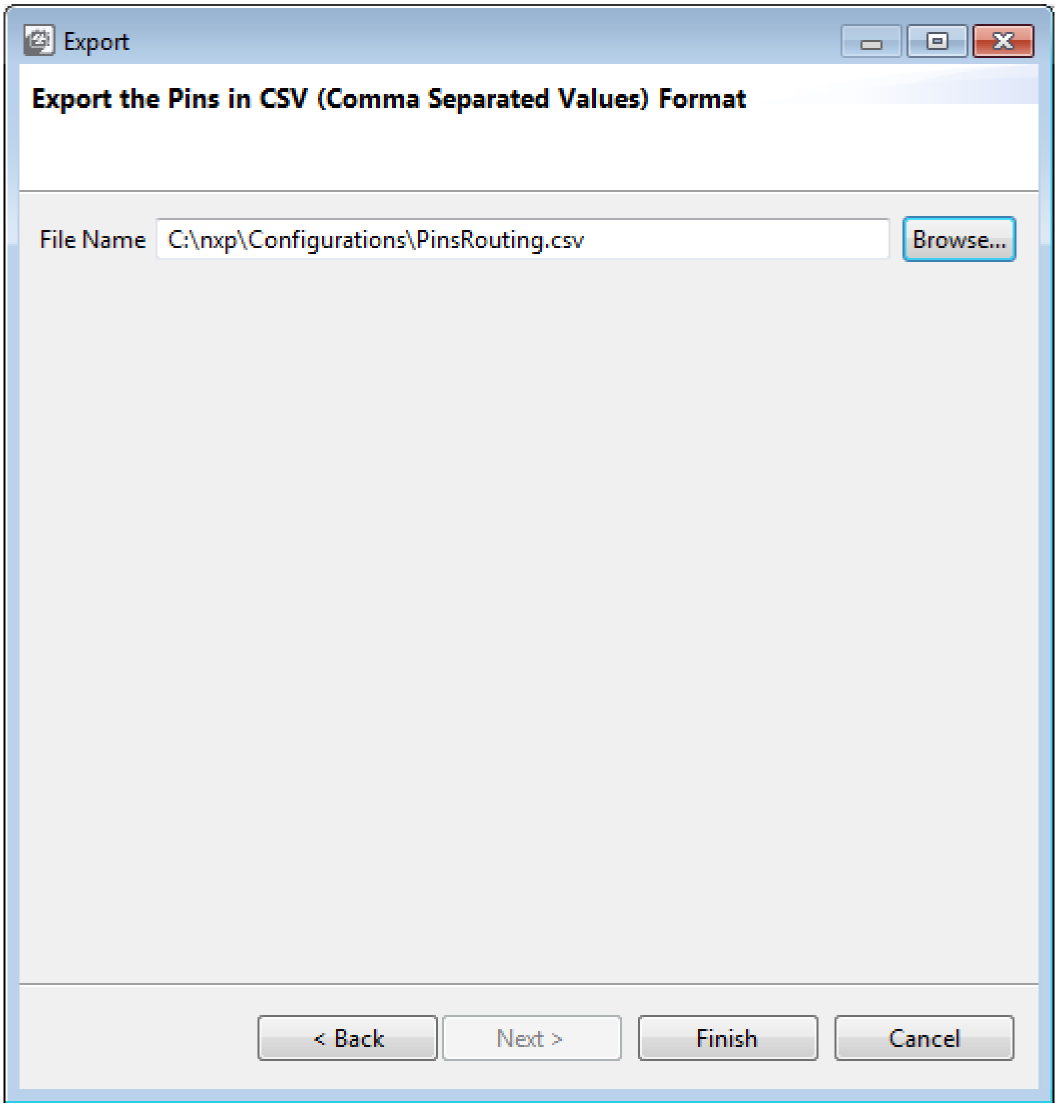
type filter text

Export Source Files

Export the Pins in CSV (Comma Separated Values) Format

Figure 5-3. Export dialog

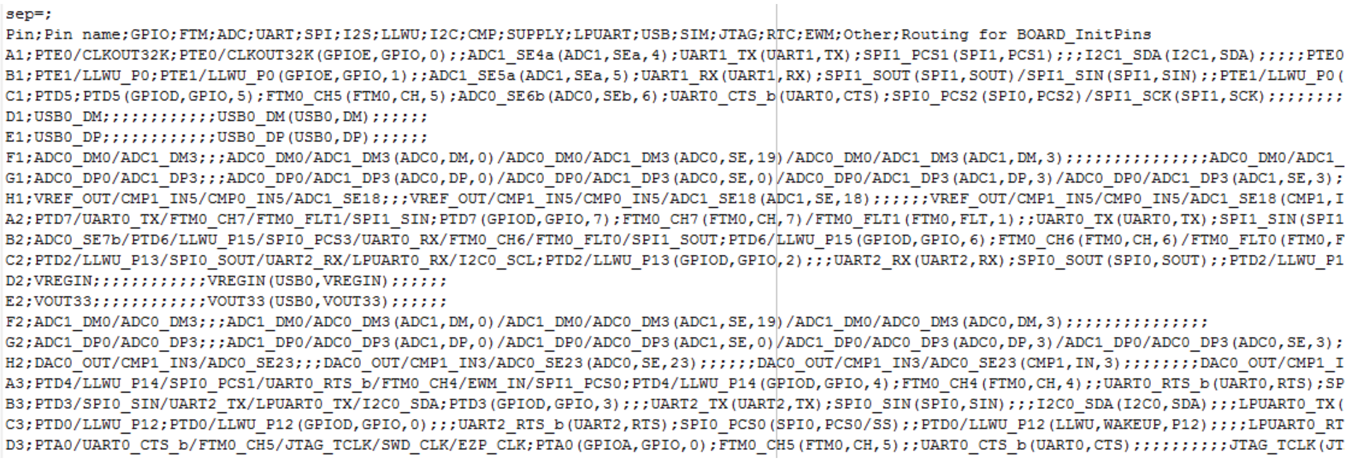
3. Click **Next**.
4. Select the folder and specify the file name to which you want to export.



File Name C:\nxp\Configurations\PinsRouting.csv

Figure 5-4. Export the Pins in CVS

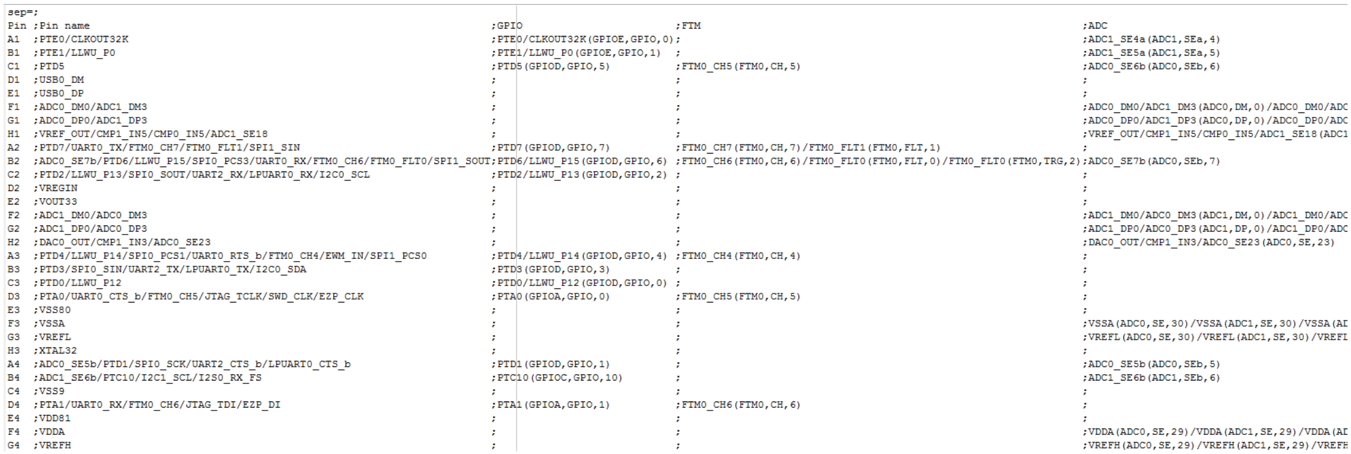
5. The exported file contains content of the current Pins view table, plus list of functions and selected routed pins.



```
sep=;
Pin;Pin name;GPIO;FTM;ADC;UART;SPI;I2S;LLWU;I2C;CMP;SUPPLY;LPUART;USB;SIM;JTAG;RTC;EWM;Other;Routing for BOARD_InitPins
A1;PTE0/CLKOUT32K;PTE0/CLKOUT32K(GPIOE,GPIO,0);;ADC1_SE4a(ADC1,SEa,4);UART1_TX(UART1,TX);SPI1_PCS1(SPI1,PCS1);;;I2C1_SDA(I2C1,SDA);;;;;PTE0
B1;PTE1/LLWU_P0;PTE1/LLWU_P0(GPIOE,GPIO,1);;ADC1_SE5a(ADC1,SEa,5);UART1_RX(UART1,RX);SPI1_SOUT(SPI1,SOUT)/SPI1_SIN(SPI1,SIN);;PTE1/LLWU_P0(
C1;PTD5;PTD5(GPIOD,GPIO,5);FTM0_CH5(FTM0,CH,5);ADC0_SE6b(ADC0,SEb,6);UART0_CTS_b(UART0,CTS);SPI0_PCS2(SPI0,PCS2)/SPI1_SCK(SPI1,SCK);;;;;;;
D1;USB0_DM;;;;;;;;;;;;USB0_DM(USB0,DM);;;;;;
E1;USB0_DP;;;;;;;;;;;;USB0_DP(USB0,DP);;;;;;
F1;ADC0_DM0/ADC1_DM3;;;ADC0_DM0/ADC1_DM3(ADC0,DM,0)/ADC0_DM0/ADC1_DM3(ADC0,SE,19)/ADC0_DM0/ADC1_DM3(ADC1,DM,3);;;;;;;;;;;;;;;ADC0_DM0/ADC1_
G1;ADC0_DP0/ADC1_DP3;;;ADC0_DP0/ADC1_DP3(ADC0,DP,0)/ADC0_DP0/ADC1_DP3(ADC0,SE,0)/ADC0_DP0/ADC1_DP3(ADC1,DP,3)/ADC0_DP0/ADC1_DP3(ADC1,SE,3);
H1;VREF_OUT/CMP1_IN5/CMP0_IN5/ADC1_SE18;;;VREF_OUT/CMP1_IN5/CMP0_IN5/ADC1_SE18(ADC1,SE,18);;;;;;VREF_OUT/CMP1_IN5/CMP0_IN5/ADC1_SE18(CMP1,I
A2;PTD7/UART0_TX/FTM0_CH7/FTM0_FLT1/SPI1_SIN;PTD7(GPIOD,GPIO,7);FTM0_CH7(FTM0,CH,7)/FTM0_FLT1(FTM0,FLT,1);;UART0_TX(UART0,TX);SPI1_SIN(SPI1
B2;ADC0_SE7b/PTD6/LLWU_P15/SPI0_PCS3/UART0_RX/FTM0_CH6/FTM0_FLT0/SPI1_SOUT;PTD6/LLWU_P15(GPIOD,GPIO,6);FTM0_CH6(FTM0,CH,6)/FTM0_FLT0(FTM0,F
C2;PTD2/LLWU_P13/SPI0_SOUT/UART2_RX/LPUART0_RX/I2C0_SCL;PTD2/LLWU_P13(GPIOD,GPIO,2);;;UART2_RX(UART2,RX);SPI0_SOUT(SPI0,SOUT);;PTD2/LLWU_P1
D2;VREGIN;;;;;;;;;;;;VREGIN(USB0,VREGIN);;;;;;
E2;VOUT33;;;;;;;;;;;;VOUT33(USB0,VOUT33);;;;;;
F2;ADC1_DM0/ADC0_DM3;;;ADC1_DM0/ADC0_DM3(ADC1,DM,0)/ADC1_DM0/ADC0_DM3(ADC1,SE,19)/ADC1_DM0/ADC0_DM3(ADC0,DM,3);;;;;;;;;;;;;;;
G2;ADC1_DP0/ADC0_DP3;;;ADC1_DP0/ADC0_DP3(ADC1,DP,0)/ADC1_DP0/ADC0_DP3(ADC1,SE,0)/ADC1_DP0/ADC0_DP3(ADC0,DP,3)/ADC1_DP0/ADC0_DP3(ADC0,SE,3);
H2;DAC0_OUT/CMP1_IN3/ADC0_SE23;;;DAC0_OUT/CMP1_IN3/ADC0_SE23(ADC0,SE,23);;;;;;DAC0_OUT/CMP1_IN3/ADC0_SE23(CMP1,IN,3);;;;;;;;DAC0_OUT/CMP1_I
A3;PTD4/LLWU_P14/SPI0_PCS1/UART0_RTS_b/FTM0_CH4/EWM_IN/SPI1_PCS0;PTD4/LLWU_P14(GPIOD,GPIO,4);FTM0_CH4(FTM0,CH,4);;UART0_RTS_b(UART0,RTS);SP
B3;PTD3/SPI0_SIN/UART2_TX/LPUART0_TX/I2C0_SDA;PTD3(GPIOD,GPIO,3);;;UART2_TX(UART2,TX);SPI0_SIN(SPI0,SIN);;;I2C0_SDA(I2C0,SDA);;;LPUART0_TX(
C3;PTD0/LLWU_P12;PTD0/LLWU_P12(GPIOD,GPIO,0);;;UART2_RTS_b(UART2,RTS);SPI0_PCS0(SPI0,PCS0/SS);;PTD0/LLWU_P12(LLWU,WAKEUP,P12);;;;LPUART0_RT
D3;PTA0/UART0_CTS_b/FTM0_CH5/JTAG_TCLK/SWD_CLK/EZP_CLK;PTA0(GPIOA,GPIO,0);FTM0_CH5(FTM0,CH,5);;UART0_CTS_b(UART0,CTS);;;;;;;;;;JTAG_TCLK(JT
```

Figure 5-5. Exported file content

The exported content can be used in other tools for further processing. For example, see it after aligning to blocks in the image below.



```
sep=;
Pin ;Pin name                                                               ;GPIO                        ;FTM                                                            ;ADC
A1  ;PTE0/CLKOUT32K                                                         ;PTE0/CLKOUT32K(GPIOE,GPIO,0);                                                               ;ADC1_SE4a(ADC1,SEa,4)
B1  ;PTE1/LLWU_P0                                                           ;PTE1/LLWU_P0(GPIOE,GPIO,1)  ;                                                               ;ADC1_SE5a(ADC1,SEa,5)
C1  ;PTD5                                                                   ;PTD5(GPIOD,GPIO,5)          ;FTM0_CH5(FTM0,CH,5)                                            ;ADC0_SE6b(ADC0,SEb,6)
D1  ;USB0_DM                                                                ;                            ;                                                               ;
E1  ;USB0_DP                                                                ;                            ;                                                               ;
F1  ;ADC0_DM0/ADC1_DM3                                                      ;                            ;                                                               ;ADC0_DM0/ADC1_DM3(ADC0,DM,0)/ADC0_DM0/ADC
G1  ;ADC0_DP0/ADC1_DP3                                                      ;                            ;                                                               ;ADC0_DP0/ADC1_DP3(ADC0,DP,0)/ADC0_DP0/ADC
H1  ;VREF_OUT/CMP1_IN5/CMP0_IN5/ADC1_SE18                                   ;                            ;                                                               ;VREF_OUT/CMP1_IN5/CMP0_IN5/ADC1_SE18(ADC1
A2  ;PTD7/UART0_TX/FTM0_CH7/FTM0_FLT1/SPI1_SIN                              ;PTD7(GPIOD,GPIO,7)          ;FTM0_CH7(FTM0,CH,7)/FTM0_FLT1(FTM0,FLT,1)                      ;
B2  ;ADC0_SE7b/PTD6/LLWU_P15/SPI0_PCS3/UART0_RX/FTM0_CH6/FTM0_FLT0/SPI1_SOUT;PTD6/LLWU_P15(GPIOD,GPIO,6) ;FTM0_CH6(FTM0,CH,6)/FTM0_FLT0(FTM0,FLT,0)/FTM0_FLT0(FTM0,TRG,2);ADC0_SE7b(ADC0,SEb,7)
C2  ;PTD2/LLWU_P13/SPI0_SOUT/UART2_RX/LPUART0_RX/I2C0_SCL                   ;PTD2/LLWU_P13(GPIOD,GPIO,2) ;                                                               ;
D2  ;VREGIN                                                                 ;                            ;                                                               ;
E2  ;VOUT33                                                                 ;                            ;                                                               ;
F2  ;ADC1_DM0/ADC0_DM3                                                      ;                            ;                                                               ;ADC1_DM0/ADC0_DM3(ADC1,DM,0)/ADC1_DM0/ADC
G2  ;ADC1_DP0/ADC0_DP3                                                      ;                            ;                                                               ;ADC1_DP0/ADC0_DP3(ADC1,DP,0)/ADC1_DP0/ADC
H2  ;DAC0_OUT/CMP1_IN3/ADC0_SE23                                            ;                            ;                                                               ;DAC0_OUT/CMP1_IN3/ADC0_SE23(ADC0,SE,23)
A3  ;PTD4/LLWU_P14/SPI0_PCS1/UART0_RTS_b/FTM0_CH4/EWM_IN/SPI1_PCS0          ;PTD4/LLWU_P14(GPIOD,GPIO,4) ;FTM0_CH4(FTM0,CH,4)                                            ;
B3  ;PTD3/SPI0_SIN/UART2_TX/LPUART0_TX/I2C0_SDA                             ;PTD3(GPIOD,GPIO,3)          ;                                                               ;
C3  ;PTD0/LLWU_P12                                                          ;PTD0/LLWU_P12(GPIOD,GPIO,0) ;                                                               ;
D3  ;PTA0/UART0_CTS_b/FTM0_CH5/JTAG_TCLK/SWD_CLK/EZP_CLK                    ;PTA0(GPIOA,GPIO,0)          ;FTM0_CH5(FTM0,CH,5)                                            ;
E3  ;VSS80                                                                  ;                            ;                                                               ;
F3  ;VSSA                                                                   ;                            ;                                                               ;VSSA(ADC0,SE,30)/VSSA(ADC1,SE,30)/VSSA(AD
G3  ;VREFL                                                                  ;                            ;                                                               ;VREFL(ADC0,SE,30)/VREFL(ADC1,SE,30)/VREFL
H3  ;XTAL32                                                                 ;                            ;                                                               ;
A4  ;ADC0_SE5b/PTD1/SPI0_SCK/UART2_CTS_b/LPUART0_CTS_b                      ;PTD1(GPIOD,GPIO,1)          ;                                                               ;ADC0_SE5b(ADC0,SEb,5)
B4  ;ADC1_SE6b/PTC10/I2C1_SCL/I2S0_RX_FS                                    ;PTC10(GPIOC,GPIO,10)        ;                                                               ;ADC1_SE6b(ADC1,SEb,6)
C4  ;VSS9                                                                   ;                            ;                                                               ;
D4  ;PTA1/UART0_RX/FTM0_CH6/JTAG_TDI/EZP_DI                                 ;PTA1(GPIOA,GPIO,1)          ;FTM0_CH6(FTM0,CH,6)                                            ;
E4  ;VDD81                                                                  ;                            ;                                                               ;
F4  ;VDDA                                                                   ;                            ;                                                               ;VDDA(ADC0,SE,29)/VDDA(ADC1,SE,29)/VDDA(AD
G4  ;VREFH                                                                  ;                            ;                                                               ;VREFH(ADC0,SE,29)/VREFH(ADC1,SE,29)/VREFH
```

Figure 5-6. Aligning to block

Chapter 6
Support

If you have any questions or need additional help, perform a search on the Kinetis or i.MX community or post a new question. Visit https://community.freescale.com/community/kinetis or https://community.freescale.com/community/imx.

How to Reach Us:

Home Page:
nxp.com

Web Support:
nxp.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. Freescale reserves the right to make changes without further notice to any products herein.

Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals”, must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.