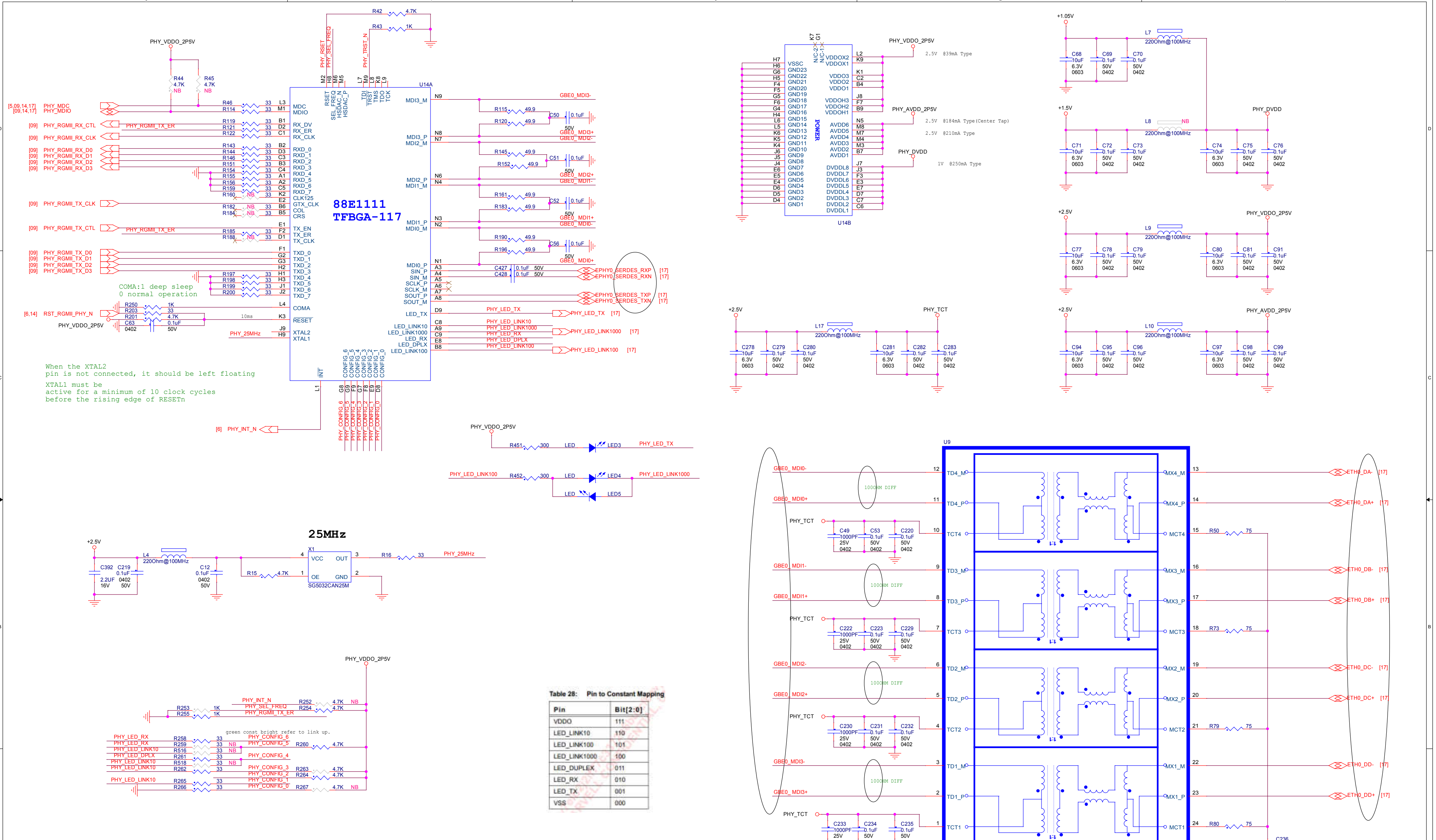


Table 28: Pin to Constant Mapping

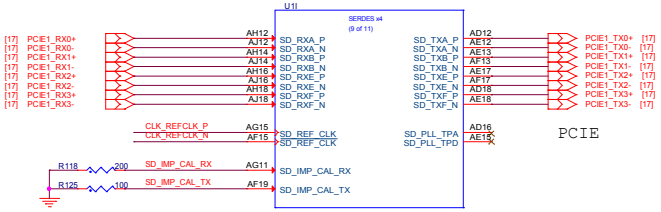
Pin	Bit[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

Table 30: 88E1111 Device Pin to Configuration Bit Mapping

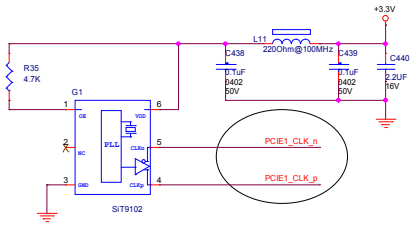
Pin	Bit[2]	Bit[1]	Bit[0]
CONFIG0	PHYADR[2][1]	PHYADR[1][1]	PHYADR[0][1]
CONFIG1	ENA_PAUSE	PHYADR[4][1]	PHYADR[3][1]
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG3	ANEG[0]	ENA_XC	DIS_125
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]
CONFIG6	SEL_TWSI	INT_POL	75/50 OHM

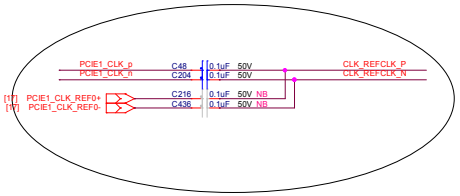
1. For the TWSI device address, the lower 5 bits (PHYADR[4:0]), are latched during hardware reset, and the device address bits ([6:5]) are fixed at '10'.

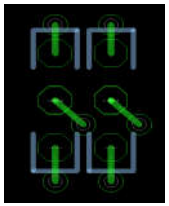
PIN	bit[2]	bit[1]	bit[0]	Copper	SGMII	Fiber	NOTE
config0	PHYADR[2]	PHYADR[1]	PHYADR[0]	000	000	000	MDIO ADDR is 1010000
config1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	110	110	110	Auto-geg, advetise all
config2	ANEG[3]	ANEG[2]	ANEG[1]	111	111	111	
config3	ANEG[0]	ENA_XC	DIS_125	110	110	110	capabilities,prefer slave enable crossover, DISABLE 125M clock
config4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]	011	110	011	RGMII to Copper/SGMII/Fiber
config5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]	111	110	110	
config6	SEL_TWSI	INT_POL	75/50 OHM	010	010	010	MDIO, INT LOW,50HM

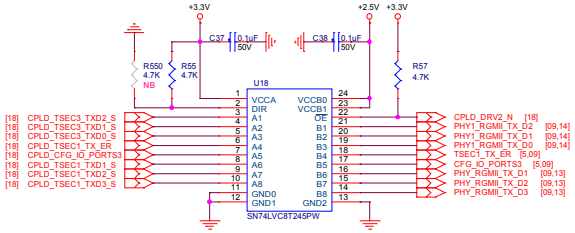


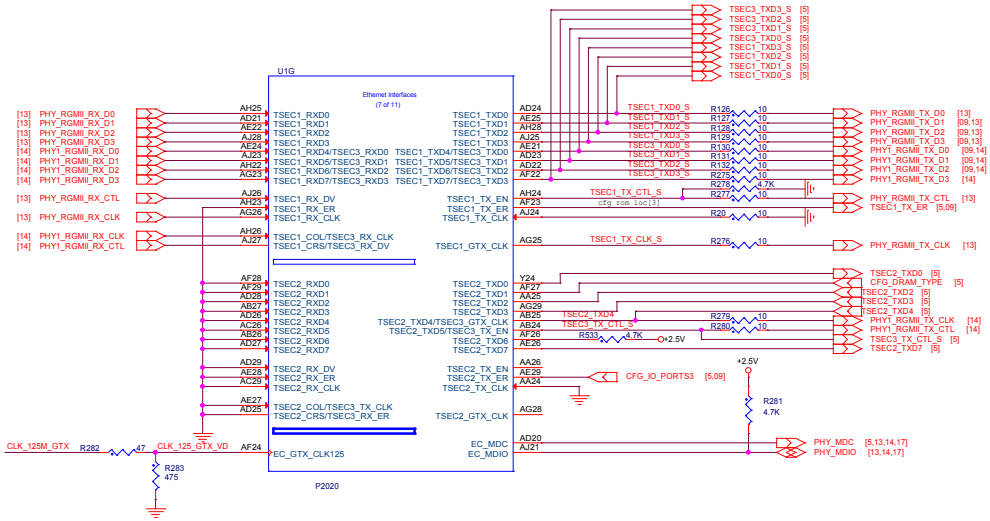
100MHz FOR PCIe



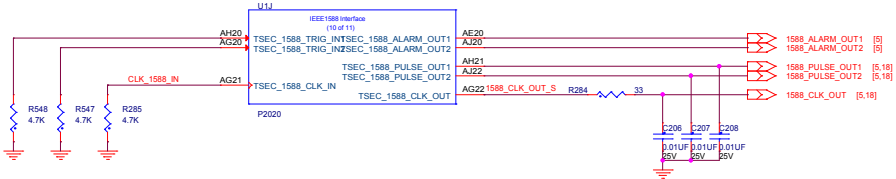


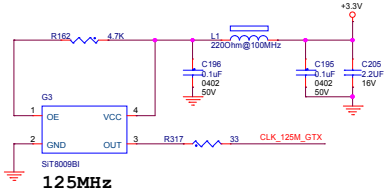


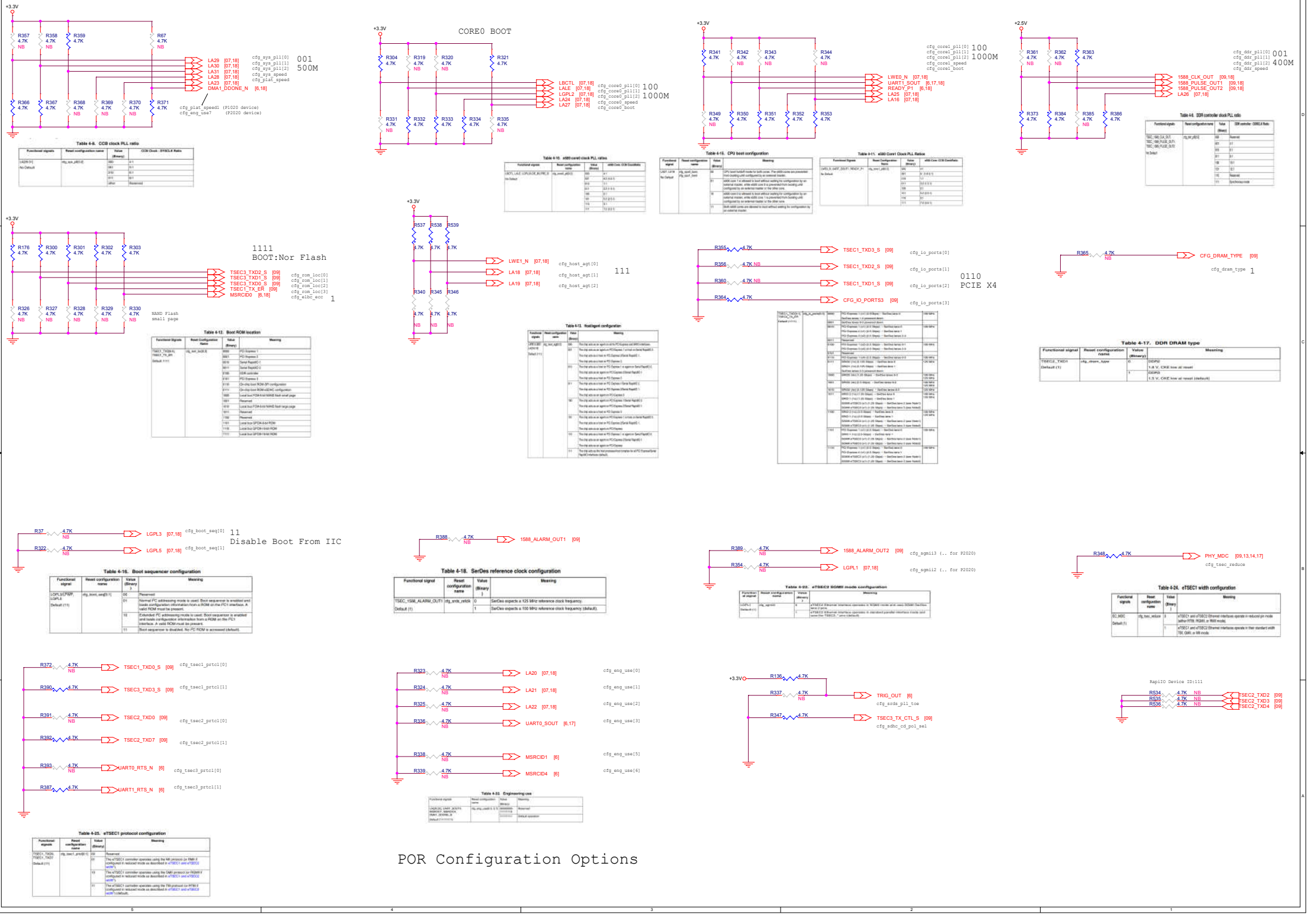




NOTE: 1588 Interface Powered off LVDD = 2.5V






+3.3V
R357 4.7K NB
R358 4.7K NB
R359 4.7K
R67 4.7K NB
R366 4.7K
R367 4.7K
R368 4.7K NB
R369 4.7K NB
R370 4.7K NB
R371 4.7K
LA29 [07,18]
LA30 [07,18]
LA31 [07,18]
LA28 [07,18]
LA23 [07,18]
DMA1_DDONE_N [6,18]
cfg_sys_pll1[0]
cfg_sys_pll1[1]
cfg_sys_pll1[2]
cfg_sys_speed
cfg_plat_speed
001
500M
cfg_plat_speed1 (P1020 device)
cfg_eng_use7 (P2020 device)
Table 4-8. CCB clock PLL ratio
CORE0 BOOT
+3.3V
R304 4.7K
R319 4.7K NB
R320 4.7K NB
R321 4.7K
R331 4.7K NB
R332 4.7K
R333 4.7K
R334 4.7K
R335 4.7K NB
LBCTL [07,18]
LALE [07,18]
LGPL2 [07,18]
LA24 [07,18]
LA27 [07,18]
cfg_core0_pll1[0]
cfg_core0_pll1[1]
cfg_core0_pll1[2]
cfg_core0_speed
cfg_core0_boot
100
1000M
Table 4-10. e500 core0 clock PLL ratios
Table 4-15. CPU boot configuration
Table 4-11. e500 Core1 Clock PLL Ratios
+3.3V
R341 4.7K
R342 4.7K NB
R343 4.7K NB
R344 4.7K NB
R349 4.7K NB
R350 4.7K
R351 4.7K
R352 4.7K
R353 4.7K
LWE0_N [07,18]
UART1_SOUT [6,17,18]
READY_P1 [6,18]
LA25 [07,18]
LA16 [07,18]
cfg_core1_pll1[0]
cfg_core1_pll1[1]
cfg_core1_pll1[2]
cfg_core1_speed
cfg_core1_boot
100
1000M
+2.5V
R361 4.7K NB
R362 4.7K NB
R363 4.7K
R373 4.7K
R384 4.7K
R385 4.7K NB
R386 4.7K
1588_CLK_OUT [09,18]
1588_PULSE_OUT1 [09,18]
1588_PULSE_OUT2 [09,18]
LA26 [07,18]
cfg_ddr_pll1[0]
cfg_ddr_pll1[1]
cfg_ddr_pll1[2]
cfg_ddr_speed
001
400M
Table 4-6. DDR controller clock PLL ratio
+3.3V
R176 4.7K
R300 4.7K
R301 4.7K
R302 4.7K
R303 4.7K
R326 4.7K NB
R327 4.7K NB
R328 4.7K NB
R329 4.7K NB
R330 4.7K NB
TSEC3_TXD2_S [09]
TSEC3_TXD1_S [09]
TSEC3_TXD0_S [09]
TSEC1_TX_ER [09]
MSRCID0 [6,18]
cfg_rom_loc[0]
cfg_rom_loc[1]
cfg_rom_loc[2]
cfg_rom_loc[3]
cfg_elbc_ecc
1111
BOOT:Nor Flash
1
NAND Flash small page
Table 4-12. Boot ROM location
+3.3V
R537 4.7K
R538 4.7K
R539 4.7K
R340 4.7K NB
R345 4.7K NB
R346 4.7K NB
LWE1_N [07,18]
LA18 [07,18]
LA19 [07,18]
cfg_host_agt[0]
cfg_host_agt[1]
cfg_host_agt[2]
111
Table 4-13. Host/agent configuration
R355 4.7K
R356 4.7K NB
R360 4.7K NB
R364 4.7K
TSEC1_TXD3_S [09]
TSEC1_TXD2_S [09]
TSEC1_TXD1_S [09]
CFG_IO_PORTS3 [09]
cfg_io_ports[0]
cfg_io_ports[1]
cfg_io_ports[2]
cfg_io_ports[3]
0110
PCIE X4
R365 4.7K NB
CFG_DRAM_TYPE [09]
cfg_dram_type
1
Table 4-17. DDR DRAM type
R37 4.7K NB
R322 4.7K NB
LGPL3 [07,18]
LGPL5 [07,18]
cfg_boot_seq[0]
cfg_boot_seq[1]
11
Disable Boot From IIC
Table 4-16. Boot sequencer configuration
R388 4.7K NB
1588_ALARM_OUT1 [09]
Table 4-18. SerDes reference clock configuration
R389 4.7K NB
R354 4.7K NB
1588_ALARM_OUT2 [09]
LGPL1 [07,18]
cfg_sgmii3 (.. for P2020)
cfg_sgmii2 (.. for P2020)
Table 4-22. eTSEC3 SGMII mode configuration
R348 4.7K
PHY_MDC [09,13,14,17]
cfg_tsec_reduce
Table 4-24. eTSEC1 width configuration
R372 4.7K NB
R390 4.7K NB
R391 4.7K NB
R392 4.7K NB
R393 4.7K NB
R387 4.7K NB
TSEC1_TXD0_S [09]
TSEC3_TXD3_S [09]
TSEC2_TXD0 [09]
TSEC2_TXD7 [09]
UART0_RTS_N [6]
UART1_RTS_N [6]
cfg_tsec1_prtcl[0]
cfg_tsec1_prtcl[1]
cfg_tsec2_prtcl[0]
cfg_tsec2_prtcl[1]
cfg_tsec3_prtcl[0]
cfg_tsec3_prtcl[1]
R323 4.7K NB
R324 4.7K NB
R325 4.7K NB
R336 4.7K NB
R338 4.7K NB
R339 4.7K NB
LA20 [07,18]
LA21 [07,18]
LA22 [07,18]
UART0_SOUT [6,17]
MSRCID1 [6]
MSRCID4 [6]
cfg_eng_use[0]
cfg_eng_use[1]
cfg_eng_use[2]
cfg_eng_use[3]
cfg_eng_use[5]
cfg_eng_use[6]
Table 4-33. Engineering use
+3.3V
R136 4.7K
R337 4.7K NB
R347 4.7K
TRIG_OUT [6]
TSEC3_TX_CTL_S [09]
cfg_srds_pll_toe
cfg_sdhc_cd_pol_sel
RapidIO Device ID:111
R534 4.7K NB
R535 4.7K NB
R536 4.7K NB
TSEC2_TXD2 [09]
TSEC2_TXD3 [09]
TSEC2_TXD4 [09]
Table 4-25. eTSEC1 protocol configuration
POR Configuration Options

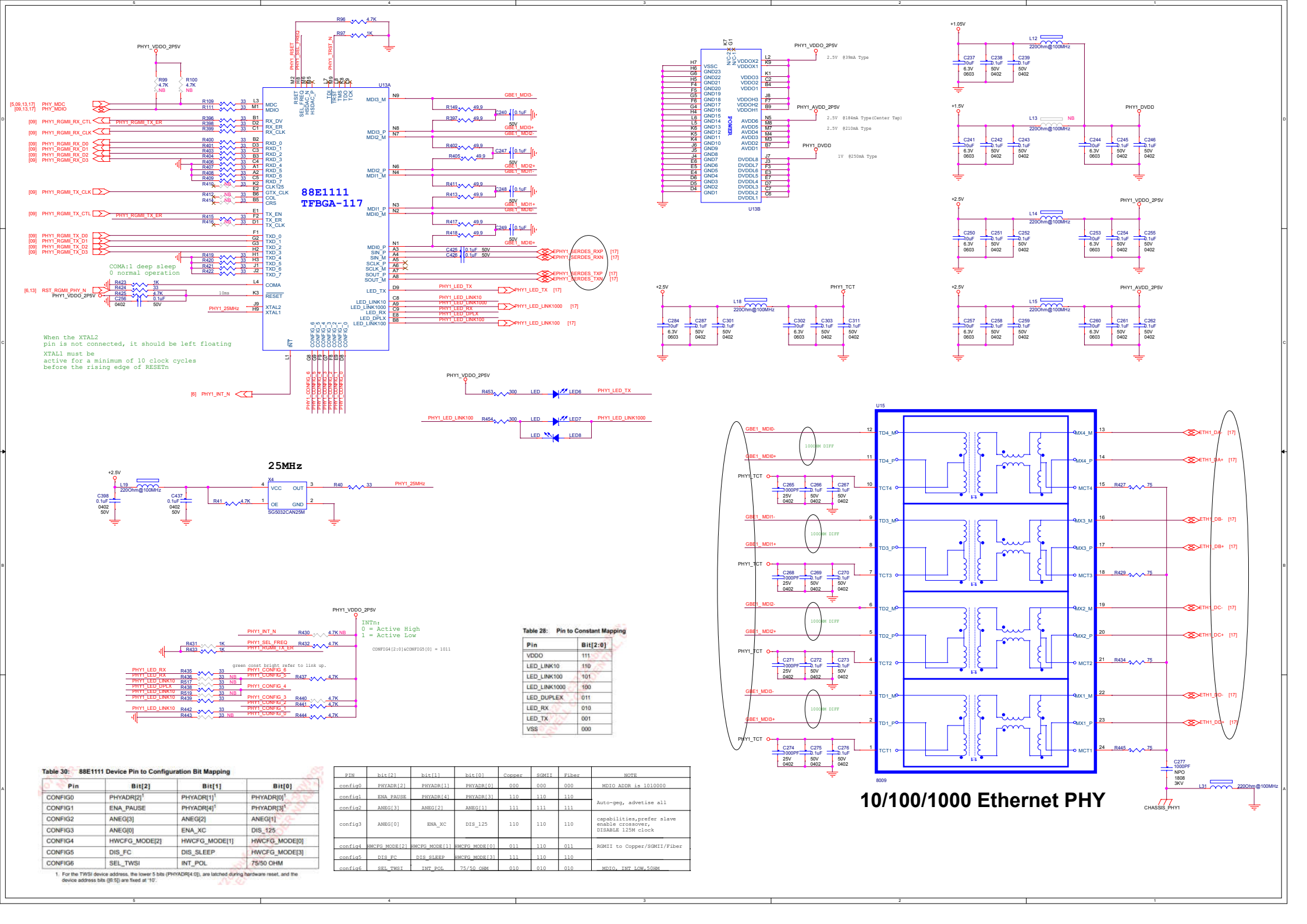


Table 28: Pin to Constant Mapping

Pin	Bit[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

Table 30: 88E1111 Device Pin to Configuration Bit Mapping

Pin	Bit[2]	Bit[1]	Bit[0]
CONFIG0	PHYADR[2][1]	PHYADR[1][1]	PHYADR[0][1]
CONFIG1	ENA_PAUSE	PHYADR[4][1]	PHYADR[3][1]
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG3	ANEG[0]	ENA_XC	DIS_125
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]
CONFIG6	SEL_TWSI	INT_POL	75/50 OHM

1. For the TWSI device address, the lower 5 bits (PHYADR[4:0]), are latched during hardware reset, and the device address bits ([6:5]) are fixed at '10'.

PIN	bit[2]	bit[1]	bit[0]	Copper	SGMII	Fiber	NOTE
config0	PHYADR[2]	PHYADR[1]	PHYADR[0]	000	000	000	MDIO ADDR is 1010000
config1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	110	110	110	Auto-geg, advetise all
config2	ANEG[3]	ANEG[2]	ANEG[1]	111	111	111	
config3	ANEG[0]	ENA_XC	DIS_125	110	110	110	capabilities,prefer slave enable crossover, DISABLE 125M clock
config4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]	011	110	011	RGMII to Copper/SGMII/Fiber
config5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]	111	110	110	
config6	SEL_TWSI	INT_POL	75/50 OHM	010	010	010	MDIO, INT LOW,50HM