NXP Semiconductors

Production Quality Information Package

Supplier : NXP Semiconductors Nijmegen, the Netherlands

Device : NVT4557HK

SEC Code : 1003-003240

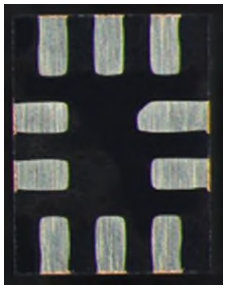
Function : SIM card interface level translator with EMI filter and ESD protection

Weight : 2.144000 mg

Remarks : Comply with 'Samsung electronics Standards for control of substances concerning product environment (0QA-2049)'

Top view

Bottom view



Process Site

Process / Site	Product flow
FAB	SSMC, Singapore
Assembly	NXP ATBK, Thailand
Final Test	NXP ATBK, Thailand

RoHS COMPLIANT

HALOGEN FREE

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• Approval Sheet Revision History

Revision	Date	Initiator	Description of Change
Issue 1.0	2021.08.23	Jack Lee	Initial release

Product Quality Information Package

NVT4557HK

Doc Rev 1.0 21 Apr 2021

Document information

Info	Content
Keywords	*NVT4557HK*, Product Quality Information Package
Abstract	This document describes the product quality information

Revision History

Revision	Date	Description
1.0	04082021	PQIP generated

Contents

1. Introduction

1.1 Device description

SIM card interface level translator with EMI filter and ESD protection

1.2 Product Information

Commercial type		NVT4557HK
Version		NVT4557A0
12 NC		9354 045 93115
Functional description		***SIM card interface level translator with EMI filter and ESD protection***
Product status maturity		Released
Operating Supply voltage	V_{CCA}	1.95V
Absolute maximum rating	V_{CCA}	2.2V
Maximum power dissipation		1000 mW
Operating temperature range		-40ºC to +85ºC

1.3 Data sheet

	NVT4557
Revision	Rev. 1.0 21 April 2021
For the latest version, please visit:	http://www.nxp.com

2. Manufacturing locations

Wafer-Fab	*SSMC, Singapore*
Assembly plant	*ATBK, Thailand*
Final test plant	*ATBK, Thailand*
Quality responsibility	NXP Semiconductors, Chandler, Arizona
Quality contact	Dennis Dill Andrea Bruton NXP Semiconductors. U.S.A. 1300 North Alma School Rd Chandler, AZ 85224 Email1: dennis.dill@nxp.com Email2: andrea.bruton@nxp.com

3. Product Data

3.1 Die for NVT4557

Process Technology	CMOS
Process	C14
Die thickness	75.0μm
Feature size	0.140μm
Wafer Size	200mm

3.2 Package for XQFN [Halogen-Free]

	NVT4557HK
Chemical content	Lead-free and Dark Green (Halogen and Antimony free)
Encapsulation	XQFN10: SOT1160-1
Mould material	EME-G700
Mould process	Transfer molding
Lead frame material	CuNi3
Lead frame plating	Rt-NiPdAu
Chip assembly process	Adhesive: ATB-F125
Wire bond process	Thermosonic ball bond
Wire material	Cu
Wire diameter	20µm
Moisture Sensitivity Level	1

3.3 Certifications

NXP Semiconductors quality and reliability

http://www.nxp.com/about/technology-leadership/quality/quality-certifications:QUALITY_CERT

4. Quality and Reliability

4.1 Electrical for NVT4557

Electrical Characterization		Min
Vesd	ESD- Electrical Discharge HBM – Human Body Model; Jedec: JS-001	*>2000V*
	ESD- Electrical Discharge CDM – Charged Device Model; Jedec JS-002	*>500V*
	Latch up; Jedec: JESD78	*Latch up testing is done to JEDEC standard JESD78 which meets* VddImax ± 100 mA

4.2 NVT4557 qualification results

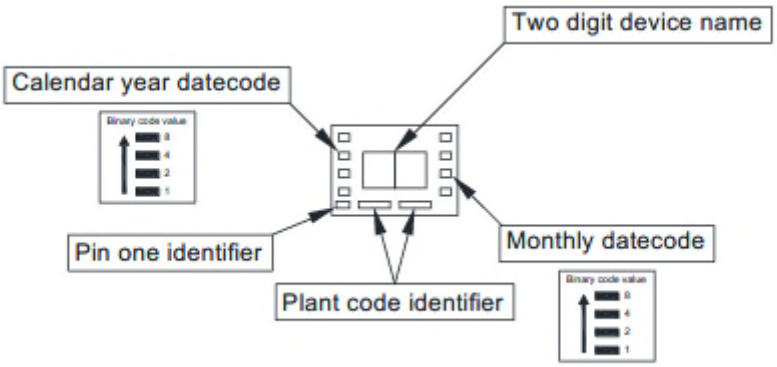
Test	Requirements			
	Number of lots	Read point	# fails / # qty	
HTOL T_a=150°C IFR	2 1	500 hours 1000 hours	0/80	NVT4557 results.
HAST 130°C/85% R.H	3	512 hours	0/775	QBS NTP52101GOJHK XQFN16
AL-TMCL -65º to 150º C	4 2	500 cycles 1000 cycles	0/77	QBS NTP52101GOJHK XQFN16
HTSL T_a=175°C	3	400 hours	0/77	QBS NTP52101GOJHK XQFN16

4.3 Standards

TMCL	Temperature Cycle Life -65º to 150º C, Jedec: JESD22-A104E Temperature Cycling with Preconditioning. This test is aimed at the mechanical integrity of the whole product, under the severe circumstances of rapid changes in temperature.
AL-TMCL	Temperature Cycle Life on PCB -40º C to +125º C. Parts are 2x reflowed and then assembled on a PCB. This test is aimed at the mechanical integrity of the system (part on PCB) to emulate use conditions in the customer's application.
UHST	Unbiased HAST MSL-1, 130°C, 85%RH, Jedec: JESD22-A110-B Unbiased Highly Accelerated Stress Test with Preconditioning, though NO electrical bias. This test is a suitable, accepted replacement for Autoclave with the goal to evaluate moisture resistance of the package.
PPOT	Unbiased Autoclave, 121°C, 100% RH Jedec: JESD22-A102 This test is particularly suitable to evaluate the moisture resistance of the package.
HTSL	High Temperature Storage Life 150°C , Jedec: JESD22-A103 This test evaluates the reliability of the product after long term storage.
HTOL/DHTL	High Temperature Operational Life Tj = +150°C, Jedec: JESD22-A103E This test is the primary test to determine the long-term reliability of the product. Generally there is limited influence of the package on this test. It is nevertheless included to demonstrate the long-term reliability of the product/package combination.
IME/EFR	Electrical endurance with electrical bias (Tj) at 150°C. This test is the primary test to determine the short-term reliability of the product. And also to determine gate oxide, metallization layer and other infant mortality defects. Burn-in requirement will depend on product maturity and supplier ability to demonstrate that known defect mechanisms have either been eliminated or adequate test screens are in place to capture intrinsic and random defects.
HAST	Highly Accelerated Stress Test, 130°C/85% R.H.Jedec: JESD22-A118 Highly Accelerated Stress Test with electrical bias and Preconditioning. This test stresses both the electrical endurance of the design/process, as well as the resistance to moisture of the package.
THBS	Temperature Humidity Biased Stress Test (85°C/85% R.H., 168 hrs release time point), with electrical bias and Preconditioning. This test stresses both the electrical endurance of the design/process, as well as the resistance to moisture of the package. This test may be replaced by HAST.

5. Marking Information

Marking line A	57



6. Package outline

Package outline information can be found on the NXP website. www.nxp.com

7. Packing

SOT1160-1 XQFN10; Reel NDP; SMD, 7" Q1 Standard product orientation Orderable part number ending ,115 or X Ordering code (12NC) ending 115	Rev. 1 — 30 September 2020 http://www.nxp.com/documents/packing/SOT1160-1_115.pdf

8. Solder information

Per JEDEC Standard

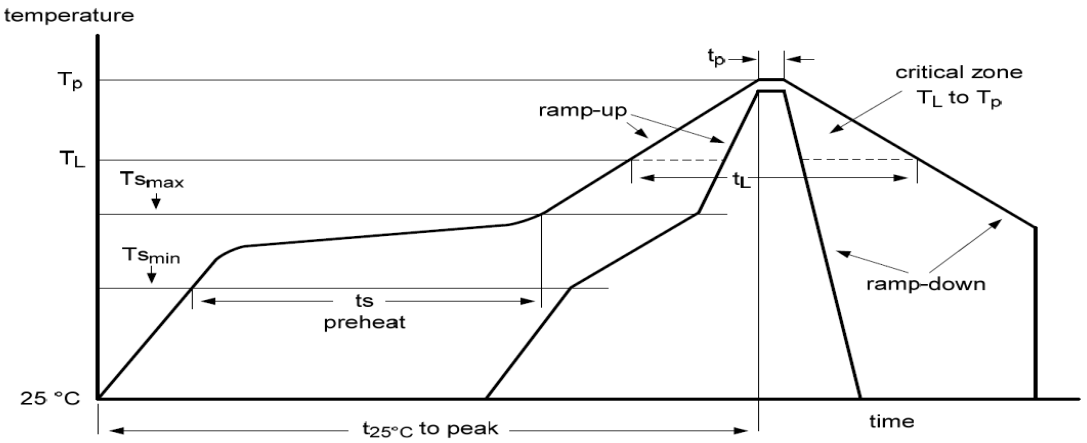
8.1 Reflow Soldering Profile

Limiting Values*

The below temperature profile for moisture sensitivity characterization is based on the IPC/JEDEC joint industry standard: J-STD-020E.

Profile Feature	SnPb eutectic assembly	Pb-free assembly
Average ramp-up rate (T_{smax} to T_p)	3 °C/s maximum	3 °C/s maximum
Preheat		
Temperature minimum (T_{smin})	100 °C	150 °C
Temperature maximum (T_{smax})	150 °C	200 °C
Time (t_{smin} to t_{smax})	60 s to 120 s	60 s to 120 s
Time maintained above		
Temperature (T_L)	183 °C	217 °C
Time (t_L)	60 s to 150 s	60 s to 150 s
Peak/classification temperature (T_p)	235 °C	260 °C
Number of allowed reflow cycles	3	3
Time within 5 °C of actual peak temperature (t_p)	20s minimum	30s minimum
Ramp-down rate	6 °C/s maximum	6 °C/s maximum
Time 25 °C to peak temperature	3 - 6 minutes	5 - 8 minutes

* applicable for devices from NXP. Pb-free assembly data on base of SAC-solder.
All temperatures refer to the topside of the package as measured on the center of the plastic body surface.



9. Chemical content

Chemical content can be found on the NXP website. www.nxp.com

The IC package is Dark Green: Halogen and antimony free.

http://www.nxp.com/chemical-content/search/

10.Legal information

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NVT4557

SIM card interface level translator with EMI filter and ESD protection

Rev. 1.0 — 21 April 2021 Product data sheet

1 General description

The NVT4557 device is built for interfacing a SIM card with a single low-voltage 1.08 V to 1.95 V host side interface. The NVT4557 contains three 1.65 V to 3.6 V level translators to convert the data, RSTn and CLKn signals between a SIM card and a host microcontroller.

The NVT4557 is compliant with all ETSI, IMT-2000 and ISO-7816 SIM/Smart card interface requirements.

2 Features and benefits

- Supports clock speed up to 10 MHz clock
- Compliant with all ETSI, IMT-2000 and ISO-7816 SIM/Smart card interface requirements
- Support SIM card supply voltages with range of 1.65 V to 3.6 V
- Host microcontroller operating voltage range: 1.08 V to 1.95 V
- Automatic level translation of I/O, RSTn and CLKn between SIM card and host side interface with capacitance isolation
- Incorporates shutdown feature for the SIM card signals according to ISO-7816-3
- Automatic enable and disable through V_{CCB}
- Integrated pull-up and pull-down resistors: no external resistors required
- Integrated EMI filters suppress higher harmonics of digital I/Os
- Integrated 8 kV ESD protection according to IEC 61000-4-2, level 4 on all SIM card contact pins
- Level shifting buffers keep ESD stress away from the host (zero-clamping concept)
- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- Available in 10-pin XQFN10 package with 0.4 mm pitch

3 Applications

- NVT4557 can be used with a range of SIM card attached devices including:
  - Mobile and personal phones
  - Wireless modems
  - SIM card terminals

4 Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
NVT4557HK	57	XQFN10	plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.40 x 1.80 x 0.50 mm	SOT1160-1

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NVT4557HK	NVT4557HKX	XQFN10	Reel 7" Q1/T1 [1]	4000	T_{amb} = -40 °C to +85 °C

[1] Find packing information - www.nxp.com/docs/en/packing/SOT1160-1_115.pdf

5 Functional diagram

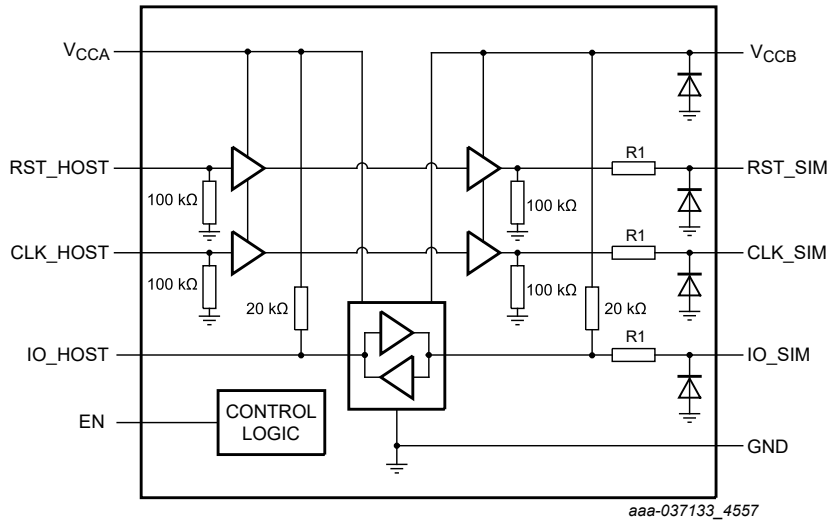


Figure 1. Functional diagram

6 Pinning information

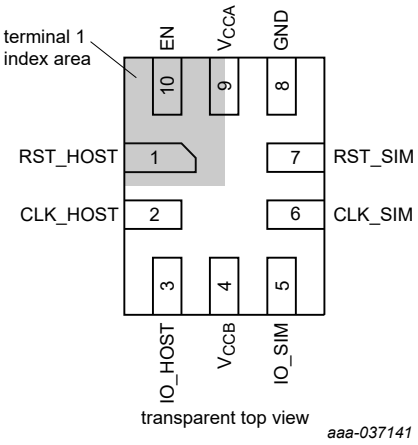


Figure 2. Pin configuration for XQFN10

6.1 Pin description

Table 3. Pin description

Symbol	Pinning for XQFN10	Type	Description
RST_HOST	1	I	Reset input from host controller.
V_{CCA}	9	supply	Supply voltage for the host controller side input/output pins (CLK_HOST, RST_HOST, IO_HOST). This pin should be bypassed with a 0.1 µF ceramic capacitor close to the pin.
RST_SIM	7	O	Reset output pin for the SIM card.
CLK_HOST	2	I	Clock input from host controller.
GND	8	ground	Ground for the SIM card and host controller. Proper grounding and bypassing are required to meet ESD specifications.
CLK_SIM	6	O	Clock output pin for the SIM card.
IO_HOST	3	I/O	Host controller bidirectional data input/output. The host output must be on an open-drain driver.
V_{CCB}	4	supply	SIM card supply voltage. When V_{CCB} is below the $V_{CCBdisable}$, the device is disabled. This pin should be bypassed with a 0.1 µF ceramic capacitor close to the pin.
IO_SIM	5	I/O	SIM card bidirectional data input/output. The SIM card output must be on an open-drain driver.
EN	10	I	Host controller driven enable pin. This pin should be HIGH (V_{CCA}) for normal operation, and LOW to help avoid race conditions specifically during the shutdown sequence.

7 Functional description

Table 4. Function table

Supply Voltage		Input	Input/Out		Operational Mode
V_{CCA}	V_{CCB}	EN [1] [2]	Host	SIM Card	
1.08 V to 1.95 V	1.65 V to 3.6 V	H	HOST = SIM Card	SIM Card = HOST	Active
1.08 V to 1.95 V	1.65 V to 3.6 V	L	See Table 5, Condition B		Shutdown Mode
GND	1.65 V to 3.6 V	X	See Table 5, Condition B		Shutdown Mode
1.08 V to 1.95 V	GND	X	See Table 5, Condition A		Shutdown Mode
GND	GND	X	See Table 5, Condition A		Shutdown Mode

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.
[2] V_{IL} and V_{IH} are referenced to V_{CCA}. The EN can be controlled by an external device limit of V_{CCA} + 0.3 V.

Table 5. Pin condition

Pin condition	Condition A	Condition B
RST_HOST	100 kΩ pull low	100 kΩ pull low
CLK_HOST	100 kΩ pull low	100 kΩ pull low
IO_HOST	20 kΩ pull to V_{CCA}	20 kΩ pull to V_{CCA}
RST_SIM	100 kΩ pull low	400 Ω pull low
CLK_SIM	100 kΩ pull low	400 Ω pull low
IO_SIM	High Z	400 Ω pull low

Refer to Figure 1.

7.1 Shutdown sequence of NVT4557

The ISO 7816-3 specification specifies the shutdown sequence for the SIM card signals to ensure that the card is properly disabled for power savings. Also during hot swap, the orderly shutdown of these signals helps to avoid any improper write and corruption of data.

When the enable, EN, is asserted LOW, the shutdown sequence is initiated by powering down the RST_SIM channel. Once the RST_SIM channel is powered down, CLK_SIM and IO_SIM are powered down sequentially one-by-one. An internal pull-down resistor on the SIM pins is used to pull these channels LOW. The shutdown sequence is completed in a few microseconds. It is important that EN is pulled LOW before V_{CCA} and V_{CCB} supplies go LOW to ensure that the shutdown sequence is properly initiated.

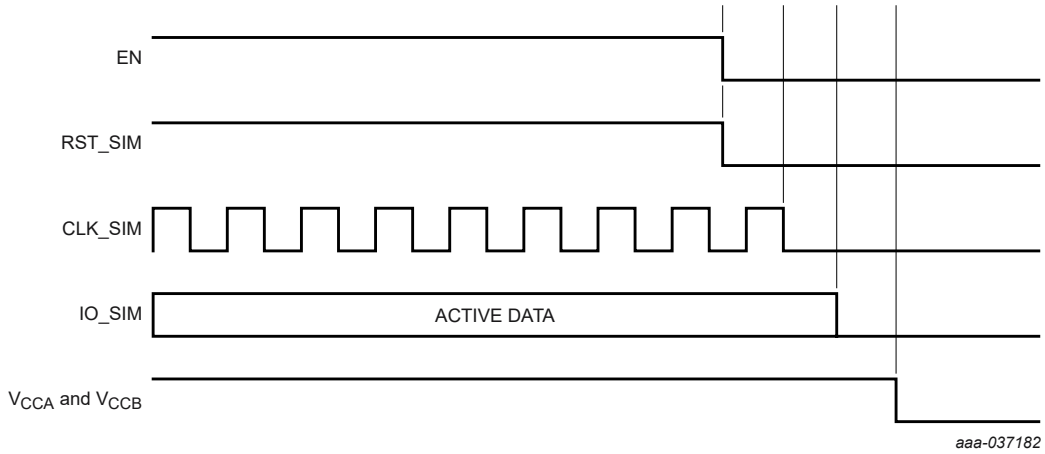
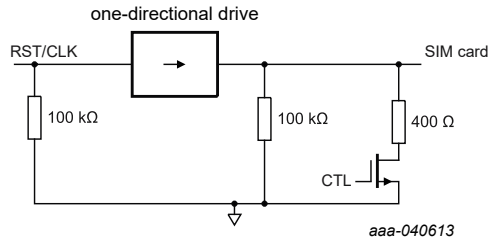


Figure 3. Shutdown sequence for RST_SIM, CLK_SIM, IO_SIM and V_{CCA}/V_{CCB} of NVT4557 SIM card translator

7.2 Embedded Enable if Enable is tied to V_{CCA}

The device contains an auto-enable feature. If V_{CCB} rises above V_{CCB_EN}, the level translator logic is enabled automatically. As soon as V_{CCB} drops below the V_{CCB_DIS}, the SIM card side drivers and the level translator logic is disabled. Host side IO pin is configured as input with a 20 kΩ resistor pulled up to V_{CCA}.

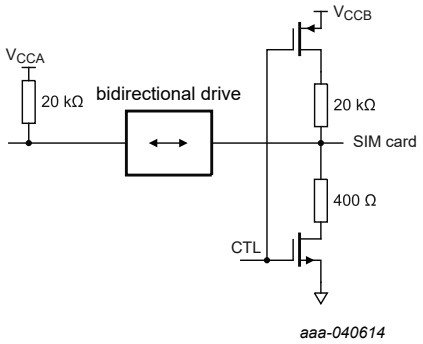
When the V_{CCB} drops below V_{CCB} disable voltage but is still higher than a MOS threshold (e.g., 0.8 V) the pulldown NMOS in the one-directional drive will be off and NMOS controlled by CTL will be on, and the 400 Ω resistor will keep the card side CLK/RST/IO low. Additionally the CLK/RST pins on both the Host and Card side have a 100 kΩ pull down resistor. The 400 Ω resistor is used for discharge at power off and the 100 kΩ resister is used for keep RST_SIM/CLK_SIM low when V_{CCB} below vth.



When V_{CCB_EN} = 0 then CTL = V_{CCB} and line is high-Z.

When V_{CCB_EN} = 1 then CTL = GND and line is active.

Figure 4. RST/CLK voltage level translation architecture



When V_{CCB_EN} = 0 then CTL = V_{CCB} and line is high-Z.

When V_{CCB_EN} = 1 then CTL = GND and line is active.

Figure 5. IO voltage level translation architecture

7.3 EMI filter

All input/output driver stages are equipped with EMI filters to reduce interferences towards sensitive mobile communication.

7.4 ESD protection

The device has robust ESD protections on all SIM card pins as well as on the V_{CCB} pin. The architecture prevents any stress for the host: the voltage translator discharges any stress to supply ground.

8 Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCA}	host supply voltage			GND - 0.5	2.2	V
V_{CCB}	SIM supply voltage			GND - 0.5	4.0	V
$V_{I(CLK\_HOST)}$	input voltage on pin CLK_HOST	input signal voltage, HOST side		GND - 0.5	2.2	V
$V_{I(RST\_HOST)}$	input voltage on pin RST_HOST	input signal voltage, HOST side		GND - 0.5	2.2	V
$V_{I(IO\_HOST)}$	input voltage on pin IO_HOST	input signal voltage, HOST side		GND - 0.5	2.2	V
$V_{I(CLK\_SIM)}$	input voltage on pin CLK_SIM	input signal voltage, SIM side		GND - 0.5	4.0	V
$V_{I(RST\_SIM)}$	input voltage on pin RST_SIM	input signal voltage, SIM side		GND - 0.5	4.0	V
$V_{I(IO\_SIM)}$	input voltage on pin IO_SIM	input signal voltage, SIM side		GND - 0.5	4.0	V
T_{stg}	storage temperature			-55	+125	°C
T_{amb}	ambient temperature			-40	+85	°C

Table 6. Limiting values*...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4, all memory card-side pins, V_{CCB} and GND	[1]			
		contact discharge		-8	+8	kV
		Human Body Model (HBM) JEDEC JESD22-A114F; all pins		-2000	+2000	V
		Charge Device Model (CDM) JEDEC JESD22-C101E; all pins		-500	+500	V
$I_{lu(IO)}$	input/output latch-up current	JESD 78B: $-0.5 \times V_{CC} < V_I < 1.5 \times V_{CC}$; $T_j < 125$ °C		-100	+100	mA

[1] All system level tests are performed with the application-specific capacitors connected to the supply pins V_{SUPPLY}, V_{LDO} and V_{CCA}.

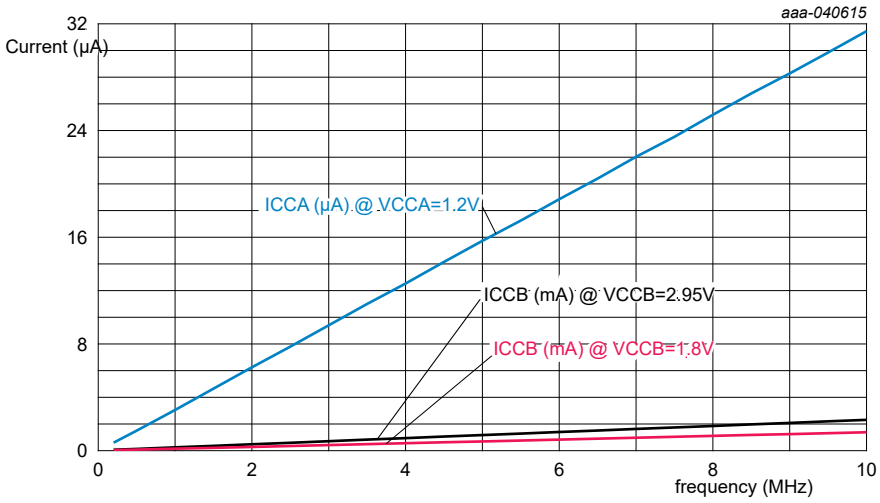
9 Characteristics

Table 7. Supplies

1.65 V ≤ V_{CCB} ≤ 3.6 V; 1.08 V ≤ V_{CCA} ≤ 1.95 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
V_{CCA}	supply voltage			1.08	-	1.95	V
I_{CCA}	supply current	operating mode; f_{CLK_HOST} = 1 MHz, EN = V_{CCA}		-	5	10	µA
		Quiescent current; EN = V_{CCA}, IO_HOST and CLK_HOST = GND		-	0.01	1	µA
		shutdown mode; EN = GND		-	-	1	µA
V_{CCB}	SIM supply voltage			1.65	-	3.6	V
I_{CCB}	SIM supply current	operating mode; f_{CLK_HOST} = 1 MHz, EN = V_{CCA}, C_l = 50 pF		-	20	30	µA
		Quiescent current; EN = V_{CCA}, IO_HOST and CLK_HOST = GND		-	3.7	4.2	µA
		shutdown mode; EN = GND		-	-	1	µA

[1] Typical values measured at 25 °C.



V_{CCA} = 1.2 V and V_{CCB} = 1.8 V or 2.95 V; C_l = 50 pF

Figure 6. Operating Mode Current over Frequency

Table 8. Static characteristics

1.65 V ≤ V_{CCB} ≤ 3.6 V; 1.08 V ≤ V_{CCA} ≤ 1.95 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
Automatic enable feature: V_{CCB}							
V_{CCB_EN}	device enable voltage level	V_{CCA} ≥ 1.0 V, V_{CCB} rising edge		1.65	-	-	V
V_{CCB_DIS}	device disable voltage level	V_{CCA} ≥ 1.0 V, V_{CCB} falling edge		-	-	1.40	V
ΔV_{CCBen}	V_{CCBen} hysteresis voltage			-	132	-	mV
Hardware enable pin							
V_{IH}	HIGH-level input voltage	EN pin threshold					
		1.08 V ≤ V_{CCA} < 1.95 V		0.7 × V_{CCA}	-	V_{CCA} + 0.3	V
V_{IL}	LOW-level input voltage	EN pin threshold		-0.15	-	0.3 × V_{CCA}	V
Level shifter							
V_{IH}	HIGH-level input voltage	IO_HOST, RST_HOST, CLK_HOST					
		1.08 V ≤ V_{CCA} < 1.95 V	[2]	0.7 × V_{CCA}	-	V_{CCA} + 0.3	V
		IO_SIM	[2]	0.7 × V_{CCB}	-	V_{CCB} + 0.3	V
V_{IL}	LOW-level input voltage	IO_HOST, RST_HOST, CLK_HOST	[2]	-0.15	-	0.3 × V_{CCA}	V
		IO_SIM	[2]	-0.15	-	0.3 × V_{CCB}	V
R_{PU}	pull-up resistance	IO_SIM connected to V_{CCB}	[3]	14	20	26	kΩ
		IO_HOST connected to V_{CCA}	[3]	14	20	26	kΩ
V_{OH}	HIGH-level output voltage	RST_SIM, CLK_SIM; I_{OH} = -1 mA	[2]	0.75 × V_{CCB}	-	V_{CCB}	V
		IO_SIM; I_{OH} = -10 µA	[2]	0.75 × V_{CCB}	-	V_{CCB}	V
		IO_HOST; I_{OH} = -10 µA	[2]	0.75 × V_{CCA}	-	V_{CCA}	V
V_{OL}	LOW-level output voltage	RST_SIM, CLK_SIM; I_{OL} = 1 mA	[2]	0	-	0.125 × V_{CCB}	mV
		IO_SIM; I_{OL} = 1 mA	[2]	0	-	0.125 × V_{CCB}	mV
		IO_HOST; I_{OL} = 1 mA	[2]	0	-	0.25 × V_{CCA}	mV
R_{pd}	pull-down resistance	CLK_HOST/SIM, RST_HOST/SIM; EN = 0		70	100	130	kΩ
EMI filter							
R_s	series resistance	IO_SIM; R1 tolerance ± 30 % [4]	[2]	-	30	-	Ω
		RST_SIM; R1 tolerance ± 30 % [4]		-	30	-	Ω
		CLK_SIM; R1 tolerance ± 30 % [4]	[2]	-	30	-	Ω
C_{io}	input/output capacitance	IO_SIM	[2]	-	8.5	-	pF
		RST_SIM		-	8.5	-	pF
		CLK_SIM	[2]	-	8.5	-	pF

[1] Typical values measured at 25 °C.
[2] V_{IL}, V_{IH} depend on the individual supply voltage per interface.
[3] See Figure 9 for details.
[4] Guaranteed by design

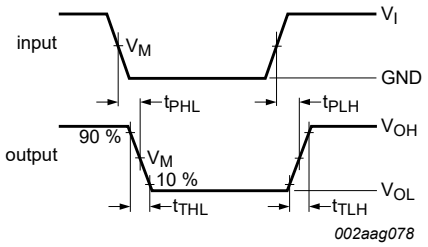
Table 9. Dynamic characteristics

1.65 V ≤ V_{CCB} ≤ 3.6 V; 1.08 V ≤ V_{CCA} ≤ 1.95 V; f_{clk} = f_{io} = 1 MHz; T_{amb} = -40 °C to +85 °C; unless otherwise specified. Refer to Figure 7.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CCA} = 1.8 V; V_{CCB} = 3.0 V; SIM card C_L ≤ 30 pF; host C_L ≤ 10 pF							
t_{PD}	propagation delay	I/O channel; SIM card side to host side		-	8	15	ns
		all channels; host side to SIM card side		-	8	15	ns
t_t	transition time			-	-	10	ns
$t_{sk(o)}$	output skew time	between channels; IO_SIM and CLK_SIM	[1]	-	2	-	ns
f_{clk}	clock frequency	CLK_SIM [2]		-	-	10	MHz
V_{CCA} = 1.2 V; V_{CCB} = 1.8 V; SIM card C_L ≤ 30 pF; host C_L ≤ 10 pF							
t_{PD}	propagation delay	I/O channel; SIM card side to host side		-	15	25	ns
		all channels; host side to SIM card side		-	15	25	ns
t_t	transition time			-	-	10	ns
$t_{sk(o)}$	output skew time	between channels; IO_SIM and CLK_SIM	[1]	-	2	-	ns
f_{clk}	clock frequency	CLK_SIM [2]		-	-	10	MHz

[1] Skew between any two outputs of the same package switching in the same direction with the same C_L.
[2] Guaranteed by design

9.1 Waveforms



Measurement points are given in Table 9.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.
t_{PHL} and t_{PLH} are t_{PD} propagation delay; t_{THL} and t_{TLH} are the transition time.

Figure 7. Data input to data output propagation delay times

10 Application information

The application circuit for the NVT4557, which shows the typical interface with a SIM card, is shown in Figure 8.

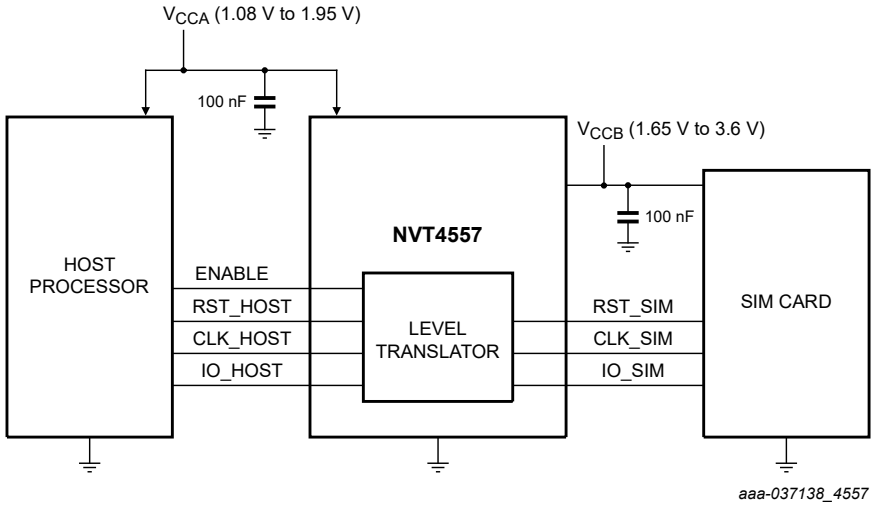


Figure 8. NVT4557 application circuit interfacing with typical SIM card

10.1 Input/output capacitor considerations

It is recommended that a 1 µF and 100 nF capacitors having low Equivalent Series Resistance (ESR) are used respectively at V_{CCA} and V_{CCB} input terminals of the device. X5R and X7R type multi-layer ceramic capacitors (MLCC) are preferred because they have minimal variation in value and ESR over temperature. The maximum ESR should be < 500 mΩ (50 mΩ typical).

10.2 Layout consideration

The capacitors should be placed directly at the terminals and ground plane. It is recommended to design the PCB so that the V_{CCA} and V_{CCB} pins are bypassed with a capacitor with each ground returning to a common node at the GND pin of the device such that ground loops are minimized.

10.3 Level translator stage

The architecture of the device I/O channel is shown in Figure 9. The device does not require an extra input signal to control the direction of data flow from host to SIM or from SIM to host. As a change of driving direction is just possible when both sides are in HIGH state, the control logic is recognizing the first falling edge granting it control about the other signal side. During a rising edge signal, the non-driving output is driven by a one-shot circuit to accelerate the rising edge. In case of a communication error or some other unforeseen incident that would drive both connected sides to be drivers at the same time, the internal logic automatically prevents stuck-at situation, so both I/Os will return to HIGH level once released from being driven LOW.

The channels RST and CLK just contain single direction drivers without the holding mechanism of the I/O channel, as these are just driven from the host to the card side.

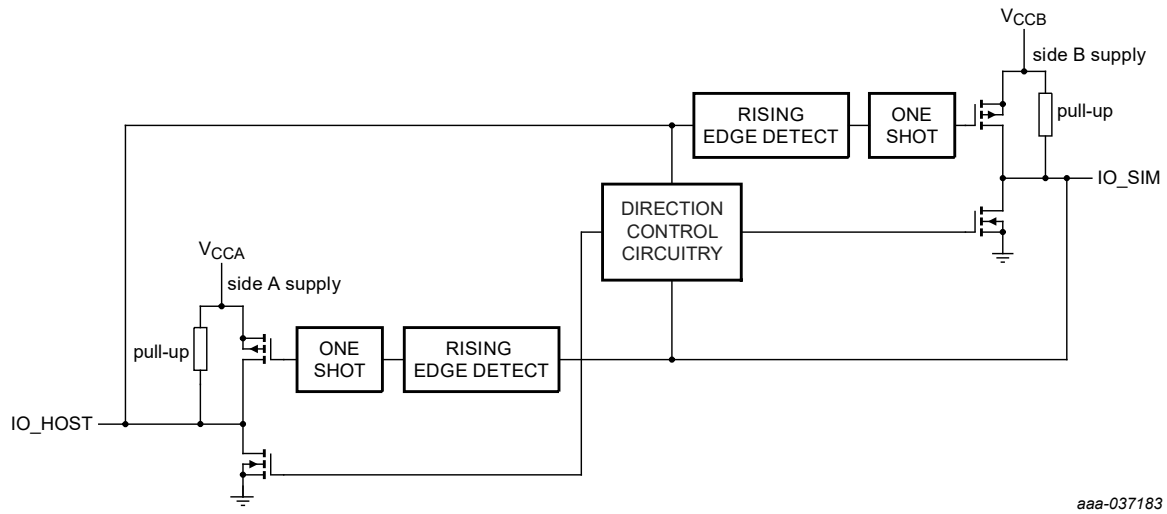
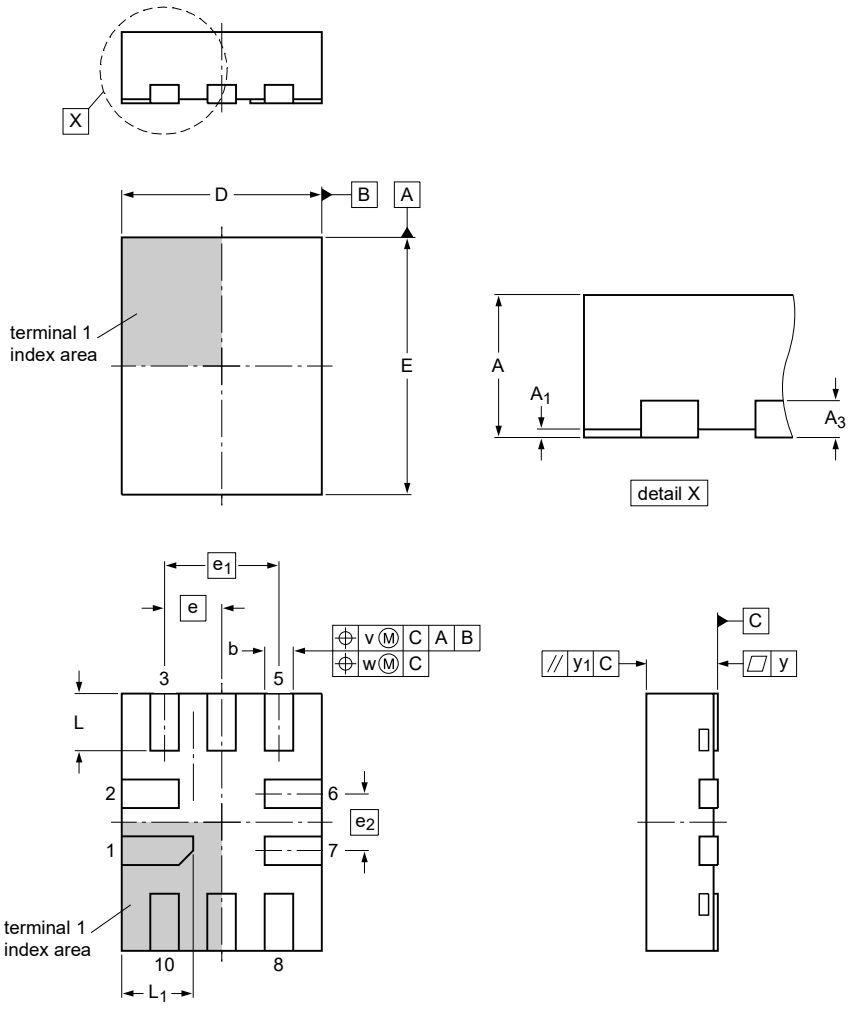


Figure 9. Automatic direction control level translator for HIGH-level direction change interfaces

11 Package outline

XQFN10: plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.40 x 1.80 x 0.50 mm **SOT1160-1**



Dimensions

Unit[1]		A	A_1	A_3	b	D	E	e	e_1	e_2	L	L_1	v	w	y	y_1
mm	max	0.50	0.05		0.25	1.5	1.9				0.45	0.55				
	nom	0.45		0.127	0.20	1.4	1.8	0.4	0.8	0.4	0.40	0.50	0.1	0.05	0.05	0.05
	min	0.40	0.00		0.15	1.3	1.7				0.35	0.45				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1160-1_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1160-1	- - -	- - -	- - -		~~09-12-29~~ 21-01-26

Figure 10. Package outline XQFN10 (SOT1160-1)

12 PCB layout

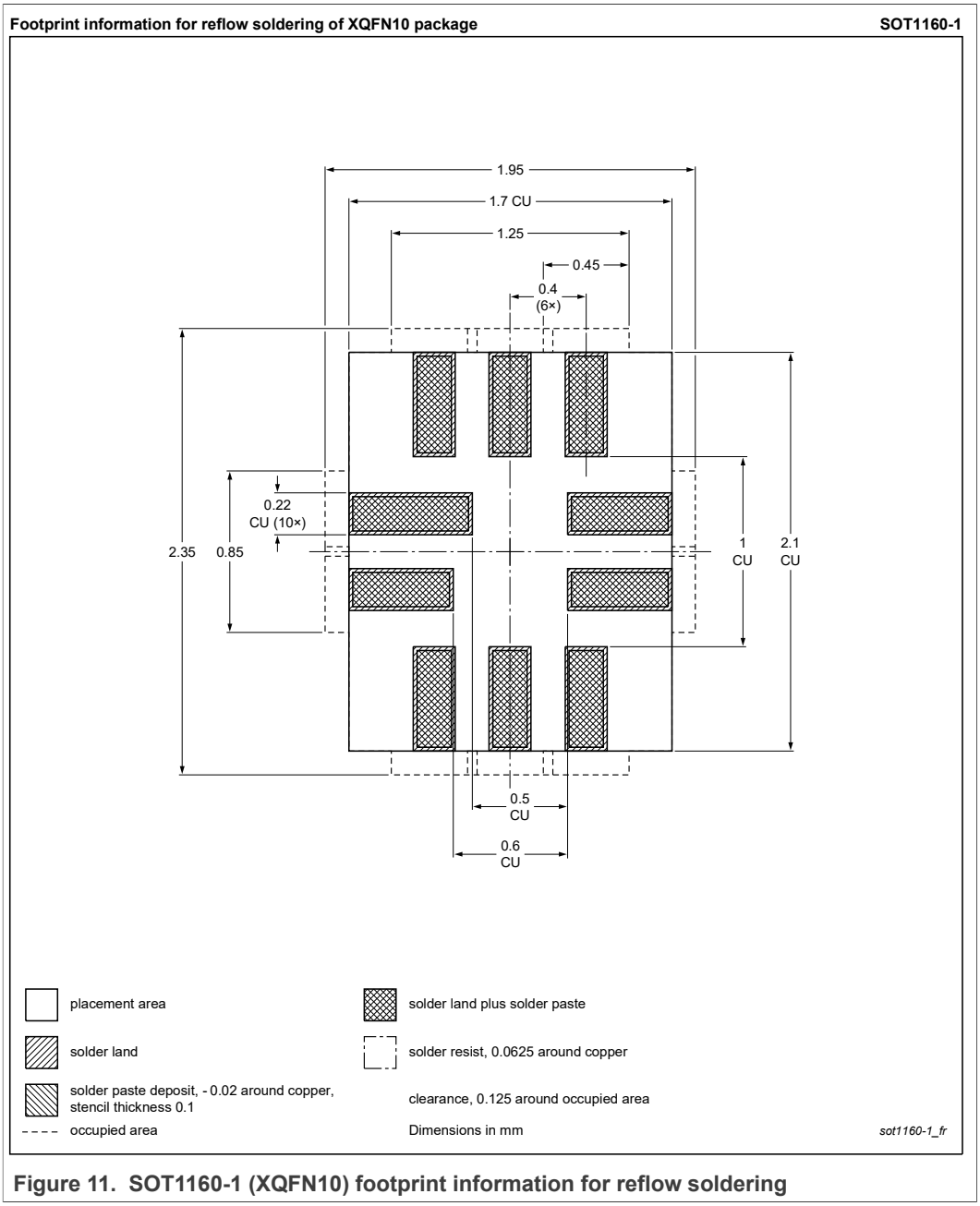


Figure 11. SOT1160-1 (XQFN10) footprint information for reflow soldering

13 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 12) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and Table 11

Table 10. SnPb eutectic process (from J-STD-020D)

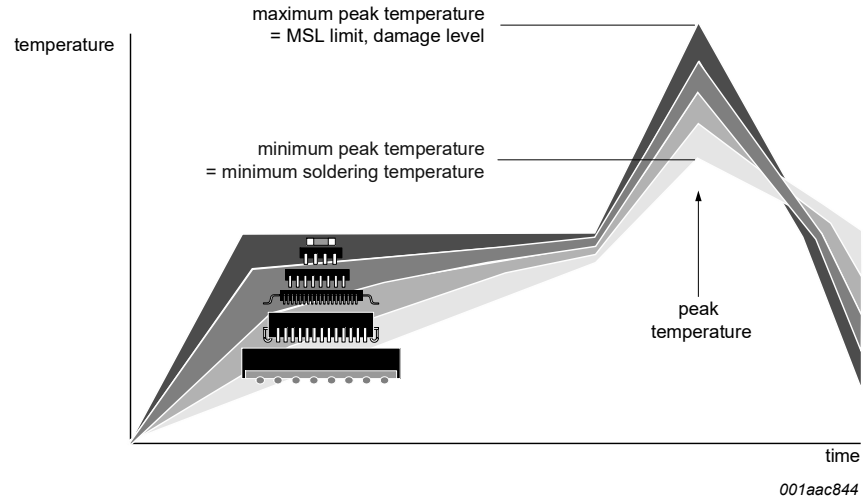
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 11. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 12.



MSL: Moisture Sensitivity Level

Figure 12. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14 Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged-Device Model
DP	Dry Pack
ESD	ElectroStatic Discharge
ESR	Equivalent Series Resistance
HBM	Human Body Model
I/O	Input/Output
LDO	Low DropOut regulator
PCB	Printed-Circuit Board
PMOS	Positive-channel Metal-Oxide Semiconductor
SIM	Subscriber Identification Module

15 Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NVT4557 v.1.0	20210421	Product data sheet	-	-

16 Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 21 April 2021
Document identifier: NVT4557

AN13158

NVT4858/NVT4557 voltage-level translator layout guideline

Rev. 1.0 — 17 March 2021 Application note

Document information

Information	Content
Keywords	NVT4858, NVT4557, Level Shifter, Level Translator, SD card, SIM card, Layout Guideline
Abstract	The NVT4858 is an SD 3.0 compliant dual voltage level translator with auto-direction control. The NVT4557 is a SIM SIO-7816 Smart Card compliant dual voltage level translator with auto-direction control. This application note details the layout guidelines to ensure the optimal operation of the device.

Revision history

Rev	Date	Description
v.1	20210317	Initial version

1 Introduction

High performance digital signals on modern microprocessors are designed using advanced CMOS process to take advantage of its low power consumption. However, CMOS logic has very fast edge rates in the range of 1 ns to 2 nS. PCB traces might exhibit ringing, signal degradation and reflection due to the effect of the signal's fast rise and fall time contributed by the PCB transmission characteristic.

This application note details the general PCB layout guidelines for High Speed Secure Digital (SD), and Smart Card (SIM) in NVT4858 and NVT4557 voltage level shifter application to minimize signal integrity issues.

2 NVT4858/NVT4557 voltage-level translator layout guidelines

To ensure optimal performance and reliability of the device, the following PCB layout guidelines are recommended.

2.1 Power and ground

- A minimum four-layer PCB stack-up is required.
- The level shifter and the card socket should be placed top of a solid, continuous ground plane.
- Preferably, the power for the level shifter should come directly from the power plane underneath it, but if the power trace must be used then the trace should be at least 20 mil wide.
- Bypass capacitors of 0.1 µF should be placed as close as possible to VCCA and VCCB pins with a very short PCB trace.

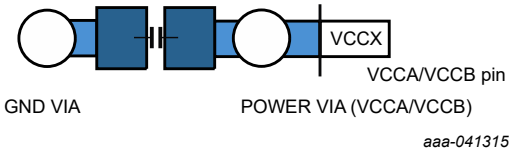

Figure 1. Bypass capacitor placement

2.2 SD and SIM signals from Host to Level Shifter

The SD interface high speed signals SD_DAT[3:0], SD_CDM and SD_CLK critical and require careful layout and consideration. These signals must be routed above a solid ground plane and should be routed with the following recommendations.

- Component Placement and Trace Impedance – high frequency signals are sensitive to impedance changes and discontinuity introduced by vias. The level shifter and the card socket should be placed on the same layer as the Hot Controller. Placing these devices on the same layer helps to reduce the need to use vias with direct routing between these devices. The PCB traces should be routed with 50 Ω characteristic impedance or close to it to reduce transmission effect. The round-trip delay of the PCB traces should be less than the rise/fall times of the signal driver. If the PCB traces are longer than the rise/fall times, then series termination resistors can be used to minimize signal reflection.
- Series Termination and Placement – if series termination resistors are to be used, the suggested values are 22 Ω to 33 Ω. The termination resistors on the Host Controller

side of the level shifter should be placed close to the level shifter. The termination resistors on the card side of the level shifter should be placed close to the card socket.

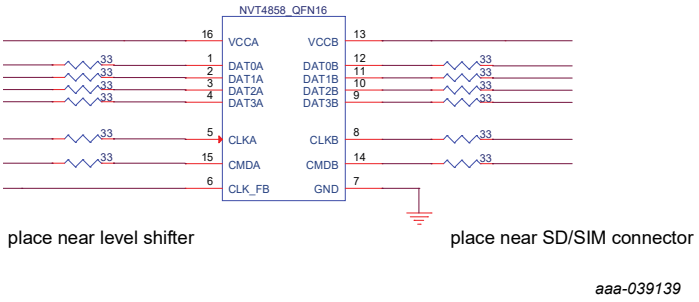

Figure 2. Termination resistors

- PCB trace separation – SD clock and data signals carry high frequency fast rise and fall time signals. Any low capacitive impedance path existed between two traces creates a path for one signal to couple onto another signal next to it. For this reason, SD clock and data must be separate from one another with the following spacing constraint.
  SD_CLK > 2 times the high of SD_CLK to the ground plane underneath it.
  SD_DATA[3:0] > 1.5 times the high of SD_CLK to the ground plane underneath it.
  SD_CMD > 1.5 times the high of SD_CLK to the ground plane underneath it.
- Trace Routing – when routing the PCB traces, it is critical to keep the trace width the same to keep the trace impedance constant from the driver to the receiver. Any trace width deviation creates impedance mismatch and creates signal reflection. Avoid using 90-degree angle and use a 45-degree bend when the trace must be routed perpendicularly.
- PCB Trace length matching - to minimize the skew between traces, route them with the same length.

2.3 SD and SIM signals from Level Shifter to Card Socket

The SD interface high speed signals SD_DAT[3:0], SD_CDM and SD_CLK are critical and require careful layout and consideration. These signals must be routed above a solid ground plane and should be routed with the following recommendations.

- Component Placement and Trace Impedance – component placement and trace impedance should follow the guideline as PCB routing from Host Controller to Level Shifter.
- Series Termination and Placement – if series termination resistors are to be used, the suggested values are 22 Ω to 33 Ω. The termination resistors on the card side of the level shifter should be placed close to the card socket as shown in Figure 2.
- PCB trace separation – the trace separation impedance should follow the guideline as PCB routing from Host Controller to Level Shifter.
- Trace Routing – when routing the PCB traces, it is critical to keep the trace width the same to keep the trace impedance constant from the driver to the receiver. Any trace width deviation creates impedance mismatch and creates signal reflection. Avoid using 90-degree angle and use 45-degree bend when the trace must be routed perpendicularly

- The total capacitance between the level shifter and the card should follow the recommendation in the SD Physical Layer specification.

Driver Type	Symbol	Driver Rise / Fall Time Requirements				Condition
		Min.	Typ.	Max.	Units	C_L
Type B for UHS104	T_RB, T_FB	0.40	0.88	1.32	ns	15pF
Type B for UHS50	T_RB, T_FB	0.70	1.83	2.75	ns	30pF

- PCB Trace length matching - to minimize the skew between traces, route them with the same length.

3 Conclusion

Proper PCB layout is critical for the success of the NT4858/NVT4557 operation. All high-speed PCB rules, techniques, component placement and trace routing must be followed and taken into consideration during the PCB layout phase.

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Figures

Contents

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For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 17 March 2021
Document identifier: AN13158

Introduction

This document is designed to help you gain a better understanding of semiconductor devices, so as to ensure the quality and reliability of the devices that you incorporate into your designs.

Electrostatic charge generation

In neutral material, the net charge of protons (positive charge) and electrons (negative charge) is zero. When the surface of one material is rubbed along that of another, local (frictional) heating can transfer energy to the electrons near the surface in excess of the Coulomb binding energy. Such electrons may leave their outer valence orbit and be trapped in an outer valence orbit in the other material. Thus two ions will be formed: 1) positive, for electron-donor material and 2) negative, for electron-acceptor material. Friction between any two surfaces involving at least one non-conductive material is a potential generator of electrostatic (triboelectric) charge; the magnitude and polarity of the charge depends on: □□the materials involved. Charge magnitude and polarity depends on the sum of the separations from the neutral boundary of the two materials in the triboelectric series (Table 1) frictional heat, which depends on speed and applied force surface conductivity. Part of the charge may be drained off during and after rubbing, inhibiting build up of maximum possible voltage, but this is true only for surface conductivities below 10E9 per Surface Square.

A grounded operator cannot drain charge from a non-conductive object. Thus, an operator's clothing may be charged even though a conductive wrist strap grounds his body. Similarly, charged plastic boxes or trays will not be discharged by a grounded operator or bench top.

Induction

Static charges can be transferred by induction; that is, without direct contact. Objects that can transfer charges by induction include the plastic boxes, trays and covers used extensively in production lines. An ESD-sensitive device charged by induction can be damaged if touched by a grounded operator. Removing static charges from insulating materials can only be achieved by use of ionizers.

ESD precautions

In the following section are some hints to avoid ESD damage.

For more detailed information see JEDEC standard JESD625-A, which establishes the minimum requirements for Electrostatic Discharge (ESD) control methods and materials used to protect electronic devices that are susceptible to damage or degradation from electrostatic discharge (ESD).

The ESD workstation

Essential features of a workstation for handling ESD devices are shown in Fig. 1. Adaptations for inspection, assembly, repair and other purposes should respect these guidelines:

- Conductive work-surface sheet resistance 10 KΩ to 1 MΩ per square meter
- Resistor for grounding wrist strap between 0.9MΩ and 5MΩ.
  Maximum ground current 2 mA: enough for operator to feel a fault but well below danger level
- All test equipment grounded
- Switching transients suppressed
- All metal table trim, support frames and brackets grounded
- Cotton working garments
- Static-safe rails, bags, foam pads and shorting clips available, if needed.

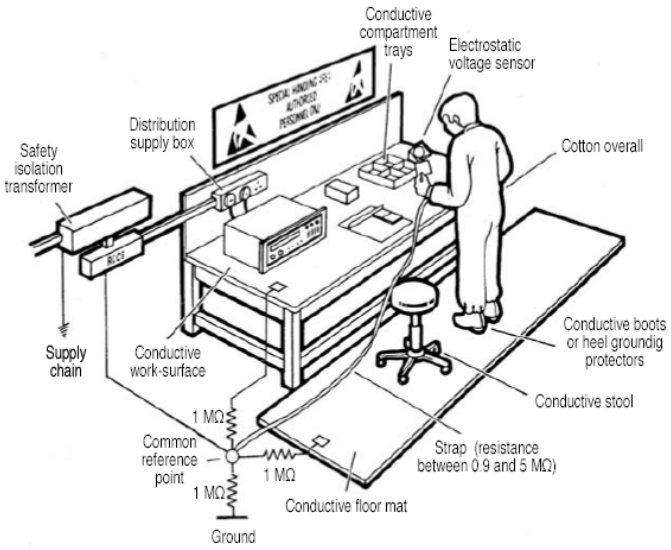


Fig 1. Essential features of an ESD work station.

Circuit layout precautions

Designing of a circuit board for ESD-sensitive devices should allow for handling by persons unaware of the ESD hazard. Observe the following precautions:

- Tracks to and from ESD-sensitive devices should not pass board edges, to minimize the risk of their being touched in handling.
- Where possible, connect a resistor of about 1 MΩ between conductors from ESD-sensitive devices and board inputs and outputs.
- Avoid long signal lines; they increase the risk of induced large-signal pick-up.
- Observe the maximum rated values for supply turn-on and turn-off transients. Suppress power supply turn-on and turn-off transients, power supply ripple or regulation and ground noise, to avoid exceeding the Absolute Maximum ratings. Fast zener protection diodes are useful here.
- Label the board with an ESD warning.
- Make sure that the service documentation calls attention to the use of ESD-sensitive devices and the precautions to be taken with them.

Marking of ESD-sensitive devices

IEC 417 and MIL-STD-1686 recommend that the symbol shown in Fig. 2(a) is used to mark ESD sensitive devices. The symbol should be supplemented by the notice 'ATTENTION – observe precautions for handling ELECTROSTATIC SENSITIVE DEVICES'. Where space is restricted, the simplified symbol shown in Fig. 2(b) may be used. Symbol and lettering should be in black on a yellow ground.

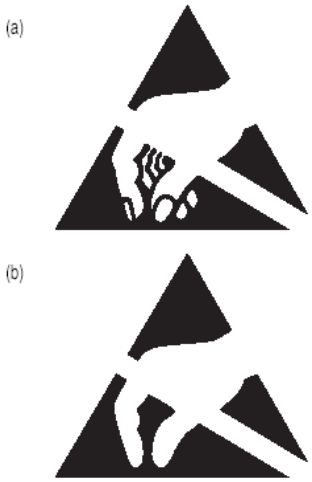


Fig 2 (a) symbol according to IEC 417

Fig 2 (b) Simplified version for use where space is restricted

ESD warning symbols for ESD sensitivity

User precautions

As a general rule, ESD-sensitive devices should always be handled at an ESD station conforming to Fig. 1. Pay particular attention to stores and inspection areas where personnel may not be fully aware of ESD hazards.

Packing and storage

ESD-sensitive devices are packed in antistatic or conductive boxes or rails. Intimate (tube, tape, bag etc.) and proximity (level 1 box) packing is marked with the Fig. 2 symbol. ESD-sensitive devices not supplied in antistatic packing should be returned to the supplier. ESD-sensitive devices should be stored in their original packing, preferably in a cool place set aside for the purpose. Do not unpack them until they are required for incoming inspection or use in production.

Receiving inspection

Do not put ESD-sensitive devices where static discharges can occur, even if they have protective packing. In their immediate vicinity avoid the presence of:

- Materials which can develop static charges (see Fig. 3)
- Electrical switching equipment and tools.

These precautions also apply to assemblies that incorporate ESD-sensitive devices.

Unpack and handle the devices at an ESD workstation generally conforming to Fig. 1. Take care that the devices are not exposed to the voltage pulses that can occur when switching the power supply on and off. Increase the supply voltage slowly to its normal value before applying test signals, to avoid the latching effect that occurs when the signal voltage exceeds the supply voltage. During testing, and especially when going from one test to another, ensure that all supplied voltages are under control. If possible, ground all unused inputs during tests. Do not allow a signal to

remain on an input when the power supply is switched off. If necessary, connect a buffer stage between the signal source and the input in such a way that it automatically switches off the signal when the power supply is switched off.

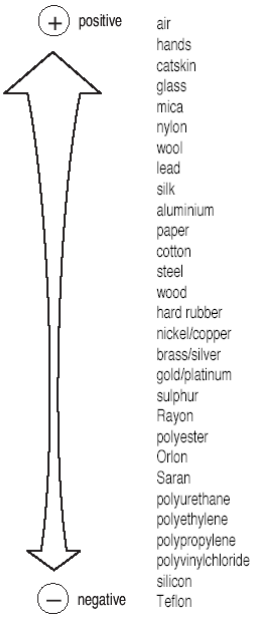


Fig 1. Triboelectric series of some common materials

After testing, repack the devices in their original anti-static packing; keeping the warning label intact. Repack at an ESD workstation. ssembly precautions

ESD-sensitive devices should be the last components to be inserted in a circuit board or system.

Manual insertion: Use an ESD workstation.

Automatic insertion: Ground insertion equipment and machinery. Use only tools of conductive or antistatic material.

Use grounded component tongs to remove ESD sensitive devices from their antistatic packing. Do not remove more components at a time than are immediately required.

Ground the soldering iron or bath. Do not solder to circuits that are connected to a switched-on power supply. Ensure that every work surface on which a circuit board may be placed is provided with a conductive or anti-static sheet big enough to receive the whole board.

Handle boards that contain ESD-sensitive devices as single components. Pack them in antistatic or conductive packing. Label them with an ESD warning. Ground all handling personnel.

Measurement precautions

Place the board, soldered side down, on a conductive or antistatic foam pad to discharge any static electricity. Remove short-circuit clips. Handle the board only by its edges, remove it from the foam pad for testing. After testing, replace it on the foam pad for transport.

Repair and maintenance precautions

Switch off the equipment in which the board is incorporated before removing a board containing ESD-sensitive devices. For repair and maintenance use an ESD workstation arranged as shown in Fig. 1. Place the board on an

antistatic foam pad. Observing the 'Assembly precautions', remove and replace the faulty device. After testing, replace the board in the equipment.

Static detection and prevention equipment

A wide range of commercial products is available to help detect static electricity, equip workstations and prevent ESD. They range from conductive bags, gloves, mats, foam, wrist straps and boxes, through to static voltmeters, ionizers and ESD simulators. Careful use of available products can help locate and prevent ESD hazards, and so improve quality wherever semiconductors are**.**

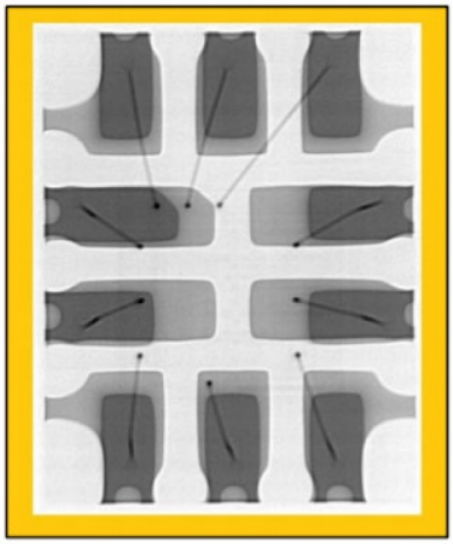
Limitations of anti-static agents

Anti-static agents – conductive sprays – are commonly used to protect against ESD. Although they do protect against charging by friction, they do not form an effective shield and therefore give no protection against charge induction. The only sure protection against charge induction is a Faraday cage shielding the protected object from all possible sources of induced charge**.**

- ## X-ray

NVT4557HK
XQFN10
ATBK

X-Ray Photo



- ## Cross section

Cross Section Analysis:

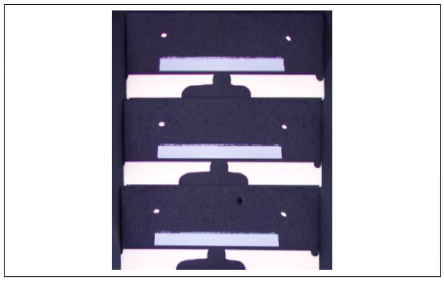
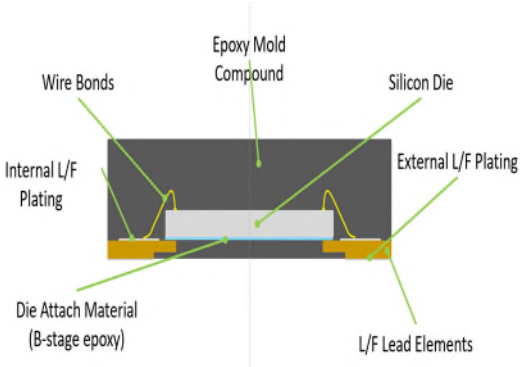


Figure 3. Photo of the cross-section showed internal package structure.



- ## Package dimension measurement

Under redo the measurement with 30pcs samples and will update the table.

Lot	Dimensions (mm)	Average (mm)	Maximum (mm)	Minimum (mm)	Sample Size	Outline Spec. (mm)
Lot ID N0S039676100	Package body length	1.814	1.817	1.811	10	1.8-1.9
	Package body width	1.361	1.417	1.142		1.4-1.5
	Package body Thickness	0.483	0.485	0.4981		Max 0.5

- ## Coplanarity

≤ 50um

Under working Coplanarity measurement with 10pcs and will update the table.

SOT1160-1

XQFN10 ; Reel NDP, SMD, 7" Q1 standard product orientation Ordering code (12NC) ending 115

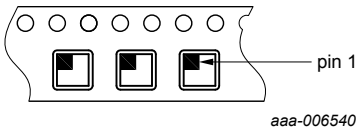
Rev. 1 — 30 September 2020 Packing information

1 Dimensions and quantities

Reel dimensions d × w (mm) [1]	SPQ/PQ (pcs)[2]	Reels per box
180 × 8	4000	1

[1] d = reel diameter; w = tape width.
[2] Packing quantity dependent on specific product type. View ordering and availability details at NXP order portal, or contact your local NXP representative.

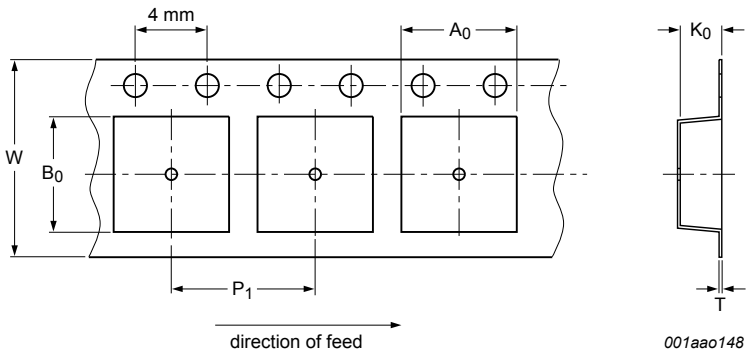
2 Product orientation



Pin 1 is in quadrant 1.

Figure 1. Product orientation in carrier tape

3 Carrier tape dimensions



Not drawn to scale.

Figure 2. Carrier tape dimensions

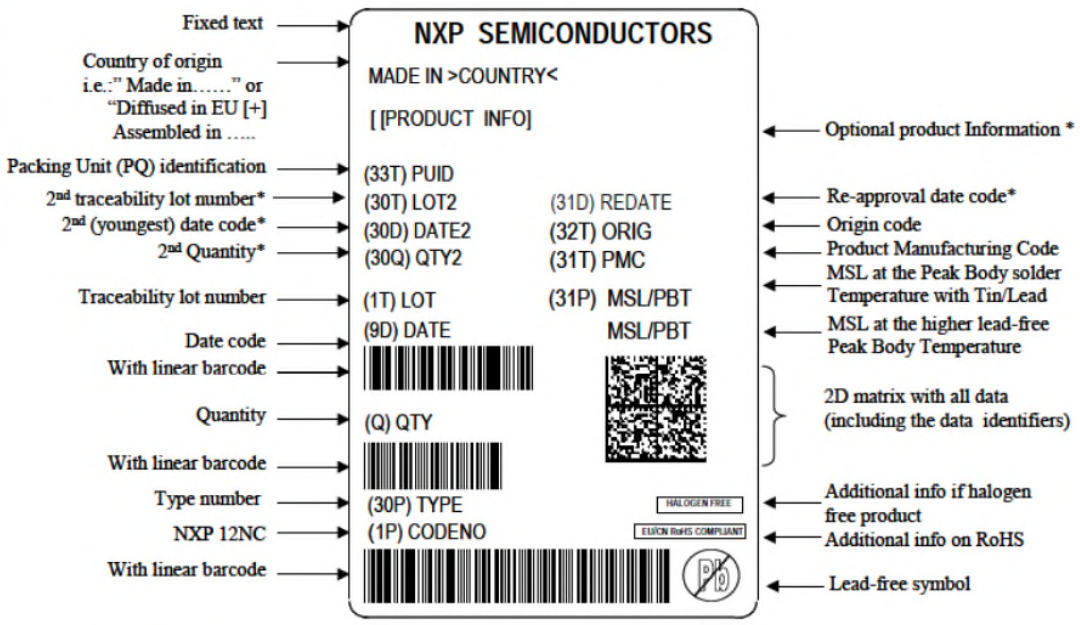
In accordance with IEC 60286-3/EIA-481.

A_0 (mm)	B_0 (mm)	K_0 (mm)	T (mm)	P_1 (mm)	W (mm)
1.60±0.03	2.00±0.03	0.61±0.05	0.25±0.03	4.00±0.10	8.00±0.10

		Datasheet / Test limit.						FT	QA
Tnum	**Name**	**LoLimit**	**HiLimit**	**Unit**	**Mean**	**Sigma**	**Count**	**Cpk**	**Cpk**
300	Pre_Icc:IccA_Oper_enH_1v95_3V60_iox@VCCA	3.6	10	uA	5.398	0.153	1,782	3.92	3.989349
301	Pre_Icc:IccB_Oper_enH_standby_1v95_3V60_iox@VCCB	2.7	4.2	uA	3.723	0.090	1,782	1.77	1.799184
302	Pre_Icc:IccA_Shut_enH_1v95_3V60_iox@VCCA	-0.183	1	uA	4.479	15.200	1,782	4.11	4.205716
303	Pre_Icc:IccB_Shut_enH_1v95_3V60_iox@VCCB	-0.14	1	uA	57.661	6.766	1,782	9.74	9.818617
400	VCCBen_1V10_3V00:Auto_EN_VCCB	1.65	1.7	V	1.471	0.015	1,782	5.07	5.094447
401	VCCBen_1V10_3V00:Auto_DIS_VCCB	1.1	1.4	V	1.339	0.014	1,782	5.54	5.765541
402	VCCBen_1V10_3V00:VCCBen_Hyst	70	200	mV	131.793	3.411	1,782	6.04	5.723323
5000	OVS_HVS_2V50_4V50_100ms:OVS_IOH_2V5_4V5_100mS_EN@EN				-0.072	0.084	1,782	4.26	-
5001	OVS_HVS_2V50_4V50_100ms:OVS_IOH_2V5_4V5_100mS_RST_HOST@RST_HOST				28.682	0.505	1,782	7.47	-
5002	OVS_HVS_2V50_4V50_100ms:OVS_IOL_2V5_4V5_100mS_CLK_HOST@CLK_HOST				-0.062	0.085	1,782	5.61	-
5003	OVS_HVS_2V50_4V50_100ms:OVS_IOL_2V5_4V5_100mS_IO_SIM@IO_SIM				-227.739	2.003	1,782	7.95	-
600	VIHL_FUNC:Vih_en_1v10_3v00	1	1	fct	1.000	0.000	1,782	-	-
601	VIHL_FUNC:Vil_en_1v10_3v00	1	1	fct	1.000	0.000	1,782	-	-
602	VIHL_FUNC:Vih_en_1v80_3v00	1	1	fct	1.000	0.000	1,782	-	-
603	VIHL_FUNC:Vil_en_1v80_3v00	1	1	fct	1.000	0.000	1,782	-	-
604	VIHL_FUNC:Vih_host_clk_rst_io_1v10_3v00	1	1	fct	1.000	0.000	1,782	-	-
605	VIHL_FUNC:Vil_host_clk_rst_io_1v10_3v00	1	1	fct	1.000	0.000	1,782	-	-
606	VIHL_FUNC:Vih_host_clk_rst_io_2v00_3v00	1	1	fct	1.000	0.000	1,782	-	-
607	VIHL_FUNC:Vil_host_clk_rst_io_2v00_3v00	1	1	fct	1.000	0.000	1,782	-	-
608	VIHL_FUNC:VIH_io_sim_1v20_1v65	1	1	fct	1.000	0.000	1,782	-	
609	VIHL_FUNC:VIL_io_sim_1v20_1v65	1	1	fct	1.000	0.000	1,782	-	
610	VIHL_FUNC:VIH_io_sim_1v20_3v60	1	1	fct	1.000	0.000	1,782	-	
611	VIHL_FUNC:VIL_io_sim_1v20_3v60	1	1	fct	1.000	0.000	1,782	-	
650	Volh_iohost_1v10_3v30:Voh_iohost_1v10_3v30@IO_HOST	0.825	1.1	V	907.254	1.771	1,782	4.19	14.19312
651	Volh_iohost_1v10_3v30:Vol_iohost_1v10_3v30@IO_HOST	0	275	mV	46.405	0.658	1,782	4.35	21.67924
652	Volh_iohost_1v80_3v30:Voh_iohost_1v80_3v30@IO_HOST	1.35	1.8	V	1.607	0.002	1,782	4.36	33.62708
653	Volh_iohost_1v80_3v30:Vol_iohost_1v80_3v30@IO_HOST	0	450	mV	43.370	0.543	1,782	4.07	25.32131
700	Volh_iosim_1v10_1v65:Voh_iosim_1v10_1v65@IO_SIM	1.23	1.65	V	1.448	0.002	1,782	4.16	34.62146
701	Volh_iosim_1v10_1v65:Vol_iosim_1v10_1v65@IO_SIM	0	200	mV	36.955	0.435	1,782	4.56	25.81318
720	Volh_iosim_1v10_3v30:Voh_iosim_1v10_3v30@IO_SIM	2.46	3.3	V	3.102	0.002	1,782	5.26	33.97235
721	Volh_iosim_1v10_3v30:Vol_iosim_1v10_3v30@IO_SIM	0	275	mV	36.117	0.444	1,782	4.41	24.97619
740	Volh_clksim_1v10_1v65:Voh_clksim_1v10_1v65@CLK_SIM	1.23	1.65	V	1.610	0.001	1,782	5.39	20.80342
741	Volh_clksim_1v10_1v65:Vol_clksim_1v10_1v65@CLK_SIM	0	200	mV	36.841	0.419	1,782	4.91	27.11871
742	Volh_clksim_1v10_3v30:Voh_clksim_1v10_3v30@CLK_SIM	3.25	3.3	V	3.261	0.001	1,782	4.71	4.417111
743	Volh_clksim_1v10_3v30:Vol_clksim_1v10_3v30@CLK_SIM	0	275	mV	35.867	0.418	1,782	4.09	25.84746
500	Resister_pullup_down:R_pullup_IO_HOST@IO_HOST	17	26	kOHM	19.245	0.118	1,782	4.94	4.273891
501	Resister_pullup_down:R_pullup_IO_SIM@IO_SIM	18	26	kOHM	19.871	0.136	1,782	4.58	3.260796
502	Resister_pullup_down:R_pulldown_RST_HOST@RST_HOST	60	130	kOHM	87.102	1.514	1,782	5.04	5.691657
503	Resister_pullup_down:R_pulldown_CLK_HOST@CLK_HOST	60	140	kOHM	87.300	1.495	1,782	5.06	6.117008

- ## NXP PQ label

Below, the PQ label is shown that will be fixed on the reel, the bag and the plano box.

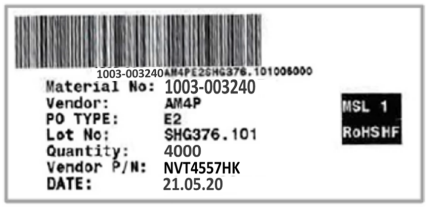


Note: The linear barcodes and the 2D matrix in the example labels are not drawn to scale and do not show relevant data.

NXP Semiconductors

- ## Customized label for Samsung Mobile (example purpose)

: Customer label (Level 2&3) : Paste on PQ box and dry pack by storekeeper



: Customer label (Level 1) : Paste on shipping carton by storekeeper

Below, the Samsung customized label is shown that will be fixed on the bag and the box.

Aluminum bag	Inner Box	Outer Box
		

□ **작업 환경 유해 물질 기준 및 시험 결과**

접착제(본드, 테이프 등), 러버, 가죽, 도료, 플라스틱 등의 원재료 또는 공정에 사용된 화학 물질에는 벤젠, 톨루엔, 포름알데히드, 포스핀(적인)등 VOC 물질이 발생 할 수 있으므로 아래 관리 기준을 준수합니다.

기준 1: 벤젠, 톨루엔, 포름알데히드, 포스핀(적인) 물질이 사용되지 않았습니다.(**Yes**, No)
기준 2: 위 4 가지 물질을 원재료 또는 공정상에 사용하였으나 표1-1 기준으로 관리합니다
(Product content data(MSDS data) 참고 요망)

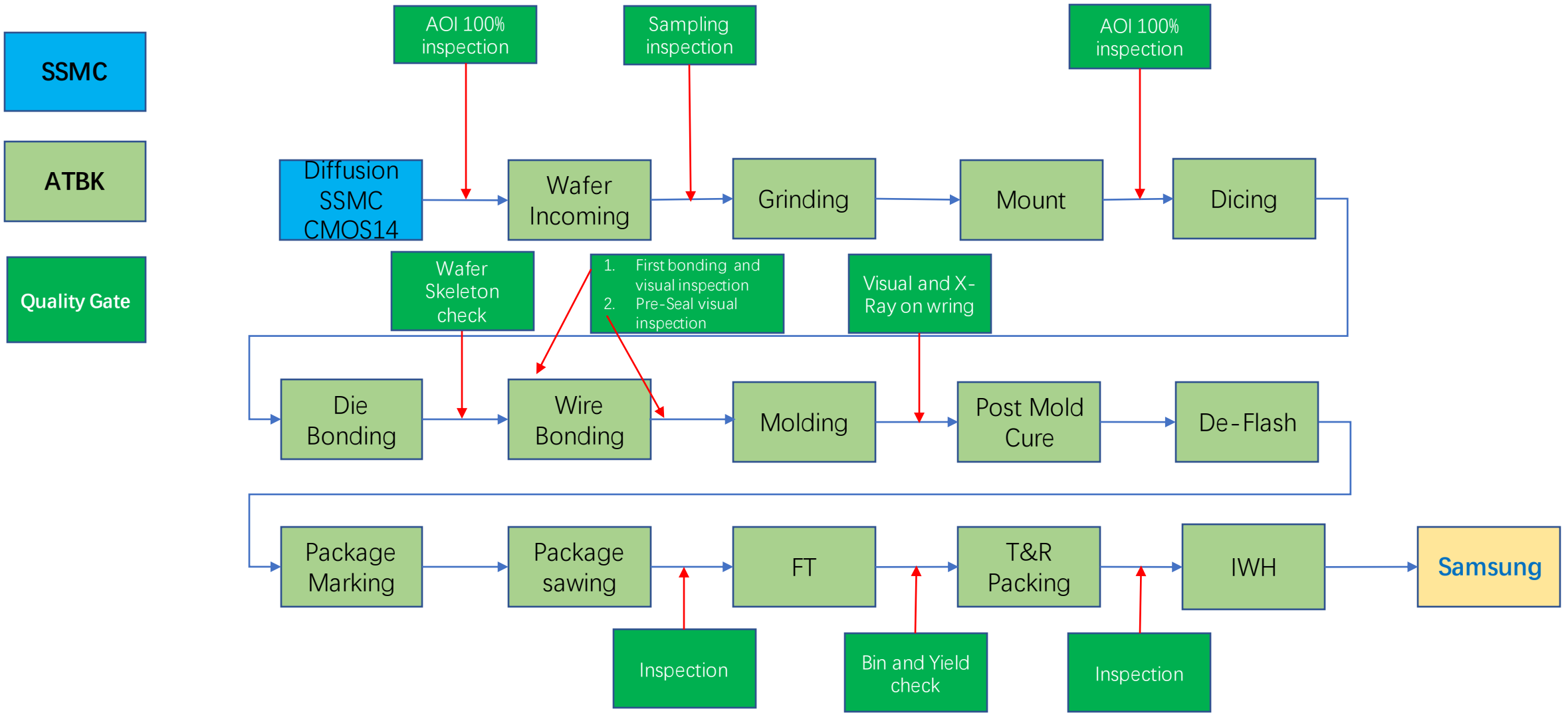
구분	측정항목	Spec (ppm)	결과
작업환경 유해물질	톨루엔	16.0	-
	벤젠	0.8	-
	포름알데히드	0.08	-
	포스핀(케이블류 한정)	0.08	-
측정 설비	ex) 측정 장비 : Mini RAE , Gastek 검지관 , GC/MS		
측정 조건	수량 : F-PCB XX 개		
	Gas Sampling 조건 기술 : 40℃ × 30min 방출 후 25cm × 30cm 지퍼백 포집		
MSDS	위 4 가지 물질 사용 자재의 MSDS 첨부 (첨부 파일 참고) ex) 1. 접착제 ex) 2. 보호비닐		

[표 1-1]

※ VOC (Volatile Organic Compounds): 휘발성 유기화합물

Quality Control In Production

- Detailed process flow NVT4557HK



Remark: This product flow updated as July16, 2021 as being under safelauch program

SMD DATA (승인원용)

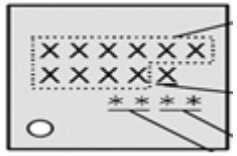
* SEC 코드:1003-003240, 업체 P/N:NVT4557HK

실물 사진 (부품 상, 하면)

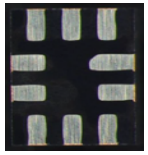
극성 관리 필요 유무

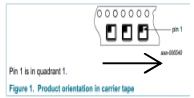
실물 사진 (Reel 담긴 사진, 부품3ea 이상)

1. 고정으로 기재되는 부품 마킹 정보



항 목	문자 or 숫자
고정 마킹 정보	57

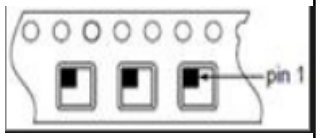




극성이 필요한 경우

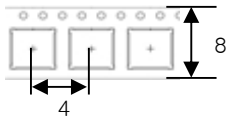
X

무극성



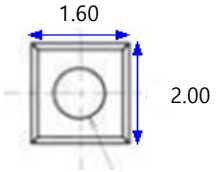
2. Carrier Width, Pitch

항 목	치수(㎜)
Width	8
Pitch	4
POCKET 재질	EMBOSS / PAPER



3. 포켓 사이즈

항 목	치수(㎜)
L	1.60
W	2.00

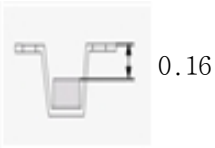


4. Cover tape / carrier 제전처리 및 접합 방식

항 목	기준 (100V)
Cover tape 내측	1*10^4 ~ 1*10^10 Ω 이하
Carrier tape	1*10^4 ~ 1*10^9 Ω 이하
Reel	Low Charging (Anti-static coated)
접합 방식	열 압착방식

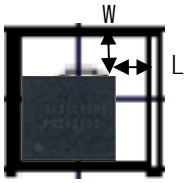
5. Carrier / Tray Height

항 목	치수(㎜)
Nozzle 흡착깊이	0.16
부품 T 값(TYP)	0.45
Carrier Height	0.61
TRAY Height	-

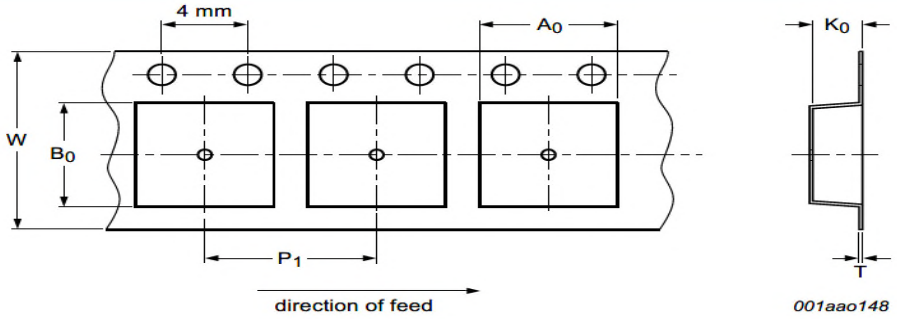


6. Carrier 내부와 부품간의 GAP

항 목	치수(㎜)
L	0.2
W	0.2



※ 첨부 도면(TAPE or TRAY) 선명하게



Not drawn to scale.

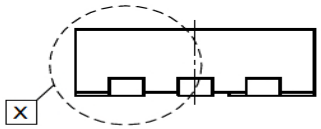
Figure 2. Carrier tape dimensions

In accordance with IEC 60286-3/EIA-481.

A_0 (mm)	B_0 (mm)	K_0 (mm)	T (mm)	P_1 (mm)	W (mm)
1.60±0.03	2.00±0.03	0.61±0.05	0.25±0.03	4.00±0.10	8.00±0.10

※ 첨부 도면 (부품, TOP & SIDE & BOT) 선명하게

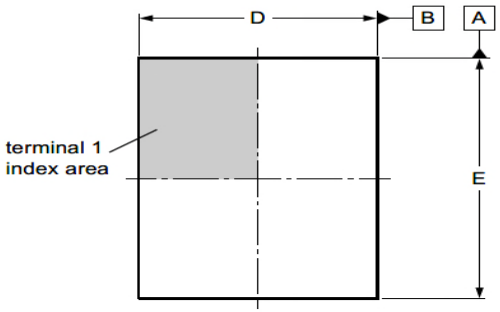
XQFN10: plastic, extremely thin quad flat package; no leads;
10 terminals; body 1.40 x 1.80 x 0.50 mm **SOT1160-1**

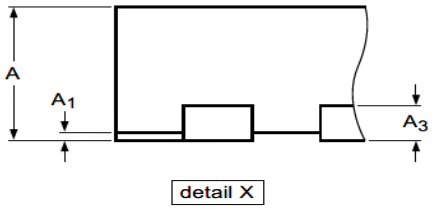


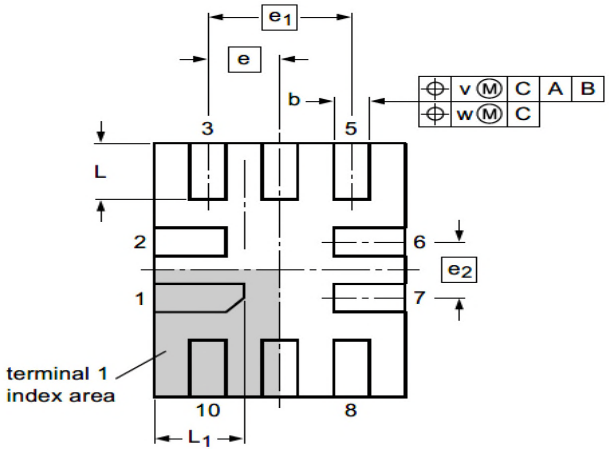
Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

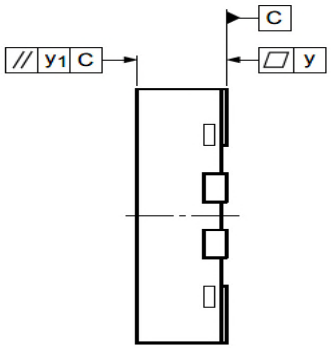
sot1160-1_po

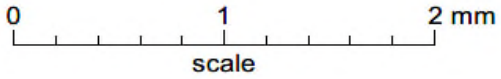
Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1160-1	---	---	---		~~09-12-29~~ 21-01-26











Dimensions

Unit(1)		A	A_1	A_3	b	D	E	e	e_1	e_2	L	L_1	v	w	y	y_1
	max	0.50	0.05		0.25	1.5	1.9				0.45	0.55				
mm	nom	0.45		0.127	0.20	1.4	1.8	0.4	0.8	0.4	0.40	0.50	0.1	0.05	0.05	0.05
	min	0.40	0.00		0.15	1.3	1.7				0.35	0.45				