DSPA56371 Software User's Manual for Audio SA

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Section 1
Introduction

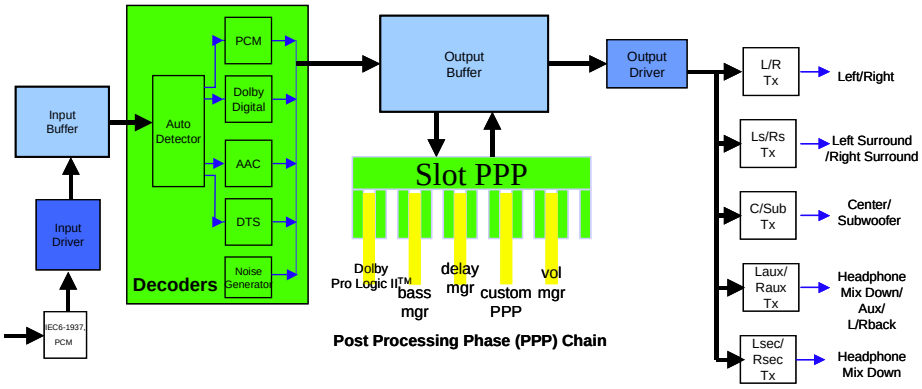
1.1 FEATURE AND ARCHITECTURE

DSP56371A is the name of the audio decoding product, a Digital Signal Processor (DSP) which is used in applications such as AV receivers, DVD players, set-top boxes, and minisystems. Within the architecture, the High-Level Executive (HLX), Low-Level Executives (LLX), Post-Processing Phases (PPP), and Input/Output are four independent, but related, components, which are shown in Figure 1-1. The HLX administers and presides over the Software Architecture (SA), controlling the coordination of the other components. The LLX controls the decoders for the different standard input bit-stream formats. DSP56371A supports PCM, AC3, AAC, and DTS. The capabilities of LLX are outlined briefly below:

All LLX support multi-channel output for subsequent 10-channel post processing and possible output, although not all HLXs support 10-channel outputs.

- The AAC LLX supports decoding of AAC-formatted input bit streams presented in IEC format.
- The AC-3 LLX supports decoding of Dolby-Digital-formatted input bit streams presented in IEC format.
- The DTS LLX supports decoding of Digital-Theater-Sound-formatted input bit streams presented in IEC and CD-DA format.
- The Auto LLX supports decoding of PCM bit streams delivered in IEC 61937 format along with automatic detection of encoded bit streams. The PCM LLX provides related functionality without automatic detection capabilities.

The PPP provides additional operation to satisfy customers with various sound effects. Every system has the option to allow customers to insert their own PPP program. The PPP component of the SA allows customers to add various sound-processing algorithms to perform functions such as graphic EQ, soundfields, bass / treble control, and even karaoke. There are numerous PPPs readily available from the Motorola PPP software library, and customers can even create their own PPPs with minimal training.



Software Architecture Data Flow

Figure 1-1 The Architecture of DSP56371A

1.2 USER MANUAL STRUCTURE

The DSP56371A Software User Manual (SUM) describes the system functionality and lists the important Chirp commands to check the running status and adjust the system configuration. Section 1 is an introduction that gives customers a brief overview of the SA. Section 2 describes the High-Level Executive, and Section 3 describes the Low-Level Executives and gives the common behaviors as well as their separate functions. Section 4 is a description of each of the standard Post Processing Phases. Section 5 is a description of the I/O part. Furthermore, customers can look up the DSP56371A system free memory maps and GPIO usage in the appendix. See Appendix C for examples of initializing different HLXs.

Section 2
High-Level Executive

2.1 OVERVIEW

All HLX of the DSP56371A provide for multi-channel decoding and post processing of input bit streams, as well as noise generation. Each HLX may be classified as an "8-channel" HLX. The HLX provides 8-channel decoding capabilities via decoders (LLX) such as Dolby Digital and matrix decoders (PPP) such as Dolby Pro Logic II. 10 output buffers are provided for post processing of data in all HLX except Blue, but only 8 of these are used for post processing of the main audio stream directly. The other channels remain free for other purposes, such as providing an additional stereo output for headphones or some other purpose. The Volume Manager engages the Master Volume Control Register and the Tracking Volume Control Register for only these 8 channels and not the other channels, thus establishing volume control zones as appropriate for 8-channel processing. All HLX utilize 8-channel Subwoofer Management. The HLX may provide 8 channels of rate doubling; 8 channels of data are output via the ESAI peripheral. All HLX provide detection capabilities for many kinds of bit streams input via the ESAI peripheral in various formats including PCM, Dolby Digital, DTS, and AAC. The following bit-stream formats are recognized: IEC 60958, IEC 61937, DTS CD-DA 14-bit format and DTS CD-DA 16-bit format. In the case where a type of bit-stream encoding is not recognized, that bit stream will be processed as PCM. In the case where a bit-stream encoding is recognized and detected but decoding capabilities are not provided, the output will be muted.

Each HLX may be classified as a 48 kHz HLX, a 96 kHz HLX, or a 96 kHz rate-doubling HLX. A 48 kHz HLX can process all forms of input correctly and output data at that rate, except in the case of a 96 kHz PCM input that cannot be processed correctly because the delay requirements cannot be met. A 96 kHz HLX is similar to a 48 kHz HLX except that a 96 kHz PCM input can be processed correctly—delay requirements can be met even for a 96 kHz PCM input. A 96 kHz rate-doubling HLX allows, in addition to the capabilities provided by a 96 kHz HLX, the generation of 96 kHz output from 48 kHz input and the generation of 88.2 kHz output from a 44.1 kHz input.

All HLX provide Dolby Pro Logic II matrix decoding but may provide other forms of matrix decoding as well, e.g., from DTS. All HLX provide a comprehensive Volume Control System via a collection of firmware components.

An HLX is established for activation via a standard initialization sequence that establishes default values for jump table entries and control registers, examples of which may be found in Appendix C. This initialization sequence can be altered to create variants of the standard HLX described below as desired by the customer. Any perceived deficiency in the default values of various registers or components included with the standard HLX can be corrected in this manner. These standard HLX, then, should be taken not as hard-and-fast feature sets but as possible starting points for building a system with the desired set of capabilities and balance of ROM-based *vs*. customer-supplied features as needed for any particular application.

2.2 HLX MODELS

HLX in DSP56371A refers to three models: Red, Blue and Green HLX. The following table indicates their basic features and differences.

Table 2-1 HLX in 56371A

HLX	Decoder	Ch	SWM	Delay	48/96	Secondary PCM DAX	PPP
Red	PCM AC3 Noise generator	10	7.1	C 5ms LS 15ms RS 15ms LB 15ms RB 15 ms	96k	Secondary PCM DAX	Reserved De-emphasis Secondary L/R Pro Logic 2 LFE Attenuate SurroundEX SWM Delay Manager Volume Manager Digital Gain
Blue	PCM AC3 DTS ES Discrete 6.1 Matrix 6.1 Noise generator	8	7.1	Disabled by default Delay buffers arrangement for Blue: C 5ms LS 15ms RS 15ms LB 15ms	48k	DAX	Reserved De-emphasis Pro Logic 2 DTS Logic (NEO6) LFE Attenuate Surround EX DTS Matrix6.1 SWM Delay Manager Volume Manager Digital Gain
Green	PCM AC3 DTS ES Discrete 6.1 Matrix 6.1 96/24 AAC Noise generator	10	7.1	L 5ms R 5ms C 5ms SW 5ms LS 15ms RS 15ms LB 15ms RB 15ms	96k Rate-Doubling	DAX	DoubleRate0 Reserved De-emphasis Pro Logic 2 DTS Logic (NEO6) LFE Attenuate Surround EX DTS Matrix 6.1 SWM Delay Manager Volume Manager Digital Gain DoubleRate1

Red HLX

The Red HLX of DSP56371A provides multi-channel decoding and post processing of PCM and Dolby Digital bit streams, as well as noise generation.

The Red HLX provides 8-channel decoding capabilities via decoders and matrix decoders. Ten output buffers are provided for post processing of data; however, only 8 of these are used for post processing of the main audio stream directly—the Volume Manager engages the Master Volume Control Register and the Tracking Volume Control Register for only these 8 channels; furthermore it utilizes 8-channel Subwoofer Management. The Red HLX does not provide rate doubling.

The Red HLX provides detection capabilities for all forms of bit streams input via the ESAI in IEC or DTS CD-DA format but decoding capabilities for only PCM and Dolby Digital. The Red HLX provides Dolby (Pro Logic II) matrix decoding for 2-channel input and Surround EX decoding for multi-channel input. It supports a DAX Data Stream Output from the Secondary Channels and generation of Secondary Left/Right Channel output by mixing data from the first six channels. The Red HLX provides Delay Management for the five Channels and supports 96 kHz PCM input, and thus the Red HLX is a 96 kHz HLX.

The internal memory usage of this HLX is described in Appendix A.

Blue HLX

The Blue HLX of DSP56371A provides for multi-channel decoding and post processing of PCM, Dolby Digital, and DTS bit streams, as well as noise generation.

The Blue HLX provides 8-channel decoding capabilities via decoders and matrix decoders. 8 output buffers are provided for post processing of data, which are used for post processing of the main audio stream directly—the Volume Manager engages the Master Volume Control Register and the Tracking Volume Control Register for these 8 channels. The Blue HLX utilizes 8-channel Subwoofer Management. It does not provide rate doubling.

The Blue HLX provides detection capabilities for all forms of bit streams input via the ESAI in IEC or DTS CD-DA format and decoding capabilities for PCM, Dolby Digital, and DTS. The Blue HLX provides both Dolby (Pro Logic II) and DTS (Neo:6) matrix decoding for 2-channel input and DTS-ES matrix and Surround EX decoding for multi-channel input. It is also able to support the Dolby Headphone and Dolby Virtual Speaker algorithms via downloadable custom PPPs.

The Blue HLX disables the Delay Management by default, although the user can enable Delay Management manually. Blue HLX provides 4 channels delay capability. It is a 48 kHz HLX. The internal memory usage of this HLX is described in Appendix A.

Green HLX

The Green HLX of DSP56371A provides for multi-channel decoding and post processing of PCM, Dolby Digital, DTS, and AAC bit streams, as well as noise generation.

The Green HLX provides 8-channel decoding capabilities via decoders and matrix decoders. Ten output buffers are provided for post processing of data; however, eight of these are used for post processing of the main audio stream directly—The Volume Manager engages the Master Volume Control Register and the Tracking Volume Control Register for only these eight channels. The Green HLX utilizes 8-channel Subwoofer Management. Furthermore, it provides 10-channel rate doubling and 10-channel output.

The Green HLX provides detection capabilities for all forms of bit streams input via the ESAI in IEC or DTS CD-DA format and decoding capabilities for PCM, Dolby Digital, DTS and AAC. The Green HLX provides

both Dolby (Pro Logic II) and DTS (Neo:6) matrix decoding for 2-channel input, and DTS-ES matrix and Surround EX decoding for multi-channel input. It can also support DTS 96/24 decoding.

The Green HLX provides 8-channel Delay Management. The delay capabilities of the Green HLX support 96 kHz PCM input as well as 96 kHz audio produced by a rate-doubling decoder, and this is a 96 kHz rate-doubling HLX. The internal memory usage of this HLX is described in Appendix A.

Omega HLX, Omega/SPI3

The Omega/SPI HLX provides Chirp/SPI3 and Crimp processing. Crimp provides capabilities that allow Chirp opcodes to be processed from within user code executing on the DSP56371.

Two-word Chirp Type II and Type III Write opcodes can be processed using the RunCrimpA10 entry point, as shown below.

One-word Chirp Type IV and Type V Write opcodes and Type II–V Read opcodes can be processed using the RunCrimpA1 entry point, as shown below.

Type 0 Chirp Write and Read opcodes can be processed using the RunCrimpA10 and RunCrimpA1 entry points for Chirp Type II Write and Read opcodes. Multi-word Type I Chirp opcodes cannot be processed using the Crimp facility.

Table 2-2 Crimp Processing Entry

Chirp Type	Number of Words	Read/Write	Run Crimp Entry
II III	2	Write	RunCrimp A10
IV V	1	Write	RunCrimp A1
II-V	1	Read	RunCrimp A1
0	Any	Read/Write	RunCrimpA10 RunCrimp A1
I	Any	Read/Write	N/A

Crimp Type II/III Write Example

```
move    #setHLXSpeakerFront,a1
move    #setHLXSpeakerFrontDefault,a0
jsr     RunCrimpA10; process 2-word write opcode
```

Crimp Type IV/V Write Example

```
move    #setHLXSourceModePCM,a1
jsr     RunCrimpA1;process 1-word write opcode
```

Crimp Type II–V Read Example

```
move    #getHLXStatusSourceModePCM,a1
jsr     RunCrimpA1; process read opcode
move    a1, x:value; save result
```

Omega/I2C

The Omega / I^2C HLX provides Chirp / I^2C and Crimp processing capabilities.

Omega/I2C'

The Omega / I^2C HLX provides Chirp / I^2C and Crimp processing capabilities. Chirp / I^2C processing capabilities are the same as Chirp / SPI commands except that the SHI peripheral used to transmit the commands is in I^2C rather than SPI mode.

2.3 HLX CONTROL FUNCTION

2.3.1 System error number status

The ERRNO Status Register is written and read using the opcodes shown below. The Error Number Register reflects any error types that may occur while the system is running or if there has been a system reboot. The Error PC Register records the Program Counter value when an illegal instruction is encountered.

Table 2-3 System Symbolic Opcodes

Symbol	Description	Value
setERRNO	Set error number register value	0xc20100
getERRNO	Report error number register value.	0x820100
ERRNO_ROMReset	System boot	$000000
ERRNO_RAMReset	Hardware RESET	$000001
ERRNO_StackError	Stack Error	$000002
ERRNO_IllegalInstruction	Illegal Instruction	$000003
ERRNO_DebugRequest	Debug Request	$000004
ERRNO_Trap	Trap	$000005
ERRNO_NMI	Non Maskable Interrupt	$000006
setERRPC	Set error PC register value.	0xc20101
getERRPC	Report error PC register value.	0x820101

Note: Anytime a "get***" command is used, the user must follow this command with a subsequent 24-bit zero word; this is to flush out the SPI register in the DSP, e.g., getERRNO = cmd 820100 000000.

2.3.2 Mute Processing

Non-Omega HLX provide mute processing via HLX commands, a control register, a status register, a logical GPIO input pin and a logical GPIO output pin. The actual realization of this mute processing capability relies, however, on the mapping of the logical GPIO pins to physical signals for DSP56371A.

With the LOCK* and MUTE* logical GPIO pins not connected to physical pins as per the physical-to-logical GPIO mapping provided in these GPIO Models, mute processing capabilities are not provided. In this case, the mute processing operations have no effect on the rest of the system. Details on the GPIO mapping modes available can be viewed in Appendix B.

Table 2-4 Mute Processing Symbolic Opcodes

Symbol	Description	Value
setHLXConfigMuteOff	MUTE* is low (Unmute)	0xe00406
setHLXConfigMuteOn	MUTE* is high (Mute)	0xe00407
setHLXUnmuteBlockLimit_0	Set number of blocks by which to delay unmute	0xe02500
getHLXStatusMute	Get mute status -- non-zero indicates that mute is active	0xa02300
getHLXUnmuteBlockLimit	Get number of blocks by which to delay unmute	0xa02500
getHLXUnmuteBlockCount	Get delay unmute count	0xa02600

2.3.3 Source Mode Support

DSP56371A supports 6 source modes: Auto, PCM, AC3, DTS, AAC and Noise Generator. Auto mode will set the HLX to auto-detection. The others are available so that customers can force LLX to decode according to a specific source; in most cases Auto mode is recommended.

Table 2-5 Source Mode Control Symbolic Opcodes

Symbol	Description	Value
setHLXSourceModeAuto	Set control register value.	0xe00900
setHLXSourceModeNoise		0xe00901
setHLXSourceModePCM		0xe00902
setHLXSourceModeAC3		0xe00903
setHLXSourceModeDTS		0xe00904
setHLXSourceModeAAC		0xe00908
getHLXSourceMode	Report control register value.	0xa00900

Table 2-6 Source Mode Control Checking Symbolic Opcodes

Symbol	Description	Value
getHLXStatusSourceMode	Report source mode status register	0xa02100
gotHLXStatusSourceModeAuto	The values corresponding to source modes.	0x000000
gotHLXStatusSourceModeNoise		0x000001
gotHLXStatusSourceModePCM		0x000002
gotHLXStatusSourceModeAC3		0x000003
gotHLXStatusSourceModeDTS		0x000004
gotHLXStatusSourceModeAAC		0x000008

2.3.4 Listening Mode Support

There are six listening modes: Lt/Rt, Mono, Stereo, Phantom, 3-Stereo and Surround. The DSP56371A controls speaker count in front and rear (Audio Mode), compression mode and dynamic range. Note that if confliction happens between the Listening Mode Control Register and the Speaker Control Register listed below, then the listening mode control is subject to what speakers are available via the speaker control, e.g., you will not be able to listen to full surround mode if only the Left and Right speakers are available (provided speaker control is enabled).

Table 2-7 Listening Mode Control Symbolic Opcodes

Symbol	Description	Value
setHLXListeningModeProLogic	Set control register value.	0xe00a00
setHLXListeningModeMono		0xe00a01
setHLXListeningModeStereo		0xe00a02
setHLXListeningModePhantom		0xe00a03
setHLXListeningMode3Stereo		0xe00a04
setHLXListeningModeSurround		0xe00a05
getHLXListeningMode	Report control register value.	0xa00a00

2.3.5 Speaker Control Support

In the DSP56371A, the speaker controls opcodes will be applied to create downmix and output configuration, if enabled.

Table 2-8 Speaker Control Symbolic Opcodes

Symbol	Description	Value
setHLXSpeakerControlEnable	Enable or disable speaker control.	0xe00d01
setHLXSpeakerControlDisable		0xe00d00
setHLXSpeakerSubwooferNone	Set the attributes of Left, Right, Center, Surround, Back and Subwoofer speaker respectively.	0xe00e00
setHLXSpeakerSubwooferWide1		0xe00e11
setHLXSpeakerLeftRightNarrow2		0xe01102
setHLXSpeakerLeftRightWide2		0xe01112
setHLXSpeakerCenterNone		0xe01200
setHLXSpeakerCenterNarrow1		0xe01201
setHLXSpeakerCenterWide1		0xe01211
setHLXSpeakerSurroundNone		0xe01300
setHLXSpeakerSurroundNarrow1		0xe01301
setHLXSpeakerSurroundNarrow2		0xe01302
setHLXSpeakerSurroundWide1		0xe01311
setHLXSpeakerSurroundWide2		0xe01312
setHLXSpeakerBackNone		0xe00f00
setHLXSpeakerBackNarrow1		0xe00f01
setHLXSpeakerBackNarrow2		0xe00f02
setHLXSpeakerBackWide1		0xe00f11
setHLXSpeakerBackWide2		0xe00f12
GetHLXSpeakerControl	Get the attribute of Left, Right, Center, Surround, Back and Subwoofer speaker respectively.	0xa00d00
GetHLXSpeakerSubwoofer		0xa00e00
GetHLXSpeakerBack		0xa00f00
GetHLXSpeakerLeftRight		0xa01100
GetHLXSpeakerCenter		0xa01200
GetHLXSpeakerSurround		0xa01300

2.3.6 Audio Mode Support

When speaker control is disabled, customers can directly define the suitable audio mode in the LLX downmix control register. The MLX (Medium Level Executive) audio mode status register reflects this setting.

Table 2-9 Audio Mode Control and Status Symbolic Opcodes

Symbol	Description	Value
setLLXDownmix	Set downmix directly when speaker control is disabled.	0xc80803
setLLXDownmixProLogic		0xe20c00
setLLXDownmixMono		0xe20c01
setLLXDownmixStereo		0xe20c02
setLLXDownmixStereo3		0xe20c03
setLLXDownmixPhantom		0xe20c06
setLLXDownmixSurround		0xe20c07
setLLXDownmixPhantom1		0xe20c04
setLLXDownmixSurround1		0xe20c05
setLLXDownmixMono2		0xe20c08
setLLXDownmixStereoUnknown		0xe20c09
setLLXDownmixPhantom3		0xe20c0c
setLLXDownmixSurround3		0xe20c0d
setLLXDownmixPhantom4		0xe20c0e
setLLXDownmixSurround4		0xe20c0f
	Set corresponding audio mode with subwoofer.	0xe20c1X (0…f)
getLLXDownmix	Reports audio mode at LLX (The definition of the return value is the same as MLX audio mode register)	0x880803
getMLXAudioMode	Reports audio mode at output.	0x880403
gotMLXAudioModeProLogic	0/0: 2 front and 0 rear speakers	0x000000
gotMLXAudioModeMono	1/0: 1 front and 0 rear speakers	0x000001
gotMLXAudioModeStereo	2/0: 2 front and 0 rear speakers	0x000002
gotMLXAudioModeStereo3	3/0: 3 front and 0 rear speakers	0x000003
gotMLXAudioModePhantom1	2/1: 2 front and 1 rear speakers	0x000004
gotMLXAudioModeSurround1	3/1: 3 front and 1 rear speakers	0x000005
gotMLXAudioModePhantom	2/2: 2 front and 2 rear speakers	0x000006
gotMLXAudioModeSurround	3/2: 3 front and 2 rear speakers	0x000007
gotMLXAudioModeMonoOnLR	1/0: 1 front and 0 rear speakers	0x000008
gotMLXAudioModeStereoUnknown	2/0: 2 front and 0 rear speakers	0x000009
gotMLXAudioModeMonoMono	2/0: 2 front and 0 rear speakers	0x00000a
gotMLXAudioMode_b	0: without anything	0x00000b
gotMLXAudioModePhantom3	2/3: 2 front and 3 rear speakers	0x00000c

Table 2-9 Audio Mode Control and Status Symbolic Opcodes (Continued)

Symbol	Description	Value
gotMLXAudioModeSurround3	3/3: 3 front and 3 rear speakers	0x00000d
gotMLXAudioModePhantom4	2/4: 2 front and 4 rear speakers	0x00000e
gotMLXAudioModeSurround4	3/4: 3 front and 4 rear speakers	0x00000f
gotBitMLXAudioModeBass	1:1 subwoofer	0x000010

2.3.7 Listening Format and Program Format Support

The DSP56371A abstracts Listening Format information from the MLX audio mode status to show the currently working channels. This reflects the current output of the LLX and may be different from the Program format which is a description of the currently available channels at the input.

Table 2-10 Program Format Status Symbolic Opcodes

Symbol	Description	Value
getHLXStatusProgramFormat	Report program format.	0x880006
gotBitLeft	Value reflecting the working channel at input.	0x000001
gotBitRght		0x000002
gotBitLSur		0x000004
gotBitRSur		0x000008
gotBitCntr		0x000010
gotBitSubw		0x000020
gotBitLAux		0x000040
gotBitRAux		0x000080
gotBitLSec		0x000100
gotBitRSec		0x000200
gotBitSSur	Report Single Surround channel (Ls) at Input	0x010000
gotBitStatusProgramFormatNotSurround	Report No surround channel encoded at in input bitstream	0x020000
gotBitStatusProgramFormatYesSurround	Report surround channel encoded at input bitstream	0x040000
gotBitStatusProgramFormatDualMono	Report Mono on L R channels at input bitstream	0x080000
gotBitLFE	Report LFE channel exists at input bitstream	0x100000
gotBitValidAudioMode	Report Input bitstream Audio mode is supported.	0x800000

Table 2-11 Listening Format Status Symbolic Opcodes

Symbol	Description	Value
getHLXStatusListeningFormat	Report listening format.	0x880007
gotBitLeft	Value reflecting the working channel at output.	0x000001
gotBitRght		0x000002
gotBitLSur		0x000004
gotBitRSur		0x000008
gotBitCntr		0x000010
gotBitSubw		0x000020
gotBitLAux		0x000040
gotBitRAux		0x000080
gotBitLSec		0x000100
gotBitRSec		0x000200
gotBitSSur		0x010000
GotBitHLXStatusListeningFormatProLogic	Pro Logic or NEO6 is working	0x400000

2.3.8 Free MIPS Report

DSP56371A can display minimum free MIPS count over interval following two chirp commands, setHLXConfigFreeMIPS, and next, getHLXStatusFreeMIPS shown at the below table.

Note that the MIPS counter may not always be accurate enough to provide reliable information; it is recommended that a back-up method be used, in which the available MIPS (via the PLL control register) be reduced until distortion occurs.

Table 2-12 Free MIPS Symbolic Opcodes

Symbol	Description	Value
setHLXConfigFreeMIPS	Set free MIPS config.	0xe00408
getHLXStatusFreeMIPS	Report free MIPS	0xa02200

2.3.9 Sample Rate Support

Support for processing at various input and output sample rates varies across HLX in DSP56371A. In this respect, the DSP56371A HLX can be broken into two distinct sets, non-rate-doubling HLX and rate-doubling HLX. The non-rate-doubling HLX are Red and Blue, and the rate-doubling HLX is Green. The support for processing at various input and output sample rates is summarized separately for the non-rate-doubling and rate-doubling HLX in DSP56371A in Table 2-13 and Table 2-14, respectively.

Table 2-13 Sample Rate Support in Non-Rate-Doubling HLX

Source	Rate Conversion Request Sample Rate			Sample Rate		
	LLX	PPP	DAX	Input	ESAI Output	DAX Output
PCM	1:1	1:1	1:1	48 kHz	48 kHz	48 kHz
				44.1 kHz	44.1 kHz	44.1 kHz
				32 kHz	32 kHz	32 kHz
				96 kHz	96 kHz	96 kHz
				88.2 kHz	88.2 kHz	88.2 kHz
			2:1	48 kHz	48 kHz	24 kHz
				44.1 kHz	44.1 kHz	22.05 kHz
				32 kHz	32 kHz	16 kHz
				96 kHz	96 kHz	48 kHz
				88.2 kHz	88.2 kHz	44.1kHz
Dolby Digital	1:1	1:1	1:1	48 kHz	48 kHz	48 kHz
				44.1 kHz	44.1 kHz	44.1 kHz
				32 kHz	32 kHz	32 kHz
			2:1	48 kHz	48 kHz	24 kHz
				44.1 kHz	44.1 kHz	22.05 kHz
				32 kHz	32 kHz	16 kHz
DTS	1:1	1:1	1:1	48 kHz	48 kHz	48 kHz
			2:1	44.1 kHz	44.1 kHz	44.1 kHz
				48 kHz	48 kHz	24 kHz
				44.1 kHz	44.1 kHz	22.05 kHz
AAC	1:1	1:1	1:1	48 kHz	48 kHz	48 kHz
			2:1	48 kHz	48 kHz	24 kHz

Table 2-14 Sample Rate Support in Rate-Doubling HLX

Source	Rate Conversion Request Sample Rate			Sample Rate		
	LLX	PPP	DAX	Input	ESAI Output	DAX Output
PCM	1:1	1:1	1:1	48 kHz	48 kHz	48 kHz
				44.1 kHz	44.1 kHz	44.1 kHz
				32 kHz	32 kHz	32 kHz
				96 kHz	96 kHz	96 kHz
				88.2 kHz	88.2 kHz	88.2 kHz
			2:1	48 kHz	48 kHz	24 kHz
				44.1 kHz	44.1 kHz	22.05 kHz
				32 kHz	32 kHz	16 kHz
				96 kHz	96 kHz	48 kHz
				88.2 kHz	88.2 kHz	44.1kHz
		1:2	1:1	48 kHz	96 kHz	96 kHz
				44.1 kHz	88.2 kHz	88.2 kHz
				32 kHz	64 kHz	64 kHz
				96 kHz	96 kHz	96 kHz
				88.2 kHz	88.2 kHz	88.2 kHz
			2:1	48 kHz	96 kHz	48 kHz
				44.1 kHz	88.2 kHz	44.1 kHz
				32 kHz	64 kHz	32 kHz
				96 kHz	96 kHz	96 kHz
				88.2 kHz	88.2 kHz	88.2 kHz
Dolby Digital	1:1	1:1	1:1	48 kHz	48 kHz	48 kHz
				44.1 kHz	44.1 kHz	44.1 kHz
				32 kHz	32 kHz	32 kHz
			2:1	48 kHz	48 kHz	24 kHz
				44.1 kHz	44.1 kHz	22.05 kHz
				32 kHz	32 kHz	16 kHz
		1:2	1:1	48 kHz	98 kHz	98 kHz
				44.1 kHz	88.2 kHz	88.2 kHz
				32 kHz	64 kHz	64 kHz
			2:1	48 kHz	98 kHz	48 kHz
				44.1 kHz	88.2 kHz	44.1 kHz
				32 kHz	64 kHz	32 kHz

Table 2-14 Sample Rate Support in Rate-Doubling HLX (Continued)

Source	Rate Conversion Request Sample Rate			Sample Rate		
	LLX	PPP	DAX	Input	ESAI Output	DAX Output
DTS	1:1	1:1	1:1	48 kHz	48 kHz	48 kHz
				44.1 kHz	44.1 kHz	44.1 kHz
			2:1	48 kHz	48 kHz	24 kHz
				44.1 kHz	44.1 kHz	22.05 kHz
		1:2	1:1	48 kHz	96 kHz	96 kHz
				44.1 kHz	88.2 kHz	88.2 kHz
			2:1	48 kHz	96 kHz	48 kHz
				44.1 kHz	88.2 kHz	44.1 kHz
	1:2	1:1	1:1	48 kHz	96 kHz	96 kHz
				44.1 kHz	88.2 kHz	88.2 kHz
			2:1	48 kHz	96 kHz	48 kHz
				44.1 kHz	88.2 kHz	44.1 kHz
AAC	1:1	1:1	1:1	48 kHz	48 kHz	48 kHz
			2:1	48 kHz	48 kHz	24 kHz
		1:2	1:1	48 kHz	96 kHz	96 kHz
			2:1	48 kHz	96 kHz	48 kHz

LLX encoded and decoded sample rate registers reflect the sample rates encoded in the bitstream for Dolby Digital, DTS and AAC bitstream.

DSP56371A reports the output sample rate via MLX sample rate register.

Note that the sample rate status will not be updated automatically if the input is PCM and should be set by the host microcontroller.

Table 2-15 Sample Rate Status Symbolic Opcodes

Symbol	Description	Value
getMLXSampleRate	Report the sample rate at the output of the system.	0x880402
gotMLXSampleRate48000Hz		0x000000
gotMLXSampleRate44100Hz		0x000001
gotMLXSampleRate32000Hz		0x000002
gotMLXSampleRate96000Hz		0x000003
gotMLXSampleRate88200Hz		0x000004

Table 2-15 Sample Rate Status Symbolic Opcodes

Symbol	Description	Value
getLLXStatusEncodedSampleRate	Report the sample rate of the bit stream at the input to the decoder.	0xa23300
getLLXStatusDecodedSampleRate	Report the sample rate of the bit stream at the output of the decoder.	0xa23700
SetMLXSampleRate48000Hz	Set the sample rate to 48kHz (valid for PCM only)	0xE21000
SetMLXSampleRate44100Hz	Set the sample rate to 44.1kHz (valid for PCM only)	0xE21001
SetMLXSampleRate32000Hz	Set the sample rate to 32kHz (valid for PCM only)	0xE21002
SetMLXSampleRate96000Hz	Set the sample rate to 96kHz (valid for PCM only)	0xE21003
SetMLXSampleRate88200Hz	Set the sample rate to 88.2kHz (valid for PCM only)	0xE21004

2.3.10 Audio Status Report

The MLX audio status register informs the DSP56371A of the following messages, as shown below.

Table 2-16 Audio Status Symbolic Opcodes

Symbol	Description	Value
getMLXAudioStatus	Report audio status at output	0x880404
gotBitMLXAudioStatusProLogic	Surround channel is formed by Prologic 2 or DTS Neo6	0x000001
gotBitMLXAudioStatusLFEPresent	LFE is generated by the LLX	0x000002
gotBitMLXAudioStatusEncodedKaraoke	Encoded Karaoke Status in input	0x000010
gotBitMLXAudioStatusEncodedSurround	Indicates surround channels encoded at input bitstream	0x000020
gotBitMLXAudioStatusDecodedSurround	Indicate decoder hasn't decoded the surround channels encoded in the input bitstream, Output channels are still surround encoded.	0x000040
gotBitMLXAudioStatusChangedSampleRate	Input and output sample rates differ	0x000080

2.3.11 Volume Control Support

In the DSP56371A, the Volume Control Register consists of three parts: VCR Track Volume, VCR Master Volume and VCR Channel Volume. The VCR Track Volume controls the maximum output power. Setting the VCR Master Volume causes changes in all the output channels. The VCR Channel Volume is in charge of each of the respective channels.

Each of the Volume Registers contains a 24-bit value that is interpreted as a gain in dB with a stepsize of 0.5dB. That is, the bit pattern $000000 represents 0dB, #000002 represents 1dB, $FFFFFF represents -0.5dB, etc.

Table 2-17 Volume Control Symbolic Opcodes

Symbol	Description	Value
setVCRTrack	Set VCR Track Volume	0xc80200
setVCRMaster	Set VCR Master Volume	0xc80201
setVCRLeft	Set VCR Channel Volume	0xc80202
setVCRRght		0xc80203
setVCRLSur		0xc80204
setVCRRSur		0xc80205
setVCRCntr		0xc80206
setVCRSubw		0xc80207
setVCRLAux		0xc80208
setVCRRAux		0xc80209
setVCRLSec		0xc8020a
setVCRRSec		0xc8020b
getVCRTrack	Report VCR Track Volume	0x880200
getVCRMaster	Report VCR Master Volume	0x880201
getVCRLeft	Report VCR Channel Volume	0x880202
getVCRRght		0x880203
getVCRLSur		0x880204
getVCRRSur		0x880205
getVCRCntr		0x880206
getVCRSubw		0x880207
getVCRLAux		0x880208
getVCRRAux		0x880209
getVCRLSec		0x88020a
getVCRRSec		0x88020b

2.3.12 Audio Generator Report

The DSP56371A can deal with up to six bit stream sources, depending on the HLX used. The MLX audio generator register reflects the type of decoder currently working.

Table 2-18 Audio Generator Symbolic Opcodes

Symbol	Description	Value
GetMLXAudioGen	Report audio generator	0x880405
Noise Generator	The value corresponding to the decoder type.	0x000001
PCM		0x000002
AC3		0x000003
DTS		0x000004
AAC		0x000008

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Section 3
Low-Level Executive

3.1 OVERVIEW

The DSP56371A provides 6 LLXs to customers: Noise Generator, Auto, PCM, AC3, DTS, and AAC. The customer can refer to Section 2, of the SUM for more details on each of these. The Capabilities of these LLX are described below.

3.2 GENERAL LLX

3.2.1 LLX Configuration

Table 3-1 LLX Configuration Symbolic Opcodes

Symbol	Description	Value
setLLXConfig	Set LLX config.	0xc80801
setLLXConfigNone	Restart LLX	0xe20400
getLLXConfig	Report LLX config.	0x880801

3.2.2 LLX Status

The LLX should update the LLX Status Register according to the different states that exist. These can be seen in Table 3-2. (x) in the table means LLX.

The output is muted (continuous zero output in some fashion) except when continuing normal or error operation.

Table 3-2 LLX Status Symbolic Opcodes

Symbol	Description	Value
getLLXStatus	Report LLX status	0x880800
gotLLXStatusInit	Loaded but not running. (x)	0x000000
gotLLXStatusSearch	Searching for sync. (x)	0x000001
gotLLXStatusDecode	Normal operation.	0x000002
gotLLXStatusPause	IEC 60958 pause. (x)	0x000003
gotLLXStatusError	Error but continuing.	0x000004
gotLLXStatusFail	Error and stopped (x), exit because of bit-stream error.	0x000005

Table 3-2 LLX Status Symbolic Opcodes

Symbol	Description	Value
gotLLXStatusDone	No error, and stopped. (x) Exit because of request or detect.	0x000006

3.2.3 Input Configuration

LLX Input Configuration Register is divided into 3 8-bit sub-registers: LSB – LLX Input Configuration Dual-Mono (dual-mono control), ISB – LLX Input Configuration Channel (driver channel control), and MSB – LLX Input Configuration Type (driver select). DSP56371A supports two ways to set LLX input configuration register, either at the same time, shown at Table 3-3 or respectively at Table 3-4, Table 3-5, and Table 3-6.

Table 3-3 LLX Input Configuration Symbolic Opcodes

Symbol	Description	Value
setLLXInputConfig	Set input config.	0xc80805
getLLXInputConfig	Report input config.	0x880805

LLX Input Configuration Dual-Mono setting

This register tells how the input channels are to be organized if the input format is dual mono.

Table 3-4 LLX Input Configuration Dual-Mono Symbolic Opcodes

Symbol	Description	Value
setLLXInputConfigDualMonoChanBoth	Left=Chan1, Right=Chan2	0xe21500
setLLXInputConfigDualMonoChanLeft	Center=Chan1	0xe21501
setLLXInputConfigDualMonoChanRght	Center=Chan2	0xe21502
setLLXInputConfigDualMonoChanSum	Center=(Chan1+Chan2)/2	0xe21503
getLLXInputConfigDualMono	Report Dual-Mono config.	0xa21500

LLX Input Configuration Channel setting

The register holds the IEC stream number for incoming bit-stream. This number can be any of 0-7 and tells to which bit-stream a data burst in IEC 60958 belongs.

Table 3-5 LLX Input Configuration Channel Symbolic Opcodes

Symbol	Description	Value
setLLXInputConfigChannel_0	Set input channel config.	0xe21600
getLLXInputConfigChannel	Report input channel config.	0xa21600
Channel 0	Corresponding value	0
Channel 1		1
Channel 2		2
Channel 3		3
Channel 4		4
Channel 5		5
Channel 6		6
Channel 7		7

LLX Input Configuration Type setting

The LLX input configuration type control register is checked in auto-detection routines to see whether auto-detection is desired or not. If set to auto, auto-detection will be enabled and output muted initially. If set to PCM, auto-detection will be disabled and output will not be muted initially. If initialized to other values, which is the case for PES where it is initialized earlier (finished in the Initialization of HLX), it is the responsibility of that user to also set the corresponding values in this register. That is, the auto-detection algorithm is setting the status in the LLX input status register; if not enabled, something else must take its role. In these cases, the LLX input status register gets more of a control role than a status role as shown below.

Table 3-6 LLX Input Configuration Type Symbolic Opcodes

Symbol	Description	Value
setLLXInputConfigTypeAuto	Auto configuration	0xe21700
setLLXInputConfigTypePCM	PCM configuration	0xe21701
setLLXInputConfigTypeIEC	IEC configuration (Reserve)	0xe21702
setLLXInputConfigTypePES	PES configuration (Reserve)	0xe21703
getLLXInputConfigType	Report configuration type	0xa21700

Note: The DSP56371A does not support any form of asynchronous input such as PES, PESCXD, ES, or ES-SPI.

3.2.4 Input Control and Status

The LLX Input Control Register is used to set the basic form of input bit-stream decoding that is to take place. The LLX Input Status Register is used in two, distinct ways depending upon whether the Auto LLX or another LLX is in use.

LLX Input Status Register With Auto LLX

In this case, the LLX Input Status Register is a status register from the view of the host. The Auto LLX sets this register according to the basic type of bit stream that is detected at the input. This result is used to initialize the LLX selected by the Auto LLX for subsequent processing of the bit-stream input. Note that a change in the form of the input bit-stream will, in general, cause a LLX to exit back to the Auto LLX for reacquisition. No LLX is equipped to automatically detect a change in the form of the input bit-stream and continue processing.

In this case, the LLX Input Status Register can be successfully used as an indicator of the basic type of bit stream that is detected at the input. Other information regarding the input bit stream beyond the basic type must be gleaned from the LLX itself as described elsewhere. The HLX Source Mode Status Register cannot be used when input bit streams can be detected that have no corresponding, operational source mode.

LLX Input Status Register Usage With Non-Auto LLX

In this case, the LLX Input Status Register is a control register from the view of the host. The host must set this register according to the basic type of bit stream that is expected at the input. This value is used to initialize the LLX selected by the host for processing of the bit-stream input. Note that a change in the form of the input bit-stream will, in general, cause an LLX to abort and attempt reacquisition. No LLX is equipped to automatically detect a change in the form of the input bit-stream and continue processing.

In this case, the LLX Input Status Register must be used to control the type of bit-stream input to the system. Other information regarding the input bit stream beyond the basic type must be gleaned from the LLX itself as described elsewhere.

LLX Input Status Register Setting

The LLX Input Status Register is divided into three 8-bit sub-registers, MSB – LLX Input Status Type (bit stream type), ISB – LLX Input Status Type Sub (bit-stream sub-type), and LSB – LLX Input Status Type Aux (bit-stream auxiliary), which are initialized respectively if auto-detection enabled: LLX Input Status Type - Unknown, LLX Input Status Type Sub - Unknown, and LLX Input Status Type Aux - Default. Then they are updated accordingly in the auto-detection algorithm (for IEC and PCM input streams) to the specific type that is indicated in the LLX Input Status Type. Bits 0-4 of preamble burst data word 3 is copied to LLX Input Status Type Sub if it's an IEC bit stream, and auxiliary information, if needed, is put in LLX Input Status Type Aux. Typically, auto-detection is only enabled for IEC and PCM bit streams; so, for PES input bit streams, these registers are set up earlier by the HLX. The operation on LLX input status register refers to Table 3-7, and configurations for all these registers together can be seen in Table 3-8.

Table 3-7 LLX Input Status Symbolic Opcodes

Symbol	Description	Value
setLLXInputStatus	Set input status	0xc80806
setLLXInputStatusTypeUnknown	Set input status type	0xe21b00
setLLXInputStatusTypePCM		0xe21b01
setLLXInputStatusTypeIEC		0xe21b02
setLLXInputStatusTypePES		0xe21b03
setLLXInputStatusTypePCMSubUnknown	Set input status sub-type	0xe21a00
setLLXInputStatusTypePCMSubAudio		0xe21a01
setLLXInputStatusTypePCMSubDTS		0xe21a02
setLLXInputStatusTypeIECSubNull		0xe21a00
setLLXInputStatusTypeIECSubAC3		0xe21a01
setLLXInputStatusTypeIECSubTimeStamp		0xe21a02
setLLXInputStatusTypeIECSubPause		0xe21a03
setLLXInputStatusTypeIECSubMPEG1L1		0xe21a04
setLLXInputStatusTypeIECSubMPEG2B		0xe21a05
setLLXInputStatusTypeIECSubMPEG2X		0xe21a06
setLLXInputStatusTypeIECSubMPEG2L1Lsr		0xe21a08
setLLXInputStatusTypeIECSubMPEG2L23Lsr		0xe21a09
setLLXInputStatusTypeIECSubDTSB		0xe21a0b
setLLXInputStatusTypeIECSubDTSC		0xe21a0c
setLLXInputStatusTypeIECSubDTSD		0xe21a0d
setLLXInputStatusTypePESSubUnknown		0xe21a00
setLLXInputStatusTypePESSubATSC		0xe21a01
setLLXInputStatusTypePESSubDVD		0xe21a02
setLLXInputStatusTypePESSubNoP		0xe21a03
getLLXInputStatus	Report input status	0x880806
getLLXInputStatusType	Report input status type	0xa21b00
getLLXInputStatusTypeSub	Report input status sub-type	0xa21a00

Note: The DSP56371A does not support any form of asynchronous input such as PES, PESCXD, ES, or ES-SPI.

Table 3-8 LLX Input Status Type, LLX Input Status Type Sub, and LLX Input Status Type Aux

LLX Input Status Type, LLX Input Status Type Sub, LLX Input Status Type Aux	LLX Input Status Type (hex. value)	LLX Input Status Type Sub (hex. value)	LLX Input Status Type Aux (hex. value)
Unknown, -, -	00	-	-
-, Unknown, -	-	00	-
-, -, Default	-	-	00
PCM, Audio, Default	01	01	00
PCM, DTS, 14b	01	02	01
PCM, DTS, 16b	01	02	02
IECNull	02	00	00
IECAC3	02	01	00
IECTimeStamp	02	02	00
IECPause	02	03	00
IECMPEG1L1	02	04	00
IECMPEG2B	02	05	00
IECMPEG2X	02	06	00
IECAAC	02	07	00
IECMPEG2L1Lsr	02	08	00

3.2.5 LLX Downmix Control

The LLX downmix control register is able to directly decide the audio mode in the system when the speaker control is disabled; otherwise, it is immediately overwritten by the speaker control register. Its content is listed in Table 2-9.

3.2.6 LLX Encoded and Decoded Status

The LLX Encoded and Decoded Status Registers provide information about the input to and output from the decoder, respectively. The LLX Encoded Status Registers provide information about the bit-stream input for decoding by the LLX. The LLX Decoded Status Registers provide information about the results of that decoding by the LLX, and, thus, also describes the data that is passed from the LLX to the post-processing chain.

There are three LLX Encoded Status Registers. These three registers can be concatenated together to form the LLX Encoded Status Register. Likewise, the three LLX Decoded Status Registers can be concatenated to form the LLX Decoded Status Register. Note the singular form of the term is used to refer to the concatenated register set in both cases.

LLX Encoded and Decoded Karaoke Status

The LLX Encoded Karaoke Status Register reports special status regarding input in various karaoke formats. The MSB signifies the presence of karaoke input of some form, while the other bits provide further information about the form of the karaoke input.

The following forms of karaoke input are recognized by DSP56371A:

- *ATSC Karaoke Form*, Dolby Digital with “Bitstream [*sic*] mode” 7 and “Audio coding mode” 2 or greater.

The LLX Decoded Karaoke Status Register is always zero, indicating that the output of the decoder is not karaoke-encoded in any manner.

Table 3-9 LLX Encoded and Decoded Karaoke Status Symbolic Opcodes

Symbol	Description	Value
getLLXStatusEncodedKaraoke	Report status register value	0xa23100
gotLLXStatusEncodedKaraokeNone	No karaoke input	0x000000
gotLLXStatusEncodedKaraokeIndicatorUnspecified	Karaoke input detected, form unspecified	0x000080
gotLLXStatusEncodedKaraokeIndicatorATSC	Karaoke input detected, ATSC form	0x000081
getLLXStatusDecodedKaraoke	Report status register value	0xa23500
gotLLXStatusDecodedKaraokeNon	No karaoke decoder output	0x000000

LLX Encoded and Decoded Surround Status

The LLX Encoded Surround Status Register reports the status regarding the possible encoding of the surround channels at the input as shown in Table 3-10. Likewise, the LLX Decoded Surround Status Register reports special status regarding the possible encoding of the surround channels at the output of the decoder, also in Table 3-10. If an LLX is capable of surround decoding, such as the DTS LLX, the LLX Encoded and Decoded Surround Status Registers may differ. Otherwise, these registers will be identical. At the different input bit stream, the LLX configuration results in the alteration of LLX encoded and decoded surround status. Refer to Table 3-20 for more details.

Table 3-10 LLX Encoded and Decoded Surround Status Symbolic Opcodes

Symbol	Description	Value
getLLXStatusEncodedSurround	Report status register value.	0xa23200
gotLLXStatusEncodedSurroundUnknown	Unknown surround encoding at input.	0x000000
gotLLXStatusEncodedSurroundNone	No surround encoding at input.	0x000001
gotLLXStatusEncodedSurroundDolbySurrEx	Dolby surround EX encoding at input.	0x000002
gotLLXStatusEncodedSurroundDTSMatrix6_1	DTS ES Matrix 6.1 surround encoding at input.	0x000003
gotLLXStatusEncodedSurroundDTSDiscrete6_1	DTS ES Discrete 6.1 surround encoding at input.	0x000004
getLLXStatusDecodedSurround	Report status register value.	0xa23600
gotLLXStatusDecodedSurroundUnknown	Unknown surround encoding at output.	0x000000
gotLLXStatusDecodedSurroundNone	No surround encoding at output.	0x000001
gotLLXStatusDecodedSurroundDolbySurrEx	Dolby surround EX encoding at output.	0x000002
gotLLXStatusDecodedSurroundDTSMatrix6_1	DTS ES Matrix 6.1 surround encoding at output.	0x000003

LLX Encoded and Decoded Sample Rate Status

The LLX Encoded Sample Rate Status Register reports the sample rate at the input Table 2-15. Likewise, the LLX Decoded Sample Rate Status Register reports the sample rate at the output of the decoder. If an LLX is capable of rate doubling, such as the DTS LLX, the LLX Encoded and Decoded Sample Rate Status Registers may differ. Otherwise, these registers will be identical.

3.3 AUTO LLX

The auto detection LLX has an excellent-sounding output when customers put a disc into a player. Equipped with the decoders in DSP56371A, auto detection automatically plays the corresponding source type. The Auto Low-Level Executive provides decoding of PCM bit streams delivered in IEC 61937 format along with automatic detection of encoded bit streams in IEC 60958 and DTS CD-DA format. Even if the receiver does not have a decoder for a particular type of bit stream, auto detection detects and mutes it to avoid unpleasant noise.

The following sample rates at the input are fully supported: 96 kHz, 88.2 kHz, 48 kHz, 44.1 kHz, and 32 kHz. All internal processing takes place at the input rate, but synchronous sample rate conversion may be applied before output as with any other LLX, 1:2 rate conversion associated with double-rate output or 2:1 rate conversion associated with DAX Data Stream Output, under the constraints outlined in Table 2-13 and Table 2-14.

Auto detection can be enabled or disabled by setting HLX Source Mode Register shown in Table 2-5. Customers are advised to use the AUTO LLX in the vast majority of applications.

3.4 PCM LLX

The PCM Low-Level Executive provides decoding of PCM bit streams delivered in IEC 61937 format. It does not provide automatic detection of encoded bit streams. If such bit streams are input, they are rendered as PCM and will sound like noise. In all other respects, the PCM LLX operates in a manner equivalent to the Auto LLX described in Section 3.3.

3.4.1 PCM Audio Mode

PCM Audio Mode Control Register determines oPDCAudioMode used in post processing, collaborating with LLX Downmix Control Register when PCM is the source type.

Table 3-11 oPDC AudioMode Calculation Table

LLX Downmix / PCM Audio mode	ProLogic 0/0.0	Stereo 2/0.0	Mono OnLR 1/0.0	Stereo Unknown/Other 2/0.0	Dual Mono 2/0.0
ProLogic 0/0.0	Lt/Rt	Lt/Rt	Lt/Rt	Lt/Rt	Lt/RtD
Mono 1/0.0	C*	C*	C*	C*	CD
Stereo 2/0.0	Lo/Ro	Lo,Ro	Lo,Ro	Lo,Ro	Lo,RoD
Mono OnLR 1/0.0	Lm/Rm~	Lm,Rm~	Lm,Rm	Lm,Rm~	Lm,RmD
StereoUnknown 2/0.0	Lu/Ru	Lu,Ru	Lu,Ru	Lu,Ru	Lu,RuD
Other	Lt/Rt	Lo,Ro	Lm,Rm	Lu,Ru	M1,M2D

Table 3-12 Symbolic Explanation Table

Symbol	Lt, Rt	C	Lo, Ro	Lm, Rm	Lu, Ru	M1, M2
oPDCAudioMode	ProLogic	Mono	Stereo	MonoOnLR	Stereo Unknown	DualMono

Symbol	Dual Mono	LLX Downmix	L, R Output	C Output	Level Adjustment
*	X	X	0, 0	(L+R)/2	0 dB
~	X	X	(L+R)/2 each	0	-3 dB
D	Both	Mono	0.0	(L+R)/2	0 dB
		MonoOnLR	(L+R)/2 each	0	-3 dB
		Any other	L, R	0	0 dB
	Left	Mono	0, 0	L	0 dB
		Not Mono	L, L	0	-3 dB
	Right	Mono	0, 0	R	0 dB
		Not Mono	R, R	0	-3 dB
	Sum	Mono	0, 0	(L+R)/2	0 dB
		Not Mono	(L+R)/2 each	0	-3 dB

Note: "X" = don't care

Table 3-13 PCM Audio Mode Control Symbolic Opcodes

Symbol	Description	Value
setPCMAudioModeProLogic	Set PCM audio mode	0xe30100
setPCMAudioModeStereo		0xe30102
setPCMAudioModeMonoOnLR		0xe30108
setPCMAudioModeStereoUnknown		0xe30109
setPCMAudioModeDualMono		0xe3010a
getPCMAudioMode	Report PCM audio mode	0xa30100
gotPCMAudioModeProLogic	Value corresponding to the audio mode	0x000000
gotPCMAudioModeStereo		0x000002
gotPCMAudioModeMonoOnLR		0x000008
gotPCMAudioModeStereoUnknown		0x000009
gotPCMAudioModeDualMono		0x00000a

3.4.2 PCM Silence Processing

The PCM silence processing register determines the silence processing within the PCM decoder auto detection routine.

Table 3-14 PCM Solence Processing Symbolic Opcodes

Symbol	Description	Value
setPCMAutoDetectionReset	Disable the unmute over-ride (which keeps mute enabled), which is enabled at PCM LLX due to a new bitstream detection. The LLX automatically reset and causes a "local restart" (PCM LLX does not exit), resetting all autodetection parameters to inital conditions. This flag is checked once per receive block prior to output processing.	0xe30d01
setPCMMuteAllDecoderExits	Enables muting for suppression of potential noise as PCM LLX is reactivated after exit of any other (compressed bitstream) LLX. The default setting of (0) provides this mute feature only for the case where DTS LLX exits	e30d03

3.5 AC3 LLX

The AC3 Low-Level Executive provides decoding of Dolby Digital formatted input bit streams presented in IEC 60958 format with multi-channel output. No maximum Dolby Digital bit rate is specified, but rates up to 640 kbps are in fact supported.

The following sample rates are fully supported: 48 kHz, 44.1 kHz, and 32 kHz. All internal processing takes place at the input rate, but synchronous sample rate conversion may be applied before output as with any other LLX, 1:2 rate conversion associated with double-rate output or 2:1 rate conversion associated with DAX Data Stream Output, under the constraints outlined in Table 2-13 and Table 2-14.

3.5.1 AC3 Extended Precision

DSP56371A provides the option of extended (48-bit rather than 24-bit) precision when decoding an AC3 bit stream. This is enabled or disabled as follows:

Table 3-15 AC3 Extended Precision Symbolic Opcodes

Symbol	Description	Value
setLLXPrecisionExtendedNone	Disable AC3 Extended Precision	0xe22200
setLLXPrecisionExtendedAC3	Enable AC3 Extended Precision	0xe22201
getLLXPrecision	Report LLX Extended Precision	0xa22200
gotBitLLXPrecisionExtendedAC3		0x000001
gotBitLLXPrecisionExtendedNone		0x000000

3.5.2 AC3 Dynamic Range

The DSP56371A allows customers to implement dynamic range control with the HLX Dynamic Range Registers. This allows users to directly adjust AC3 Dynamic Range through the AC3 Dynamic Range Registers when Speaker Control is disabled, so the user can adjust AC3 Dynamic Range regardless of the HLX Listening mode.

Table 3-16 AC3 Dynamic Range Symbolic Opcodes

Symbol	Description	Value
setAC3DynamicRangeHi_0	Set AC3 High Dynamic Range	0xc80e00
sotAC3DynamicRangeHi_zero		0x000000
sotAC3DynamicRangeHi_half		0x400000
sotAC3DynamicRangeHi_one		0x7fffff
setAC3DynamicRangeLo_0		0xc80e01

Table 3-16 AC3 Dynamic Range Symbolic Opcodes

Symbol	Description	Value
sotAC3DynamicRangeLo_zero	Set AC3 Low Dynamic Range	0x000000
sotAC3DynamicRangeLo_half		0x400000
sotAC3DynamicRangeLo_one		0x7fffff
getAC3DynamicRangeHi	Report the AC3 High and low dynamic range	0x880e00
getAC3DynamicRangeLo		0x880e01

Note that speaker control must be disabled before the above commands will take effect (see Table 2-8 for relevant commands).

3.5.3 AC3 Compression Mode

AC3 Compression Mode Control Register provides customers to adjust compression mode when speaker control is disabled.

Table 3-17 AC3 Compression Mode Symbolic Opcodes

Symbol	Description	Value
setAC3CompressionMode0	Set AC3 compression mode	0xe38900
setAC3CompressionMode1		0xe38901
setAC3CompressionModeLine		0xe38902
setAC3CompressionModeRF		0xe38903
getAC3CompressionMode	Report AC3 compression mode	0xa38900
gotAC3CompressionMode0	Value corresponding to the compression mode	0x000000
gotAC3CompressionMode1		0x000001
gotAC3CompressionModeLine		0x000002
gotAC3CompressionModeRF		0x000003

Note that speaker control must be disabled before the above commands will take effect (see Table 2-8 for relevant commands).

3.6 DTS LLX

The DTS Low-Level Executive provides decoding of DTS-formatted input bit streams presented in IEC 60958 and CD-DA format with multi-channel output. This includes DTS ES Discrete 6.1 for decoding of DTS ES 6.1 source material, DTS ES Matrix 6.1 for decoding of DTS ES 6.1, DTS ES 5.1, and DTS 5.1 source material, and DTS Neo:6 2-channel Matrix for use with DTS 2.0 source material, as well as 96 kHz / 24 bit operation.

The following sample rates at the input are fully supported: 48 kHz and 44.1 kHz. All internal processing takes place at the input rate unless the input bit stream contains extended audio data which allows internal processing to take place at twice the input rate, 96 kHz and 88.2 kHz, respectively. It supports rate-doubling processing up to DTS Discrete 6.1 source material. In addition, synchronous sample rate conversion may be applied before output as with any other LLX, 1:2 rate conversion associated with double-rate output or 2:1 rate conversion associated with DAX Data Stream Output, under the constraints outlined in Table 2-13 and Table 2-14.

3.6.1 DTS Status

The DTS Status Register is a bit-mapped register that reports status as follows:

Table 3-18 DTS Status Symbolic Opcodes

Symbol	Description	Value
getDTSStatus	Report DTS status	0x881000
getDTSStatusMode		0xa40100
getDTSStatusNeoMode		0xa40300
gotBitDTSStatusExtChansProcessing	Decoder is processing channel extension material	0x000001
gotBitDTSStatusExt96Processing	Decoder is processing 96/24 extension material	0x000002
gotBitDTSStatusExt96Detected	96/24 extension SYNC is detected	0x000004
gotBitDTSStatusExtChansDetected	Channel extension SYNC is detected	0x000008
gotBitDTSStatusNeoStereoDetected	Input bit stream is DTS Lt/Rt 2.0	0x010000
gotBitDTSStatusNeoStereoProcessing	NEO6 is processing on DTS 2.0	0x020000
gotBitDTSStatusNeoSurroundDetected	DTS ES format is detected	0x040000
gotBitDTSStatusNeoSurroundProcessing	NEO6 is processing on DTS 5.1, 5.1 ES, 6.1 or 6.1 ES	0x080000

3.6.2 DTS Configuration Mode Control

The DTS Configuration Mode Control Register is a bit-mapped register that is used to enable or disable various features included in DSP56371A and implemented as part of the DTS LLX. The corresponding bit must be set in order that the features are enabled.

Changes to the DTS Configuration Mode Control Register by the host only take effect following an LLX restart. Ostensibly, then, any change initiated by the host to the DTS Configuration Mode Control Register should be immediately followed by an opcode to restart the LLX as shown below. This second opcode will cause a momentary output mute as the system reacquires the input bit stream.

setDTSConfigMode_0+ nn # set new mode
setLLXConfigNone # restart LLX

the commands below will enable various decoding modes depending on the input bit stream. Refer to Table 3-21 for more detail.

Table 3-19 DTS Configuration Mode Control Symbolic Opcodes

Symbol	Description	Value
setDTSConfigMode_0	Bit-mapped register controls feature of the DTS LLX	0xe40500
gotBitDTSConfigModeEnableExtendedChannels	Enable channel extension processing	0x000001
gotBitDTSConfigModeEnable96kHz	Enable 96/24 extension processing	0x000002
gotBitDTSConfigModeDetect96kHz	Enable 96/24 extension SYNC processing	0x000004
gotBitDTSConfigModeDetectExtendedChannels	Enable channel extension SYNC processing	0x000008
gotBitDTSConfigModeEnableExtendedPrecision	Enable extended precision processing. Only works on non-96/24	0x000010
gotBitDTSConfigModeEnableSurroundEncoding	Enable automatic activation of extended-surround processing as controlled by the PCMR value.	0x000020
gotBitDTSConfigModeEnableExtSyncFsizeCheck	Enable validation of extension sync word location using extension FSIZE or FSIZE96 value for extended audio data	0x000040
GetDTSConfigMode	Report DTS configuration mode	0xa40500

3.6.3 DTS Configuration Neo:6 Mode Control

The DTS Configuration Neo:6 Mode Control Register is a bit-mapped register that is used to enable or disable various features included in DSP56371A and implemented as part of the DTS LLX. The corresponding bit must be set in order that the features are enabled. Changes to the DTS Configuration Neo:6 Mode Control Register by the host only take effect following an LLX restart. Ostensibly, then, any change initiated by the host to the DTS Configuration Neo:6 Mode Control Register should be immediately followed by an opcode to restart the LLX as shown below. This second opcode will cause a momentary output mute as the system reacquires the input bit stream.

setDTSConfigNeoMode_0+ nn # set new mode
setLLXConfigNone # restart LLX

The DTS Configuration Neo:6 Mode Control Register controls the operation of DTS ES Matrix 6.1 and DTS Neo:6 2-channel Matrix for DTS input. Control of operation of DTS ES Matrix 6.1 and DTS Neo:6 2-channel Matrix for other forms of input is described elsewhere. The following are pertinent features controlled by this register. Refer to Table 3-21 for more detail.

Table 3-20 DTS Configuration Neo:6 Mode Control Symbolic Opcodes

Symbol	Description	Value
setDTSConfigNeoMode_0	Bit-mapped register controls feature of the DTS LLX for Neo:6 operation	0xe40700
gotBitDTSConfigNeoModeEnableStereoEncoding	Processing Lt/Rt (AMODE=$100)	0x000001
gotBitDTSConfigNeoModeForceStereoEncoding	Processing stereo except sum-different stereo (AMODE=$10 or $100)	0x000002
gotBitDTSConfigNeoModeEnableSurroundEncoding	Matrix 6.1 processing when ES in PCMR is 1	0x000004
gotBitDTSConfigNeoModeForceSurroundEncoding	Matrix 6.1 processing and ES takes no effect	0x000008
gotBitDTSConfigNeoModeMusic	Neo 6:2-channel matrix processing in the music mode instead of normal mode.	0x000010
setDTSConfigNeoCGain	Neo6 matrix processing center channel gain	0xc81002
GetDTSConfigMode	Report DTS Neo:6 configuration mode	0xa40700

Table 3-21 DTS Configuration and Status

Input Bit Stream	Decoder Configuration	DTS Status	LLX Decoded and Encoded Status
DTS 5.1	Normal (0xe40500, 0xe40700)	Nothing (0x000000)	GotLLXStatusEncoded SurroundNone GotLLXStatusDecoded SurroundNone
	SotBitDTSConfigNeoMode EnableSurroundEncoding	Nothing (0x000000)	GotLLXStatusEncoded SurroundNone GotLLXStatusDecoded SurroundNone
	SotBitDTSConfigNeoMode ForceSurroundEncoding	GotBitDTSStatusNeo SurroundProcessing	GotLLXStatusEncoded SurroundNone GotLLXStatusDecoded SurroundNone

Table 3-21 DTS Configuration and Status (Continued)

Input Bit Stream	Decoder Configuration	DTS Status	LLX Decoded and Encoded Status
DTS 5.1 ES	Normal (0xe40500, 0xe40700)	GotBitDTSStatusNeo SurroundDetected	GotLLXStatusEncoded SurroundDTSMatrix6_1 GotLLXStatusDecoded SurroundDTSMatrix6_1
	SotBitDTSConfigNeoMode EnableSurroundEncoding	GotBitDTSStatusNeo SurroundDetected GotBitDTSStatusNeo SurroundProcessing	GotLLXStatusEncoded SurroundDTSMatrix6_1 GotLLXStatusDecoded SurroundNone
DTS 6.1	Normal (0xe40500, 0xe40700)	Nothing (0x000000)	GotLLXStatusEncoded SurroundNone GotLLXStatusDecoded SurroundNone
	SotBitDTSConfigMode DetectExtendedChannels	GotBitDTSStatusExt ChansDetected	GotLLXStatusEncoded SurroundNone GotLLXStatusDecoded SurroundNone
	SotBitDTSConfigMode DetectExtendedChannels SotBitDTSConfigMode EnableExtendedChannels	GotBitDTSStatusExt ChansProcessing GotBitDTSStatusExt ChansDetected	GotLLXStatusEncoded SurroundNone GotLLXStatusDecoded SurroundNone
DTS 6.1 ES	Normal (0xe40500, 0xe40700)	GotBitDTSStatusNeo SurroundDetected	GotLLXStatusEncoded SurroundDTSMatrix6_1 GotLLXStatusDecoded SurroundDTSMatrix6_1
	SotBitDTSConfigMode DetectExtendedChannels	GotBitDTSStatusExt ChansDetected GotBitDTSStatusNeo SurroundDetected	GotLLXStatusEncoded SurroundDTSMatrix6_1 GotLLXStatusDecoded SurroundDTSMatrix6_1
	SotBitDTSConfigMode DetectExtendedChannels SotBitDTSConfigMode EnableExtendedChannels	GotBitDTSStatusExt ChansProcessing GotBitDTSStatusExt ChansDetected	GotLLXStatusEncoded SurroundDTSDiscrete6_1 GotLLXStatusDecoded SurroundNone
	SotBitDTSConfigNeoMode EnableSurroundEncoding	GotBitDTSStatusNeo SurroundDetected GotBitDTSStatusNeo SurroundProcessing	GotLLXStatusEncoded SurroundDTSMatrix6_1 GotLLXStatusDecoded SurroundNone

Table 3-21 DTS Configuration and Status (Continued)

Input Bit Stream	Decoder Configuration	DTS Status	LLX Decoded and Encoded Status
DTS 5.1 96/24	Normal (0xe40500, 0xe40700)	Nothing (0x000000)	GotLLXStatusEncoded SurroundNone GotLLXStatusDecoded SurroundNone
	GotBitDTSConfigMode Detect96kHz	GotBitDTSStatusExt 96Detected	GotLLXStatusEncoded SurroundNone GotLLXStatusDecoded SurroundNone
	GotBitDTSConfigMode Detect96kHz GotBitDTSConfigMode Enable96kHz	GotBitDTSStatusExt 96Processing GotBitDTSStatusExt 96Detected	GotLLXStatusEncoded SurroundNone GotLLXStatusDecoded SurroundNone
DTS6.1 96/24	Normal (0xe40500, 0xe40700)	Nothing (0x000000)	GotLLXStatusEncoded SurroundNone GotLLXStatusDecoded SurroundNone
	GotBitDTSConfigMode Detect96kHz GotBitDTSConfigMode DetectExtendedChannels	GotBitDTSStatusExt 96Detected	GotLLXStatusEncoded SurroundNone GotLLXStatusDecoded SurroundNone
	GotBitDTSConfigMode Detect96kHz GotBitDTSConfigMode Enable96kHz GotBitDTSConfigMode DetectExtendedChannels GotBitDTSConfigMode EnableExtendedChannels	GotBitDTSStatusExt 96Processing gotBitDTSStatusExt 96Detected GotBitDTSStatusExt ChannelDetected GetBitDTSStatusExt ChannelProcessing	GotLLXStatusEncoded SurroundNone GotLLXStatusDecoded SurroundNone

3.6.4 DTS Configuration Dynamic Range Control Register

The DTS Configuration Dynamic Range Control Register is a bit-mapped register that provides the user with the capability to adjust the total amount of attenuation applied to the output audio channels when a bit stream is encoded with dynamic range information. Note that the system-level dynamic range control capabilities of DSP56371A, specifically automatic control of dynamic range as a function of listening mode, are not currently available with DTS input. The opcodes listed in this section must be used manually and directly to achieve similar effects when desired.

The Dynamic Range Softening features included in DSP56371A only takes effect if DYNF is set, and the customer explicitly supplies a “softening” scale value different than zero. The value of DYNF can be monitored by issuing the symbol (or equivalent opcode) in Table 3-22. The “softening” scale value may be supplied to the system by using one of the symbols (or equivalent opcodes) shown in Table 3-23. Note that issuing ’setDTSConfigDRCSoft_zero’ is equivalent to disabling the functionality, and that ’setDTSConfigDRCSoft_one’ has the effect of applying the full amount of compression that it is indicated by the encoded bitstream for the subframe being decoded.

In regard to the integration of the DTS Dynamic Range *Softening* feature within the complete system, it must be noted that none of the system level symbols of the form ‘setHLXDynamicRangeHi_*’ or ‘setHLXDynamicRangeLo_*’ allow the customer to control this functionality. Neither do the symbols ‘getHLXDynamicRangeHi’ nor ‘getHLXDynamicRangeLo’ provide information about its operation. As of now, only the symbols in Table 3-23 constitute a proper interface to the DTS Dynamic Range Softening feature implemented in DSP56371A.

Table 3-22 DTS Dynamic Range Flag Status Symbolic Opcodes

Symbol	Description	Value
getLLXDTSDynf	Report Status value	0x880909

Table 3-23 DTS Configuration Dynamic Range Control Symbolic Opcodes

Symbol	Description	Value
setDTSConfigDRCSoftDisable	Disable DTS Dynamic Range functionality	0xe40600
setDTSConfigDRCSoft_0+uu	Bit-mapped register controls softening of DTS Dynamic Range functionality	0xe406uu
setDTSConfigDRCSoft_zero	Does not apply any dynamic range attenuation	0xe40600
setDTSConfigDRCSoft_quarter	Applies only ¼ of the full dynamic range encoded in the bit stream	0xe40640
setDTSConfigDRCSoft_half	Applies only ½ of the full dynamic range encoded in the bit stream	0xe40680
setDTSConfigDRCSoft_one	Applies the full dynamic range encoded in the bit stream	0xe406ff
getDTSConfigDRCSoft	Report control register value	0xa40600

3.6.5 DTS Configuration MIPS Threshold Register

The DTS decoder supports rescue mode. Rescue mode will be activated automatically when the bitstream consumes more MIPS than the Threshold. Rescue mode will hold until e20400 is issued or an external event causes an LLX restart. To disable rescue mode, the user can set this Threshold Register to a value large enough such as $7ffffff.

Table 3-24 DTS Configuration MIPS Threshold Register

Symbol	Description	Value
setDTSConfigMIPSThreshold	Set the MIPS Threshold for activating rescue mode.	0xc81003
getDTSConfigMIPSThreshold	Report the present MIPS threshold value for activating rescue mode.	0x881003
getDTSStatus	Report DTS status	0x881000
gotBitDTSMipsRescuemode	Report DTS decoder is running under rescue mode	0x000400

3.7 AAC LLX

The AAC Low-Level Executive provides support for decoding of AAC-formatted input bit streams presented in several formats with multi-channel output. It provides support of the AAC bit streams in IEC format only. It operates as a standard LLX, including standard downmix and standard output block size.

The following sample rates at the input are fully supported: 48 kHz. All internal processing takes place at the input rate, but synchronous sample rate conversion may be applied before output as with any other LLX, 1:2 rate conversion associated with double- rate output or 2:1 rate conversion associated with DAX Data Stream Output, under the constraints outlined in Table 2-13 and Table 2-14.

3.8 NOISE GENERATOR LLX

The Noise Generator Low-Level Executive provides three signal sources: white noise, pink noise, as well as sine tone, composite operation modes-band pass filter (BPF), soft mute, and unmute function, and output mode-sequence mode and pause mode.

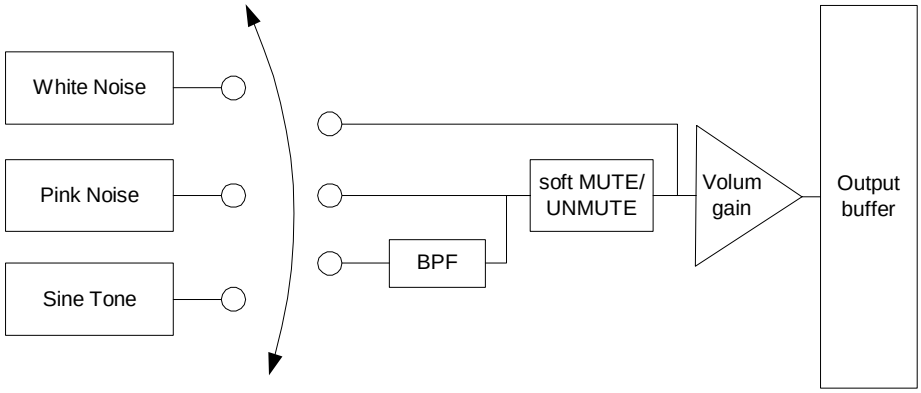

Figure 3-1 Noise Generator LLX Structure

3.8.1 NG Configuration

NG supports three output modes, scanning the channels in sequence, stopping at a channel for the long time and altering an output channel in the order. The first is sequence mode running by Configuration Sequence. Next is provided by pause mode. In pause mode, users can point the special channel via NG Status Register, described below. The final is advance mode which command is Configuration Advance. Note that the output channels are limited by listening mode.

Table 3-25 NG Configuration Symbolic Opcodes

Symbol	Description	Value
setNGConfigNone	Disable NG	0xe28400
setNGConfigSequence	Sequence Mode	0xe28401
setNGConfigPause	Pause Mode	0xe28402
setNGConfigAdvance	Advance Mode	0xe28403
getNGConfig	Report configuration register value	0x880a01

3.8.2 NG Status

NG Status Register has two uses in the DSP56371A system. One is to report the current output channel, the other is to point the output channel in pause mode.

Table 3-26 NG Status Symbolic Opcodes

Symbol	Description	Value
getNGStatus	Report status register value	0x880a00
setNGStatusLeft	Point the output channel in pause mode.	0xe28000
setNGStatusRght		0xe28001
setNGStatusLSur		0xe28002
setNGStatusRSur		0xe28003
setNGStatusCntr		0xe28004
setNGStatusSubw		0xe28005
setNGStatusLAux		0xe28006
setNGStatusRAux		0xe28007
setNGStatusNone		0xe28008

3.8.3 NG Flag

NG provides three generators-white noise, pink noise, and sine tone-and two operation modes-BPF, soft mute, and unmute. Users can switch the different composite modes in NG Flag Register shown at the below table.

Table 3-27 NG Composite Mode

Command for Generator	Command for Operation Mode	White Noise	Pink Noise	Sine Tone	BPF	Mute and Unmute	Mute and Unmute at the same time
1	1	OFF	OFF	ON	OFF	OFF	OFF
2	1	OFF	ON	OFF	OFF	OFF	OFF
4	1	ON	OFF	OFF	OFF	OFF	OFF
1	2	OFF	OFF	ON	OFF	ON	OFF
2	2	OFF	ON	OFF	OFF	ON	OFF
4	2	ON	OFF	OFF	OFF	ON	OFF
1	3	OFF	OFF	ON	OFF	ON	ON
2	3	OFF	ON	OFF	OFF	ON	ON
4	3	ON	OFF	OFF	OFF	ON	ON
1	4	OFF	OFF	ON	ON	ON	OFF
2	4	OFF	ON	OFF	ON	ON	OFF
4	4	ON	OFF	OFF	ON	ON	OFF

Table 3-27 NG Composite Mode (Continued)

Command for Generator	Command for Operation Mode	White Noise	Pink Noise	Sine Tone	BPF	Mute and Unmute	Mute and Unmute at the same time
1	5	OFF	OFF	ON	ON	ON	ON
2	5	OFF	ON	OFF	ON	ON	ON
4	5	ON	OFF	OFF	ON	ON	ON
1	6	OFF	OFF	ON	ON	ON	OFF
2	6	OFF	ON	OFF	ON	ON	OFF
4	6	ON	OFF	OFF	ON	ON	OFF
1	7	OFF	OFF	ON	ON	ON	ON
2	7	OFF	ON	OFF	ON	ON	ON
4	7	ON	OFF	OFF	ON	ON	ON

Table 3-28 NG Flag Symbolic Opcodes

Symbol	Description	Value
setNGFlag	Set flag register value	0xe28800
gotBitNGFlagWhiteNoise	The corresponding generator or operation mode	0x000040
gotBitNGFlagPinkNoise		0x000020
gotBitNGFlagSineTone		0x000010
gotBitNGFlagBPF		0x000004
gotBitNGFlagMuteUnMute		0x000002
gotBitNGFlagSameTime		0x000001
gotBitNGFlagSwfLPF		0x000008
getNGFlag	Report flag register value	0x880a02

3.8.4 NG Pink Filter

NG Pink Filter Register is a pointer to call a coefficient table for the filter function entrance, which alters white noise to pink noise. Putting a new filter function entrance in the register, users can take advantage of their own algorithm.

Table 3-29 NG Configuration Symbolic Opcodes

Symbol	Description	Value
setNGFilter	Set pink filter register value	0xC80a03
getNGFilter	Report pink filter register value	0x880a03

3.8.5 NG Time Duration

NG Time Duration Register stipulates the time used in sequence mode, that is, it tells the system how long the output channel should be switched. The accounting unit is 0.116 μS per count.

Table 3-30 NG Time Duration Symbolic Opcodes

Symbol	Description	Value
setNGTimeDuration	Set time duration register value	0xC80a04
getNGTimeDuration	Report time duration register value	0x880a04

3.8.6 NG Sine Frequency

Choosing sine tone generator, users transform the signal frequency into the data needed by DSP36371A system according to the following equation.

$$NGSwgSinW = \sin\left(2\pi f / f_s\right)$$

$$NGSwgCosW = \cos\left(2\pi f / f_s\right)$$

In the equation, f is signal frequency and f_s is the sampling frequency. Note that the couple should be changed at the same time. Users are requested to give the preferable frequency before running sine tone generator.

Table 3-31 NG Sine Frequency Symbolic Opcodes

Symbol	Description	Value
setNGSwgSinW	Set sine frequency register value	0xc80a05
setNGSwgCosW		0xc80a06
getNGSwgSinW	Report sine frequency register value	0x880a05
getNGSwgCosW		0x880a06

3.8.7 NG Mute and Unmute Step

NG Mute & Unmute Step Register is to manage the mute & unmute time.

Table 3-32 NG Mute and Unmute Symbolic Opcodes

Symbol	Description	Value
setNGMuteStep	Set mute & unmute step register value	0xc80a07
setNGUnMuteStep		0xc80a08
getNGMuteStep	Report mute & unmute step register value	0x880a07
getNGUnMuteStep		0x880a08

3.8.8 BPF Coefficients

BPF consists of a low pass filter and the high pass filter, whose coefficients can be managed by users in NG BPF Coefficient Register. The filter equation is:

$$y[n] + 2*A1*y[n-1] + 2*A2*y[n-2] = 2*B0*x[n] + 2*B1*x[n-1] + 2*B2*x[n-2]$$

Table 3-33 NG BPF Coefficient Symbolic Opcodes

Symbol	Description	Value
setNGBPFCoefLA2	Low pass filter coefficients	0xc80a0a
setNGBPFCoefLA1		0xc80a0b
setNGBPFCoefLB2		0xc80a0c
setNGBPFCoefLB1		0xc80a0d
setNGBPFCoefLB0		0xc80a0e
getNGBPFCoefLA2		0x880a0a
getNGBPFCoefLA1		0x880a0b
getNGBPFCoefLB2		0x880a0c
getNGBPFCoefLB1		0x880a0d
getNGBPFCoefLB0		0x880a0e

Table 3-33 NG BPF Coefficient Symbolic Opcodes (Continued)

Symbol	Description	Value
setNGBPFCoefHA2	High pass filter coefficients	0xc80a0f
setNGBPFCoefHA1		0xc80a10
setNGBPFCoefHB2		0xc80a11
setNGBPFCoefHB1		0xc80a12
setNGBPFCoefHB0		0xc80a13
getNGBPFCoefHA2		0x880a0f
getNGBPFCoefHA1		0x880a10
getNGBPFCoefHB2		0x880a11
getNGBPFCoefHB1		0x880a12
getNGBPFCoefHB0		0x880a13

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Section 4
Post-Processing Phases (PPPs)

4.1 OVERVIEW[1]

The post processing chain is the part of the software architecture designed to process audio data after it has been decoded and placed in the output buffer. It is designed to handle multiple independently controlled audio processing blocks. Each block or Post Processing Phase (PPP) is passed through program control so that it may process decoded audio data in the output buffer. The Post Processing Chain can be thought of as a collection of serially executed standard and custom Post Processing Phases. A Post Processing Phase is implemented through a set of subroutines to enable a unique audio processing feature like bass management or volume control. A standard Post Processing Phase is a pre-defined audio processing routine which is initialized and installed automatically by the executive. A custom Post Processing Phase is a modular piece of audio processing software which may be additionally installed to the system.

Standard Post Processing Phases

A standard Post Processing Phase is one of several pre-defined and implemented software components which are executed serially in the Post Processing Chain. The executive initializes standard PPPs during the executive initialization. The executive also manages their periodic invocation to perform post processing of decoded audio data.

Currently available Motorola standard PPPs for use in the Software Architecture 56371A include:

- New De-emphasis
- Dolby ProLogicII
- DTS Logic (aka Neo6)
- LFE Attenuate
- Surround EX
- DTS Matrix
- Dolby Bass Manager
- Dolby Delay Manager
- General Delay Manager
- Volume Manager
- Digital Gain Manager
- Double Rate Manager

Custom Post Processing Phases – via the Slot

Within the Post Processing Chain Block are PPPs described as Slot*X*, where X is a number. The Slot is a very special standard PPP which allows for the dynamic installation of a custom PPP. The Slot provides a shell from which RAM based software can be loaded and run. Unlike other standard PPPs, the Slot does

1.The detail about PPP architecture refers to *PPP Developer's Quick Start Guide*.

not perform audio processing, but is rather software which enables custom software to be added to the post processing chain. The Slot PPP is what enables an independent software developer to produce the custom PPPs that this document also describes. Several copies of the slot are implemented throughout the post processing chain to provide a scaleable configuration of custom PPPs. The Slots are by default-initialized disabled. Through custom initialization and activation techniques, custom PPP software can be added.

Each Slot has been allocated its own zone from which standard commands can be issued. The Standard Zone Table provides an indirect table to allow standard command mapping through CHIRP. This feature is of particular importance for a PPP developer who wishes to install their custom PPP in a slot although it is not essential that zone tables are used to control PPPs. Table 4-1shows the standard zone mappings to the Standard and Slot PPPs.

Table 4-1 PPP Slots and Zone Offset for Red HLX

PPP Number	Zone Offset	Type of PPP	Notes
1		Reserved	
2	$33	New De-Emphasis	
3	$37	Secondary L R	
4	$18	Slot NoiseImmune0	Noise immune
5	$19	Slot 0	
6	$1A	Slot1	
7	$1B	Slot2	
8	$1C	Pro Logic II	
9	$1D	Slot NoiseImmune1	
10	$1E	Slot 3	
11	$1F	Slot 4	
12	$20	Slot 5	
13	$21	LFE Attenuation	
14	$22	Slot NoiseImmune2	Noise immune.
15	$23	Slot 6	Noise immune.
16	$24	Slot 7	
17	$25	Slot 8	
18	$3D	Surround EX	
19	$26	Subwoofer Manager	
20	$27	Slot NoiseImmune3	Noise immune.
21	$28	Slot 9	
22	$29	Slot 10	
23	$2A	Slot 11	
24	$2B	Delay Manager	

Table 4-1 PPP Slots and Zone Offset for Red HLX (Continued)

PPP Number	Zone Offset	Type of PPP	Notes
25	$2C	Volume Manager	
26	$2D	8-channel Gain	
27	$2E	Slot NoiseImmune4	Noise immune.

Table 4-2 PPP Slots and Zone Offset for Blue HLX

PPP Number	Zone Offset	Type of PPP	Notes
1		Reserved	
2	$33	New De-Emphasis	
3	$18	Slot NoiseImmune0	Noise immune
4	$19	Slot 0	
5	$1A	Slot1	
6	$1B	Slot2	
7	$1C	Pro Logic II	
8	$3A	DTS Logic (Neo6)	
9	$1D	Slot NoiseImmune1	
10	$1E	Slot 3	
11	$1F	Slot 4	
12	$20	Slot 5	
13	$21	LFE Attenuation	
14	$22	Slot NoiseImmune2	Noise immune.
15	$23	Slot 6	Noise immune.
16	$24	Slot 7	
17	$25	Slot 8	
18	$3D	Surround EX	
19	$39	DTS Matrix6.1	
20	$26	Subwoofer Manager	
21	$27	Slot NoiseImmune3	Noise immune.
22	$28	Slot 9	
23	$29	Slot 10	
24	$2A	Slot 11	
25	$2B	Delay Manager	
26	$2C	Volume Manager	

Table 4-2 PPP Slots and Zone Offset for Blue HLX (Continued)

PPP Number	Zone Offset	Type of PPP	Notes
27	$2D	8-channel Gain	
28	$2E	Slot NoiseImmune4	Noise immune.

Table 4-3 PPP Slots and Zone Offset for Green HLX

PPP Number	Zone Offset	Type of PPP	Notes
1	$3b	Double Rate	
2		Reserved	
3	$33	New De-Emphasis	
4	$18	Slot NoiseImmune0	Noise immune
5	$19	Slot 0	
6	$1A	Slot1	
7	$1B	Slot2	
8	$1C	Pro Logic II	
9	$3A	DTS Logic (Neo6)	
10	$1D	Slot NoiseImmune1	
11	$1E	Slot 3	
12	$1F	Slot 4	
13	$20	Slot 5	
14	$21	LFE Attenuation	
15	$22	Slot NoiseImmune2	Noise immune.
16	$23	Slot 6	Noise immune.
17	$24	Slot 7	
18	$25	Slot 8	
19	$3D	Surround EX	
20	$39	DTS Matrix6.1	
21	$26	Subwoofer Manager	
22	$27	Slot NoiseImmune3	Noise immune.
23	$28	Slot 9	
24	$29	Slot 10	
25	$2A	Slot 11	
26	$2B	Delay Manager	
27	$2C	Volume Manager	

Table 4-3 PPP Slots and Zone Offset for Green HLX (Continued)

PPP Number	Zone Offset	Type of PPP	Notes
28	$2D	8-channel Gain	
29	$3C	DoubleRate1	
30	$2E	Slot NoiseImmune4	Noise immune.

Note that “Noise Immune” simply means that the PPP in that particular slot will not run if the Noise Generator is being used as the audio source.

4.2 GENERAL DELAY MANAGER

The Delay Post Processing Phase or Delay Manager provides the capabilities required to implement delay control in standard manner for multi-channel data within the Executive Programming Environment.

4.2.1 Delay Manager Status

Via the Delay Manager Status Register, the system reports the active channel count through the delay manager.

Table 4-4 Delay Manager Status Symbolic Opcodes

Symbol	Description	Value
getDLMStatus	Report status register value.	0x882b00

4.2.2 Delay Manager Configuration

Delay Manager Configuration Register is set with six modes: Milliseconds and Half-milliseconds (time); Inches, Feet, Centimeters, and Meters (distance). Users can choose the convenient mode then give system the corresponding delay values for different channels in the Delay Value Register.

Table 4-5 Delay Manager Configuration Symbolic Opcodes

Symbol	Description	Value
setDLMConfigDisable	Disable delay manager	0xeac400
setDLMConfigMilliseconds	Milliseconds mode	0xeac401
setDLMConfigMilliseconds2	Half-milliseconds mode	0xeac402
setDLMConfigInches	Inches mode	0xeac403
setDLMConfigFeet	Feet mode	0xeac404
setDLMConfigCentimeters	Centimeters mode	0xeac405
setDLMConfigMeters	Meters mode	0xeac406
setDLMConfigNoInitDisable	The following commands perform the same action as the above set, however they do not initialize the delay buffers.	0xeac500
setDLMConfigNoInitMilliseconds		0xeac501
setDLMConfigNoInitMilliseconds2		0xeac502
setDLMConfigNoInitInches		0xeac503
setDLMConfigNoInitFeet		0xeac504
setDLMConfigNoInitCentimeters		0xeac505
setDLMConfigNoInitMeters		0xeac506
getDLMConfig	Report configuration register value.	0x882b01

4.2.3 Delay Value Register

Table 4-6 Delay Value Register Symbolic Opcodes

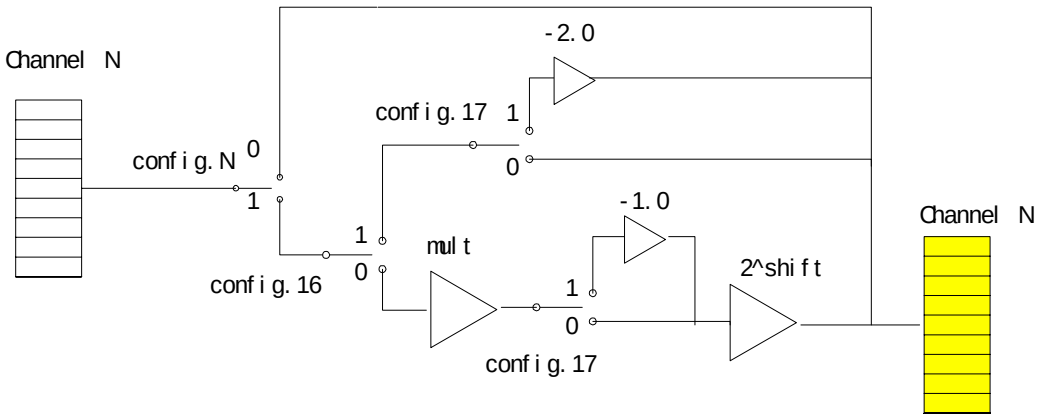
Symbol	Description	Value
setDLMDelayLeft	Set delay values of the corresponding channels according to ‘time’ modes.	0xc82b03
setDLMDelayRght		0xc82b04
setDLMDelayLSur		0xc82b05
setDLMDelayRSur		0xc82b06
setDLMDelayCntr		0xc82b07
setDLMDelaySubw		0xc82b08
setDLMDelayLAux		0xc82b09
setDLMDelayRAux		0xc82b0a
setDLMDelayLSec		0xc82b0b
setDLMDelayRSec		0xc82b0c

Table 4-6 Delay Value Register Symbolic Opcodes (Continued)

Symbol	Description	Value
setDLMSpeakerLocationLeft	Set delay values of the corresponding channels according to 'distance' modes.	0xc82b03
setDLMSpeakerLocationRght		0xc82b04
setDLMSpeakerLocationLSur		0xc82b05
setDLMSpeakerLocationRSur		0xc82b06
setDLMSpeakerLocationCntr		0xc82b07
setDLMSpeakerLocationSubw		0xc82b08
setDLMSpeakerLocationLAux		0xc82b09
setDLMSpeakerLocationRAux		0xc82b0a
setDLMSpeakerLocationLSec		0xc82b0b
setDLMSpeakerLocationRSec		0xc82b0c
getDLMDelayLeft	Report the delay values of the corresponding channels.	0x882b03
getDLMDelayRght		0x882b04
getDLMDelayLSur		0x882b05
getDLMDelayRSur		0x882b06
getDLMDelayCntr		0x882b07
getDLMDelaySubw		0x882b08
getDLMDelayLAux		0x882b09
getDLMDelayRAux		0x882b0a
getDLMDelayLSec		0x882b0b
getDLMDelayRSec		0x882b0c

4.3 GAIN MANAGER

The Gain Manager Post-Processing Phase provides the capabilities required to implement digital gain in a standard manner for multi-channel data within the Executive Programming Environment. In conjunction with compatible operation of the Digital Volume Control Method Post-Processing Function, the Gain PPP provides an implementation of volume control as following figure.



config.N Corresponding with channel N
0 means channel N is masked
1 means channel N is active
config.16 bypass flag
0 means bypass flag is cleared
1 means bypass flag is set
config.17 invert flag
0 means invert flag is cleared
1 means invert flag is set

Figure 4-1 Gain Manager Structure

4.3.1 Gain Manager Status

Table 4-7 Gain Manager Status Symbolic Opcodes

Symbol	Description	Value
getGMStatus	Report status register value.	0x882d00
gotGMStatusOkay	Result is okay	0x000000
gotGMStatusOverflow	Overflow in the computation	0x400000

4.3.2 Gain Manager Configuration

Table 4-8 Gain Manager Configuration Symbolic Opcodes

Symbol	Description	Value
setGMConfig	Set all of bits 23-0. Bit 17: Inversion flag - invert output. Bit 16: Bypass flag - don't apply gains. Bits 15-0: Channel mask	0xc82d01
setGMConfigFlagNone	Clear both bypass and invert flag	0xeb4700
setGMConfigFlagBypass	Set bypass flag	0xeb4701
setGMConfigFlagInvert	Set Invert flag	0xeb4702
setGMConfigFlagAll	Set both bypass and invert flag	0xeb4703
getGMConfig	Report configuration register value	0x882d01
getGMConfigMask	Report configuration channel mask	0xab4500
getGMConfigFlag	Report configuration control flag status	0xab4700

4.3.3 Gain Manager Coefficient Register

If Gain Manager is not bypassed but not automatically controlled by the Volume Manager, as is the case with the Digital Volume Control Method, the exponent and mantissa of each channel can be set separately to realize origin adjustment. The gain represented by the exponent-mantissa pair E, M is M*2^(E+1). Note that the values of E and M have a scope in [-2, 2).

Table 4-9 Gain Manager Coefficient Register Symbolic Opcodes

Symbol	Description	Value
setGMGainLeftExponent	Set the exponent and mantissa for the corresponding channel	0xc82d02
setGMGainLeftMantissa		0xc82d03
setGMGainRghtExponent		0xc82d04
setGMGainRghtMantissa		0xc82d05
setGMGainLSurExponent		0xc82d06
setGMGainLSurMantissa		0xc82d07
setGMGainRSurExponent		0xc82d08
setGMGainRSurMantissa		0xc82d09
setGMGainCntrExponent		0xc82d0a
setGMGainCntrMantissa		0xc82d0b
setGMGainSubwExponent		0xc82d0c
setGMGainSubwMantissa		0xc82d0d
setGMGainLAuxExponent		0xc82d0e
setGMGainLAuxMantissa		0xc82d0f
setGMGainRAuxExponent		0xc82d10
setGMGainRAuxMantissa		0xc82d11
setGMGainLSecExponent		0xc82d12
setGMGainLSecMantissa		0xc82d13
setGMGainRSecExponent		0xc82d14
setGMGainRSecMantissa		0xc82d15
getGMGainLeftExponent	Report the exponent and mantissa for the corresponding channel	0x882d02
getGMGainLeftMantissa		0x882d03
getGMGainRghtExponent		0x882d04
getGMGainRghtMantissa		0x882d05
getGMGainLSurExponent		0x882d06
getGMGainLSurMantissa		0x882d07
getGMGainRSurExponent		0x882d08
getGMGainRSurMantissa		0x882d09
getGMGainCntrExponent		0x882d0a
getGMGainCntrMantissa		0x882d0b
getGMGainSubwExponent		0x882d0c
getGMGainSubwMantissa		0x882d0d
getGMGainLAuxExponent		0x882d0e
getGMGainLAuxMantissa		0x882d0f
getGMGainRAuxExponent		0x882d10
getGMGainRAuxMantissa		0x882d11

4.4 VOLUME MANAGER

The Volume Post Processing Phase or Volume Manager provides the capabilities required to implement volume control in a standard manner for multi-channel data within the Executive Programming Environment. The overall process is summarized in Figure 4-2.

The Volume Manager provides a mechanism to attach a scale factor or size to the 24-bit fixed-point field of bits that are used to represent the audio data within the data buffers. The scale factor is not applied to the data field at the point in the processing chain at which it is generated, but rather it is held in waiting to be applied at a later point in the processing chain. Throughout the decoding and post-processing chain, these scale factors are accumulated, and only at the very end of the audio processing chain are they combined with the data, in some cases even after digital-to-analog conversion. This technique allows gross gain and attenuation factors to be applied to the data in the buffers, reducing neither the headroom that provides protection from overflow with large signals nor the precision that provides protection from noise.

The Volume Manager must be run in conjunction with *Digital Gain PPP* to allow realization of the Digital Method of Volume Control.

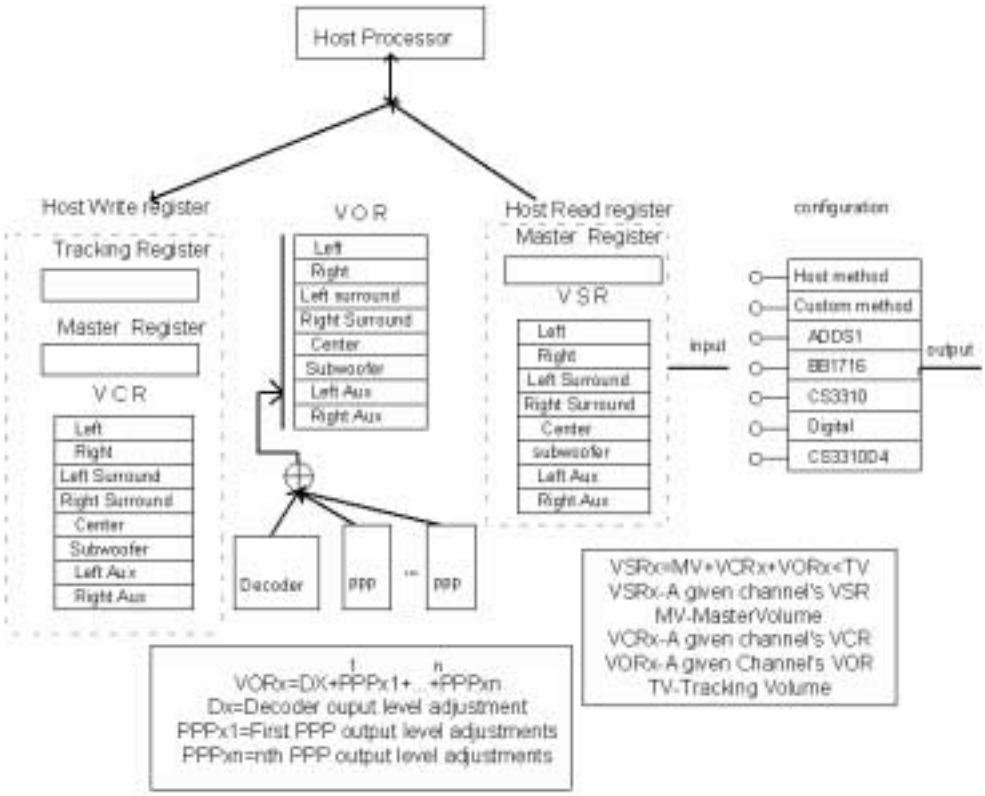


Figure 4-2 Volume Manager Structure

4.4.1 Volume Manager Status

The Volume Manager Status Register should be always 0, indicating successful operation of the Volume Manager.

Table 4-10 Volume Manager Status Symbolic Opcodes

Symbol	Description	Value
getVMStatus	Report status register value.	0x882c00

4.4.2 Volume Manager Configuration

Table 4-11 Volume Manager Configuration Symbolic Opcodes

Symbol	Description	Value
setVMConfig	Set volume manager configuration	0xc82c01
sotVMConfigNone	The corresponding volume control method. Refer to the following table.	0x000000
sotVMConfigCustom		0x010000
sotVMConfigADDS1		0x020000
sotVMConfigADDS1_6		0x022906
sotVMConfigADDS1_8		0x022908
sotVMConfigADDS1_12		0x02290c
sotVMConfigBB1716		0x030000
sotVMConfigCS3310		0x040000
sotVMConfigCS3310_8		0x040008
sotVMConfigDigital		0x050000
sotVMConfigCS3310D		0x060000
sotVMConfigCS3310D_8		0x060008
getVMConfig	Report volume manager configuration	0x882c01

Table 4-12 Volume Control Method

Value	Volume Control Method
$000000	Host Method
$010000	Custom Method

Table 4-12 Volume Control Method (Continued)

Value		Volume Control Method
$020000	020000	DLC Method, Reserved for ADDS-1
	022906	DLC Method, Reserved for ADDS-1/6 channel
	02290c	DLC Method, Reserved for ADDS-1/12 channel
$0300nn	030000	DLC Method, Reserved for PCM1716
	030008	DLC Method, Reserved for PCM1716/8 channel
	03000a	DLC Method, Reserved for PCM1716/10 channel
$0400nn	040000	DLC Method, Reserved for CS3310
	040008	DLC Method, Reserved for CS3310/ 8 channel
	04000a	DLC Method, Reserved for CS3310/ 10 channel
$0500nn	050000	Digital Gain Method
$0600nn	060000	DLC Method ,Reserved for CS3310D
	060008	DLC Method, Reserved for CS3310D/8 channel
$0700nn		DLC Method, Reserved for CS3310D4

Bits 23-18 of the configuration represent Implementation method. The detailed information is as follows.

00: Host Method

If this option is selected, no method is provided for implementation of volume control. The correct values are computed into the Volume Status Registers, but these values are not useful in this case. It is assumed that host processor will provide an implementation of volume control.

01: Custom Method

If this option is selected, no implementation of volume control is provided directly by the Volume Manager, but an activation of an implementation is provided directly, and, thus an implementation is provided indirectly, via custom code provided by the user. The correct values are computed into the Volume Status register, and these values are passed to the custom code which has been “installed ” via the Code register in the post-processing control block.

02: Digital Level Control using the ADDS-1

03: Digital Level Control using the PCM1716

04: Digital Level Control using the CS3310

05: Digital Method

If this option is selected, volume control is provided via software within the Executive Programming Environment in the digital domain. The Digital Method of volume control requires that Volume Manager should be augmented by Digital Gain PPP.

Bits 15-8 represent the header of different implementation methods.

Bits 7-0 represent the channel count.

4.4.3 Subwoofer Manager

The Subwoofer Manager Post Processing Phase provides the capabilities to implement subwoofer management or bass management for 6 or 8 channel data within the Executive Programming Environment, as shown in Figure 4-3. It assumes that the channel mapping in use is made up of the Left, Right, Left Surround, Right Surround, Center, and LFE channels or the Left, Right, Left Surround, Right Surround, Center, LFE, Left Aux (Back), and Right Aux (Back) channels. These occupy the first 6 or 8 positions in the data block control list, while the other channels can be presented in the last 10/8 of the 16 positions that are the standard in Executive Programming Environment, These latter channels are not distributed by this PPP (i.e., the SWM can only work on the first 6 or 8 channels). At its output, the subwoofer Management produces 6 or 8 equivalent channels: Left, Right, Left Surround, Right Surround, Center, and Subwoofe,r or Left, Right, Left Surround, Right Surround, Center, Subwoofer, Left Aux (Back,) and Right Aux (Back).

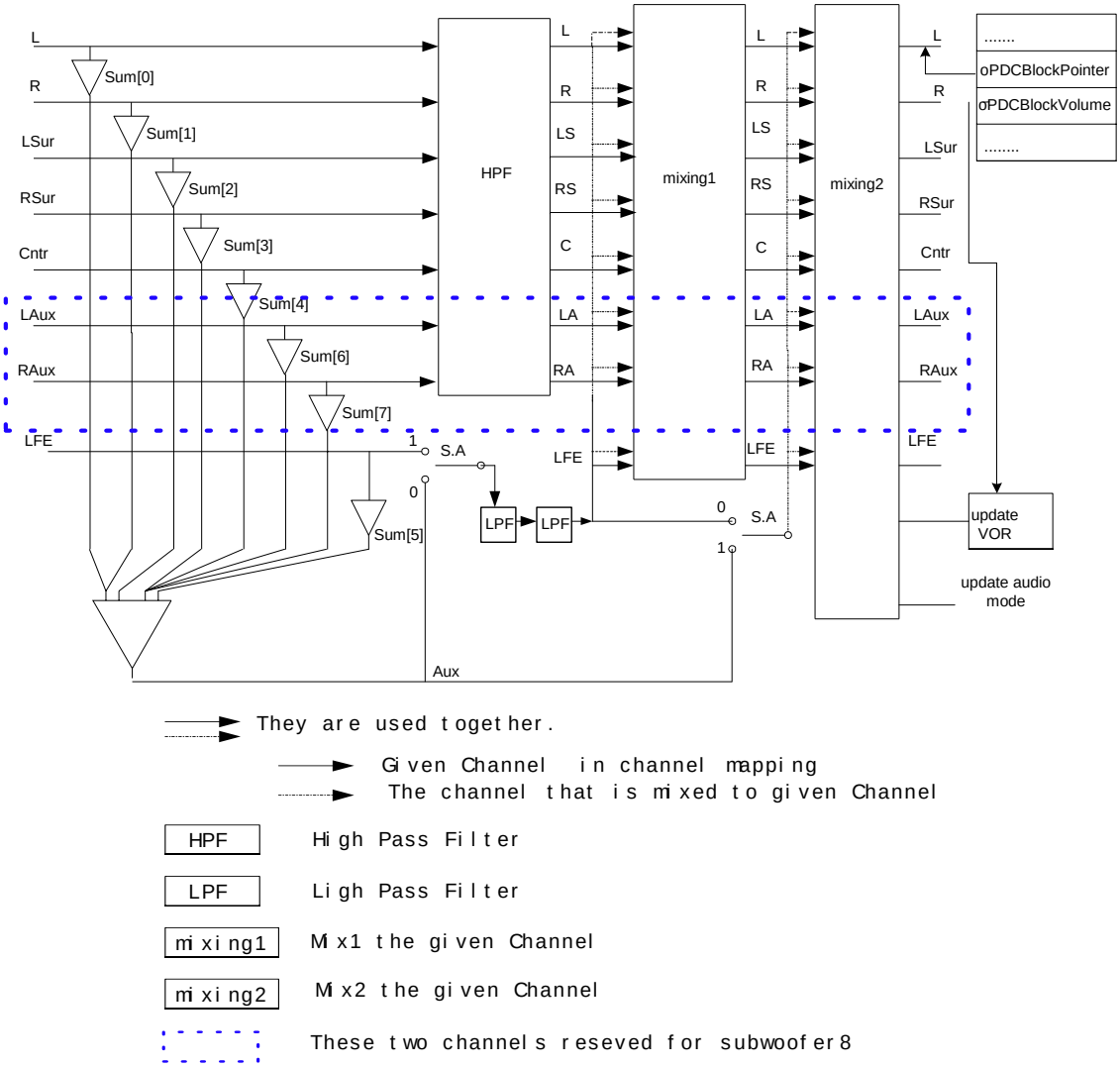


Figure 4-3 Subwoofer Manager Structure

4.4.4 Subwoofer Manager Status

The Subwoofer Manager Status Register reflects the actual subwoofer manager configuration, such as the concatenate mode, filter, and output configuration. The status is obtained by issuing the chirp command below with the result being equivalent to that shown in Figure 4-14.

Table 4-13 Subwoofer Manager Status Symbolic Opcodes

Symbol	Description	Value
getSWMStatus	Report status register value.	0xa98000

4.4.5 Subwoofer Manager Configuration

In the Subwoofer Manager Configuration Register, bits 0-7 represent Output Configuration; 8-15 represent cross filter frequency; 16 is “auto speaker” flag, and 17 is “auto pro logic” flag.

Output Configuration

The 56371A system supports both basic Dolby configurations and custom mode. The Subwoofer Manager Configuration Register[7:0] controls the output configuration mode.

Note that output configurations are different for the case where Pro Logic is active in auto pro logic mode.

Table 4-14 Output Configuration

Output Configuration Value		ProLogic Mode	Output Configuration Mode
Dolby configuration	0	OFF	Disable
	1		Dolby Configuration 0
	2		Dolby Configuration 1
	3		Dolby Configuration 2
	4		Dolby Configuration 2V2
	5		Dolby Configuration 3,small center with subwoofer
	6		Dolby Configuration 3,small center sans subwoofer
	7		Not use
	8	ON	Disable
	9		Pro Logic Configuration 0
	10		Pro Logic Configuration 1
	11		Pro Logic Configuration 2
	12		Pro Logic Configuration 2V2
	13		Dolby Configuration 3,small center with subwoofer
	14		Dolby Configuration 3,small center sans subwoofer
Custom mode	FF		Custom mode configuration

Crossover Filter Selection

Subwoofer Manager Configuration Register[15:8] controls the choice of the cross filter frequency as shown in the following table.

Table 4-15 Crossover Frequency Selection

Value	Cross Frequency
0	None
1	60 HZ
2	70 HZ
3	80 HZ
4	90 HZ
5	100 HZ
6	110 HZ
7	120 HZ
8	130 HZ
9	140 HZ
10	150 HZ
11	160 HZ
12	170 HZ
13	180 HZ
14	190 HZ
15	200 HZ
16	210 HZ
17	220 HZ

Concatenate Mode

Subwoofer Manager Configuration Register[23:16] decides the selection of concatenate modes. The 56371A system provides 4 concatenate modes to users: manual, auto speaker, auto pro logic, as well as auto all. Manual mode permits users to decide their configuration for the subwoofer manager freely. Auto speaker mode makes the configuration of the subwoofer manager under the control of speaker control. Note it is not in effect if speaker control is disabled. In auto pro logic mode, the subwoofer manager uses the special output configuration when Pro Logic is active. Auto all mode integrates the features of both auto speaker and auto pro logic mode.

Table 4-16 Subwoofer Manager Configuration Symbolic Opcodes

Symbol	Description	Value
SetSWMConfig	Set configuration register	0xc82601
SetSWMDisable	Disable subwoofer manager	0xe98400
setSWMConfigOutConDisable	Set output configuration, refer to Table 4-15.	0xe98500
setSWMConfigOutConDolby0		0xe98501
setSWMConfigOutConDolby1		0xe98502
setSWMConfigOutConDolby2		0xe98503
setSWMConfigOutConDolby2V2		0xe98504
setSWMConfigOutConDolby3NarrowCenterWithSubwoofer		0xe98505
setSWMConfigOutConDolby3NarrowCenterSansSubwoofer		0xe98506
setSWMConfigFilterNone	Select crossover filter, refer to Figure 4-15.	0xe98600
setSWMConfigFilter60Hz		0xe98601
setSWMConfigFilter70Hz		0xe98602
setSWMConfigFilter80Hz		0xe98603
setSWMConfigFilter90Hz		0xe98604
setSWMConfigFilter100Hz		0xe98605
setSWMConfigFilter110Hz		0xe98606
setSWMConfigFilter120Hz		0xe98607
setSWMConfigFilter130Hz		0xe98608
setSWMConfigFilter140Hz		0xe98609
setSWMConfigFilter150Hz		0xe9860a
setSWMConfigFilter160Hz		0xe9860b
setSWMConfigFilter170Hz		0xe9860c
setSWMConfigFilter180Hz		0xe9860d
setSWMConfigFilter190Hz		0xe9860e
setSWMConfigFilter200Hz		0xe9860f
setSWMConfigFilter210Hz		0xe98610
setSWMConfigFilter220Hz		0xe98611
SetSWMConfigModeManual	Set concatenate mode.	0xe98700
SetSWMConfigModeAutoSpeaker		0xe98701
SetSWMConfigModeAutoProLogic		0xe98702
SetSWMConfigModeAutoAll		0xe98703
GetSWMConfig	Report configuration register value	0xa98400

4.4.6 Subwoofer Manager Count Register

The Subwoofer Manager Count Register represents input-channel count, which can be 6 or 8.

Table 4-17 Subwoofer Manager Count Register Symbolic Opcodes

Symbol	Description	Value
setSWMChannelCount	Set count register value.	0xc82602

4.4.7 Subwoofer Manager HPF and LPF Operation Register

The HPF and LPF Function Registers are the pointers to the HPF and LPF algorithms in the system. Users are permitted to give the system their own algorithms. HPF and LPF Section Count Registers stipulate how many times HPF and LPF should be run.

Table 4-18 Subwoofer Manager HPF and LPF Operation Register Symbolic Opcodes

Symbol	Description	Value
setSWMHPFFunction	HPF Function Register	0xc82607
getSWMHPFFunction		0x882607
setSWMHPFFunction	LPF Function Register	0xc82608
getSWMLPFFunction		0x882608
setSWMHPFSectionCount_0	HPF Section Count Register	0xe9a700
getSWMHPFSectionCount		0xa9a700
setSWMLPFSectionCount_0	LPF Section Count Register	0xe9a600
getSWMLPFSectionCount		0xa9a600

4.4.8 Subwoofer Manager Coefficient Register

In Custom Mode, the subwoofer manager provide users with the mechanism to use their own coefficient table rather than that of the system. Users should switch the subwoofer manager to custom mode and then set the corresponding coefficient register.

Table 4-19 Subwoofer Manager Coefficient Register Symbolic Opcodes

Symbol	Description	Value
setSWMFilterMask	Mask registers inform subwoofer manager the processing channels in the respective algorithm.	0xc8260d
setSWMMix1Mask		0xc8260e
setSWMMix2Mask		0xc8260f
setSWMVORMask		0xc82638
getSWMFilterMask		0x88260d
getSWMMix1Mask		0x88260e
getSWMMix2Mask		0x88260f
getSWMVORMask		0x882638
setSWMSumGainLeft	Sum gain registers represent the gain coefficients for each channel.	0xc82610
setSWMSumGainRight		0xc82611
setSWMSumGainLSur		0xc82612
setSWMSumGainRSur		0xc82613
setSWMSumGainCenter		0xc82614
setSWMSumGainSubwoofer		0xc82615
setSWMSumGainLaux		0xc82616
setSWMSumGainRaux		0xc82617
getSWMSumGainLeft		0x882610
getSWMSumGainRight		0x882611
getSWMSumGainLSur		0x882612
getSWMSumGainRSur		0x882613
getSWMSumGainCenter		0x882614
getSWMSumGainSubwoofer		0x882615
getSWMSumGainLaux		0x882616
getSWMSumGainRaux		0x882617

Table 4-19 Subwoofer Manager Coefficient Register Symbolic Opcodes (Continued)

Symbol	Description	Value
setSWMMix1GainsLFE1	Mix1 gain registers represent the gain coefficients for each active channel and its respective LFE mixing in the mix1 processing.	0xc82618
setSWMMix1GainsActiveChannel		0xc82619
setSWMMix1GainsLFE2		0xc8261a
setSWMMix1GainsActiveChanne2		0xc8261b
setSWMMix1GainsLFE3		0xc8261c
setSWMMix1GainsActiveChanne3		0xc8261d
setSWMMix1GainsLFE4		0xc8261e
setSWMMix1GainsActiveChanne4		0xc8261f
setSWMMix1GainsLFE5		0xc82620
setSWMMix1GainsActiveChanne5		0xc82621
setSWMMix1GainsLFE6		0xc82622
setSWMMix1GainsActiveChanne6		0xc82623
setSWMMix1GainsLFE7		0xc82624
setSWMMix1GainsActiveChanne7		0xc82625
setSWMMix1GainsLFE8		0xc82626
setSWMMix1GainsActiveChanne8		0xc82627
getSWMMix1GainsLFE1		0x882618
getSWMMix1GainsActiveChannel		0x882619
getSWMMix1GainsLFE2		0x88261a
getSWMMix1GainsActiveChanne2		0x88261b
getSWMMix1GainsLFE3		0x88261c
getSWMMix1GainsActiveChanne3		0x88261d
getSWMMix1GainsLFE4		0x88261e
getSWMMix1GainsActiveChanne4		0x88261f
getSWMMix1GainsLFE5		0x882620
getSWMMix1GainsActiveChanne5		0x882621
getSWMMix1GainsLFE6		0x882622
getSWMMix1GainsActiveChanne6		0x882623
getSWMMix1GainsLFE7		0x882624
getSWMMix1GainsActiveChanne7		0x882625
getSWMMix1GainsLFE8		0x882626
getSWMMix1GainsActiveChanne8		0x882627

Table 4-19 Subwoofer Manager Coefficient Register Symbolic Opcodes (Continued)

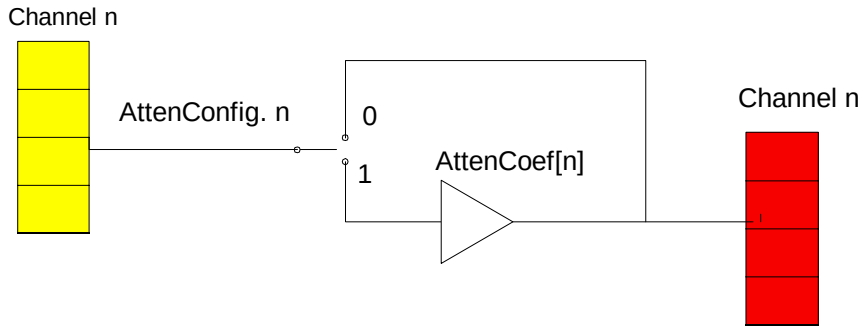
Symbol	Description	Value
setSWMMix2GainsLFE1	Mix2 gain registers represent the gain coefficients for each active channel and its respective LFE mixing in the mix2 processing.	0xc82628
setSWMMix2GainsActiveChannel		0xc82629
setSWMMix2GainsLFE2		0xc8262a
setSWMMix2GainsActiveChanne2		0xc8262b
setSWMMix2GainsLFE3		0xc8262c
setSWMMix2GainsActiveChanne3		0xc8262d
setSWMMix2GainsLFE4		0xc8262e
setSWMMix2GainsActiveChanne4		0xc8262f
setSWMMix2GainsLFE5		0xc82630
setSWMMix2GainsActiveChanne5		0xc82631
setSWMMix2GainsLFE6		0xc82632
setSWMMix2GainsActiveChanne6		0xc82633
setSWMMix2GainsLFE7		0xc82634
setSWMMix2GainsActiveChanne7		0xc82635
setSWMMix2GainsLFE8		0xc82636
setSWMMix2GainsActiveChanne8		0xc82637
getSWMMix2GainsLFE1		0x882628
getSWMMix2GainsActiveChannel		0x882629
getSWMMix2GainsLFE2		0x88262a
getSWMMix2GainsActiveChanne2		0x88262b
getSWMMix2GainsLFE3		0x88262c
getSWMMix2GainsActiveChanne3		0x88262d
getSWMMix2GainsLFE4		0x88262e
getSWMMix2GainsActiveChanne4		0x88262f
getSWMMix2GainsLFE5		0x882630
getSWMMix2GainsActiveChanne5		0x882631
getSWMMix2GainsLFE6		0x882632
getSWMMix2GainsActiveChanne6		0x882633
getSWMMix2GainsLFE7		0x882634
getSWMMix2GainsActiveChanne7		0x882635
getSWMMix2GainsLFE8		0x882636
getSWMMix2GainsActiveChanne8		0x882637

Table 4-19 Subwoofer Manager Coefficient Register Symbolic Opcodes (Continued)

Symbol	Description	Value
setSWMVORGains1	Complemented gains in VOR for each channel.	0xc82638
setSWMVORGains2		0xc82639
setSWMVORGains3		0xc8263a
setSWMVORGains4		0xc8263b
setSWMVORGains5		0xc8263c
setSWMVORGains6		0xc8263d
setSWMVORGains7		0xc8263e
setSWMVORGains8		0xc8263f
getSWMVORGains1		0x882639
getSWMVORGains2		0x88263a
getSWMVORGains3		0x88263b
getSWMVORGains4		0x88263c
getSWMVORGains5		0x88263d
getSWMVORGains6		0x88263e
getSWMVORGains7		0x88263f
getSWMVORGains8		0x882640

4.5 ATTENUATION MANAGER

The Attenuation Manager Post Processing Phase provides the capabilities required to implement digital attenuation in a standard manner for multi-channel data within the Executive Programming Environment.



AttenConfig.n Corresponding with channel N
0 means channel n is maskeD
1 means channel n is active
AttenCoef[n] The attenuation for active channel n

Figure 4-4 Attenuation Manager Structure

4.5.1 Attenuation Manager Status

The Attenuation Manager Status Register reports the number of active channels.

Table 4-20 Attenuation Manager Status Register Symbolic Opcodes

Symbol	Description	Value
getAttenStatus	Set status register value.	0x882100

4.5.2 Attenuation Manager Configuration

The Attenuation Manager Configuration Register reflects the channel mask for this processing.

Table 4-21 Attenuation Manager Configuration Register Symbolic Opcodes

Symbol	Description	Value
setAttenConfigMask	Set configuration register value.	0xc82101
getAttenConfigMask	Report configuration register value.	0x882101

4.5.3 Attenuation Manager Coefficients

The Attenuation Manager provides the attenuation coefficients to the active channels via the Attenuation Manager Coefficient Register.

Table 4-22 Attenuation Manager Coefficient Register Symbolic Opcodes

Symbol	Description	Value
setAttenValueActiveChan1	Set the coefficient for the respective active channel.	0xc82102
setAttenValueActiveChan2		0xc82103
setAttenValueActiveChan3		0xc82104
setAttenValueActiveChan4		0xc82105
setAttenValueActiveChan5		0xc82106
setAttenValueActiveChan6		0xc82107
setAttenValueActiveChan7		0xc82108
setAttenValueActiveChan8		0xc82109
getAttenValueActiveChan1	Report the coefficient for the respective active channel.	0x882102
getAttenValueActiveChan2		0x882103
getAttenValueActiveChan3		0x882104
getAttenValueActiveChan4		0x882105
getAttenValueActiveChan5		0x882106
getAttenValueActiveChan6		0x882107
getAttenValueActiveChan7		0x882108
getAttenValueActiveChan8		0x882109

4.6 DE-EMPHASIS MANAGER

De-emphasis is often used to compensate for the Pre-emphasis process. Pre-emphasis is an intentional change made in the frequency response of a recording system to improve the signal-to-noise ratio or to reduce distortion. Typically, a high-frequency boost is used during recording, followed by complementary de-emphasis (a high-frequency cut) during playback. Users are allowed to open or close De-emphasis manager by setting configuration register.

Table 4-23 De-Emphasis Manager Configuration Register Symbolic Opcodes

Symbol	Description	Value
setDeemphasisConfigDisable	Disable De-emphasis	0xecc400
setDeemphasisConfigEnable	Enable De-emphais	0xecc402
getDeemphasisConfig	Report configuration register value.	0xacc400
gotDeemphasisConfigDisable		0x000000
gotDeemphasisConfigEnable		0x000002

4.7 DOUBLE RATE MANAGER

The Double Rate Manager Post Processing Phase provides the capabilities required to implement Double Rate control in a standard manner for multi-channel data within the Executive Programming Environment. Note that, in fact, there are two Double Rate Managers in the DSP56371A system called the Input and Output Double Rate Manager. Refer to Section 2.3.9, *Sample Rate Support*.

4.7.1 Double Rate Manager Status

Table 4-24 Double Rate Manager Register Symbolic Opcodes

Symbol	Description	Value
getDRIStatus	Report double rate manager status for input	0x883b00
gotDRIStatusUninitialized	Un-initialized	0x000000
gotDRIStatusDisabled	Disabled	0x000001
gotDRIStatusInactiveSampleRateUnsupported	Enabled but inactive as input sample rate is not supported.	0x000002
gotDRIStatusInactiveBufferSizeError	Enabled but inactive as buffers are too small	0x000003
gotDRIStatusInactiveTransmitterEngaged	Enabled but inactive as transmitter already started.	0x000004
gotDRIStatusInactiveDecoderUnsupported	Enabled but inactive as input decoder type is not supported.	0x000005
gotDRIStatusInactiveSampleRateNotDoubled	Enabled but inactive as input rate change not needed.	0x000006
gotDRIStatusActive	Enable and active.	0x000080
getDROStatus	Report double rate manager status for output	0x883c00
gotDROStatusUninitialized	Un-initialized	0x000000
gotDROStatusDisabled	Disabled	0x000001
gotDROStatusInactiveSampleRateUnsupported	Enabled but inactive as output sample rate is not supported.	0x000002
gotDROStatusInactiveBufferSizeError	Enabled but inactive as buffers are too small	0x000003
gotDROStatusInactiveTransmitterEngaged	Enabled but inactive as transmitter already started.	0x000004
gotDROStatusInactiveDecoderUnsupported	Enabled but inactive as output decoder type is not supported.	0x000005
gotDROStatusInactiveSampleRateNotDoubled	Enabled but inactive as output rate change not needed.	0x000006
gotDROStatusActive	Enable and active.	0x000080

4.7.2 Double Rate Manager Configuration

The Double Rate Manager has two sections: input and output double rate control, each of which should be controlled independently.

Table 4-25 Double Rate Manager Configuration Symbolic Opcodes

Symbol	Description	Value
setDRIConfig	Set input double rate manager configuration register value.	0xc83b01
setDRIConfigEnable	Enable input double rate manager.	0xeec711
setDRIConfigDisable	Disable input double rate manager.	0xeec710
setDRIConfigChannelMask0None	Set channel mask for input double rate manager.	0xeec500
setDRIConfigChannelMaskLeftRight		0xeec503
setDRIConfigChannelMaskSurround		0xeec50c
setDRIConfigChannelMaskCenterSubwoofer		0xeec530
setDRIConfigChannelMaskAuxiliary		0xeec5c0
setDRIConfigChannelMask1None		0xeec600
setDRIConfigChannelMaskSecondary		0xeec603
getDRIConfig	Report input double rate manager configuration register value.	0x883b01
getDRIConfigChannelMask0	Report the channel mask set in input double rate configuration register	0xaec500
getDRIConfigChannelMask1		0xaec600
setDROConfig	Set output double rate manager configuration register value. (refer to input double rate manager configuration register)	0xc83c01
setDROConfigModeDisable	Disable output double rate manager	0xef0700
setDROConfigModeEnable	Enable output double rate manager	0xef0701
getDROConfig	Report output double rate manager configuration register value.	0x883c01

4.8 PRO LOGIC II PPP

The ProLogic II Post-Processing Phase provides the capabilities required to implement Pro Logic II matrix surround decoding within the Executive Programming Environment. Pro Logic II matrix decoding is the process of deriving 5 full bandwidth from a 2-channel input. The 5-decoded-channesl are then processed according to the corresponding audio mode. The 2-channel input can be either one of L/R, Lt/Rt, Lu/Ru, and Lo/Ro while the output audio mode can be 03, 04, 05, 06, 07.

Table 4-26 Signal Processing in Pro Logic PPP

Output audio mode (Not include “bass”)	2-channel-input	5-decoded-channel	X-channel-output
03 (L, C, R)	Lo/Ro, Lu/Ru &Lt/Rt	L/C/R/Ls/Rs	L’=L, R’=R, C’=C
04 (L, R, S)			L’= L+C*(-3dB) R’ = R + C*(-3dB) S = Ls*(-3dB)+Rs*(-3dB)
05 (L, C, R, S)			L’=L, R’=R, C’=C S = Ls*(-3dB)+Rs*(-3dB)
06 (L, R, Ls, Rs)			L’= L+C*(-3dB) R’ = R + C*(-3dB) Ls’=Ls, Rs’ =Rs
07 (L, C, R, Ls, Rs)			L’=L, R’=R, C’=C Ls’=Ls, Rs’ =Rs

4.8.1 Pro Logic II PPP Status

Pro Logic II PPP Status Register remembers the first error after running the PPP program. This allows the register to be checked in case of an error.

Table 4-27 Pro Logic II PPP Status Register Symbolic Opcodes

Symbol	Description	Value
getPLStatus	Set status register value.	0x881c00
gotPLStatusActive	PPP is running successful	0x040000
gotPLStatusDisabled	PPP is disabled.	0x7f0081
gotPLStatusLevel	Exit for source not reaching control condition.	0x7f0082
gotPLStatusNoProc	Exit for unsuitable audio mode.	0x7f0083

4.8.2 Pro Logic II PPP Configuration

The Pro Logic II PPP Configuration Register determines what type of signals are to be processed by the PLII PPP: surround-encoded stereo audio mode only, stereo mode, non-surround-encoded stereo audio mode or anything but noise.

Table 4-28 Pro Logic II PPP Configuration Register Symbolic Opcodes

Symbol	Description	Value
setPLConfigDisable	Disable Pro Logic II	0xe70400
setPLConfigEnableLtRtOnly	Enable for surround-encoded stereo audio mode only	0xe70401
setPLConfigEnableNotLoRo	Enable for stereo	0xe70402
setPLConfigEnableStereo	Enable for no surround-encoded stereo audio mode	0xe70403
setPLConfigForce	Enable for non-noise	0xe70404
getPLConfig	Report configuration register value	0x881c01

4.8.3 Pro Logic II PPP Standard Mode

The flexibility of Pro Logic II allows it to be tailored for specific applications. “Movie” mode is used as default mode with all other modes being optional. The following table summarizes the feature of the standard Pro Logic II modes.

Table 4-29 Standard Pro Logic II Modes and Features

Parameter / Modes	Movie	Music	Virtual	Pro Logic	Matrix	Custom
Panorama mode	Off	Option	Off	Off	Off	Option
Dimension control	Off	Option	Off	Off	Off	Option
Center Width control	Off	Option	Off	Off	Off	Option
Surround delay	10-25 ms	0-15 ms	None	10-25 ms	0-15 ms	Option
Surround filter	No	Shelf	None	7 kHz LPF	Shelf	Option
Auto balance	On	Off	On	On	Off	Option

Panorama Mode

This extends the front stereo image to include the surround speakers for an exciting “wraparound” effect with sidewall imaging.

Dimension Control

This allows the user to gradually adjust the sound field either towards the front or towards the rear. This can be useful to help achieve a more suitable balance from all the speakers with certain recordings.

Center Width Control

The Center Width control allows the steered decoder center output signal to be mixed to the left and right (L and R) outputs. At one extreme, there is no signal from the Center (C) output, and all C information is carried in L and R outputs at -3 dB to maintain the same acoustic power (aka, phantom center mode). At the other extreme, all of the information is carried in the Center output and is not present in the L and R outputs.

Surround Time Delay

Car products need only enough delay for the worst case seating and speaker arrangement. For example, a rear seat passenger with the rear speakers very close, and the front speakers some 5 feet ahead would need 5ms delay to equalize the arrival times. The Music mode would then need a maximum of 5ms delay, and the Movie mode would need up to 15 ms.

For a home decoder, the surround delay range in Music mode needs to cover 0–15 ms, the same as for Dolby Digital, as the goal of coincident arrivals from all speakers to the listening area is the same. For Movie mode, the goal is 10 ms of additional delay to invoke the Haas precedence effect, so the delay range needs to cover 10–25 ms.

Surround Filter

There is a mild high-frequency shelf filter provided in the surround channels for Music mode. It results in a more natural, believable sound field, since ambient sounds normally have a high-frequency roll off induced by room reflections and absorption.

Auto Balance

This is used to track out and adjust mismatches between Lt and Rt. The auto balance is turned off in Music mode as some recordings may intentionally have the center channel audio off center.

Table 4-30 Pro Logic II PPP Mode Register Symbolic Opcodes

Symbol	Description	Value
setPL2ModeProLogic	Set the corresponding mode.	0xe71500
setPL2ModeVirtual		0xe71501
setPL2ModeMusic		0xe71502
setPL2ModeMovie		0xe71503
setPL2ModeMatrix		0xe71504
setPL2ModeCustom		0xe71507
setPL2ModeMusicPanorama		0xe71512
setPL2ModeCustomPanorama		0xe71517
getPL2Mode	Report mode register value.	0xa71500
gotPL2ModeProLogic	The corresponding mode.	0x000000
gotPL2ModeVirtual		0x000001
gotPL2ModeMusic		0x000002
gotPL2ModeMovie		0x000003
gotPL2ModeMatrix		0x000004
gotPL2ModeCustom		0x000007
gotPL2ModeMusicPanorama		0x00000a
gotPL2ModeCustomPanorama		0x00000f

4.8.4 Pro Logic II PPP Center Width Control

The Center Width control allows the steered decoder center output signal to be mixed to the left and right (L and R) outputs. The DSP56371A system has eight center width control choices listed in the below table.

Table 4-31 Center Width Control Table

Name	Description
PL2CenterWidth0	L'=L; R'=R;C'=C
PL2CenterWidth1	L'=L+C*sin(20.8)*(-3dB) R'=R+C*sin(20.8)*(-3dB) C'= C*cos(20.8)
PL2CenterWidth2	L'=L+C*sin(28)*(-3dB) R'=R+C*sin(28)*(-3dB) C'= C*cos(28
PL2CenterWidth3	L'=L+C*sin(36)*(-3dB) R'=R+C*sin(36)*(-3dB) C'= C*cos(36)
PL2CenterWidth4	L'=L+C*cos(36)*(-3dB) R'=R+C*cos(36)*(-3dB) C'= C*sin(36)
PL2CenterWidth5	L'=L+C*cos(28)*(-3dB) R'=R+C*cos(28)*(-3dB) C'= C*sin(28)
PL2CenterWidth6	L'=L+C*cos(20.8)*(-3dB) R'=R+C*cos(20.8)*(-3dB) C'= C*sin(20.8)
PL2CenterWidth7	L'=L+C*(-3dB) R'=R+C*(-3dB) C'= 0

Table 4-32 Pro Logic II PPP Center Width Control Register Symbolic Opcodes

Symbol	Description	Value
setPL2CenterWidth0	The respective center width control mode.	0xe71600
setPL2CenterWidth1		0xe71601
setPL2CenterWidth2		0xe71602
setPL2CenterWidth3		0xe71603
setPL2CenterWidth4		0xe71604
setPL2CenterWidth5		0xe71605
setPL2CenterWidth6		0xe71606
setPL2CenterWidth7		0xe71607
getPL2CenterWidth	Report center width control register value.	0xa71600

4.8.5 Pro Logic II PPP Dimension Control

DSP56371A system provides seven dimension control modes to users, listed in the below table.

Table 4-33 Dimension Control Table

Name	Description
Dimension0	Lt' = Lt - 0.1875 (Lt+Rt) Rt' = Rt - 0.1875 (Lt+Rt)
Dimension1	Lt' = Lt - 0.125 (Lt+Rt) Rt' = Rt - 0.125 (Lt+Rt)
Dimension2	Lt' = Lt - 0.0625 (Lt+Rt) Rt' = Rt - 0.0625 (Lt+Rt)
Dimension3	Lt'=Lt Rt'=Rt
Dimension4	Lt' = Lt - 0.0625 (Lt-Rt) Rt' = Rt - 0.0625 (Lt-Rt)
Dimension5	Lt' = Lt - 0.125 (Lt-Rt) Rt' = Rt - 0.125 (Lt-Rt)
Dimension6	Lt' = Lt - 0.1875 (Lt-Rt) Rt' = Rt - 0.1875 (Lt-Rt)

Table 4-34 Pro Logic II PPP Dimension Control Register Symbolic Opcodes

Symbol	Description	Value
setPL2Dimension0	The respective dimension control mode.	0xe71700
setPL2Dimension1		0xe71701
setPL2Dimension2		0xe71702
setPL2Dimension3		0xe71703
setPL2Dimension4		0xe71704
setPL2Dimension5		0xe71705
setPL2Dimension6		0xe71706
getPL2Dimension	Report dimension control register value.	0xa71700

4.8.6 Pro Logic II PPP Auto Balance Control

Table 4-35 Pro Logic II PPP Auto Balance Control Register Symbolic Opcodes

Symbol	Description	Value
setPL2AutobalanceDisable	Disable auto balance.	0xe71900
setPL2AutobalanceEnable	Enable auto balance.	0xe71901
getPL2Autobalance	Report auto balance control register value.	0xa71900

4.8.7 Pro Logic II PPP Matrix Coefficients

Table 4-36 Pro Logic II PPP Matrix Coefficient Register Symbolic Opcodes

Symbol	Description	Value
setPL2MatrixCoefs0	Only for PL2 mode.	0xe71a00
setPL2MatrixCoefs1	All modes but PL2 mode.	0xe71a01
setPL2MatrixCoefs2	For panorama mode	0xe71a02
getPL2MatrixCoefs	Report matrix coefficient register value.	0xa71a00

4.8.8 Pro Logic II PPP Surround Filter Choice

Table 4-37 Pro Logic II PPP Surround Filter Register Symbolic Opcodes

Symbol	Description	Value
setPL2WideSurround	No Surround Filtering	0xe71d00
setPL2LPFSurround	7kHz Low Pass Filter	0xe71d01
setPL2ShelfSurround	Shelving Filter	0xe71d02
getPL2SurroundFilter	Report surround filter choice register value.	0xa71d00

4.8.9 Pro Logic II PPP Right Surround Polarity Control

Table 4-38 Pro Logic II PPP Right Surround Polarity Control Register Symbolic Opcodes

Symbol	Description	Value
setPL2RsPolarityInverseDisable	Normal Polarity	0xe71e00
setPL2RsPolarityInverseEnable	Invert Polarity	0xe71e01
getPL2RsPolarityInverse	Report right surround filter polarity control register value.	0xa71e00

4.8.10 Pro Logic II PPP Surround Delay Control

Table 4-39 Pro Logic II PPP Surround Delay Control Register Symbolic Opcodes

Symbol	Description	Value
setPL2SurroundDelayDisable	Disable 10 ms delay	0xe71f00
setPL2SurroundDelayEnable	Enable 10 ms delay	0xe71f01
getPL2SurroundDelay	Report surround delay control register value.	0xa71f00

Note that autobalance, filter choice, polarity contro,l and delay control commands will only take effect in costom mode. Refer to Table 4-29 to determine which controls are available for particular modes.

4.9 DTS LOGIC PPP (also known as DTS-ES Neo6)

The DTS Logic (Neo6) PPP can be applied to non DTS-encoded bit streams in encoded and not encoded stereo audio modes, i.e., audio mode 2/0 encoded or not encoded. This is valid unless DTS Logic PPP is forced to run. If it is forced to run it will do so regardless of audio mode. Note that it cannot be forced to run

for DTS-encoded bit streams. The DTS Logic PPP uses the Neo:6 algorithm to provide capabilities for generation of up to 8 channels of output. It allows two modes for selecting the optimum decoding for the signal source.

Normal Mode (also known as Movie or Cinema Mode)

This mode is optimum for playing movies. Decoding is performed with emphasis on separation performance to achieve the same atmosphere with 2-channel sources as with 6.1 channel sources. This mode is effective for playing sources recorded in conventional surround formats as well, because the in-phase component is assigned mainly to the center channel and the reversed phase component to the surround (SL, SR and SB) channels.

Music Mode

This mode is suited mainly for playing music. The front (L and R) channel signals bypass the decoding process and are played directly. These two channel signals are output after being subtracted from by a center signal that has been scaled down, so there is no loss of sound quality, and the effect of the surround signals output from the center (C) and surround (SL, SR, and SB) channels add a natural sense of expansion to the sound field. In music mode, Stereo non-matrix recordings are expanded into the five- or six-channel layout, in a way, which does not diminish the subtlety, and keeps the integrity of the original stereo recording.

4.9.1 DTS Logic PPP Status

DTS Logic PPP Status Register informs the error happening at the PPP running.

Table 4-40 DTS Logic PPP Status Register Symbolic Opcodes

Symbol	Description	Value
getDTSLogStatus	Report status register value.	0x883a00
gotDTSLogStatusActive	PPP is running successful	0x050000
gotDTSLogStatusDisabled	PPP is disabled.	0x700081
gotDTSLogStatusLevel	Exit as source not reaching control condition.	0x700082
gotDTSLogStatusNoProc	Exit as unsuitable audio mode.	0x700083
gotDTSLogStatusDecoder	Exit as DTS source.	0x700084
gotDTSLogStatusSampleRate	Exit as sample rate is too high (greater than 48k).	0x700085

4.9.2 DTS Logic PPP Configuration

Table 4-41 DTS Logic PPP Configuration Register Symbolic Opcodes

Symbol	Description	Value
setDTSLogConfigDisable	Disable DTS Logic PPP.	0xee8500
setDTSLogConfigEnableLtRt	Enable DTS Logic PPP for encoded stereo material.	0xee8501

Table 4-41 DTS Logic PPP Configuration Register Symbolic Opcodes

Symbol	Description	Value
setDTSLogConfigEnableLuRu	Enable DTS Logic PPP for unknown stereo material.	0xee8502
setDTSLogConfigEnableLoRo	Enable DTS Logic PPP for non-encoded stereo material (as well as encoded stereo).	0xee8503
setDTSLogConfigForce	Force DTS Logic PPP to be enabled regardless of input audio mode in use.	0xee8504
getDTSLogConfig	Report configuration register value	0x883a01

4.9.3 DTS Logic PPP Mode

Table 4-42 DTS Logic PPP Mode Register Symbolic Opcodes

Symbol	Description	Value
setDTSLogConfigNormalMode	Enable normal (cinema) mode.	0xee8600
setDTSLogConfigMusicMode	Enable music mode.	0xee8601
getDTSLogConfigMode	Report mode register value.	0xae8600

4.9.4 DTS Logic PPP Center Gain

In the music mode, the data in the left and right channel should be modified via the following equation

Left = Left - Center * Cgain

Right = Right – Center * Cgain

Table 4-43 DTS Logic Center Gain Register Symbolic Opcodes

Symbol	Description	Value
setDTSLogMDCBCgain	Set center gain register value.	0xc83a12
getDTSLogMDCBCgain	Report center gain register value.	0x883a12

4.10 DTS ES MATRIX 6.1 PPP

The DTS ES Matrix 6.1 PPP can be applied to non DTS-encoded bit streams in encoded and not encoded stereo-surround audio modes. The audio modes for which this is supported are 2/2 and 3/2 unless DTS ES Matrix 6.1 PPP is forced to run. If it is forced to run it will do so regardless of audio mode. Note that it cannot be forced to run for DTS encoded bit streams. DTS ES Matrix 6.1 PPP uses the Neo:6 algorithm to provide capabilities for generation of 7 or 8 channels of output.

4.10.1 DTS ES Matrix 6.1 PPP Status

The DTS ES Matrix 6.1 PPP Status Register remembers the first error after running the PPP. This allows the register to be checked in the case of an error.

Table 4-44 DTS ES Matrix 6.1 PPP Status Register Symbolic Opcodes

Symbol	Description	Value
getDTSMatrStatus	Report status register value.	0x883900
gotDTSMatrStatusActive	PPP is running successful	0x050000
gotDTSMatrStatusDisabled	PPP is disabled.	0x700081
gotDTSMatrStatusLevel	Exit for source not reaching control condition.	0x700082
gotDTSMatrStatusNoProc	Exit for unsuitable audio mode.	0x700083
gotDTSMatrStatusDecode	Exit for DTS source.	0x700084
gotDTSMatrStatusSampleRate	Exit for the high sample rate (greater than 48k).	0x700085

4.10.2 DTS ES Matrix 6.1 PPP Configuration

Table 4-45 DTS ES Matrix 6.1 PPP Configuration Register Symbolic Opcodes

Symbol	Description	Value
setDTSMatrConfigDisable	Disable DTS ES Matrix 6.1 PPP.	0xee4400
setDTSMatrConfigEnableLtRt	Enable DTS ES Matrix 6.1 PPP for encoded stereo-surround material.	0xee4401
setDTSMatrConfigEnableLuRu	Enable DTS ES Matrix 6.1 PPP for unknown stereo-surround material.	0xee4402
setDTSMatrConfigEnableLoRo	Enable DTS ES Matrix 6.1 PPP for non-encoded stereo-surround material.	0xee4403
setDTSMatrConfigForce	Force DTS ES Matrix 6.1 PPP to be enabled regardless of input audio mode in use.	0xee4404
getDTSMatrConfig	Report configuration register value.	0x883901

4.11 SURROUND EX

The Surround EX PPP can be applied to the bit streams in encoded and not encoded stereo-surround audio modes. The audio modes for which this is supported are 2/2 and 3/2 unless the Surround EX PPP is forced to run when it will do so regardless of audio mode taking whatever content is on the surround channels in that mode as it's input. The Surround EX PPP uses the ProLogic II algorithm to provide capabilities for generation of 7 or 8 channels of output.

4.11.1 Surround EX PPP Status

The Surround EX PPP Status Register remembers the first error after running the PPP. This allows the register to be checked in the case of an error.

Table 4-46 Surround EX PPP Status Register Symbolic Opcodes

Symbol	Description	Value
getSurroundEXStatus	Report status register value.	0x883d00
gotSurroundEXStatusActive	PPP is running successfully	0x040000
GotSurroundEXStatusDisabled	PPP is disabled	0x700081
gotSurroundEXStatusLevel	Exit as source did not reach control condition.	0x700082
gotSurroundEXStatusNoProc	Exit as unsuitable audio mode.	0x700083

4.11.2 Surround EX Configuration

Table 4-47 Surround EX PPP Configuration Register Symbolic Opcodes

Symbol	Description	Value
SetSurroundEXConfigDisable	Disable Surround EX PPP.	0xef4400
setSurroundEXConfigEnableLtRt	Enable Surround EX PPP for encoded stereo-surround material.	0xef4401
setSurroundEXConfigEnableLuRu	Enable Surround EX PPP for unknown stereo-surround material.	0xef4402
setSurroundEXConfigEnableLoRo	Enable Surround EX PPP for non-encoded stereo-surround material.	0xef4403
setSurroundEXConfigForce	Force Surround EX PPP to be enabled regardless of input audio mode in use.	0xef4404
GetSurroundEXConfig	Report configuration register value.	0x883d01

Section 5
Input / Output Drivers

5.1 OVERVIEW

Within the Software Architecture, the Input Driver operates on a data stream being brought into the system. The primary task of the input driver is to parse and buffer the input data streams into an optimized input buffer of encoded audio data for proper decoder processing. Input drivers are therefore typically tightly coupled and unique for each decoder. However, the overall abstract purpose for an input driver remains the same regardless of decoder and, therefore, is presented as a unique functional block.

The currently supported input data streams are:

- Interleaved Primary Stereo (PCM)
- IEC 958 Standard for encoded bit streams

The DSP56371A uses the ESAI as the source for the input driver, the ESAI receiver works in slave mode with SDI1operating as the input data pin and SDI0 as the auxiliary input data pin.

The Output Driver takes the data in the output buffer after it has passed through the post processing chain and performs the proper output sequencing and delivery out of the processor/system. Typically, the output driver is configured to deliver data to one or more D/A converters.

The ESAI transmitter is the output peripheral used to stream out the processed data. It operates in master mode by default, but the user can change the TCCR register to have it work in slave mode instead. SDO0, SDO3 and SDO5 are the output data pins.

Before the input or output driver are started, a special subroutine, called an event handler can be designed to do some input or output related configuration by the customer. This handler could trigger a GPIO pin, send a word through GPIO, or set a flag in DSP memory, which could be polled by the host controller. There are two event handlers, one is for the input driver, and the other is for the output driver. For the 56371A, the user can fill the entry address of event handler for input or output driver in $11d and $12d of P memory, respectively, to realize these functions.

Input Format Control

The format of the input processed by the DSP56371A is controlled by the Receiver Control Registers; these refer to the Receiver Clock Control Register and the Receiver Control Register. These registers are used to implement a register-based input format control, Peripheral Receiver Control. In addition, another form of input format control is used that does not involve registers, Direct Receiver Control.

Peripheral Receiver Control

These registers are written directly with values used for IEC 60958 and 61937 input. Such write operations should be executed only when the DSP56371A is in a non-decoding state, such as during HLX initialization or during operation with an illegal HLX Source Mode. The values written to these registers apply to decoding of all subsequent IEC input for that peripheral. These registers are initialized with default values appropriate for use with many industry-standard devices, referred to here as the Standard IEC values. These values are listed in Table 5-2, and they can be determined for the active system using the opcodes presented in Table 5-1.

Table 5-1 Peripheral Receiver Control Symbolic Opcodes

Symbol	Description	Value
setRCCR	Set control register value.	0xc1ffb8
setRCR		0xc1ffb7
setRCCR_1		0xc2ff98
setRCR_1		0xc2ff97
getRCCR	Report control register value.	0x81ffb8
getRCR		0x81ffb7
getRCCR_1		0x82ff98
getRCR_1		0x82ff97

Table 5-2 Receiver Control Register Values

Peripheral	Name	Register	Value
ESAI	Standard IEC	RCCR	0x0c0200
		RCR	0x717d00
	Standard PES	RCCR	0x0c0000
		RCR	0x500902
	SPI	RCCR	0x080000
		RCR	0x500902
	CXD Form 1	RCCR	0x040200
		RCR	0x507d82
	CXD Form 2	RCCR	0x040200
		RCR	0x507d02
ESAI_1	Standard IEC	RCCR_1	0x0c0200
		RCR_1	0x017d00
	Standard PES	RCCR_1	0x0c0000
		RCR_1	0x000900
	SPI	RCCR_1	0x080000
		RCR_1	0x000900
	CXD Form 1	RCCR_1	0x040200
		RCR_1	0x007d80
	CXD Form 2	RCCR_1	0x040200
		RCR_1	0x007d00

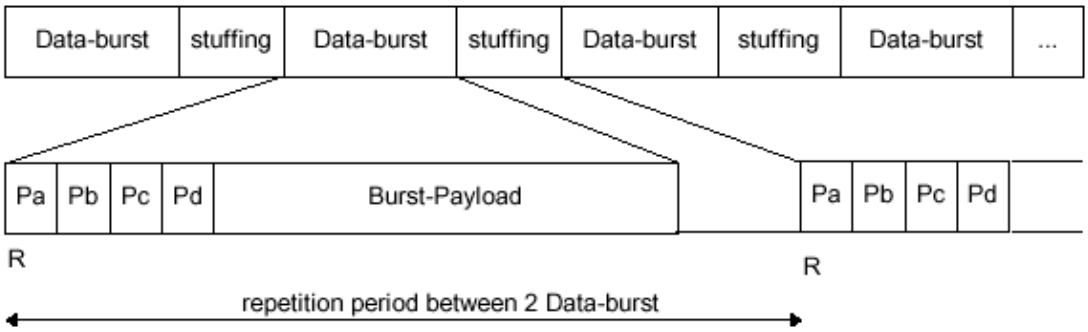
Note: Note that 56371A does not support any form of asynchronous input, such as PES, PES CXD, ES, or ES-SPI.

Direct Receiver Control

With a Source Mode of Auto,the LLX Input Status is selected automatically by the system. With a Source Mode other than Auto, the LLX Input Status should be selected by the host manually. See section 3.2.4. These opcodes will not affect operation of the system until an LLX restart occurs, either as a result of changes in the input bit stream or in response to an LLX configuration command.

5.2 IEC958 INPUT DRIVER

The IEC958 Standard specifies a way in which the IEC958 interface may be used to convey bit-streams such as AC-3 and DTS, etc. The non-PCM encoded audio bit-stream transported over this interface is formed into a sequence of data-bursts. Each data-burst consists of 4 16-bit preambles, followed by the burst-payload data and stuffing data, showed in Figure 5-1. Every 16 bits of data-burst are packed into an IEC958 sub-frame.



(Pa -- sync word 1; Pb -- sync word 2; Pc -- burst-info; Pd -- burst-length)

Figure 5-1 Structure of Data-Burst

This input driver is used to receive the 16-bit serial data from ESAI Receive Channel 1 and transfer them to the input buffer. (The IEC958 data streams have been unpacked to 16-bit serial data by the IEC958 Receiver chip before entering into DSP ESAI.)

5.3 DTS-CD (14-BIT) INPUT DRIVER

Substituting encoded data for the stereo 16 bit linear PCM track, DTS Digital Surround® CDs carry up to 5.1 discrete channels of 24 bit music content. The multi-channel music material is encoded using a bit rate up to 1,234 kbps at the standard CD sampling rate of 44.1 kHz.

Generally, the DTS bit-stream is stored in 16 bit words, but when encoding for CD, in order to diminish the noise output level resulting from the DTS bit-stream being mistakenly played back as PCM format, the DTS bitstream can be stored only in the least significant 14 bits of a 16 bit word. The most significant 2 bits are not used.

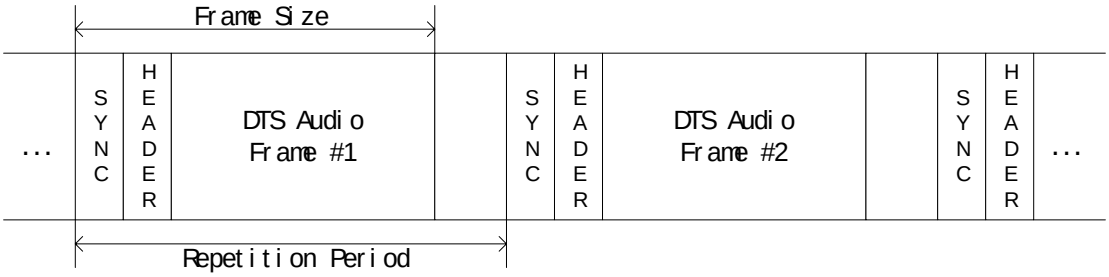


Figure 5-2 DTS-CD Bit Stream

This module is used to receive a “14-bit” formatted DTS-CD bit stream from ESAI Receive Channel 1 and transfer it to the input buffer.

5.4 DTS-CD (16-BIT) INPUT DRIVER

DTS-CD format is as described above, but this module is used to receive a “16-bit” formatted DTS-CD bit stream from ESAI Receive Channel 1 and transfer it to the input buffer.

5.5 SECONDARY/AUXILIARY PCM INPUT DRIVER

5.5.1 Secondary/Auxiliary PCM Status

The Secondary or Auxiliary PCM Input allows PCM data input at the ESAI SDI0 data pin to be clocked into the DSP for processing using the same clocks as used for the bit-stream input at the ESAI SDI1 data pin. This primary bit-stream input may be of either a synchronous, encoded (*i.e.*, Dolby Digital) format or a synchronous, non-encoded (*i.e.*, PCM) format, but it cannot be of an asynchronous, encoded format (*i.e.*, PES). The format of this PCM input should be the same as that used for PCM input on the ESAI SDI1 data pin. The DSP56371A supports both interrupt-driven and DMA-driven software for secondary/Auxiliary PCM input.Secondary/Auxiliary PCM Status.

Table 5-3 Secondary / Auxiliary PCM Status Symbolic Opcodes

Symbol	Description	Value
getRY0Status	Return status register value for this bitmapped register.	0x881600
gotRY0StatusNotInstalled	Indicates that input driver is not properly installed.	0x0dead0
gotBitRY0StatusFail	Bit 23 indicates that a fatal error has occurred, and the driver is disabled.	0x800000

Table 5-3 Secondary / Auxiliary PCM Status Symbolic Opcodes (Continued)

Symbol	Description	Value
gotBitRY0StatusFailUnspecified	If no other failure bit is set, this indicates an unspecified error condition. This can occur, for example, during mode changes.	0x000000
gotBitRY0StatusFailEnabledOther	Bit 22 indicates that the peripheral is in use by some other input driver.	0x400000
gotBitRY0StatusFailOverrun	Bit 21 indicates that the receive data register of the peripheral has been overwritten (an internal error).	0x200000
gotBitRY0StatusFailOverflow	Bit 20 indicates that the input buffer has overflowed, most likely because the attached device did not respond to the READY signal.	0x100000
gotBitRY0StatusFailUnderflow	Bit 19 indicates that the input buffer has underflowed, and the input driver has been disabled	0x 080000
gotBitRY0StatusFailDoubleWrap	Bit 18 indicates that the input buffer has wrapped around, and the input driver has been disabled.	0x 040000
gotBitRY0StatusFailDisabled	Bit 17 indicates that the input driver has been disabled.	0x020000
gotBitRY0StatusFailUninitialized	Bit 16 indicates that the input driver has been initialized but is not running.	0x010000
gotBitRY0StatusWarnOverflow	Bit 8 indicates that overflow has occurred and input has been lost, but the driver continues to operate.	0x000100
gotBitRY0StatusInternalBits	Bits 0–7 flag internal processing states and should be ignored.	0x 0000ff

5.5.2 Secondary/Auxiliary PCM Configuration

Table 5-4 Secondary / Auxiliary PCM Configuration Symbolic Opcodes

Symbol	Description	Value
setRY0Config	Set control register value as 24-bit quantity.	0xc81601
setRY0ConfigChannelLeftRight	Select channels to which input data is routed.	0xe58500
setRY0ConfigChannelSurround		0xe58502
setRY0ConfigDisable	Disable driver and output.	0xe58603
setRY0ConfigEnableDriver	Enable driver but not output.	0xe58602
setRY0ConfigEnable	Enable driver and output.	0xe58600

Table 5-4 Secondary / Auxiliary PCM Configuration Symbolic Opcodes (Continued)

Symbol	Description	Value
setRY0ConfigEnableChannelLeftRight	Enable driver and output, and select channels to which input data is routed.	0xe58400
setRY0ConfigEnableChannelSurround		0xe58402
getRY0Config	Report control register value.	0x881601
getRY0ConfigChannel		0xa58500
getRY0ConfigEnable		0xa58600

5.5.3 Secondary/Auxiliary PCM Scale

The buffered PCM input is *scaled* before it is placed into the selected channels. The scale factor is, by default 0.5, representing the scaling necessary to convert full-scale inputs to the scaled representation used for internal processing within the 56371A in a fieldsize of 2.0. The scale factor can be set to a value less than 0.5 to provide input scaling for the Secondary/Auxiliary PCM Input. The value 0.0 can be used to effectively mute the input, and a negative value can be used to provide phase inversion. A scale factor value greater than 0.5 in magnitude should not be used.

Table 5-5 Secondary / Auxiliary PCM Scale Symbolic Opcodes

Symbol	Description	Value
setRY0Scale	Set scale factor, where the value is a 24-bit fractional value in a fieldsize of 2.0.	0x c81602
getRY0Scale	Report control register value.	0x881602

5.6 DAX OUTPUT DRIVER

In a DSP56371A system, the DAX can be used for transmitting PCM samples or a consecutive non-PCM bit stream, using IEC958 format. The bit stream is transmitted from two output buffers, which are decided by the DAX Configuration Register. The driver delivers the sample in one of the output buffers to the frame channel A in the DAX and that in another to the frame channel B.

5.6.1 DAX Status

Table 5-6 DAX Status Data Stream Symbolic Opcodes

Symbol	Description	Value
GetDAXStatus	Report status register value	0x881500
GetDAXStatusFlags	Report stream type of the driver	0xa54200

Table 5-6 DAX Status Data Stream Symbolic Opcodes (Continued)

Symbol	Description	Value
getDAXStatusFlagsNone	Driver is of data-stream type	0x000000
getDAXStatusFlagsBitStream	Driver is of bit-stream type	0x000001
getDAXStatusDriver	Report the type of the driver	0xa54300
gotDAXStatusDriverNone	No driver	0x000000
gotDAXStatusDriverTxD	TxD driver	0x000001
gotDAXStatusDriverTdd	Tdd driver	0x000002
gotDAXStatusDriverTad	Tad driver	0x000003

5.6.2 DAX Configuration

Tje DAX Configuration Register consists of three parts: Data Stream, Ratio and Enable. The DAX Configuration Data Stream Register chooses the two output buffers where the sample should be transmitted by the DAX. The Configuration Ratio Register decides the output ratio. Taking Table 5-7 and Table 5-8 for reference, the Configuration Enable Register is to enable the DAX output driver and choose the transmission mode.

DAX Configuration Data Stream

Table 5-7 DAX Configuration Data Stream Symbolic Opcodes

Symbol	Description	Value
setDAXConfigDataStreamPrimary	Primary left and right channel	0xe54500
setDAXConfigDataStreamSurround	Surround left and right channel	0xe54502
setDAXConfigDataStreamCenter	Center and Subwoofer channel	0xe54504
setDAXConfigDataStreamAuxiliary	Auxiliary left and right channel	0xe54506
setDAXConfigDataStreamSecondary	Secondary left and right channel	0xe54508
getDAXConfigDataStream	Report configuration data stream register value.	0xa54500

DAX Configuration Date Ratio

- For all HLX of the DSP56371A, the “default form” of rate conversion is nondestructive. Thus, for all HLX of the DSP56371A, this opcode is exactly equivalent to setDAXConfigRatio2to1N.
- The “destructive form” of rate conversion leaves the output buffer in a state that is not suitable for use by other system components, such as the ESAI output driver.
- The “non-destructive form” of rate conversion preserves the output buffer in a state that remains suitable for use by other system components, such as the ESAI output driver. This form is more costly in terms of memory requirements.

Table 5-8 DAX Configuration Ratio Symbolic Opcodes

Symbol	Description	Value
setDAXConfigRatio1to1	Set output ratio 1:1	0xe54600
setDAXConfigRatio2to1	Set output ratio 2:1, default form	0xe54601
setDAXConfigRatio2to1D	Set output ratio 2:1, destructive form	0xe54602
setDAXConfigRatio2to1N	Set output ratio 2:1, non-destructive form	0xe54603
getDAXConfigRatio	Report configuration ratio register value.	0xa54600

DAX Configuration Date Enable

- Non-Continuous Transmission:

  In the default mode in the DSP56371A, when no valid data is available for transmission, the DAX Data Stream Output Driver transmits zero-valued data with zero-valued CSW marked as invalid, with the V bit of the IEC 958 frame set. This marks the data as “not reliable.” This default mode is termed the non-continuous channel data mode. The existent, related mode where channel transmission is enabled but data transmission is disabled, is termed the non-continuous channel mode.

- Continuous Transmission:

  In the continuous channel and continuous channel data modes of DSP56371A, when no valid data is available for transmission the DAX transmits zero-valued data with the present CSW marked as valid, with the V bit of the IEC 958 frame zeroed. The “present CSW” is the last CSW value queued for transmission by the HLX prior to cessation of data transmission by the DAX Data Stream Output Driver.

Table 5-9 DAX Configuration Enable Symbolic Opcodes

Symbol	Description	Value
setDAXConfigEnableNone	Disable	0xe54700
setDAXConfigEnableChannel	Enable channel but not data, non-continuous	0xe54701
setDAXConfigEnableChannelData	Enable channel and data, non-continuous	0xe54703
setDAXConfigEnableContinuousChannel	Enable channel but not data, continuous	0xe54705
setDAXConfigEnableContinuousChannelData	Enable channel and data, continuous	0xe54707
getDAXConfigEnable	Report configuration enable register value.	0xa54700

Appendix A
Memory Maps

Note that the memory maps below do not include any additional patches which may be required to obtain full functionality of the DSP. Note also that all unused areas should be verified by the user.

A.1 RED HLX MEMORY MAP

X Memory

Start	End	Length	Section
$000000	$0000ff	256	scratch
$000126	$00013f	26	unused
$00016c	$00017f	20	unused
$000c63	$000fff	925	unused
$0013e0	$0013ff	32	unused
$0015e0	$0015ff	32	unused
$0017e0	$0017ff	32	unused
$001da0	$001fff	608	unused
$00c200	$00c3ff	512	unused
$00c6d0	$00c7ff	304	unused
$00cbc0	$011fff	21568	unused

Y Memory

Start	End	Length	Section
$000000	$0000ff	256	scratch
$0002e1	$0002ea	10	unused
$0003d0	$0003ff	48	unused
$0006d0	$000719	74	unused
$000740	$0007ff	192	unused
$000d00	$000fff	768	unused
$001500	$0017ff	768	unused
$001da0	$001dff	96	unused
$001fe0	$001fff	32	unused
$00c400	$012cff	26880	unused
$012d78	$015fff	12936	unused

P Memory

Start	End	Length	Section
$0001bc	$0001c0	4	unused
$0001f2	$000fff	3598	unused

A.2 BLUE HLX MEMORY MAP

X Memory

Start	End	Length	Section
$000000	$0000ff	256	scratch
$000126	$00013f	26	unused
$0013f0	$0013ff	16	
$00cc00	$00dbff	4096	unused
$00ded0	$00efff	4400	unused
$00f112	$11fff	12014	unused

Y Memory

Start	End	Length	Section
$000000	$0000ff	256	scratch
$0002e7	$0002ea	4	unused
$0003f0	$0003ff	16	unused
$0006d0	$000709	58	unused
$001ad0	$001bff	304	unused
$001de0	$001dff	32	unused
$001ef0	$001fff	272	unused
$00d09e	$012cff	23650	unused
$12d78	$015fff	8584	unused

P Memory

Start	End	Length	Section
$0001bc	$0001bf	4	unused
$000204	$000fff	3580	unused

A.3 GREEN HLX MEMORY MAP

X Memory

Start	End	Length	Section
$000000	$0000ff	256	scratch
$000126	$00013f	26	unused
$00f112	$011fff	12014	unused

Y Memory

Start	End	Length	Section
$000000	$0000ff	256	scratch
$0002e7	$0002ea	4	unused
$000400	$000709	778	unused
$001200	$0013ff	512	unused
$001e00	$001fff	512	unused
$00f400	$012cff	14592	unused
$012d78	$12d7f	8	unused
$012db5	$12dbf	11	unused
$012df5	$12dff	11	unused
$012fe0	$012fff	32	unused
$0135a0	$0135bf	32	unused
$0135f5	$0135ff	11	unused
$0137e0	$0137ff	32	unused
$013da0	$013dbf	32	unused
$013df5	$013dff	11	unused
$013fe0	$013fff	32	unused
$0145a0	$0145bf	32	unused
$0145f5	$0145ff	11	unused
$0147e0	$0147ff	32	unused
$014da0	$014dbf	32	unused
$014df5	$014dfff	11	unused
$014e35	$014e3f	11	unused
$014e75	$014e7f	11	unused
$014eb5	$014ebf	11	unused
$014ef5	$014eff	11	unused

P Memory

Start	End	Length	Section
$0001bc	$0001bf	4	unused
$000204	$000fff	3580	unused

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Appendix B
GPIO Mode

Appendix B.1 Nil GPIO Mode

In the Nil GPIO mode, none of the following GPIO pins is assigned by the Software Architecture and so can be freely assigned as GPIO inputs or outputs by the user:

Available GPIO – PE0-PE11, PF0-PF10, PC2

The following command will initiate Nil GPIO Mode (the command should be contained within the initialization macro used):

```
# InitGPIONil
cmd C40002 48 FF0100 410000
```

Appendix B.2 LTE GPIO Mode

Logic Signal	Physic Signal	Direction(I/O)	Default
Mute	PE11	Output	L
Lock	PF6	Input	
Boot0	TIO0	Input	H
Boot1	TIO1	Input	L
Double Speed	PE10	Output	H
Unused	PE0-PE7 PF0-PF5 PF7-PF10 PC2		

The following command will initiate LTE GPIO Mode (the command should be contained within the initialization macro used):

```
# InitGPIOLTE
cmd C40002 48 FF0105 410000
```

Appendix B.3 LTF GPIO Mode

Logic Signal	Physical Signal	Direction (I/O)	Default
Mute	PE11	Output	L
Lock	None		
Boot0	TIO0	Input	H
Boot1	TIO1	Input	L
Double Speed	PE10	Output	H
Unused	PE0-PE7 PC2 PF0 PF1 PF3~PF5		

The following command will initiate LTF GPIO Mode (the command should be contained within the initialization macro used):

```
# InitGPIOLTF
cmd C40002 48 FF0106 410000
```

Appendix B.4 LTH GPIO Mode

This mode is intended for the slave chip of a dual DSP design.

Logic Signal	Physic Signal	Direction (I/O)	Default
Mute	PF0	Output	L
Lock	PF6	Input	
Boot0	TIO0	Input	H
Boot1	TIO1	Input	L
Double Speed	PF1	Output	L
Unused	PF4 PF5 PF7-PF10		

The following command will initiate LTH GPIO Mode (the command should be contained within the initialization macro used):

```
# InitGPIOLTH
```

cmd C40002 48 FF0107 410000

Pin Descriptions for the above tables

Mute – This pin is designed to be used in conjunction with the analogue muting circuitry of the system. Any time that there is an interruption in the bitstream processing, e.g., a source change or an error in the bitstream, the Software Architecture will assert this pin to signal the analogue output to mute. This helps to minimize the amount of pops/clicks heard in the system.

Lock - This pin is designed to be used with an external SPDIF receiver chip; it should be connected to the lock pin of the SPDIF receiver used. Any time that 'lock' is lost on the SPDIF receiver, the Software Architecture of the DSP automatically mutes its output. This helps to minimize the amount of pops/clicks heard in the system.

Double Speed – This pin is used to signal when 'double speed' mode is in operation, i.e., either DTS 96/24 mode is being used, or the Double Rate Manager is being used, so that the output frequency is double that of the input frequency. This signal can be monitored by an external microcontroller, which could determine the correct MCLK for the D/A or SPDIF transmitter in the system (i.e., either 256FS or 128FS).

Boot0/Boot1 – These pins should be fixed in the system to determine the serial bus used for DSP to host communication via the CHIRP protocol. The following two options are available:

Boot0/TIO0 – High Boot1/TIO1 – Low=>SPI mode

Boot0/TIO0 – Low Boot1/TIO1 – High=>I2C mode

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Appendix C
Initialization Macros

Below are sample initialization macros for the different HLX modes available. Note that they are designed to be used with the DSPAUDIOEVMMB1/DSPA371DB1 Evaluation Board and SDI Debugger tool.

These macros will allow basic operation of the decoders on the DSP. For certification of some of the more complex decoders (e.g. DTS96/24), an additional software patch may be required. More details on this can be obtained from your local Motorola applications contact.

Note that further information on the setting of the PLL Control Register (PCTL) can be found in Section 5 of the DSP56371 User's Manual.

APPENDIX C.1 Red HLX Initialization Macro

```
# Macro to boot up the 56371 Red HLX
# Daughterboard Jumper Settings - B, I, K, N, P and T
# SW1 - switches 3 and 6 on
# EXTAL SELECT - XTAL

# Set PCTL
# Ext crystal 24.576 MHz,
#PLLOutput=45.056 MHz
cmd C1FFFD 03E10B
Delay 1

# ZoneRed
cmd C40002 48 FF00D0 410000

# InitGPIONil
cmd C40002 48 FF0100 410000

# InitRed
cmd C40002 48 FF00D2 410000

# Disable DAX
cmd C0015F FF0C0F


# PLLOutput=180.224 MHz
cmd C1FFFD 03A00B
Delay 1

# RunRed
cmd C40002 48 FF00D3 810000
```

APPENDIX C.2 Blue HLX Initialization Macro

```
# Macro to boot up the 56371 Blue HLX
# Daughterboard Jumper Settings - B, I, K, N, P and T
# SW1 - switches 3 and 6 on
# EXTAL SELECT - XTAL

# Set PCTL
# Ext crystal 24.576 MHz,
#PLLOutput=45.056 MHz
cmd C1FFFD 03E10B
Delay 1

# ZoneBlue
cmd C40002 48 FF00D8 410000

# InitGPIONil
cmd C40002 48 FF0100 410000

# InitBlue
cmd C40002 48 FF00DA 410000

# Disable DAX
cmd C0015F FF0D7F

# PLLOutput=180.224 MHz
cmd C1FFFD 03A00B
Delay 1

# RunBlue
cmd C40002 48 FF00DB 810000
```

APPENDIX C.3 Green HLX Initialization Macro

```
# Macro to boot up the 56371 Green HLX
# Daughterboard Jumper Settings - B, I, K, N, P and T
# SW1 - switches 3 and 6 on
# EXTAL SELECT - XTAL

# Set PCTL
# Ext crystal 24.576 MHz,
#PLLOutput=45.056 MHz
cmd C1FFFD 03E10B
Delay 1

# ZoneGreen
cmd C40002 48 FF00D4 410000

# InitGPIONil
```

```
cmd C40002 48 FF0100 410000

# InitGreen
cmd C40002 48 FF00D6 410000

# Disable DAX
cmd C0015f FF0D7F

# PLLOutput=180.224 MHz
cmd C1FFFD 03A00B
Delay 1

# RunGreen
cmd C40002 48 FF00D7 810000
```

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