PFS2613AMDA2AD – NXP Standard

Configuration report for FS26-D OTP program ID: A2 rev F

Rev. 1.0 - 1/20/2022 **Report**

1 General description

The FS26 is a power system basis chip (Power SBC) designed for low and mid-end micro controllers units. It features advance power managment conversion to support battery voltage from 3.2 V up to 40 V.

System level power is provided with a high efficiency buck controller, two programable LDOs, a high precision voltage reference and two voltage tracker with high voltage protection to support loads off-module.

The FS26 features fully indepenent and configurable functional safety state machine with up to two fail-safe outputs and system level monitoring mechanism to reach a high integrity safety level targeting system up to ASIL-D. Electrical characteristics are maintained in the FS26 data sheet

2 Features and benefits

- High voltage boost converted supporting front-end or independent operation
- One high voltage buck pre-regulator with low power mode support
- One high efficency buck regulator for MCU core voltage support
- Two linear regulators with low power mode support
- High precission 1% accurate voltage reference
- Two Voltage tracking regulator with high voltage protection for off-module load support
- Fully independent safety state machine with monitoring mechanism targeting ASIL-B applications
- Long duration timer, counting up to 6 months with 1.0 s resolution
- Selectable wake-up sources to bring the system back from low power modes
- Two configurable GPIO pins
- 10 MHz SPI communication interface

3 Applications

- Automotive motor control / gate driver systems
- 48 V battery systems
- Hybrid battery systems
- Electric vehicle battery systems
- Body controller systems

All information provided in this document is subjected to legal disclaimers. ©NXP B.V. 2022. All rights reserved.

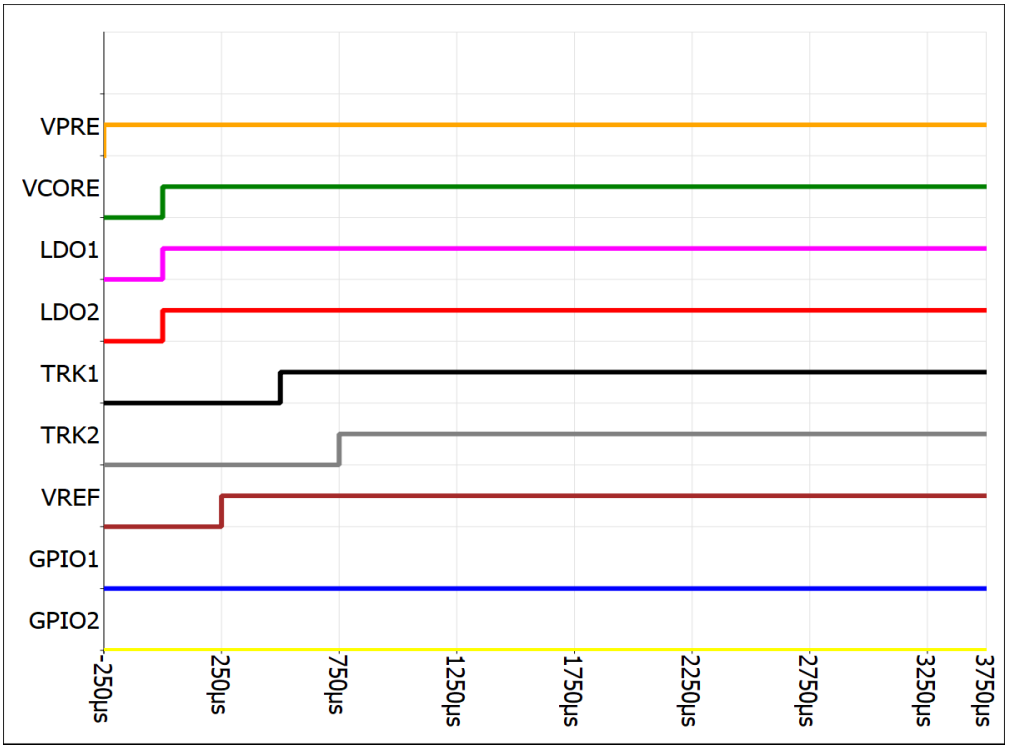
4 Ordering information

Table 1. Ordering information

Type number[1]	Package		
	Name	Description	Version
PFS2613AMDA2AD	LQFP48 AE	HLQFP48-EP plastic thermally enhanced low profile quad flat package. 48 terminals; 0.5mm pitch; 7 mm x 7 mm x 1.4 mm body	SOT1571-1

[1] To order parts in tape and reel, add the R2 suffix to the part number.

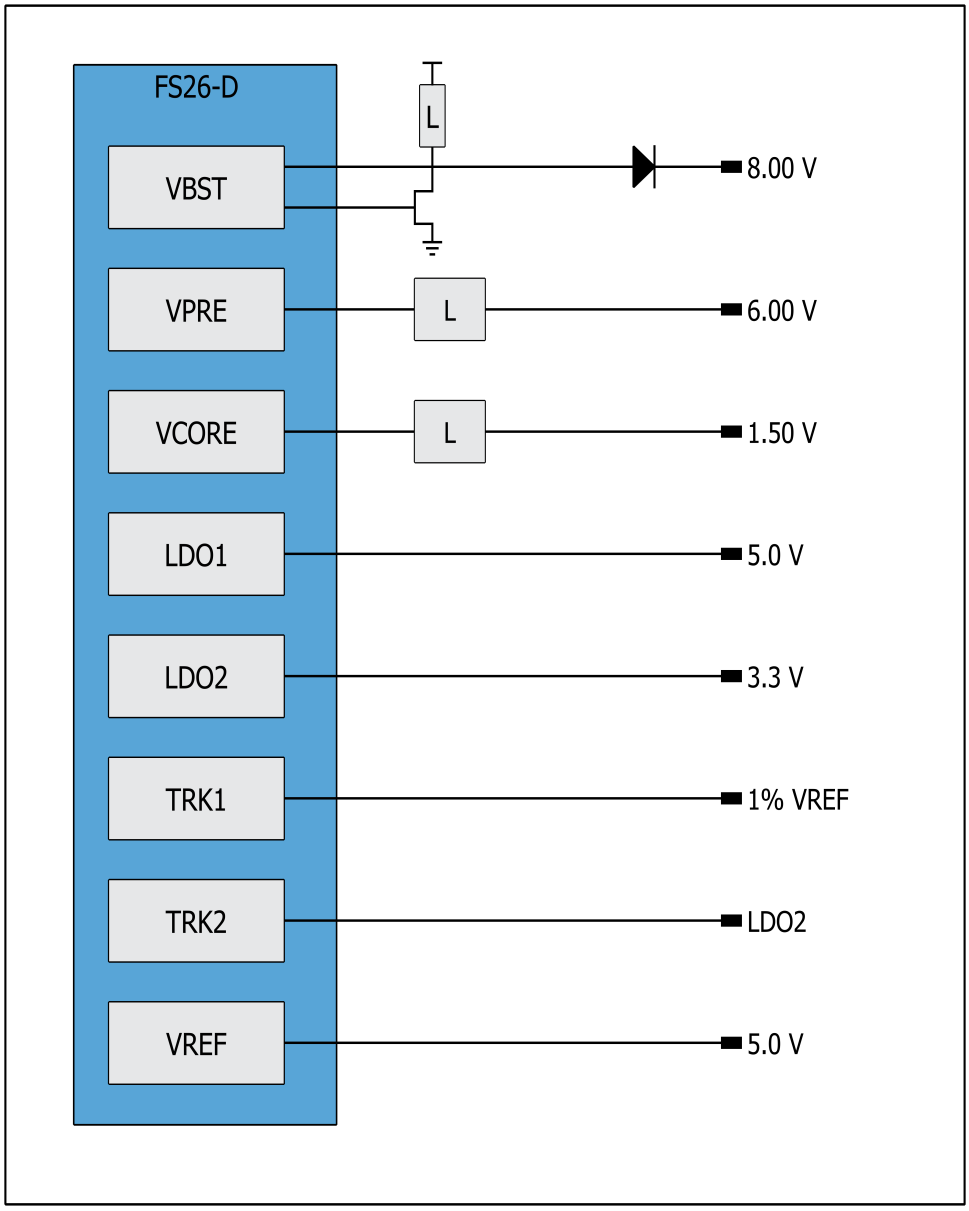
5 Power-up sequence summary



The signals depicted above are enable signals for each regulator. They don't represent the actual ramp voltage

All information provided in this document is subjected to legal disclaimers. ©NXP B.V. 2022. All rights reserved.

6 Hardware configuration diagram



All information provided in this document is subjected to legal disclaimers. ©NXP B.V. 2022. All rights reserved.

7 OTP configuration

See FS26 datasheet for parametric details. The OTP configuration summary for A2 sequence ID is provided in Tables below.

Table 2. Device OTP configuration

Functional block	Feature	OTP selection
System configuration	VSUP UV Threshold	4.8 V/4.3 V
	Exit DFS On WAKE1 Event	DFS Exit on Wake1 Event Enabled
	Auto-retry Power Up From DFS	Auto-retry Enabled
	Auto-retry Mode	Infinite retry
	Auto-retry Timer Limit	800 ms
	Clock Frequency Selection	18 MHz
	VBOS Input Selection	Auto Transition on VPRE_UVH
	VBST Clock Selection	450 KHz
Power-up Sequence	Power-up Slot Time	250 us
	Power-up Slot Bypass	Bypass Disabled
	VCORE Power-up Slot	Slot 0
	LDO1 Power-up Slot	Slot 0
	LDO2 Power-up Slot	Slot 0
	TRK1 Power-up Slot	Slot 2
	TRK2 Power-up Slot	Slot 3
	VREF Power-up Slot	Slot 1
	GPIO1 Power-up Slot	OFF
	GPIO2 Power-up Slot	OFF
I/O Configuration	GPIO1 Configuration	IO1 configured as an Input
	IO1 Low Side Polarity	GPIO1 LS active high

All information provided in this document is subjected to legal disclaimers. ©NXP B.V. 2022. All rights reserved.

	GPIO1 Pull-up	Pull-Up Disabled
	GPIO1 Pull-down	Pull-Down Enabled
	GPIO1 Detection Threshold	Low voltage threshold
	GPIO1 TSD Pull-down	Pull-down enabled in TSD
	GPIO2 Configuration	Low Side Driver
	IO2 Low Side Polarity	GPIO2 LS active high
	IO2 VCORE PGOOD	IO2 is not driven by VCORE PGOOD
	GPIO2 Pull-up	Pull-Up Disabled
	GPIO2 Pull-down	Pull-Down Disabled
	GPIO2 Detection Threshold	Low voltage threshold
	WAKE1 Detection Threshold	High voltage threshold
	WAKE2 Detection Threshold	High voltage threshold
	WAKE1 Pull-down	Pull-Down Enabled
	WAKE2 Pull-down	Pull-Down Enabled
	WAKE1 Pull-down Selection	200 KOhm
	WAKE2 Pull-down Selection	200 KOhm

Table 3. Switching Regulators

Functional block	Feature	OTP selection
VPRE Configuration	VPRE In Normal Mode	6.00 V
	VPRE In Standby Mode	5.35 V
	DVS Ramp Rate	22 mV/us
	VPRE Over Current Flag	2.2 A
	Over Current Deglitch	2000 us
	Soft-start Ramp	2150 us

All information provided in this document is subjected to legal disclaimers. ©NXP B.V. 2022. All rights reserved.

	VPRE Power Down Delay	100 us
	VPRE Transition Voltage	5.35 V
	VPRE Phase Delay	No delay
	VPRE LX Slew Rate	Fast mode
	Transconductance Amp	15 uSiemens
	Comp Capacitance	12.0 pF
	Comp Resistance	1300 KOhm
	Slope Compensation	266 mV/us
	Minimum On Time In PFM	1100 ns
	Minimum Off Time In PFM	720 ns
	VPRE Clock Selection	FSW/40
	TSD Behavior	Go to DFS
	TSD Pull-down	Pull-down enabled in TSD
VBST Configuration	VBST Voltage	8.00 V
	VBST Configuration	Front-end boost
	VBSTFB OV Monitor Mode	Auto-enable mode
	Phase Delay	1 Clock Cycle
	Low-side Slew Rate	PU = 1.5 Ohm / PD = 1.0 Ohm
	Minimum TON	200 ns
	VBST Soft Start	425 us
	Max Duty-cycle	87.50%
	Comp Capacitance	200 pF
	Comp Transconductance	3.9 us
	Comp Resistance	740 KOhm

All information provided in this document is subjected to legal disclaimers. ©NXP B.V. 2022. All rights reserved.

	Current Limit	180 mV/RSNS
	Slope Compensation	155 mV/us
VCORE Configuration	VCORE Voltage	1.50 V
	Control Type	Valley mode control
	Operating Mode	CCM only
	Soft Start	5 mV/us
	VCORE Current Limit	2.4 A
	Phase Delay	2 Clock Cycles
	High-side Slew Rate	Rise = 1.8 V/ns; Fall = 1.2 V/ns
	Transconductance Amp	53 us
	Comp Capacitance	50 pF
	Comp Resistance	200 KOhm
	VCORE Inductor	1 uH
	TSD Behavior	Go to DFS
	TSD Pull-down	Pull-down enabled in TSD

Table 4. Regulators

Functional block	Feature	OTP selection
LDO1 configurations	LDO1 Voltage In Normal	5.0 V
	LDO1 Voltage In Standby	5.0 V
	LDO1 In Standby Mode	LDO1 Enabled
	TSD Behavior	LDO1 disabled only
	TSD Pull-down	Pull-down enabled in TSD
LDO2 configurations	LDO2 Voltage In Normal	3.3 V
	LDO2 Voltage In Standby	3.3 V

All information provided in this document is subjected to legal disclaimers. ©NXP B.V. 2022. All rights reserved.

	LDO2 In Standby Mode	LDO2 Enabled
	TSD Behavior	LDO2 disabled only
	TSD Pull-down	Pull-down enabled in TSD
VREF configurations	VREF Voltage	5.0 V
	Internal LDO Reference	1.2 V
TRK1 configurations	TRK1 Input Selection	1% VREF
	TSD Behavior	TRK1 disabled only
	TSD Pull-down	Pull-down enabled in TSD
TRK2 configurations	TRK2 Input Selection	LDO2
	TSD Behavior	TRK2 disabled only
	TSD Pull-down	Pull-down enabled in TSD

Table 5. Voltage Monitoring

Functional block	Feature	OTP selection
VMONPRE Configuration	VPRE Monitoring Voltage	6.00 V
	VPRE OV Threshold	110.5 %
	VPRE UV Threshold	94.5 %
	VMONPRE OV Deglitch	45 us
	VMONPRE UV Deglitch	40 us
VMONLDO1 Configuration	LDO1 Monitoring Voltage	5.0 V
	LDO1 OV Threshold	106.0 %
	LDO1 UV Threshold	94.0 %
	LDO1 Degraded UV Monitoring	Normal UV
	VMONLDO1 OV Deglitch	45 us
	VMONLDO1 UV Deglitch	40 us

All information provided in this document is subjected to legal disclaimers. ©NXP B.V. 2022. All rights reserved.

Configuration report for FS26-D OTP program ID: A2 rev F

	LDO1 Pin Lift Detection	LDO1 pin lift detection enabled
VMONTRK1 Configuration	TRK1 Monitoring Voltage	5.0 V
	TRK1 OV Threshold	104.5 %
	TRK1 UV Threshold	95.5 %
	VMONTRK1 OV Deglitch	45 us
	VMONTRK1 UV Deglitch	40 us
VMONCORE Configuration	VCORE Monitoring Voltage	1.50 V
	CORE OV Threshold	104.5 %
	CORE UV Threshold	95.5 %
	VMONCORE OV Deglitch	45 us
	VMONCORE UV Deglitch	40 us
VMONLDO2 Configuration	LDO2 Monitoring Voltage	3.3 V
	LDO2 OV Threshold	106.0 %
	LDO2 UV Threshold	94.0 %
	LDO2 Degraded UV Monitoring	Normal UV
	VMONLDO2 OV Deglitch	45 us
	VMONLDO2 UV Deglitch	40 us
	LDO2 Pin Lift Detection	LDO2 pin lift detection enabled
VMONTRK2 Configuration	TRK2 Monitoring Voltage	3.3 V
	TRK2 OV Threshold	104.5 %
	TRK2 UV Threshold	95.5 %
	VMONTRK2 OV Deglitch	45 us
	VMONTRK2 UV Deglitch	40 us
VMONEXT Configuration	External VMON OV Threshold	104.5 %

All information provided in this document is subjected to legal disclaimers. ©NXP B.V. 2022. All rights reserved.

	External VMON UV Threshold	95.5 %
	VMONEXT OV Deglitch	45 us
	VMONEXT UV Deglitch	40 us
VMONREF Configuration	VREF Monitoring Voltage	5.0 V
	VREF OV Threshold	104.5 %
	VREF UV Threshold	95.5 %
	VMONREF OV Deglitch	45 us
	VMONREF UV Deglitch	40 us
	VREF Pin Lift Detection	VREF pin lift detection enabled

Table 6. System Safety Configuration

Functional block	Feature	OTP selection
ABIST1 Configuration	ABIST1 On VMONPRE	ABIST1 Enabled
	ABIST1 On VMONCORE	ABIST1 Enabled
	ABIST1 On VMONLDO1	ABIST1 Enabled
	ABIST1 On VMONLDO2	ABIST1 Enabled
	ABIST1 On VMONTRK1	ABIST1 Enabled
	ABIST1 On VMONTRK2	ABIST1 Enabled
	ABIST1 On VMONREF	ABIST1 Enabled
	ABIST1 On VMONEXT	ABIST1 Disabled
System Safety Configuration	DFS Entry Mode	Go to DFS when FLT_ERR_CNT = max
	FS1B Assertion Mode	Delayed Assertion Disabled
	RSTB Delay From FS0B	0 us
	RSTB Low Detection Timer	Timer Disabled
	Watchdog Timer	WD Timer Enable

All information provided in this document is subjected to legal disclaimers. ©NXP B.V. 2022. All rights reserved.

	Bypass LBIST From Standby	Always perform LBIST
	Main DFS Availability	Deep Fail Safe Available
	Deep Failsafe State Availability	Deep Fail Safe Available

Table 7. OTP ID

Functional block	Feature	OTP selection
OTP Program ID	Program ID High	A
	Program ID Low	2
Main Version Bits	LDO2 Regulator	LDO2 available
	VCORE Regulator	CORE available
	TRK1 Regulator	TRK1 available
	TRK2 Regulator	TRK2 available
	VREF Regulator	VREF available
	VBST Regulator	VBST available
	GPIO1 Pin	IO1 available
	GPIO2 Pin	IO2 available
	LDT Function	LDT available
	TWARN Selection	155 °C
	VCORE Max Current	800 mA
	Device ID	0x10
FS Versioning Bits	VPRE Monitor	VMON Enabled
	VCORE Monitor	VMON Enabled
	LDO1 Monitor	VMON Enabled
	LDO2 Monitor	VMON Enabled
	TRK1 Monitor	VMON Enabled

All information provided in this document is subjected to legal disclaimers. ©NXP B.V. 2022. All rights reserved.

Configuration report for FS26-D OTP program ID: A2 rev F

	TRK2 Monitor	VMON Enabled
	VREF Monitor	VMON Enabled
	External Monitor	VMON Disabled
	FCCU Function	FCCU available
	Fault Recovery Function	Fault Recovery available
	Watchdog Type	Challenger WD
	FS1B Type	FS1B available
	ABIST On-demand	ABIST2 available
	Cyclic OTP Check	CORRUPT available
	ERRMON Function	ERRMON not available
	LBIST Operation	LBIST available

All information provided in this document is subjected to legal disclaimers. ©NXP B.V. 2022. All rights reserved.

8 Legal information

8.1 Definitions

Draft - The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Limited warranty and liability - Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes - NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use - NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications - Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values - Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale - NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms,unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors here by expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license - Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Suitability for use in automotive applications - This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Export control - This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations - A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

8.2 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.
NXP - is a trademark of NXP B.V.

All information provided in this document is subjected to legal disclaimers. ©NXP B.V. 2022. All rights reserved.

PFS2613AMDA2AD – NXP Standard

Configuration report for FS26-D OTP program ID: A2 rev F

Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2022 . **All rights reserved.**

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 1/20/2022
Document identifier: R_PFS2613AMDA2AD