AN11606

PTN3460I Programming Guide

Rev. 1.4

Document information

Info	Content
Keywords	PTN3460I, DisplayPort, eDP, LVDS, bridge
Abstract	This document describes the PTN3460I programming guide which is the supporting document for the DisplayPort to LVDS bridge device PTN3460I

AN11606

PTN3460I Programming Guide

Rev. 1.4

Revision history

Rev	Date	Description
v.1	20141006	Application note; initial version.
V1.1	20141210	Revise
V1.2	20150522	Revise
V1.3	20150709	Revise
V1.4	20160607	Revise

AN11606

PTN3460I Programming Guide

Rev. 1.4

1. Introduction

PTN3460I is built in a configuration table in internal SRAM, which allows user to program seven EDID and 128 configuration registers through M/S I2C-bus. It can change PTN3460I functionality by changing and storing the configuration table. This application note provides detailed explanations for the configuration table, programming method, and how to program EDID and configuration setting into PTN3460I internal flash.

2. Configuration table

2.1. Configuration table in internal SRAM memory

The configuration table is stored in the SRAM of the PTN3460I and is 1K bytes (1024 bytes) long. It consists 896 bytes to store seven EDID (128 × 7 = 896 bytes) and 128 bytes of configuration registers used to control PTN3460I functionality. This configuration table is located at a fixed address in XDATA memory (x:0x0C00 - -0x0F00) of the PTN3460I.

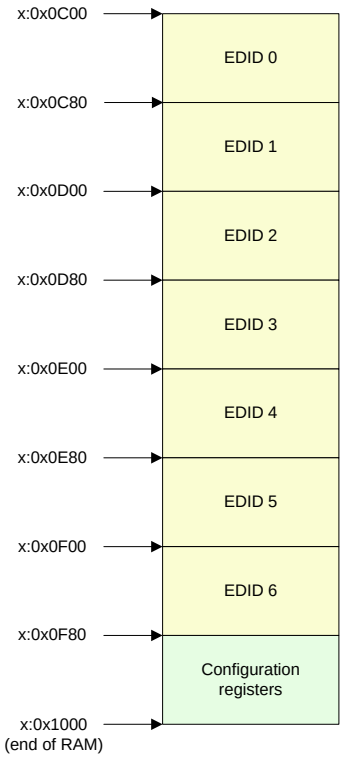


Fig 1. Configuration table location in XDATA memory

2.2. Configuration table initialization

PTN3460I offers two ways to initialize the configuration table

- Read it from internal flash memory.
- Read it from an external EEPROM.

PTN3460I firmware will first check DEV_CFG pin (pin 12 of PTN3460I) status during initialization stage, and it will read 1K bytes configuration table from external EEPROM if DEV_CFG pin is high, otherwise it will read 1K bytes configuration table from internal flash memory.

PTN3460I firmware uses all zero to initialize configuration table in SRAM in following two cases

- If DEV_CFG pin = high, but no external EEPROM exists.
- If DEV_CFG pin = open or low, but the magic number in the configuration table in internal flash is incorrect.

2.3. Configuration table access through I2C bus

- **PTN3460I is in I2C slave mode (DEV_CFG pin = open or low)**

The configuration table is a 1024 bytes table which consists of 7 EDID and 128 bytes of configuration registers. PTN3460I supports 8 bit I2C addressing mode which allows external MCU or PCH to access entire 1024 bytes of configuration table through M/S I2C interface of PTN3460I.

However when accessing PTN3460I M/S I2C as an I2C slave, it can only be addressed up to 256 bytes with standard I2C protocols, so the layout of the configuration table is modified by firmware to fit in these 256 bytes. The 256 bytes configuration table is shown in Fig 2, the Offset 0 - 255 means I2C register address 0x00 – 0xFF.

If an external MCU or PCH wants to access EDID2 which data is physically located in PTN3460I internal SRAM location 0x0D00 – 0x0D80, then it needs to set configuration register 0x85[2:0] = 0x03 (EDID ROM access control register) and reads 128 byte EDID data from I2C register 0x00 – 0x7F over PTN3460I M/S I2C bus. And firmware will move EDID2 data from internal SRAM location 0x0D00 – 0x0D80 to I2C register 0x00 – 0x7F for external MCU or PCH to access it.

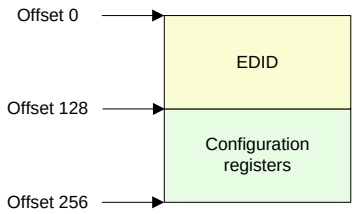


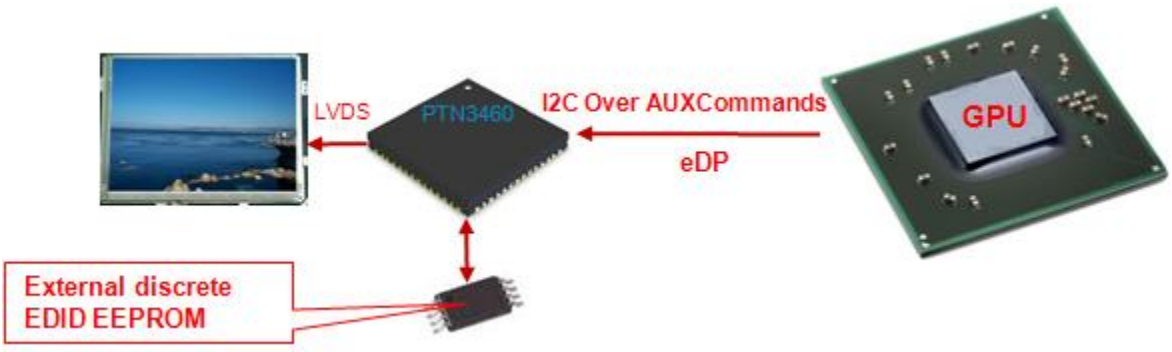
Fig 2. Configuration table layout modified by firmware to fit 256 bytes

PTN3460I M/S I2C slave address is set 0xC0 while DEV_CFG pin is set to open, and set to 0x40 while DEV_CFG pin is set to low.

PTN3460I M/S I2C pins are located at pin 24 (MS_SDA) and pin 25 (MS_SCL).

- **PTN3460I is in I2C master mode (DEV_CFG pin = high)**

PTN3460I I2C master mode application block diagram is shown in the figure below.



PTN3460I reads 256 bytes of configuration table from external EEPROM when it's set as I2C master mode (DEV_CFG pin = 1), the configuration table includes 128 bytes EDID and 128 bytes of configuration register bytes.

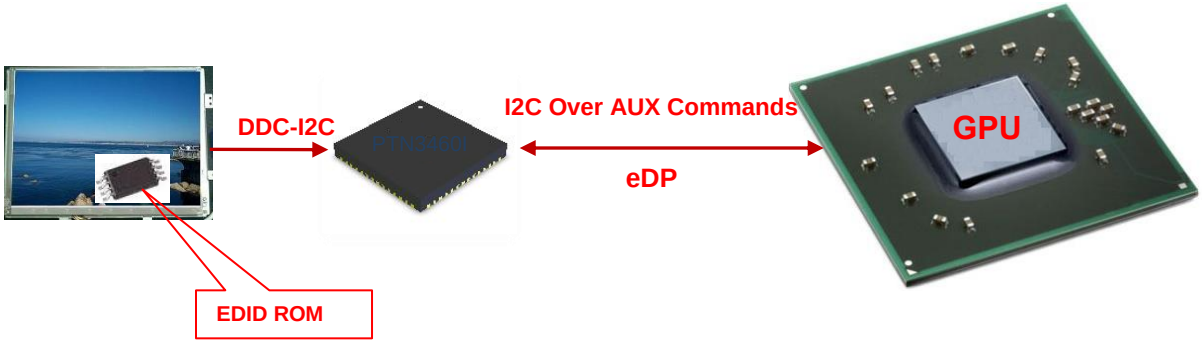
When PTN3460I is in I2C master mode, it reads 256 bytes configuration table from external EEPROM to internal SRAM in system initialization phase. It only supports one EDID storing in external EEPROM, however the system designer can change the EDID in external EEPROM easier by using EEPROM programmer to program it.

PTN3460I I2C slave mode function is disabled when it is set to I2C master mode, so PTN3460I would not be able to listen to I2C command from PCH or external MCU which means the access to PTN3460I I2C registers would not be supported through SMBus. The functional control such as brightness control and backlight control would be required through AUX commands instead of SMBus commands.

PTN3460I I2C master mode application only requires 256 bytes space in external EEPROM which the I2C address is 0xA0, the rest of space of EEPROM can be shared with other device in application.

- **PTN3460I is in EDID emulation off mode (Configuration register 0x84 bit 0 = 0)**

PTN3460I in the EDID emulation off mode application block diagram is shown in the figure below.

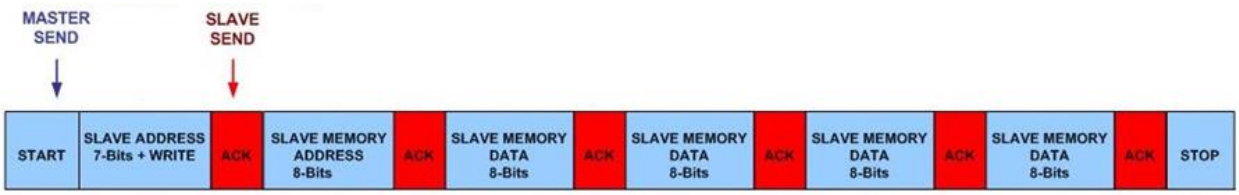


When the configuration register 0x84 [bit 0] is set to 0, then PTN3460I is in EDID emulation off mode.

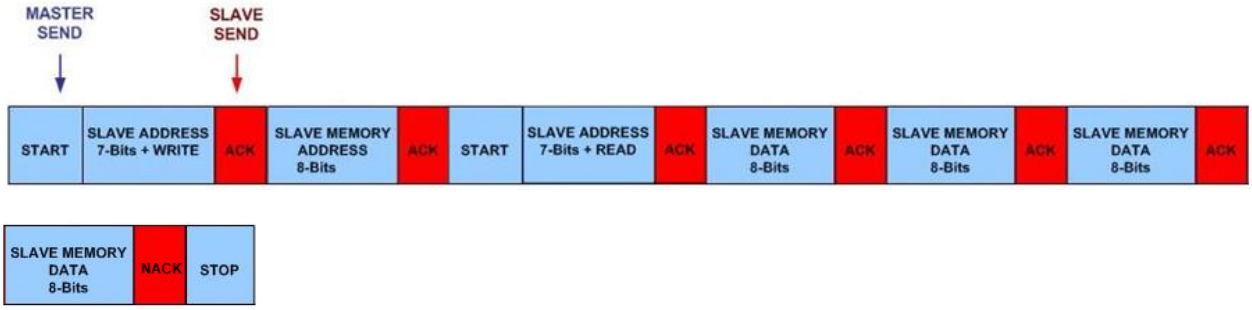
The DP source (GPU) sends IoA (I2C-over-AUX) commands to read EDID data from PTN3460I through DP AUX channel, and PTN3460I reads the EDID data from LCD panel over DDC-I2C bus according to each IoA commands. And PTN3460I sends EDID data to DP source (GPU) through AUX channel.

- **I2C Programming Protocol**

I2C master (PCH or MCU) WSRITES to I2C salve (PTN3460I) protocol



I2C master (PCH or MCU) READS from I2C slave (PTN3460I) protocol



3. EDID Table

PTN3460I stores 7 EDID in configuration table in SRAM shown as fig 3.

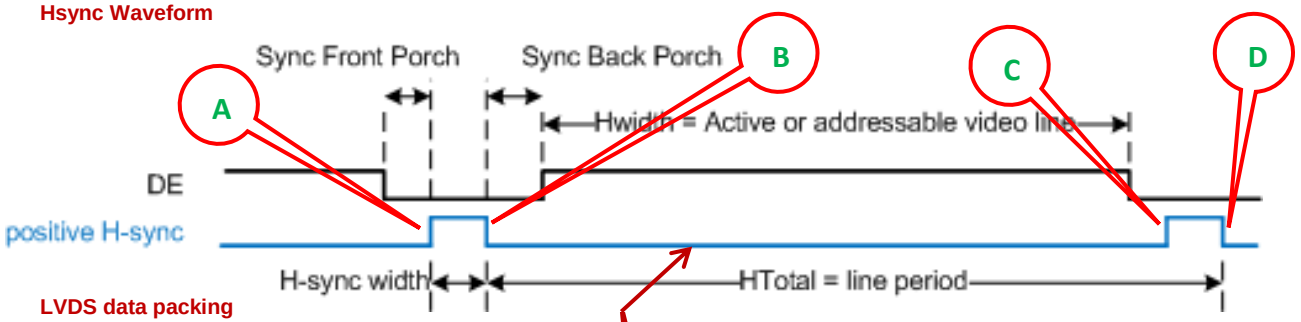
EDID N0	Resolution	EDID Description
0	1024 x 768 @60Hz	NXP Generic
1	800 x 480 @60Hz	NXP Generic
2	480 x 272 @60Hz	NXP Generic
3	1600 x 900 @60Hz	Samsung LTM200KT
4	1920 x 1080 @60Hz	Samsung LTM230HT
5	1366 x 768 @60Hz	NXP Generic
6	320 x 240 @60Hz	NXP Generic

4. Hsync, Vsync polarity settings

4.1. Hsync polarity is positive

Followings are Hsync waveform, LVDS data packing and truth table when Hsync polarity is set to positive (configuration register 0x82 [bit 6] = 0).

Hsync Waveform



LVDS data packing

Channel	Bit position						
	6	5	4	3	2	1	0
LVDS odd differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS odd differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS odd differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2
LVDS odd differential channel D	don't care	bit 7	bit 6	bit 7	bit 6	bit 7	bit 6
LVDS even differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS even differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS even differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2
LVDS even differential channel D	don't care	bit 7	bit 6	bit 7	bit 6	bit 7	bit 6

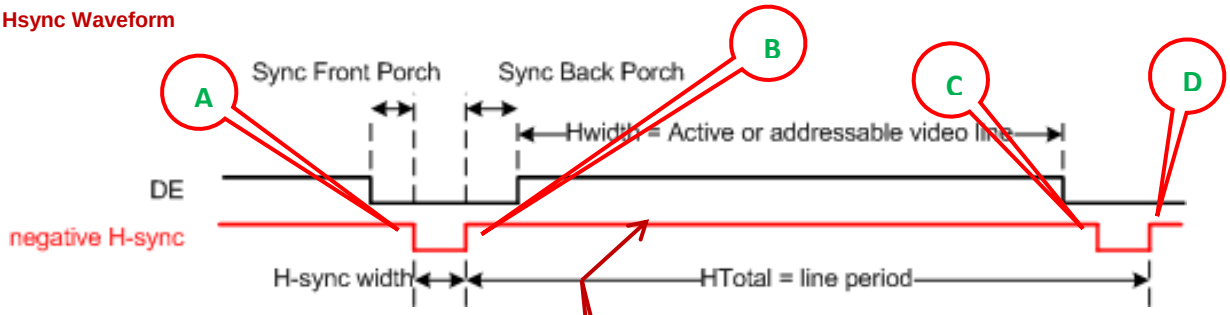
Truth table – Hsync polarity is positive

	A to B	B to C	C to D
HSYNC data	1	0	1

4.2. Hsync polarity is negative

Followings are Hsync waveform, LVDS data packing and truth table when Hsync polarity is set to negative (configuration register 0x82 [bit 6] = 1).

Hsync Waveform



Channel	Bit position						
	6	5	4	3	2	1	0
LVDS odd differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS odd differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS odd differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2
LVDS odd differential channel D	don't care	bit 7	bit 6	bit 7	bit 6	bit 7	bit 6
LVDS even differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS even differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS even differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2
LVDS even differential channel D	don't care	bit 7	bit 6	bit 7	bit 6	bit 7	bit 6

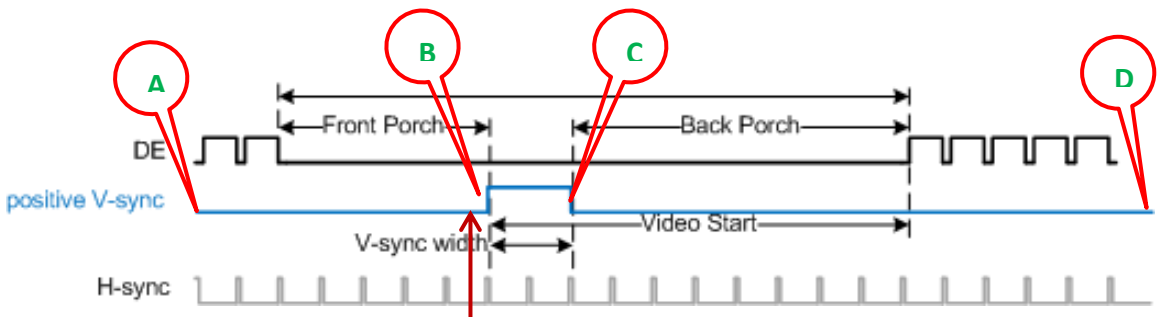
Truth table – Hsync polarity is negative

	A to B	B to C	C to D
HSYNC data	0	1	0

4.3. Vsync polarity is positive

Followings are Vsync waveform, LVDS data packing and truth table when Vsync polarity is set to positive (configuration register 0x82 [bit 7] = 0).

Vsync Waveform



LVDS data packing

Channel	Bit position						
	6	5	4	3	2	1	0
LVDS odd differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS odd differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS odd differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2
LVDS odd differential channel D	don't care	bit 7	bit 6	bit 7	bit 6	bit 7	bit 6
LVDS even differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS even differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS even differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2
LVDS even differential channel D	don't care	bit 7	bit 6	bit 7	bit 6	bit 7	bit 6

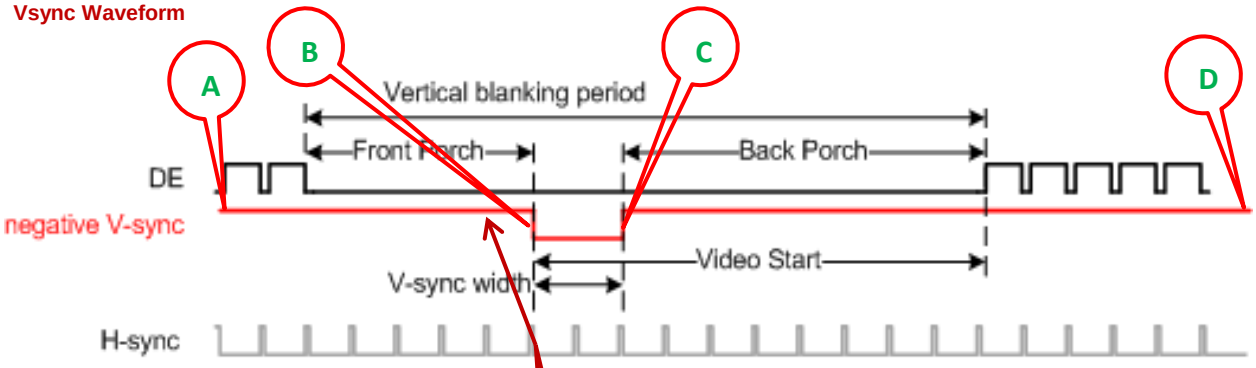
Truth table – Vsync polarity is positive

	A to B	B to C	C to D
VSYNC data	0	1	0

4.4. Vsync polarity is negative

Followings are Vsync waveform, LVDS data packing and truth table when Vsync polarity is set to negative (configuration register 0x82 [bit 7] = 1).

Vsync Waveform



LVDS data packing

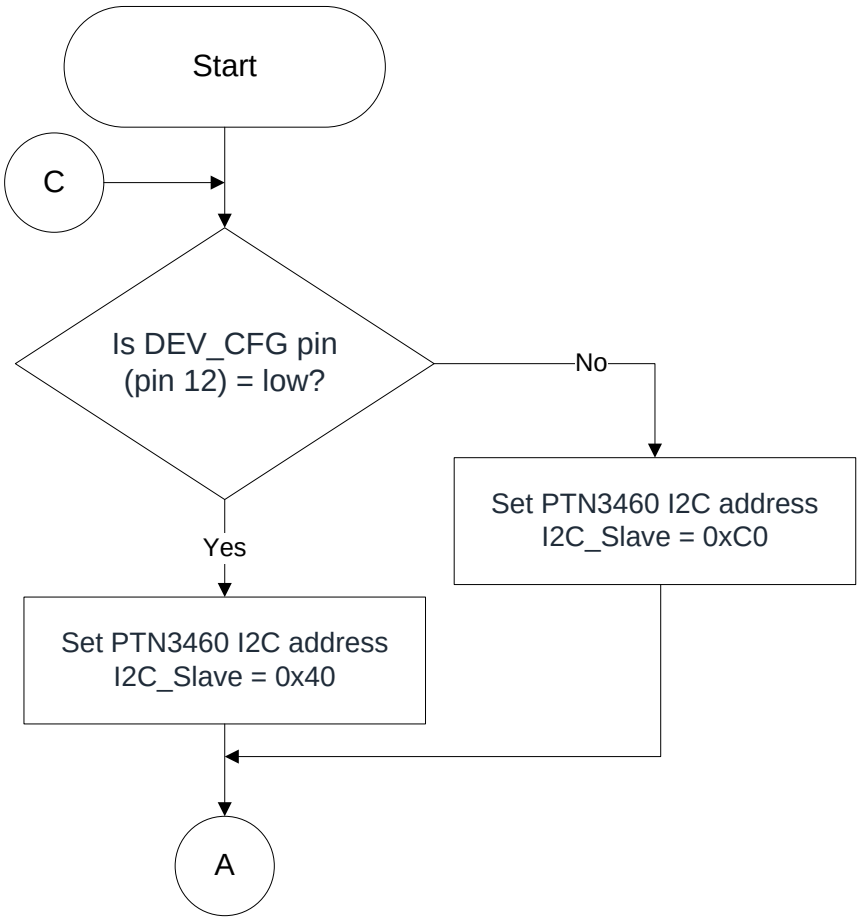
Channel	Bit position						
	6	5	4	3	2	1	0
LVDS odd differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS odd differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS odd differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2
LVDS odd differential channel D	don't care	bit 7	bit 6	bit 7	bit 6	bit 7	bit 6
LVDS even differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS even differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS even differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2
LVDS even differential channel D	don't care	bit 7	bit 6	bit 7	bit 6	bit 7	bit 6

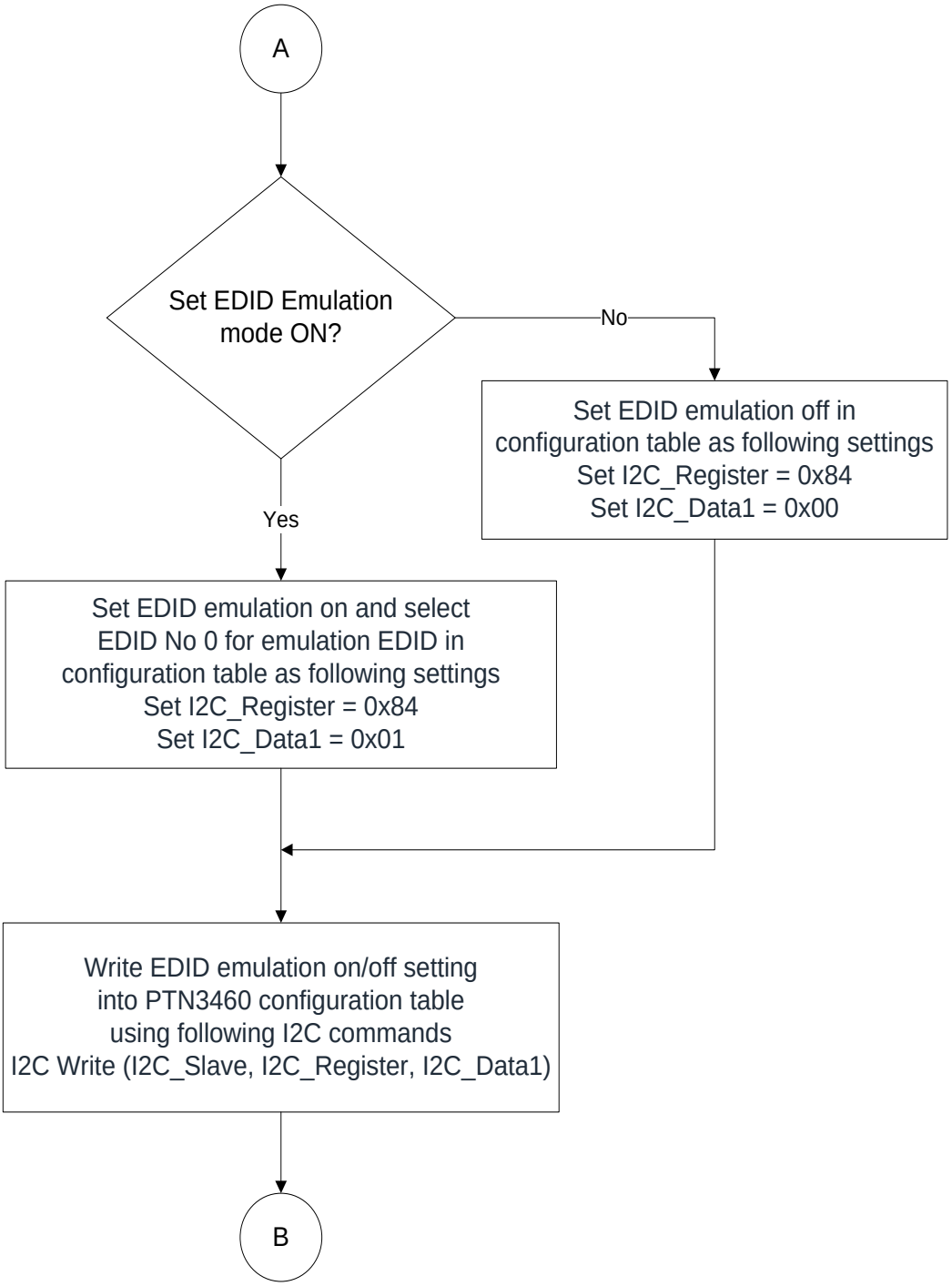
Truth table – Vsync polarity is negative

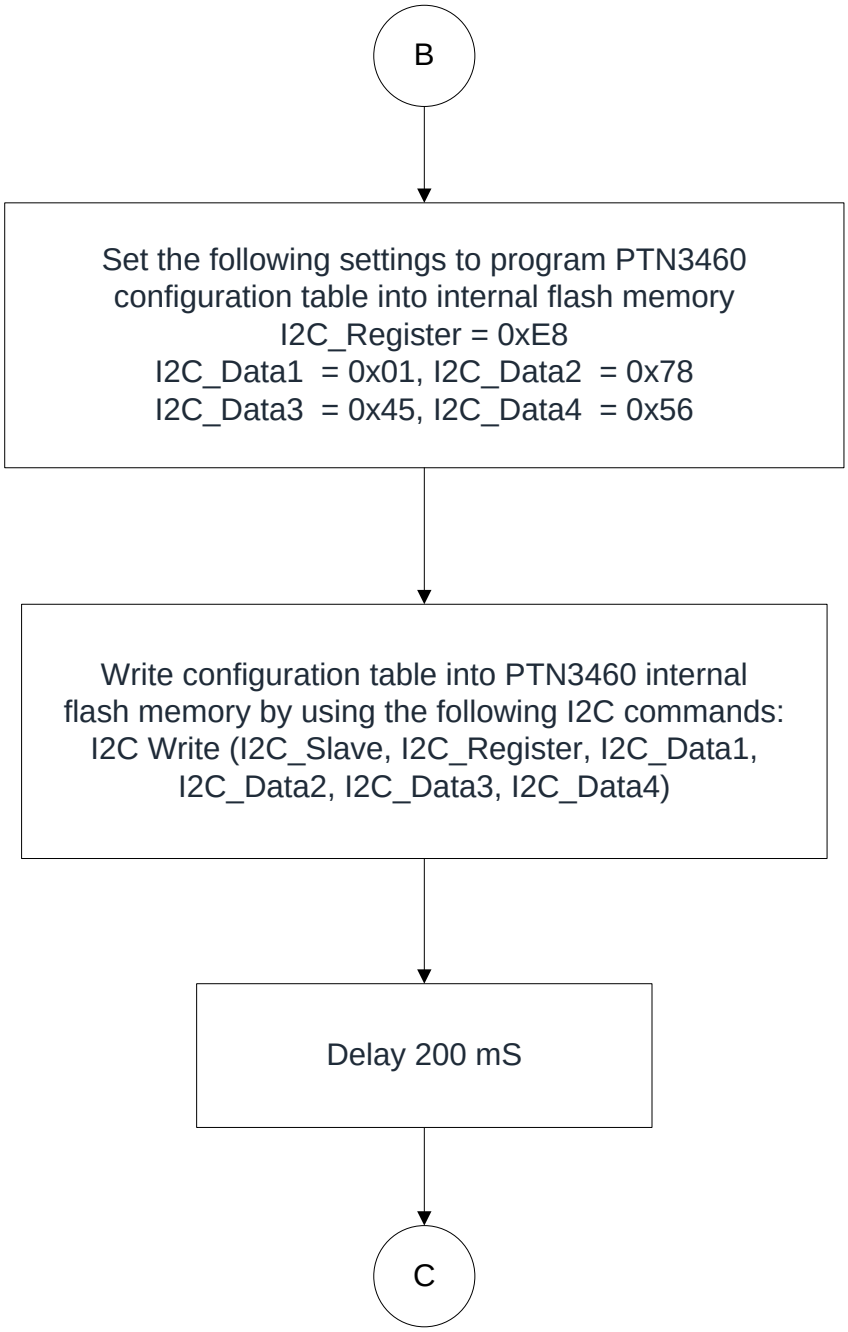
	A to B	B to C	C to D
VSYNC data	1	0	1

5. Programming Flow Chart

5.1. EDID Emulation ON/OFF Setting Control Flow

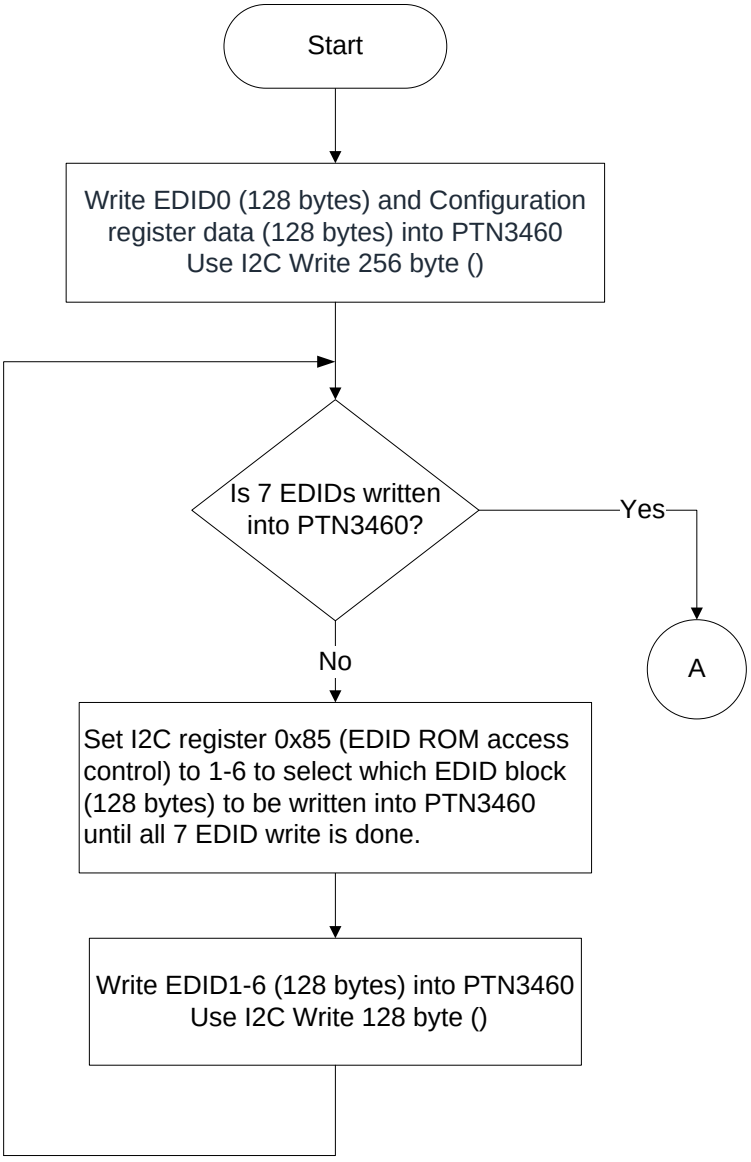


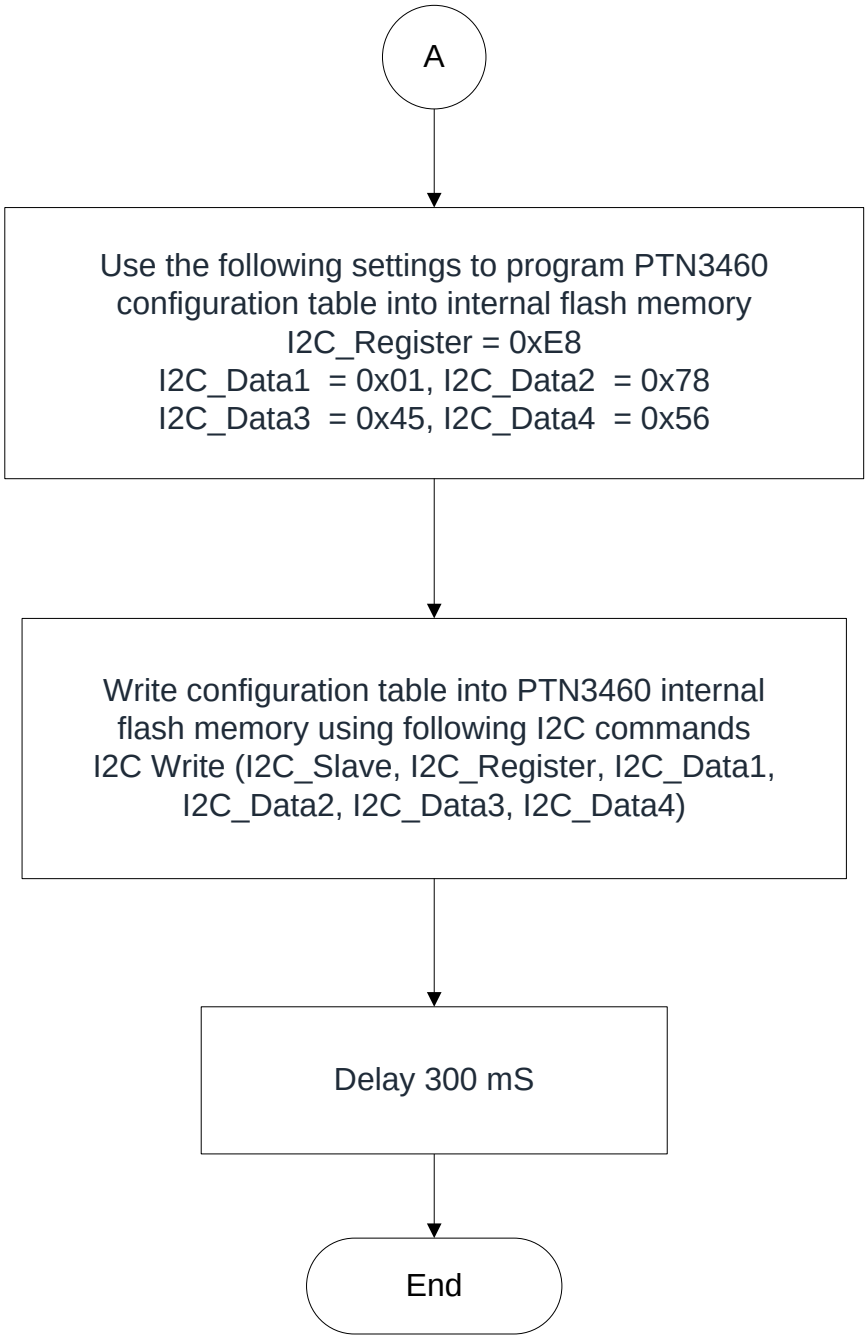

A
Set EDID Emulation mode ON?
No
Yes
Set EDID emulation off in configuration table as following settings
Set I2C_Register = 0x84
Set I2C_Data1 = 0x00
Set EDID emulation on and select EDID No 0 for emulation EDID in configuration table as following settings
Set I2C_Register = 0x84
Set I2C_Data1 = 0x01
Write EDID emulation on/off setting into PTN3460 configuration table using following I2C commands
I2C Write (I2C_Slave, I2C_Register, I2C_Data1)
B


B
Set the following settings to program PTN3460 configuration table into internal flash memory
I2C_Register = 0xE8
I2C_Data1 = 0x01, I2C_Data2 = 0x78
I2C_Data3 = 0x45, I2C_Data4 = 0x56
Write configuration table into PTN3460 internal flash memory by using the following I2C commands:
I2C Write (I2C_Slave, I2C_Register, I2C_Data1, I2C_Data2, I2C_Data3, I2C_Data4)
Delay 200 mS
C

5.2. Program 1K configuration bytes into PTN3460I flow chart

PTN3460I M/S I2C bus supports I2C 8-bit addressing, so that it can only write 256 bytes data into PTN3460I at one time ($2^8 = 256$). The following flow chart and operation steps describe how to write op_edid.bin into PTN3460I.




A
Use the following settings to program PTN3460 configuration table into internal flash memory
I2C_Register = 0xE8
I2C_Data1 = 0x01, I2C_Data2 = 0x78
I2C_Data3 = 0x45, I2C_Data4 = 0x56
Write configuration table into PTN3460 internal flash memory using following I2C commands
I2C Write (I2C_Slave, I2C_Register, I2C_Data1, I2C_Data2, I2C_Data3, I2C_Data4)
Delay 300 mS
End

6. Configuration Registers

There are 128 bytes configuration registers in configuration table shown as below.

Offset (HEX)	Name	Size (bytes)	Default Value	Bit field	Comment
0	EDID	128			EDID stored for emulation (7 EDID can be accessed from here, EDID selection is made through configuration register 0x85[2:0] - EDID ROM access control register.)
0x80	DisplayPort interface control	1	00	7:6	Reserved
				5	Enable framing support. Default value = 0 0 = Enable framing not support (DPCD reg 0x0D bit 1=0) 1 = Enable framing support (DPCD reg 0x0D bit 1 = 1)
				4	ASSR support. Default value = 0 0 = ASSR not support (DPCD reg 0x0D bit 0 = 0) 1 = ASSR support (DPCD reg 0x0D bit 0 = 1)
				3	DP link rate configuration 0 — Support HBR and RBR link rate 1 — Support RBR link rate only DP lane
				2	DP lane configuration. 0 — 2 lane configuration 1 — 1 lane configuration
				1	0 = AUX P/N swapping disabled. 1 = AUX P/N swapping enabled.
				0	0 = Main link P/N swapping disabled. 1 = Main link P/N swapping enabled.
0x81	LVDS interface control 1	1	0x0B	7	Reserved
				6	LVDS channel mirroring 0 - LVDS channel not mirroring 1 - LVDS channel mirroring
				5:4	Color depth and data packing format 00 — VESA 24 bpp 01 — JEIDA 24 bpp 10 — VESA and JEIDA18 bpp 11 — reserved
				3	Dual LVDS mode. 0 — Single LVDS bus mode 1 — Dual LVDS bus mode

Offset (HEX)	Name	Size (bytes)	Default Value	Bit field	Comment
0x81	LVDS interface control 1	See above page	See above page	2	0 — DE polarity active HIGH 1 — DE polarity active LOW
				1:0	Clock output for dual LVDS mode. 00 — valid clock output on even bus only 01 — valid clock output on odd bus only 10 — reserved 11 — valid clock output on both buses
0x82	LVDS interface control 2	1	0x03	7	V Sync polarity 0 — Positive 1 — Negative
				6	H Sync polarity 0 — Positive 1 — Negative
				5:3	LVDS clock frequency center spreading depth 000 — no spreading 001 — 0.5 % 010 — 1.0 % 011 — 1.5 % 100 — 2.0 % 101 — 2.5 % 110 to 111 — reserved
				2:0	LVDS differential output swing level 000 — 150 mV 001 — 200 mV 010 — 250 mV 011 — 300 mV 100 — 350 mV 101 — 400 mV 110 — 450 mV 111 — reserved

Offset (HEX)	Name	Size (bytes)	Default Value	Bit field	Comment
0x83	LVDS interface control 3	1	0x00	7:3	Reserved
				2	Differential pair (P/N) swapping 0 — normal (as indicated by pin name) 1 — swapped (P ↔ N)
				1	Channel differential pairs order swapping 0 — normal (as indicated by pin names) 1 — channel swapped (A ↔ D, B ↔ CLK, C ↔ C)
				0	LVDS bus swapping 0 — normal (as indicated by pin name) 1 — swapped (odd bus ↔ even bus)
0x84	EDID ROM emulation control	1	0x03	7:4	Reserved
				3:1	Emulated EDID selection. Legal values are [0..6]
				0	Enable EDID emulation 0 — emulation OFF, EDID is read from DDC bus 1 — emulation ON, EDID is read from internal flash
0x85	EDID ROM access control	1	0x00	7:3	Reserved
				2:0	EDID to be accessed through offset 0..127 legal values are [0..6]
0x86	PWM minimum frequency	3	0x000001		24-bit PWM minimum allowed frequency (big endian)
0x89	PWM maximum frequency	3	0xFE0000		24-bit PWM maximum allowed frequency (big endian)

Offset (HEX)	Name	Size (bytes)	Default Value	Bit field	Comment
0x8C	Fast link training control	1	0x08	7:4	Reserved
				3:1	Default equalizer setting for fast link training (default 4) Legal values are 0 (strong EQ) to 7 (no EQ)
				0	Enable fast link training (default 0 = disabled) 0 - FALT is disabled 1 - FALT is enabled
0x8D	Pin config control 1	1	0x00	7	Use CFG2 for Panel Self-Test 0 - Don't use CFG2 for Panel Self Test input pin. 1 - Use CFG2 for Panel Self Test input pin.
				6	Use CFG1 & CFG2 for brightness control (CFG1 = Br+, CFG2 = Br-) 0 - Don't use CFG1 & 2 for brightness control 1 - Use CFG1 & 2 for brightness control
				5	Use CFG3 & CFG4 pin for EDID selection (CFG3:CFG4 pin = EDID ROM Emulation control) 0 - Don't use CFG3 & 4 pin for EDID selection 1 - Use CFG3 & 4 pin for EDID selection - If CFG 3,4 pin = 00, then EDID 0 is used. - If CFG 3,4 pin = 01, then EDID 1 is used. - If CFG 3,4 pin = 10, then EDID 2 is used. - If CFG 3,4 pin = 11, then EDID 3 is used.
				4	Enable PWMI pass through mode (when this bit is set to 1, then the DEV_CFG pin (pin 12) will be used as PWMI pin and PTN3460I I2C slave address will be 0x40). 0 - PWMI is disabled, PWMO is internally generated 1 - PWMI is enabled and used as PWMO source
				3	PWMO disable (default 0 = enabled) 0 - PWMO output is enabled 1 - PWMO output is disabled (high impedance)
				2	Reserved
				1	Reserved
				0	Reserved

Offset (HEX)	Name	Size (bytes)	Default Value	Bit field	Comment
0x8E	Pin config control 2	1	0x00	7	Reserved
				6	Frequency Averaging Filter enable/disable. Note 1 0 – disable (default) 1 – enable
				5	Use CFG4 pin for EDID emulation mode selection 0x8D [bit 5] needs to set to "0" If 0x8E[bit 5] is set to 1. When 0x8E[bit 5] = 1, then CFG4 pin = 0 -> Emulation ON, EDID is read from internal flash CFG4 pin = 1 -> Emulation OFF, EDID is read from DDC bus
				4	Use CFG3 pin for DP lane configuration selection 0x8D[bit 5] needs to set to "0" If 0x8E[bit 4] is set to 1 When 0x8E[bit 4] = 1, then CFG3 pin = 0 -> 2 DP lane configuration CFG3 pin = 1 -> 1 DP lane configuration
				3	Override CFG4 pin 0 - CFG4 pin has priority on I2C/Flash configuration table 1 - I2C/Flash configuration table overrides CFG4 pin
				2	Override CFG3 pin 0 - CFG3 pin has priority on I2C/Flash configuration table 1 - I2C/Flash configuration table overrides CFG3 pin
				1	Override CFG2 pin 0 - CFG2 pin has priority on I2C/Flash configuration table 1 - I2C/Flash configuration table overrides CFG2 pin
				0	Override CFG1 pin 0 - CFG1 pin has priority on I2C/Flash configuration table 1 - I2C/Flash configuration table overrides CFG1 pin
0x8F	PWM default bitcount	1	0x0C	7:0	Default bitcount for PWM control value in DPCD register 0x724
0x90-91	PWM value	2	0x07FF	7:0	Actual value of PWM in DPCD registers 0x722 & 0x723
0x92	PWM default freq	1	0x1D	7:0	Default value for PWM frequency in DPCD register 0x728
0x93	Panel T3 timing	1	0x0A	7:0	Minimum T3 timing of panel power sequence to enforce (expressed in units of 50ms)

Note 1: The function is only available in FW F2 and later FW version

Offset (HEX)	Name	Size (bytes)	Default Value	Bit field	Comment
0x94	Panel T12 timing	1	0x14	7:0	Minimum T12 timing of panel power sequence to enforce (expressed in units of 50ms)
0x95	Backlight control	1	0x00	7:1	Reserved
				0	Backlight disable 0 - Backlight enabled 1 - Backlight disabled
0x96	Panel T2 delay	1	0x01	7:1	Reserved
				0	Enable T2 delay 0 - T2 is not delayed 1 - T2 is delayed by 20mS +/- 50%
0x97	Panel T4 timing	1	0x02	7:0	Minimum T4 timing of panel power sequence to enforce (expressed in units of 50ms)
0x98	Panel T5 delay	1	0x01	7:1	Reserved
				0	Enable T2 delay 0 - T2 is not delayed 1 - T2 is delayed by 20mS +/- 50%
0x99	Firmware PLL range	1	0x02	7:0	0: +/- 1.56%. Note 1 1: +/- 3.12% 2: +/- 6.25% (default) 3: +/- 12.5% 4: +/- 25% 5: +/- 50% 6: +/- 100%
0x9A - 0xD6	*Reserved*		*0x00*		
0xD7 - E7	FoA Mailbox	17	0x00		Byte area mapped to the FoA mailbox

Note 1: The function is only available in FW F2 and later FW version

Offset (HEX)	Name	Size (bytes)	Default Value	Bit field	Comment
0xE8	Flash command	1	0x00	7:0	Flash operation to be executed (default 0) 0 - Erase only 1 - Erase and flash
0xE9	Flash magic number	2	0x00	7:0	Must be equal to 0x7845 for the flash command to be actually processed (big endian) (default 0)
0xEB	Flash trigger	1	0x00	7:0	If 0x56 is written in this register and if Flash magic number is correct, then the flash command will be executed (default 0)
0xEC	Configuration magic number	4	0x12345678	7:0	Must be equal to 0x12345678 for PTN3460I to consider flashed configuration table (big endian) (default 0)

7. Programming Examples

7.1. Panel Brightness Control

// Register 0x90, 0x91 in configuration table are used for controlling PWM output for panel brightness control.

```
i2c_start();          // Generates I2C START condition
i2c_write(0x40);      // Select PTN3460I slave address (DEV_CFG pin = low)
i2c_write(0x90);      // Select I2C Register 0x90
i2c_write(0x07);      // Register 0x90 0x91: PWM value registers
i2c_write(0xFF);      // Write PWM value 0x07FF to register 0x90, 0x91
i2c_stop();           //  Sends I2C stop-condition
```

7.2. Panel LVDS channel and data format setting

// Register 0x80 in configuration table is used for LVDS channel and data format setting

```
i2c_start();          // Generates I2C START condition
i2c_write(0x40);      // Select PTN3460I slave address (DEV_CFG pin = low)
i2c_write(0x80);      // Register 0x80: LVDS interface control 1 register
i2c_write(0x0B);      // Set dual LVDS channel, VESA 24 bpp (bit per pixel)
i2c_stop();           //  Sends I2C stop-condition
```

7.3. LVDS clock frequency spreading depth setting

// Register 0x82 bit [5:3] in configuration table is used for LVDS clock frequency spreading depth setting

```
i2c_start();          // Generates I2C START condition
i2c_write(0x40);      // Select PTN3460I slave address (DEV_CFG pin = low)
i2c_write(0x82);      // Select register 0x82: LVDS interface control 2
```

```
i2c_write(0x10);    // Set Register 0x82 bit [5:3] = 0b010: Set 1% spreading
i2c_stop();         //  Sends I2C stop-condition
```

7.4. LVDS differential output swing level

```
// Register 0x82 bit [2:0] in configuration table is used for LVDS differential output swing level
i2c_start();        // Generates I2C START condition
i2c_write(0x40);    // Select PTN3460I slave address (DEV_CFG pin = low)
i2c_write(0x82);    // Select register 0x82: LVDS interface control 2
i2c_write(0x10);    // Set Register 0x82 bit [2:0] = 0b010: Set 250 mV swing level
i2c_stop();         //  Sends I2C stop-condition
```

7.5. Panel backlight control

```
// Register 0x95 bit [0] in configuration table is used for panel backlight control
i2c_start();        // Generates I2C START condition
i2c_write(0x40);    // Select PTN3460I slave address (DEV_CFG pin = low)
i2c_write(0x95);    // Select register 0x95: Backlight control
i2c_write(0x00);    // Set Register 0x95 bit [0] = 0: Set panel backlight off
i2c_stop();         //  Sends I2C stop-condition
```

7.6. PWM output frequency setting

```
// Register 0x8F, 0x92 in configuration table are used for PWM output frequency setting
// PWM output frequency formula is Fpwm = 27000000 / (2^Pn * Fd)
// Pn is register 0x8F, Fd is register 0x92
i2c_start();        // Generates I2C START condition
```

```
i2c_write(0x40);      // Select PTN3460I slave address (DEV_CFG pin = low)
i2c_write(0x8F);      // Register 0x8F: PWM default bitcount
i2c_write(0x0C);      // Register 0x8F = 0x0C
i2c_stop();           //  Sends I2C stop-condition
i2c_start();          // Generates I2C START condition
i2c_write(0x40);      // Select PTN3460I slave address (DEV_CFG pin = low)
i2c_write(0x92);      // Register 0x92: PWM default freq
i2c_write(0x2e);      // Register 0x92 = 0x1d,
                      // Fpwm = 27000000 / (2^12 * 0x1d) = 27000000 / (4096 * 29) =~ 227Hz
i2c_stop();           //  Sends I2C stop-condition
```

7.7. Program CFG3, CFG4 pins as panel selection pins

```
// Register 0x8D bit 5 (Pin config control 1) in configuration table is used to set CFG3 and CFG4
// pins for EDID (panel) selection.
i2c_start();          // Generates I2C START condition
i2c_write(0x40);      // Select PTN3460I slave address (DEV_CFG pin = low)
i2c_write(0x8D);      // Register 0x8D: Pin config control 1 register
i2c_write(0x20);      // Register 0x8D = 0x20: set CFG3 and CFG4 pins for EDID selection
i2c_stop();           //  Sends I2C stop-condition
// Set CFG 3pin = 0, CFG4 pin = 0 to select emulation EDID no. 0 (Panel A)
// Set CFG 3pin = 0, CFG4 pin = 1 to select emulation EDID no. 1 (Panel B)
// Set CFG 3pin = 1, CFG4 pin = 0 to select emulation EDID no. 2 (Panel C)
// Set CFG 3pin = 1, CFG4 pin = 1 to select emulation EDID no. 3 (Panel D)
```

7.8. Write EDID No 0 – 6 to configuration table in internal SRAM

// Register 0x85 bit [2:0] (EDID ROM access control) is used to set where the EDID is going to be written to EDID 0 – 6 in 1k bytes configuration table in PTN3460I internal SRAM.

```
i2c_start();          // Generates I2C START condition
i2c_write(0x40);      // Select PTN3460I slave address (DEV_CFG pin = low)
i2c_write(0x85);      // Register 0x85: EDID ROM access control
i2c_write(0x02);      // Register 0x85 = 0x02, the EDID writes to I2C register 0x00 – 0x7F will be
                      // written to EDID 2 in configuration table in internal SRAM
i2c_stop();           //  Sends I2C stop-condition
i2c_start();          // Generates I2C START condition
i2c_write(0x40);      // Select PTN3460I slave address (DEV_CFG pin = low)
i2c_write(0x00);      // Set EDID writing from I2C Register 0x00
i2c_write(128);     // Write 128 bytes EDID to EDID 2 into configuration table
i2c_stop();           //  Sends I2C stop-condition
```

7.9. Program configuration table into PTN3460I internal flash memory

// Register 0xE8 – 0xEB configuration table are used for programming configuration table into PTN3460I internal flash memory

```
i2c_start();          // Generates I2C START condition
i2c_write(0x40);      // Select PTN3460I slave address (DEV_CFG pin = low)
i2c_write(0xE8);      // Register 0xE8: Flash operation register
i2c_write(0x01);      // Register 0xE8 = 0x01: Perform erase and then flash operation
i2c_write(0x78);      // Register 0xE9, EA = 0x7845: Flash magic number. Only flash magic
i2c_write(0x45);      // number is correct, then flash operation can be executed
i2c_write(0x56);      // Register 0xEB = 0x56: Flash trigger register. The 1K configuration table
                      // will be written into PTN3460I internal flash memory.
```

```
i2c_stop();            //  Sends I2C stop-condition
```

7.10.Select emulation EDID No 0

```
// Register 0x84 in configuration table is used for EDID ROM emulation control and 7 EDID
// selection

i2c_start();           // Generates I2C START condition

i2c_write(0x40);       // Select PTN3460I slave address (DEV_CFG pin = low)

i2c_write(0x84);       // Register 0x84: EDID ROM emulation control register

i2c_write(0x01);       // 0x84 bit [0] = 1: EDID emulation is on. 0x84 bit [3:1] = 0: Select EDID no 0
// for EDID emulation data.

i2c_stop();            //  Sends I2C stop-condition

// When GPU uses I2C-Over-Aux to read EDID from PTN3460I, it will get emulation EDID no 0
// from PTN3460I.
// Emulation EDID no 0 in configuration table in PTN3460I firmware is 1024x768 @ 60Hz
// and the EDID data is as following.

// 0x00, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x3B, 0x10, 0x60, 0x34, 0x00, 0x00, 0x00, 0x00,

// 0x26, 0x15, 0x01, 0x03, 0x68, 0x1E, 0x16, 0x78, 0xEE, 0x37, 0x25, 0x9E, 0x58, 0x4A, 0x97, 0x26,

// 0x19, 0x50, 0x54, 0xAD, 0xEE, 0x00, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01,

// 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x64, 0x19, 0x00, 0x40, 0x41, 0x00, 0x26, 0x30, 0x18, 0x88,

// 0x36, 0x00, 0x30, 0xE4, 0x10, 0x00, 0x00, 0x18, 0x00, 0x00, 0x00, 0xFD, 0x00, 0x32, 0x4C, 0x1E,

// 0x3F, 0x08, 0x00, 0x0A, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x00, 0x00, 0xFC, 0x00, 0x41,

// 0x49, 0x4F, 0x20, 0x50, 0x43, 0x0a, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x00, 0x00, 0xFF,

// 0x00, 0x4E, 0x58, 0x50, 0x20, 0x50, 0x54, 0x4E, 0x33, 0x34, 0x36, 0x30, 0x20, 0x20, 0x00, 0xAF,
```

7.11.Select emulation EDID No 1

```
// Register 0x84 in configuration table is used for EDID ROM emulation control and 7 EDID
selection
```

```
i2c_start();            // Generates I2C START condition

i2c_write(0x40);        // Select PTN3460I slave address (DEV_CFG pin = low)

i2c_write(0x84);        // Register 0x84: EDID ROM emulation control register

i2c_write(0x03);        // 0x84 bit [0] = 1: EDID emulation is on. 0x84 bit [3:1] = 1: Select EDID no 1
// for EDID emulation data.

i2c_stop();             //  Sends I2C stop-condition

// When GPU uses I2C-Over-Aux to read EDID from PTN3460I, it will get emulation EDID no 1
// from PTN3460I.
// Emulation EDID no 1 in configuration table in PTN3460I firmware is 800 x 480 @ 60Hz        //
and the EDID data is as following.

//0x00, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x3B, 0x10, 0x60, 0x34, 0xE0, 0x36, 0x0C,0x00,

//0x10, 0x18, 0x01, 0x03, 0x80, 0x1E, 0x16, 0x78, 0x0A, 0x37, 0x25, 0x9E, 0x58, 0x4A, 0x97, 0x26,

//0x19, 0x50, 0x54, 0x00, 0x00, 0x00, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01,

//0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0xE4, 0x0C, 0x20, 0x00, 0x31, 0xE0, 0x2D, 0x10, 0xD2, 0x1E,

//0x6D, 0x04, 0x30, 0xE4, 0x10, 0x00, 0x00, 0x1A, 0x00, 0x00, 0x00, 0x10, 0x00, 0xE0, 0x2D, 0x10,

//0xD2, 0x1E, 0x6D, 0x04, 0x30, 0xE4, 0x10, 0x00, 0x00, 0x18, 0x00, 0x00, 0x00, 0x10, 0x00, 0x41,

//0x49, 0x4F, 0x20, 0x50, 0x43, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x00, 0x00, 0x00, 0x10,

//0x00, 0xE0, 0x2D, 0x10, 0xD2, 0x1E, 0x6D, 0x04, 0x30, 0xE4, 0x10, 0x00, 0x00, 0x1A, 0x00, 0x08,
```

7.12.Select emulation EDID No 2

```
// Register 0x84 in configuration table is used for EDID ROM emulation control and 7 EDID
// selection

i2c_start();            // Generates I2C START condition

i2c_write(0x40);        // Select PTN3460I slave address (DEV_CFG pin = low)

i2c_write(0x84);        // Register 0x84: EDID ROM emulation control register

i2c_write(0x05);        // 0x84 bit [0] = 1: EDID emulation is on. 0x84 bit [3:1] = 2: Select EDID no 2
for EDID emulation data.

i2c_stop();             //  Sends I2C stop-condition
```

// When GPU uses I2C-Over-Aux to read EDID from PTN3460I, it will get emulation EDID no 2
// from PTN3460I.
// Emulation EDID no 2 in configuration table in PTN3460I firmware is **480 x 272 @ 60Hz**
and the EDID data is as following.

//0x00, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0x00, 0x3b, 0x10, 0x60, 0x34, 0xd0, 0x3a, 0x06, 0x00,

//0x10, 0x18, 0x01, 0x03, 0x68, 0x1e, 0x16, 0x78, 0xee, 0x37, 0x25, 0x9e, 0x58, 0x4a, 0x97, 0x26,

//0x19, 0x50, 0x54, 0x00, 0x00, 0x00, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01,

//0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x84, 0x03, 0xe0, 0x2d, 0x10, 0x10, 0x0c, 0x10, 0x02, 0x29,

//0x2a, 0x00, 0x30, 0xe4, 0x10, 0x00, 0x00, 0x18, 0x00, 0x00, 0x00, 0xfd, 0x00, 0x32, 0x4c, 0x1e,

//0x3f, 0x08, 0x00, 0x0a, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x00, 0x00, 0xfc, 0x00, 0x48,

//0x50, 0x20, 0x76, 0x73, 0x31, 0x35, 0x63, 0x0a, 0x20, 0x20, 0x20, 0x20, 0x00, 0x00, 0x00, 0xff,

//0x00, 0x43, 0x4e, 0x4e, 0x35, 0x32, 0x38, 0x32, 0x35, 0x35, 0x43, 0x0a, 0x20, 0x20, 0x00, 0x22,

7.13.Select emulation EDID No 3

// Register 0x84 in configuration table is used for EDID ROM emulation control and 7 EDID selection

```
i2c_start();            // Generates I2C START condition

i2c_write(0x40);        // Select PTN3460I slave address (DEV_CFG pin = low)

i2c_write(0x84);        // Register 0x84: EDID ROM emulation control register

i2c_write(0x07);        // 0x84 bit [0] = 1: EDID emulation is on. 0x84 bit [3:1] = 3: Select EDID no 3
//for EDID emulation data.

i2c_stop();             //  Sends I2C stop-condition
```

// When GPU uses I2C-Over-Aux to read EDID from PTN3460I, it will get emulation EDID no 3
from // PTN3460I.

// Emulation EDID no 3 in configuration table in PTN3460I firmware is **1600 x 900 @ 60Hz**
// and the EDID data is as following.

// 0x00, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0x00, 0x3B, 0x10, 0x4a, 0x31, 0x00, 0x00, 0x00, 0x00,

// 0x00, 0x14, 0x01, 0x01, 0x80, 0x33, 0x1d, 0x78, 0x0a, 0x87, 0xf5, 0x94, 0x57, 0x4f, 0x8c, 0x27,

// 0x27, 0x50, 0x54, 0x00, 0x00, 0x00, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01,

// 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x3c, 0x2e, 0x40, 0x00, 0x62, 0x84, 0x22, 0x30, 0x58, 0xa8,

// 0x35, 0x00, 0xbb, 0xf9, 0x10, 0x00, 0x00, 0x19, 0x00, 0x00, 0x00, 0x0f, 0x00, 0x00, 0x00, 0x00,

// 0x00, 0x00, 0x00, 0x00, 0x00, 0x1e, 0x50, 0x0c, 0x13, 0x00, 0x00, 0x00, 0x00, 0xfc, 0x00, 0x41,

// 0x49, 0x4f, 0x20, 0x50, 0x43, 0x0a, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x00, 0x00, 0xfe,

// 0x00, 0x31, 0x38, 0x34, 0x48, 0x54, 0x30, 0x33, 0x2d, 0x30, 0x30, 0x31, 0x0a, 0x20, 0x00, 0x30,

7.14.Select emulation EDID No 4

// Register 0x84 in configuration table is used for EDID ROM emulation control and 7 EDID selection

i2c_start(); // Generates I2C START condition

i2c_write(0x40); // Select PTN3460I slave address (DEV_CFG pin = low)

i2c_write(0x84); // Register 0x84: EDID ROM emulation control register

i2c_write(0x09); // 0x84 bit [0] = 1: EDID emulation is on. 0x84 bit [3:1] = 4: Select EDID no 4 for EDID emulation data.

i2c_stop(); // Sends I2C stop-condition

// When GPU uses I2C-Over-Aux to read EDID from PTN3460I, it will get emulation EDID no 4
// from PTN3460I.
// The emulation EDID no 4 in configuration table in PTN3460I firmware is **1920 x 1080 @ 60Hz**
// and the data is as following.

// 0x00, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x3B, 0x10, 0x11, 0x11, 0x01, 0x00, 0x00, 0x00,

// 0x2B, 0x15, 0x01, 0x03, 0x80, 0x35, 0x1F, 0x78, 0xEE, 0x9A, 0x80, 0xA3, 0x58, 0x51, 0x9E, 0x25,

// 0x0E, 0x50, 0x54, 0x00, 0x00, 0x00, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01,

// 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x40, 0x38, 0x80, 0x00, 0x71, 0x38, 0x14, 0x40, 0x58, 0x2C,

// 0x45, 0x00, 0xFE, 0x1E, 0x11, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0xFC, 0x00, 0x4F, 0x70, 0x74,

// 0x69, 0x50, 0x6C, 0x65, 0x78, 0x20, 0x39, 0x30, 0x31, 0x30, 0x00, 0x00, 0x00, 0xFC, 0x00, 0x0A,

// 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x00, 0x00, 0xFC,

// 0x00, 0x0A, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x1D,

7.15.Select emulation EDID No 5

// Register 0x84 in configuration table is used for EDID ROM emulation control and 7 EDID selection

i2c_start(); // Generates I2C START condition

i2c_write(0x40); // Select PTN3460I slave address (DEV_CFG pin = low)

i2c_write(0x84); // Register 0x84: EDID ROM emulation control register

i2c_write(0x0B); // 0x84 bit [0] = 1: EDID emulation is on. 0x84 bit [3:1] = 5: Select EDID no 5 for EDID emulation data.

i2c_stop(); // Sends I2C stop-condition

// When GPU uses I2C-Over-Aux to read EDID from PTN3460I, it will get emulation EDID no 5
// from PTN3460I.
// Emulation EDID no 5 in configuration table in PTN3460I firmware is 1366 x 768 @ 60Hz
// and the EDID data is as following.

// 0x00, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x3B, 0x10, 0x60, 0x34, 0x84, 0x0D, 0x00, 0x00,

// 0x26, 0x15, 0x01, 0x03, 0x80, 0x33, 0x1D, 0x78, 0x0A, 0x87, 0xF5, 0x94, 0x57, 0x4F, 0x8C, 0x27,

// 0x27, 0x50, 0x54, 0x00, 0x00, 0x00, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01,

// 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x3E, 0x1C, 0x56, 0xA0, 0x50, 0x00, 0x16, 0x30, 0x30, 0x20,

// 0x25, 0x00, 0x99, 0xE6, 0x10, 0x00, 0x00, 0x19, 0x00, 0x00, 0x00, 0x0F, 0x00, 0x00, 0x00, 0x00,

// 0x00, 0x00, 0x00, 0x00, 0x00, 0x1B, 0xE8, 0x04, 0x5A, 0x00, 0x00, 0x00, 0x00, 0xFE, 0x00, 0x4E,

// 0x58, 0x50, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x00, 0x00, 0xFE,

// 0x00, 0x41, 0x49, 0x4F, 0x20, 0x50, 0x43, 0x0a, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0xC6,

7.16.Select emulation EDID No 6

// Register 0x84 in configuration table is used for EDID ROM emulation control and 7 EDID selection

i2c_start(); // Generates I2C START condition

i2c_write(0x40); // Select PTN3460I slave address (DEV_CFG pin = low)

i2c_write(0x84); // Register 0x84: EDID ROM emulation control register

i2c_write(0x0D); // 0x84 bit [0] = 1: EDID emulation is on. 0x84 bit [3:1] = 6: Select EDID no 6 for EDID emulation data.

i2c_stop(); // Sends I2C stop-condition

// When GPU uses I2C-Over-Aux to read EDID from PTN3460I, it will get emulation EDID no 6
// from PTN3460I.
// Emulation EDID no 6 in configuration table in PTN3460I firmware is **320 x 240 @ 60Hz**
// and the data is as following.

//0x00, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0x00, 0x3b, 0x10, 0x60, 0x34, 0xf0, 0xe2, 0x04, 0x00,

//0x10, 0x18, 0x01, 0x03, 0x68, 0x1e, 0x16, 0x78, 0xee, 0x37, 0x25, 0x9e, 0x58, 0x4a, 0x97, 0x26,

//0x19, 0x50, 0x54, 0x00, 0x00, 0x00, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01,

//0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x58, 0x02, 0x40, 0x50, 0x10, 0xf0, 0x0a, 0x00, 0x18, 0x20,

//0x42, 0x00, 0x30, 0xe4, 0x10, 0x00, 0x00, 0x18, 0x00, 0x00, 0x00, 0xfd, 0x00, 0x32, 0x4c, 0x1e,

//0x3f, 0x08, 0x00, 0x0a, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x00, 0x00, 0xfc, 0x00, 0x48,

//0x50, 0x20, 0x76, 0x73, 0x31, 0x35, 0x63, 0x0a, 0x20, 0x20, 0x20, 0x20, 0x00, 0x00, 0x00, 0xff,

//0x00, 0x43, 0x4e, 0x4e, 0x35, 0x32, 0x38, 0x32, 0x35, 0x35, 0x43, 0x0a, 0x20, 0x20, 0x00, 0x13

7.17. Program 1K configuration bytes into PTN3460I steps

Step1: Write EDID No0 (128 bytes) and configuration register data (128 bytes) into PTN3460I

i2c_start(); // Generates I2C START condition

i2c_write(0x40); // Select PTN3460I slave address (DEV_CFG pin = low)

i2c_write(0x00); // Set PTN3460I I2C register address = 0x00

i2c_write_256bytes(); // Write EDID No0 and configuration data (shown in below) into PTN3460I

// EDID No0 (128 bytes as below)

// 0x00, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x40, 0xA7, 0x11, 0x11, 0x01, 0x00, 0x00, 0x00,
// 0x1E, 0x15, 0x01, 0x03, 0x80, 0x33, 0x1D, 0x78, 0xEE, 0xEE, 0x20, 0xA3, 0x56, 0x51, 0x9E, 0x27,
// 0x0B, 0x50, 0x54, 0x00, 0x00, 0x00, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01,
// 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x9D, 0x34, 0x80, 0x64, 0x70, 0x38, 0x1F, 0x40, 0x1E, 0x14,
// 0x35, 0x00, 0xFD, 0x1E, 0x11, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0xFC, 0x00, 0x50, 0x45, 0x47,
// 0x31, 0x0A, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x00, 0x00, 0xFC, 0x00, 0x0A,
// 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x00, 0x00, 0xFC,
// 0x00, 0x0A, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x45,
// Configuration register data (128 bytes as below)
// 0x00, 0x0B, 0x2B, 0x00, 0x01, 0x00, 0x00, 0x00, 0x01, 0xFE, 0x00, 0x00, 0x08, 0x20, 0x00, 0x0C,
// 0x07, 0xFF, 0x00, 0x0A, 0x24, 0x00, 0x01, 0x02, 0x01, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00,
// 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00,
// 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00,
// 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00,
// 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00,
// 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x12, 0x34, 0x56, 0x78,
// 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF

i2c_stop(); // Sends I2C stop-condition

Step2: Write EDID No1 (128 bytes) into PTN3460I

i2c_start(); // Generates I2C START condition

i2c_write(0x40); // Select PTN3460I slave address (DEV_CFG pin = low)

i2c_write(0x85); // Register 0x85: EDID ROM access control register

i2c_write(0x01); // Register 0x85= 0x01: Set EDID No1 to be access through I2C register 0x00 – 0x7f

i2c_stop(); // Sends I2C stop-condition

i2c_start(); // Generates I2C START condition

i2c_write(0x40); // Select PTN3460I slave address (DEV_CFG pin = low)

i2c_write(0x00); // Set PTN3460I I2C register address = 0x00

i2c_write_128bytes(); // Write EDID No1 (shown in below) into PTN3460I

// EDID No1 (128 bytes as below)
// 0x00, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x10, 0xAC, 0x48, 0x05, 0x01, 0x00, 0x00, 0x00,
// 0x1E, 0x15, 0x01, 0x03, 0x80, 0x33, 0x1D, 0x78, 0xEE, 0x9A, 0x80, 0xA3, 0x58, 0x51, 0x9E, 0x25,
// 0x0E, 0x50, 0x54, 0x00, 0x00, 0x00, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01,

```
// 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x40, 0x38, 0x80, 0x00, 0x71, 0x38, 0x14, 0x40, 0x58, 0x2C,
// 0x45, 0x00, 0xFE, 0x1E, 0x11, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0xFC, 0x00, 0x49, 0x4E, 0x53,
// 0x50, 0x49, 0x52, 0x4F, 0x4E, 0x20, 0x4F, 0x4E, 0x45, 0x0A, 0x00, 0x00, 0x00, 0xFC, 0x00, 0x0A,
// 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x00, 0x00, 0xFC,
// 0x00, 0x0A, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x33,
```

i2c_stop(); // Sends I2C stop-condition

Step3: Write EDID No2 (128 bytes) into PTN3460I

i2c_start(); // Generates I2C START condition

i2c_write(0x40); // Select PTN3460I slave address (DEV_CFG pin = low)

i2c_write(0x85); // Register 0x85: EDID ROM access control register

i2c_write(0x02); // Register 0x85= 0x02: Set EDID No2 to be access through I2C register 0x00 – 0x7f

i2c_stop(); // Sends I2C stop-condition

i2c_start(); // Generates I2C START condition

i2c_write(0x40); // Select PTN3460I slave address (DEV_CFG pin = low)

i2c_write(0x00); // Set PTN3460I I2C register address = 0x00

i2c_write_128bytes(); // Write EDID No2 (shown in below) into PTN3460I

```
// EDID No2 (128 bytes as below)
// 0x00, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x10, 0xAC, 0x48, 0x05, 0x01, 0x00, 0x00, 0x00,
// 0x1E, 0x15, 0x01, 0x03, 0x80, 0x33, 0x1D, 0x78, 0xEE, 0xEE, 0x20, 0xA3, 0x56, 0x51, 0x9E, 0x27,
// 0x0B, 0x50, 0x54, 0x00, 0x00, 0x00, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01,
// 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x9D, 0x34, 0x80, 0x64, 0x70, 0x38, 0x1F, 0x40, 0x1E, 0x14,
// 0x35, 0x00, 0xFD, 0x1E, 0x11, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0xFC, 0x00, 0x49, 0x4E, 0x53,
// 0x50, 0x49, 0x52, 0x4F, 0x4E, 0x20, 0x4F, 0x4E, 0x45, 0x0A, 0x00, 0x00, 0x00, 0xFC, 0x00, 0x0A,
// 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x00, 0x00, 0xFC,
// 0x00, 0x0A, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0xDE,
```

i2c_stop(); // Sends I2C stop-condition

Step4: Write EDID No3 (128 bytes) into PTN3460I

i2c_start(); // Generates I2C START condition

i2c_write(0x40); // Select PTN3460I slave address (DEV_CFG pin = low)

i2c_write(0x85); // Register 0x85: EDID ROM access control register

i2c_write(0x03); // Register 0x85= 0x03: Set EDID No3 to be access through I2C register 0x00 – 0x7f

i2c_stop(); // Sends I2C stop-condition

i2c_start(); // Generates I2C START condition

i2c_write(0x40); // Select PTN3460I slave address (DEV_CFG pin = low)

i2c_write(0x00); // Set PTN3460I I2C register address = 0x00

i2c_write_128bytes(); // Write EDID No3 (shown in below) into PTN3460I

// EDID No3 (128 bytes as below)
// 0x00, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x40, 0xA7, 0x11, 0x11, 0x01, 0x00, 0x00, 0x00,
// 0x1E, 0x15, 0x01, 0x03, 0x80, 0x33, 0x1D, 0x78, 0xEE, 0xEE, 0x20, 0xA3, 0x56, 0x51, 0x9E, 0x27,
// 0x0B, 0x50, 0x54, 0x00, 0x00, 0x00, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01,
// 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x9D, 0x34, 0x80, 0x64, 0x70, 0x38, 0x1F, 0x40, 0x1E, 0x14,
// 0x35, 0x00, 0xFD, 0x1E, 0x11, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0xFC, 0x00, 0x50, 0x45, 0x47,
// 0x34, 0x0A, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x00, 0x00, 0xFC, 0x00, 0x0A,
// 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x00, 0x00, 0xFC,
// 0x00, 0x0A, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x42,

i2c_stop(); // Sends I2C stop-condition

Step5: Write EDID No4 (128 bytes) into PTN3460I

i2c_start(); // Generates I2C START condition

i2c_write(0x40); // Select PTN3460I slave address (DEV_CFG pin = low)

i2c_write(0x85); // Register 0x85: EDID ROM access control register

i2c_write(0x04); // Register 0x85= 0x04: Set EDID No4 to be access through I2C register 0x00 – 0x7f

i2c_stop(); // Sends I2C stop-condition

i2c_start(); // Generates I2C START condition

i2c_write(0x40); // Select PTN3460I slave address (DEV_CFG pin = low)

i2c_write(0x00); // Set PTN3460I I2C register address = 0x00

i2c_write_128bytes(); // Write EDID No4 (shown in below) into PTN3460I

// EDID No4 (128 bytes as below)
// 0x00, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x40, 0xA7, 0x11, 0x11, 0x01, 0x00, 0x00, 0x00,
// 0x1E, 0x15, 0x01, 0x03, 0x80, 0x33, 0x1D, 0x78, 0xEE, 0xEE, 0x20, 0xA3, 0x56, 0x51, 0x9E, 0x27,
// 0x0B, 0x50, 0x54, 0x00, 0x00, 0x00, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01,
// 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x9D, 0x34, 0x80, 0x64, 0x70, 0x38, 0x1F, 0x40, 0x1E, 0x14,
// 0x35, 0x00, 0xFD, 0x1E, 0x11, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0xFC, 0x00, 0x50, 0x45, 0x47,
// 0x35, 0x0A, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x00, 0x00, 0xFC, 0x00, 0x0A,
// 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x00, 0x00, 0xFC,
// 0x00, 0x0A, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x41,,

i2c_stop(); // Sends I2C stop-condition

Step6: Write EDID No5 (128 bytes) into PTN3460I

i2c_start(); // Generates I2C START condition

i2c_write(0x40); // Select PTN3460I slave address (DEV_CFG pin = low)

i2c_write(0x85); // Register 0x85: EDID ROM access control register

i2c_write(0x05); // Register 0x85= 0x05: Set EDID No5 to be access through I2C register 0x00 – 0x7f

i2c_stop(); // Sends I2C stop-condition

i2c_start(); // Generates I2C START condition

i2c_write(0x40); // Select PTN3460I slave address (DEV_CFG pin = low)

i2c_write(0x00); // Set PTN3460I I2C register address = 0x00

i2c_write_128bytes(); // Write EDID No5 (shown in below) into PTN3460I

// EDID No5 (128 bytes as below)
// 0x00, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x40, 0xA7, 0x11, 0x11, 0x01, 0x00, 0x00, 0x00,
// 0x1E, 0x15, 0x01, 0x03, 0x80, 0x33, 0x1D, 0x78, 0xEE, 0xEE, 0x20, 0xA3, 0x56, 0x51, 0x9E, 0x27,
// 0x0B, 0x50, 0x54, 0x00, 0x00, 0x00, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01,
// 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x9D, 0x34, 0x80, 0x64, 0x70, 0x38, 0x1F, 0x40, 0x1E, 0x14,
// 0x35, 0x00, 0xFD, 0x1E, 0x11, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0xFC, 0x00, 0x50, 0x45, 0x47,
// 0x36, 0x0A, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x00, 0x00, 0xFC, 0x00, 0x0A,
// 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x00, 0x00, 0xFC,
// 0x00, 0x0A, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x40,

i2c_stop(); // Sends I2C stop-condition

Step7: Write EDID No6 (128 bytes) into PTN3460I

i2c_start(); // Generates I2C START condition

i2c_write(0x40); // Select PTN3460I slave address (DEV_CFG pin = low)

i2c_write(0x85); // Register 0x85: EDID ROM access control register

i2c_write(0x05); // Register 0x85= 0x06: Set EDID No6 to be access through I2C register 0x00 – 0x7f

i2c_stop(); // Sends I2C stop-condition

i2c_start(); // Generates I2C START condition

i2c_write(0x40); // Select PTN3460I slave address (DEV_CFG pin = low)

i2c_write(0x00); // Set PTN3460I I2C register address = 0x00

i2c_write_128bytes(); // Write EDID No6 (shown in below) into PTN3460I

// EDID No6 (128 bytes as below)
// 0x00, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x40, 0xA7, 0x11, 0x11, 0x01, 0x00, 0x00, 0x00,
// 0x1E, 0x15, 0x01, 0x03, 0x80, 0x33, 0x1D, 0x78, 0xEE, 0xEE, 0x20, 0xA3, 0x56, 0x51, 0x9E, 0x27,
// 0x0B, 0x50, 0x54, 0x00, 0x00, 0x00, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x01,
// 0x01, 0x01, 0x01, 0x01, 0x01, 0x01, 0x9D, 0x34, 0x80, 0x64, 0x70, 0x38, 0x1F, 0x40, 0x1E, 0x14,
// 0x35, 0x00, 0xFD, 0x1E, 0x11, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0xFC, 0x00, 0x50, 0x45, 0x47,
// 0x37, 0x0A, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x00, 0x00, 0xFC, 0x00, 0x0A,
// 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x00, 0x00, 0xFC,
// 0x00, 0x0A, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x20, 0x00, 0x3F,

i2c_stop(); // Sends I2C stop-condition

Step8: Write 7 EDID and configuration register data into PTN3460I internal flash memory (1K bytes)

// Register 0xE8 – 0xEB configuration table are used for programming configuration table into PTN3460I internal flash memory

i2c_start(); // Generates I2C START condition

i2c_write(0x40); // Select PTN3460I slave address (DEV_CFG pin = low)

```
i2c_write(0xE8);     // Register 0xE8: Flash operation register
i2c_write(0x01);     // Register 0xE8 = 0x01: Perform erase and then flash operation
i2c_write(0x78);     // Register 0xE9, EA = 0x7845: Flash magic number. Only flash magic
i2c_write(0x45);     // number is correct, then flash operation can be executed
i2c_write(0x56);     // Register 0xEB = 0x56: Flash trigger register. The 1K configuration table
                     // will be written into PTN3460I internal flash memory.
i2c_stop();          //  Sends I2C stop-condition
 wait (300ms);       // Wait 300mS to have PTN3460I internal flash memory programmed properly.
```

7.18. Read 1K configuration bytes from PTN3460I

When reading out EDIDs and configuration register data from PTN3460I for verification, it should do same procedure like writing procedure just change write data command to read data command.