Cost Efficient Solutions with Freescale Microcontollers for Automotive Application

EUF-ACC-T1466

Lorenzo Daniele | Field Application Engineer

M A Y . 2 0 1 5

External Use

Agenda

- Automotive MCUs introduction
- MCUs solutions for body applications
- Powertrain and chassis
- Functional safety
- Security
- Automotive Infotainment and Instrument Cluster Applications

Automotive MCU Introduction

Freescale - A *Global Leader* in Microcontrollers and Digital Networking Processors

>50 Year Legacy

>5,500 Engineers

>6,000 Patent Families

Five Core Product Groups

- Microcontrollers
- Digital Networking
- Automotive MCU
- Analog & Sensors
- RF

Four Primary Markets

- Automotive
- Networking
- Industrial
- Consumer

Automotive Key Trends

Increased Efficiency

- Fuel efficiency and lower emissions
- Overall electrification of multiple functions

Connected Vehicle

- In-vehicle, car-to-car, car-to-infrastructure, car-to-cloud
- The ultimate smart mobile device

Enhanced Safety

- Zero vehicle-related fatalities
- Seamless integration of active and passive safety systems

Mobility for Everyone

- Cost efficient scalable products for an expanding global market

Automotive Microcontroller Portfolio

Powertrain | Safety & Chassis | Body | DIS

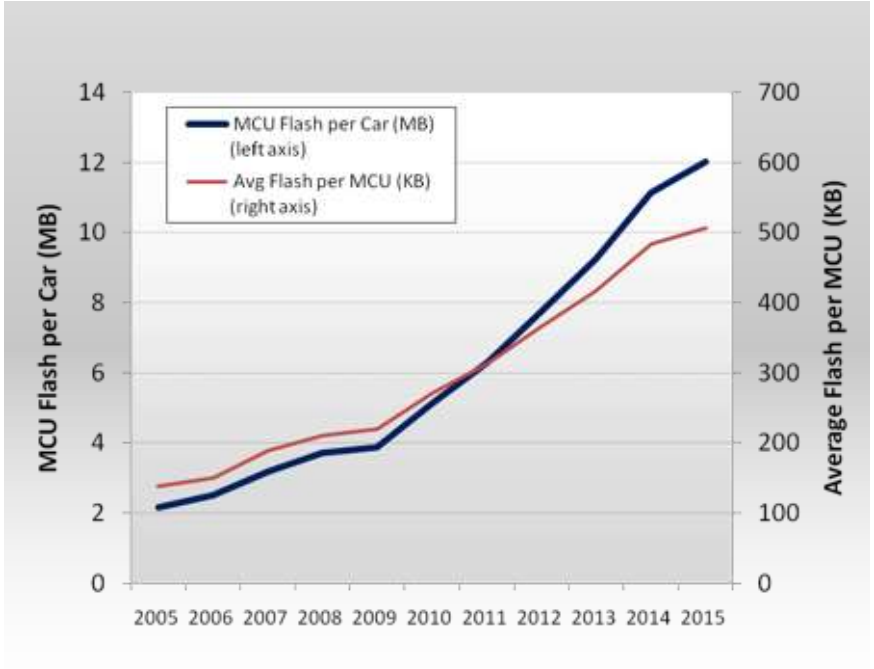
ARM 32-bit ARM®

32-bit Power Architecture®

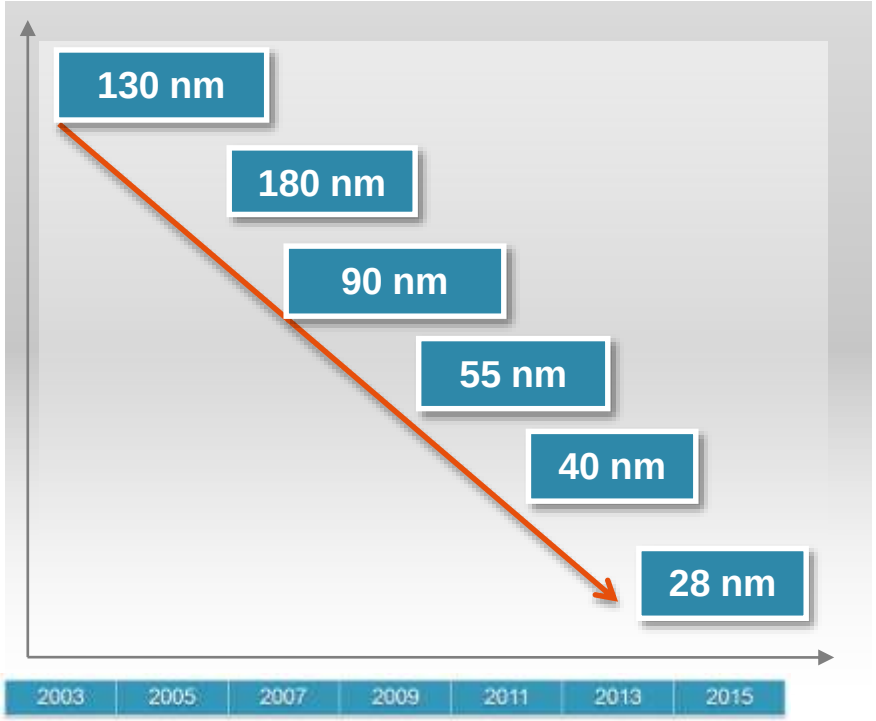
8-16-bit S08 / S12 / MagniV

Optimized architecture for each market segment

Embedded Flash Technology Innovation



Sources: Strategy Analytics (Jan'12), IHS Automotive (Jun'12)



Freescale aggressively drives embedded technology for Auto MCU applications

What is SG-TFS?

SG = Split Gate Architecture

- ✓ Fast ➡ Fast Read and Write
- ✓ Flexible ➡ Small sectors for boot, EEPROM
- ✓ Low cost ➡ Area efficient layout

+

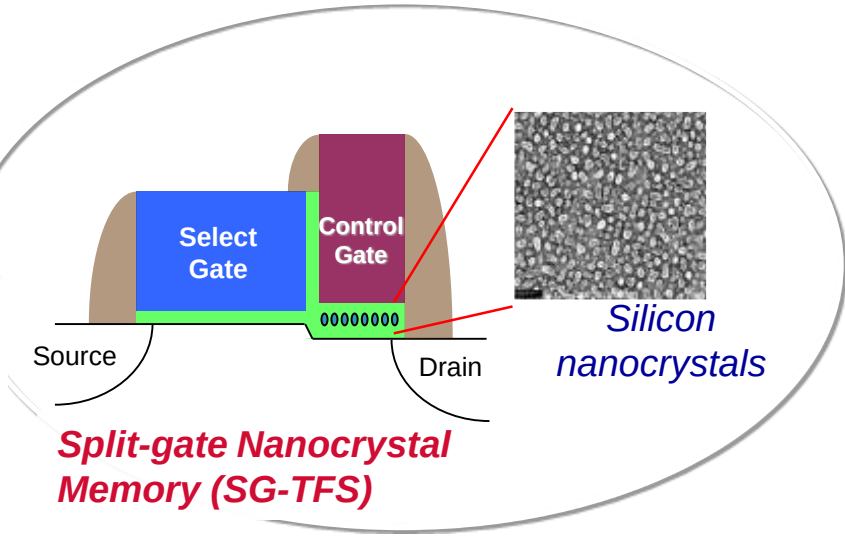
TFS: Thin-Film Storage using Silicon Nanocrystals

- ✓ Reliable ➡ Tolerant to charge loss
- ✓ Low cost ➡ Simple integration into CMOS
- ✓ Scalable ➡ Less influenced by geometry

+

Product-ready flash IP

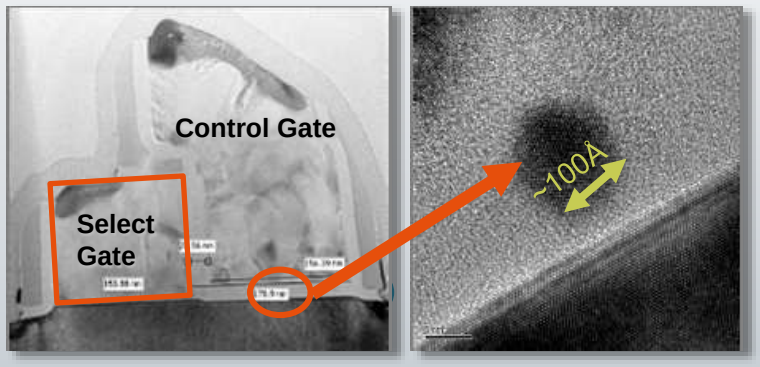
- ✓ High performance ➡ Supporting fast & wide flash for 32bit cores
- ✓ Low cost ➡ Efficient code flash and EEPROM
- ✓ Low power ➡ Minimal read/write/erase current consumption



SG-TFS wins industry Innovation award…..

UBM TechInsights (EE Times) presents 2012….

SG-TFS Embedded Memory Solution



INSIGHT AWARDS
UBM TECHINSIGHTS
WINNER

Most Innovative Process Technology

The 10th edition of the Insight Awards honors new process technology deemed to be the most innovative among those that introduced new process nodes, new manufacturing techniques and new material structures.

Tapping the Potential of Nanotechnology

Covered by **150+ worldwide patents**, SG-TFS memory technology delivers the **most reliable, scalable and high-endurance embedded memory** solution for the global MCU market.

Best-in-Class Low-Power Performance

The split-gate architecture combined with the efficiency of nanocrystals creates a potent combination of **highest performance with lowest power consumption** of any embedded flash technology in the market.

MCU Solutions for Body Applications

S12MagniV

- S12 MagniV **simplifies** system design with the integration of **high-voltage (40V)** analog IP onto **mixed-signal MCUs** for automotive applications
- Building upon **proven high-volume LL18 technology**
- Ideal for **space constraint** applications like **sensor and actuators**
- Reduces the Total Cost of Ownership (TCO) through **bill of material (BOM) and manufacturing cost reductions** (PCB assembly)

A Technology Sweetspot for Sensor and Actuators

Existing
Low Leakage 180nm CMOS+NVM

40V UHV Devices

Body Control Module/Gateway MCUs

Integration, Low Power, Security & Safety

Unprecedented Integration

Single-chip solution offering multicore architecture and advanced networking protocols for next generation communication requirements while reducing the quantity of body control/gateway ECUs

Low Power Management

New low-power modes, analog comparators, and pretended networking support help meet stringent next generation power budgets and ensure greener vehicles

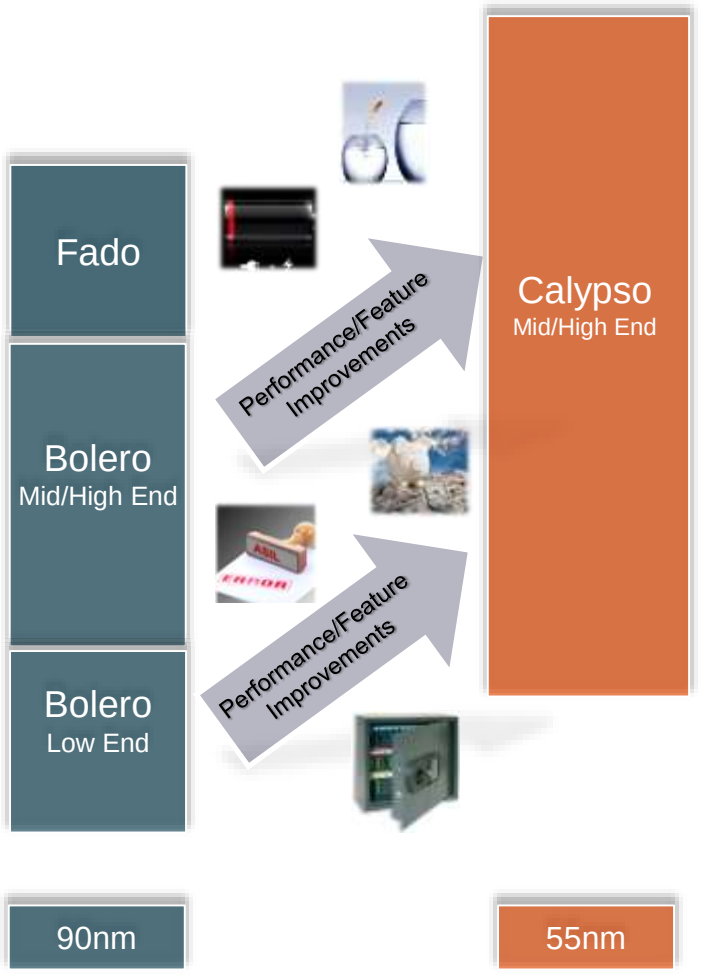
Functional Safety and Security

Security modules protect ECUs against various attack scenarios and Safety modules ensure robust operation per ISO 26262

32-bit Gen High End Body MCU Roadmap

FSL Calypso family of MCUs offers:

- **Advanced Communication Peripherals** – Ethernet AVB support, USB, SDHC, FlexRay, MOST, higher quantity of LINs, CANs, CAN FD support, etc
- **Improved Performance** - multi-core MCUs options, increased MHz
- **Large Flash and RAM** to support increased message handling/code requirements
- **New Low Power Unit** with improved functionality in low power modes
- Support of **Functional Safety** – **ISO26262 process**, targeting **ASIL-B**
- Enhanced **Hardware Security Module**
- **Family Concept** – Scalable HW and SW approach within Calypso family and migration path from the widely used Bolero family
- **Availability** – 55nm products in design, Bolero 90nm can be used for early development today.



Highly Integrated Body Control/Gateway MCU

- **Performance through Multicore**
  - Up to three e200 cores built on Power Architecture technology, with up to 160 MHz performance allows for easy division of tasks in an integrated BCM/gateway system
- **Most Diverse Set of Networking Communication**
  - Ethernet with AVB support, FlexRay™, MLB, USB, up to eight CAN with CAN Flexible Data Rate (FD) up to 18 LIN, SDIO interface, I^2S all supported on a single-chip solution
- **Flexible Memory Options**
  - Up to 6 MB Flash and 768 KB of embedded SRAM provide suitable storage to maintain the local BCM/gateway application functionality, handle message buffering, and also store additional Flash images for other nodes in the vehicle

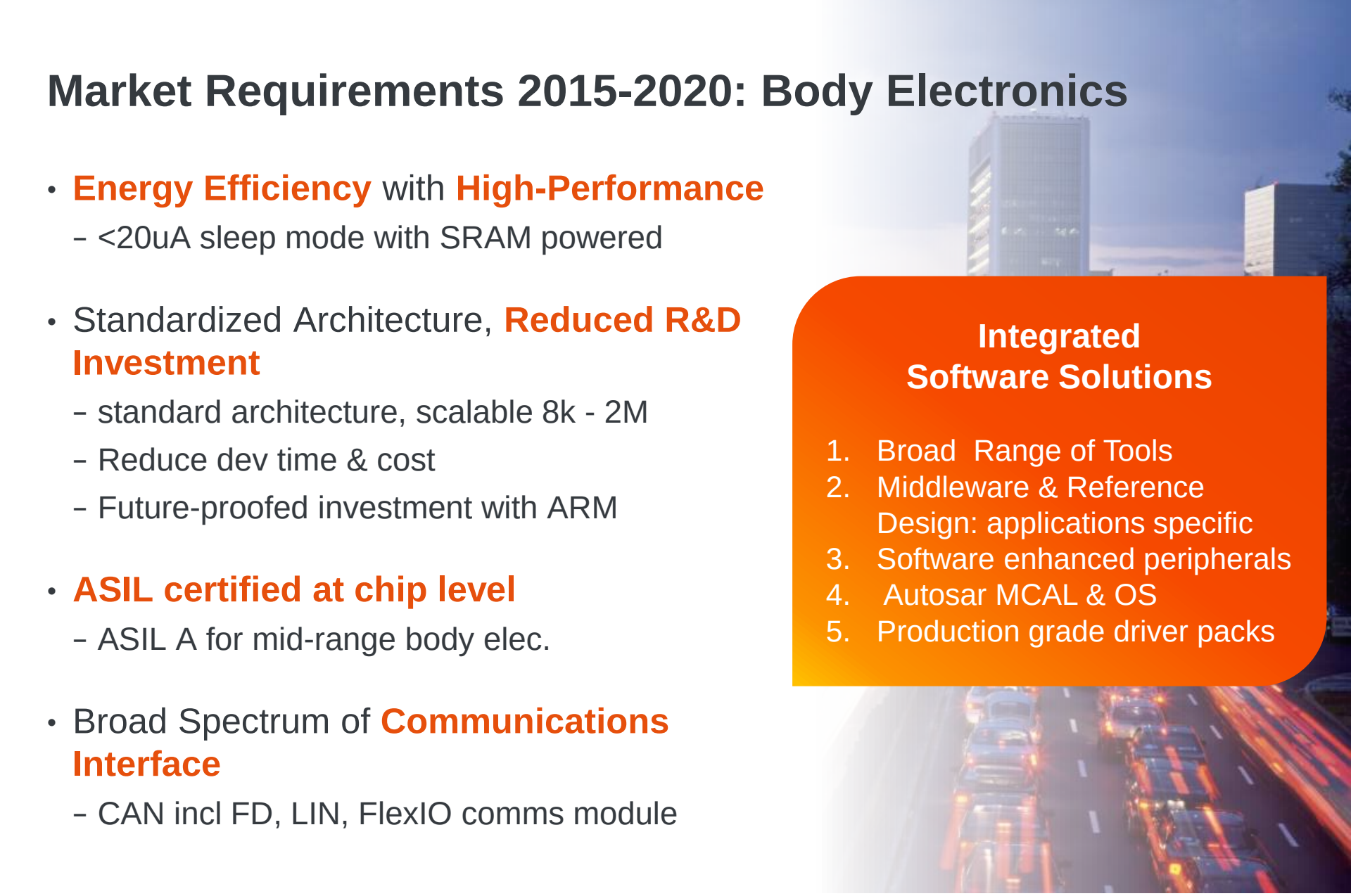
Addressing Functional Safety and Security

- **Designed with the ISO26262 process in mind**
- **Safe Assure functional safety program:**
  - **Safety Process** - integrating functional safety into dev process
  - **Safety Hardware** – built in self tests, error code correction, etc
  - **Safety Software** – Autosar MCAL, OS, core self tests, etc
  - **Safety Support** – training, documentation and tech support

- **Designed to support next generation security needs**: Security gatekeeper, immobilizers, component protection, protection of data sets
- **Hardware Security Module (HSM)**
  - Meets **SHE and EVITA** medium spec requirements
  - **Dedicated**, programmable **security core**
  - **Secure Flash** and **SRAM**
  - **Cryptographic module** – AES-128, random number generator etc.
  - Helps protects security keys, secure boot up, tamper detection, advanced debug support, etc

Market Requirements 2015-2020: Body Electronics

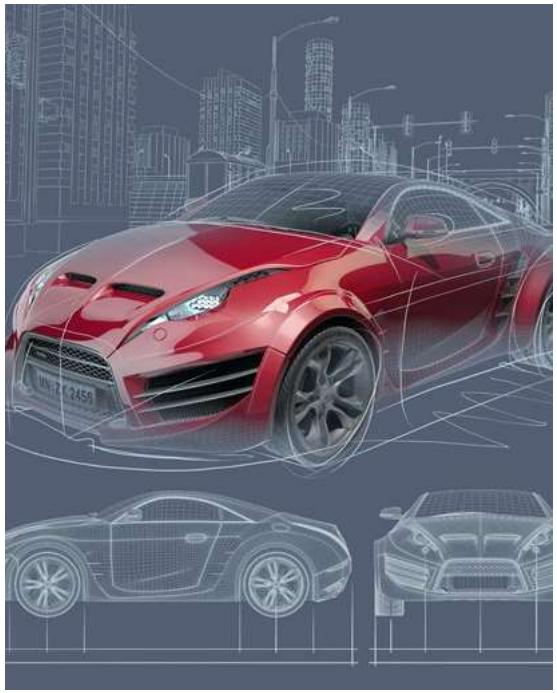
- **Energy Efficiency** with **High-Performance**
  - <20uA sleep mode with SRAM powered
- Standardized Architecture, **Reduced R&D Investment**
  - standard architecture, scalable 8k - 2M
  - Reduce dev time & cost
  - Future-proofed investment with ARM
- **ASIL certified at chip level**
  - ASIL A for mid-range body elec.
- Broad Spectrum of **Communications Interface**
  - CAN incl FD, LIN, FlexIO comms module



Integrated Software Solutions

1. Broad Range of Tools
2. Middleware & Reference Design: applications specific
3. Software enhanced peripherals
4. Autosar MCAL & OS
5. Production grade driver packs

32-Bit Automotive ARM Cortex MCU Family



Highlights

- Zero-defect automotive quality levels
- ARM-Cortex® M4 & M0+ high performance & low power
- 8 K to 2 M embedded flash, pin to pin compatible
- FlexCAN with CAN FD option
- Flex-IO for configurable number of LIN, SPI, I2C
- ASIL-A design flow
- Ta = -40˚C to 125˚C

Software driver package integrated

- Configured with:
  - Production Grade Driver Package, or
  - AutoSar MCAL and OS
- Samples 1H 2015

Powertrain and Chassis

Powertrain Introduction - “Where we play”

freescale™

Powertrain MCU Leadership

➢ **8-cyl Engine Mgmt**

HEV / EV Mgmt

6-cyl Engine Mgmt

Transmission Mgmt

<= 4-cyl Engine Mgmt

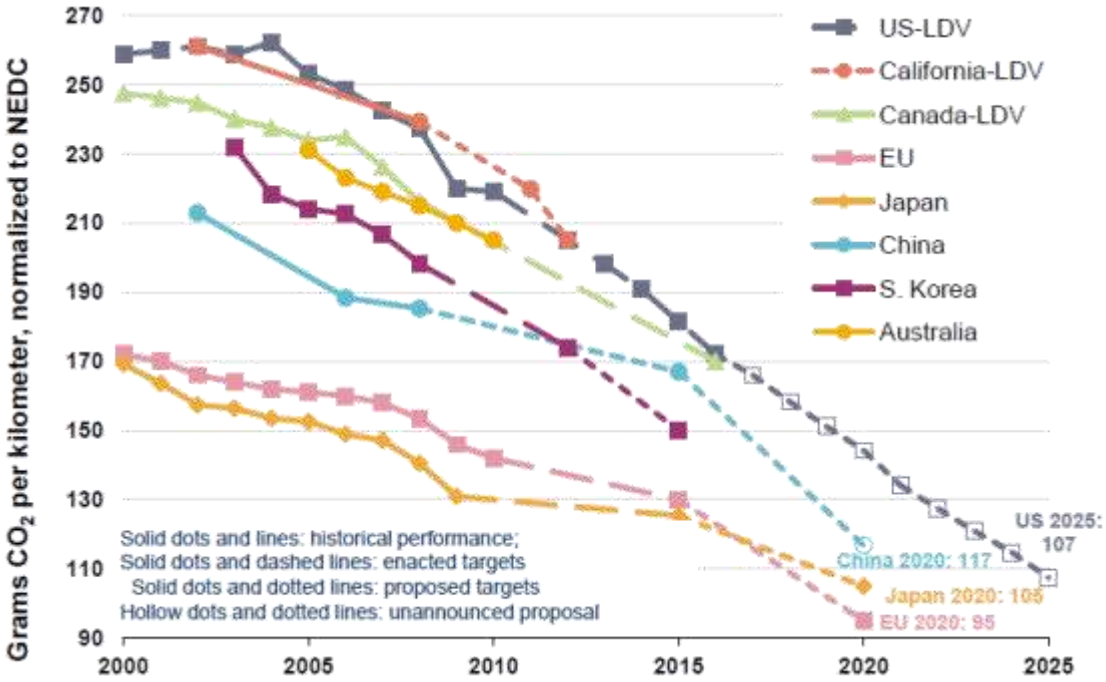
Built on

Qorivva + SAFE ASSURE™ by Freescale

Technology

Innovating for
Cleaner Technologies and Standards

Driving from regulations



- **Advanced Electronic Control Providing**:
  - Revolutionary **fuel injection, turbo charging** and **electronic valve control** reducing fuel consumption and improving emission control.
  - Low-cost micro/mini **hybrid technology** enhancing in-city fuel consumption.
  - New **multispeed dual clutch transmissions with** improved efficiency.

Source: The International Council on Clean Transportation www.theicct.org

Powertrain and Chassis Requirements

- CPU performance increase
- More complex strategies -> bigger memories (RAM, Flash)
- Functional safety (ISO 26262A)
- Protection of the ECUs -> Flash reprogramming detection and protection

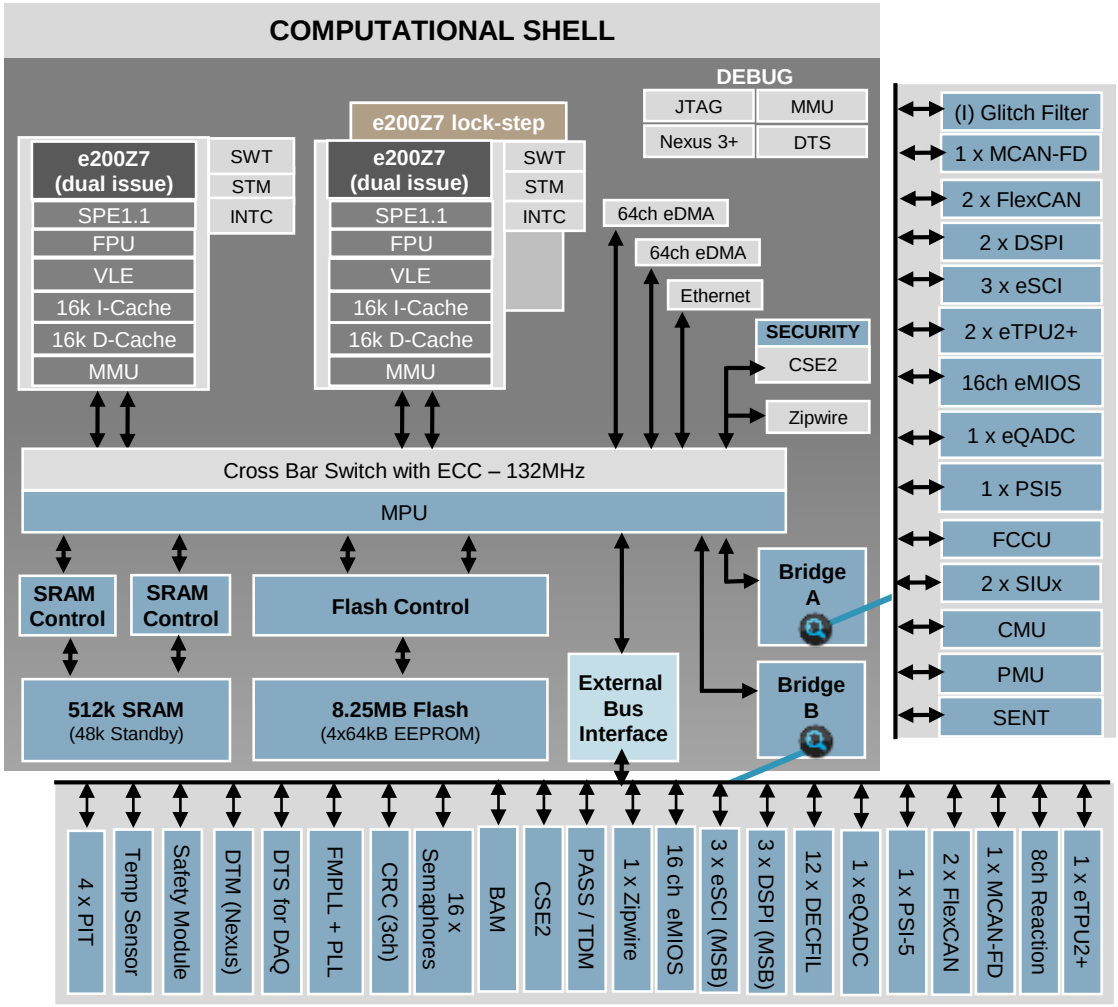
MPC5777C Cobra55 8M Block Diagram

Cores & Memory

- Two independent z7 dual issue computational cores @ 264 MHz
  - Cores include VLE, SPE1.1, FPU , MMU
  - 16 kB i-cache & 16kB data-cache w/ coherency
- Single z7 lockstep core @ 264MHz (for ISO26262 and ASIL-D)
- Up to 8.25 MB Flash RWW w/ ECC including 4 x 64 kB EEPROM
- Up to 589 kB total SRAM
  - 512 kB on chip static RAM w/ECC (up to 48 KB standby)
  - 45 kB eTPU RAM , 32kB data cache (w/line locking)
- Security
  - PASS and TDM (Tamper Detection)
  - CSE2 (Crypto Services Engine for Encryption & Secure Boot)

I/O & System

- Up to 70ch eQADC from 4 converters w/12bit resolution
  - On-chip temperature sensor and VGA (x1,x2,x4)
  - 12 x Decimation Filters w/ hardware knock integrators
- Timers – up to 128 channels (96ch eTPU2+ and 32ch eMIOS)
- 2 x 64ch eDMA support (128ch total)
- 6 x CAN ports (4 x FlexCAN + 2 x MCAN with Flexible Datarate)
- Ethernet
- DSPI – 5 *channels (2 supporting µSec ch.)*
- eSCI – *6 channels (2 supporting uSec ch.)*
- Reaction module – 8 channels for current control
- Up to 12ch SENT, Zipwire, 2ch PSI-5
- 1 x CRC unit – w/ 3 independent channels,
- 4 x protected port outputs, MPU and MMU
- FMPLL + PLL
- Safety Monitors – e2eECC, CLK, Voltage, Fault Collection



Reflects Standard Device

Packaging & Enablement

- 416 PBGA, 516 PBGA
- Calibration – VertiCal (using 552CSP)

MPC5777M Matterhorn 8M Block Diagram

Key Functional Characteristics

- Two independent 300 MHz Power Architecture z7 computational cores
  - Single 300 MHz Power Architecture z7 core in delayed lockstep for ASIL-D safety
- Single I/O 200 MHz Power Architecture z4 core
- eDMA controller – *128 channels*
- 8 M Flash with ECC
- 596k total SRAM with ECC
  - 404k of system RAM (incls. 64k standby)
  - 192k of tightly coupled data RAM
- 10 ΣΔ & 12 SAR converters – *84 channels*
- Ethernet (MII/RMII)
- DSPI – *8 channels (3 supporting µSec ch.)*
- LINFlex - *6 channels (3 supporting µSec ch.)*
- MCAN-FD/TTCAN – *4x modules/1x module*
- GTM – *248 timer channels*

Key Electrical Characteristics

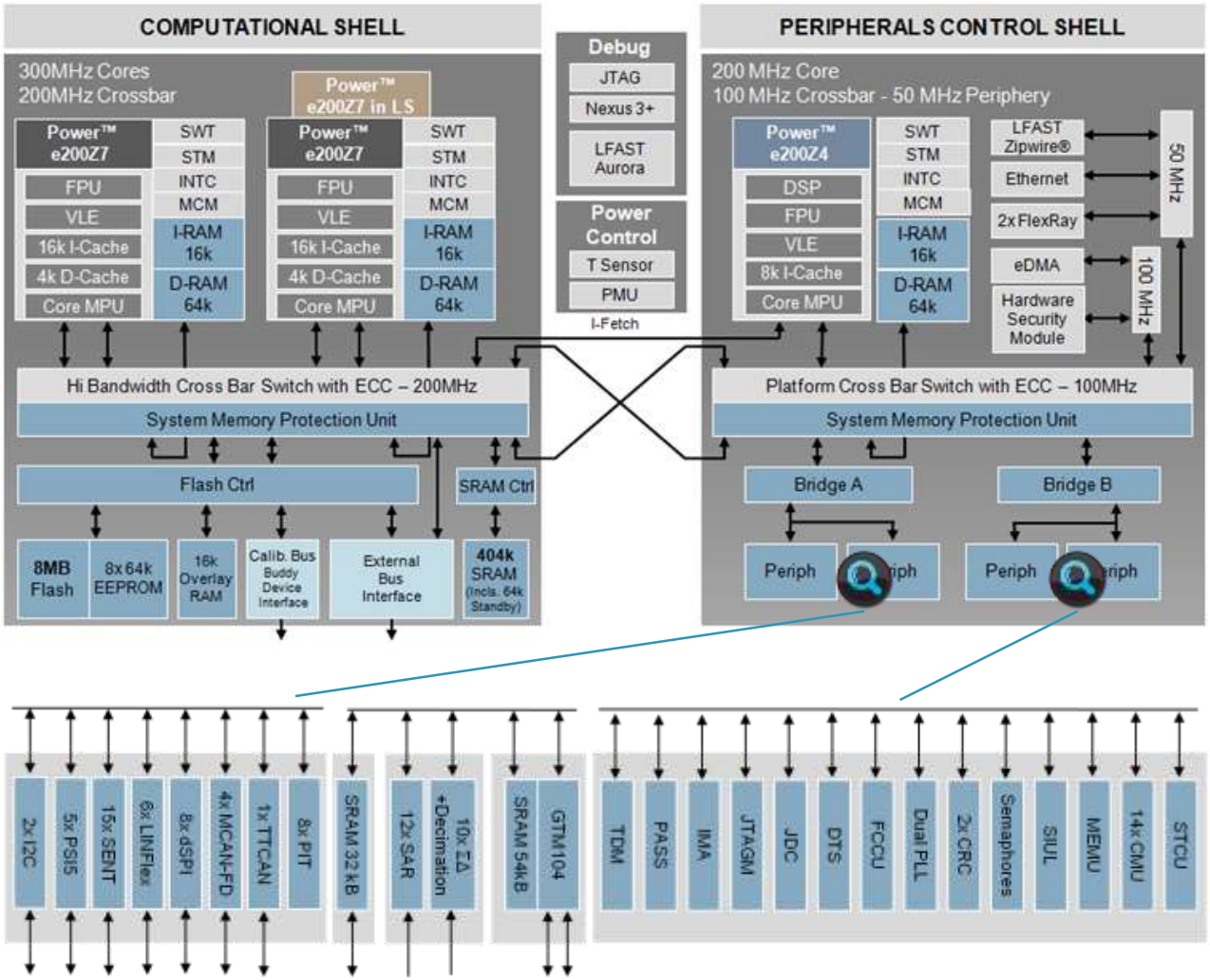
- -40 to +125 °C (ambient)
- 165 °C junction for KGD
- 1.26 V Vdd, 5.0 V I/O, 5 V ADC

Package

- 292 PBGA, 416 PBGA, 512 PBGA
- eCal emulation device for each package

Enablement

- Software: AutoSAR drivers
- Tools
  - Debugger: Green Hills, Lauterbach and PLS
  - Multicore compiler: HighTec, GCC, Wind River & Green Hills
  - Simulation tools



MPC5746R Rainier 4M Block Diagram

Key Functional Characteristics

- Two independent 200 MHz Power Architecture z4 computational cores
  - Single 200 MHz Power Architecture z4 in lockstep
- eDMA – *64 channels (w/ lockstep DMA)*
- 4M Flash with ECC
- 320 k total SRAM with ECC
  - 256k of system RAM (incls. 32k of standby RAM)
  - 64k of tightly coupled data RAM
- 3 ΣΔ ADC converters – *12 channels*
- 4 SAR converters – *52 channels*
- Cross Triggering Unit
- Ethernet (MII-lite/RMII)
- DSPI – *7 channels (2 supporting µSec channel)*
- LINFlex - *6 channels (2 supporting µSec channel)*
- FlexCAN – *4 chls, 2 w/* ***flexible data rate*** *capability*
- SENT – *6 channels*
- 2 eTPU2+ timers – *64 channels*
- 1 eMIOS – *32 channels*
- Reaction module – *10 channels*

Key Electrical Characteristics

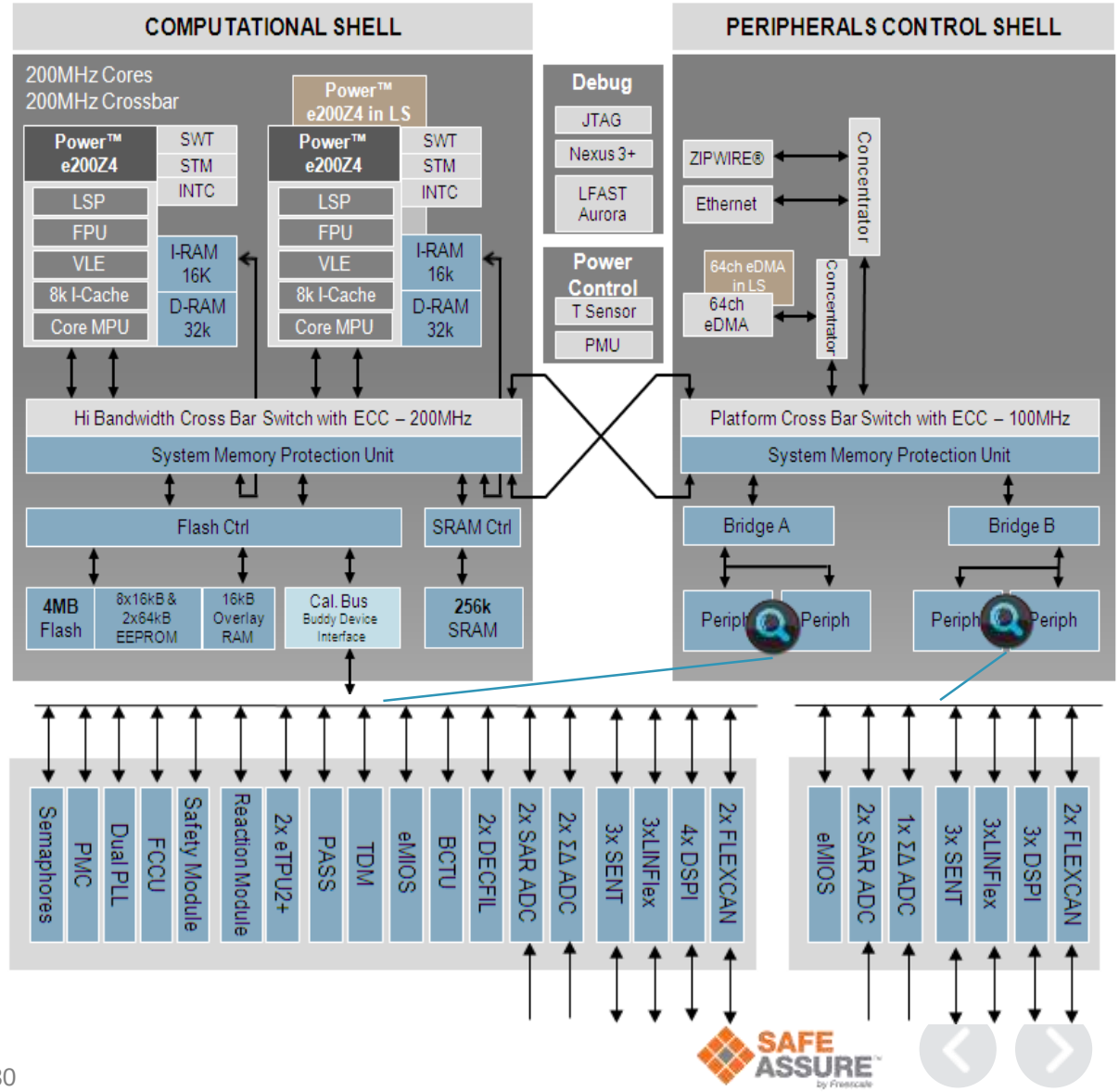
- -40 to +125 ° C (ambient)
- Single 5 V power supply

Package

- 176 LQFP, 252 MAPBGA
- 292 MAPBGA eCal package (incls. RAM buddy chip) for emulation/debug

Enablement

- Software : AutoSAR drivers
- Tools : Debugger (Lauterbach), multicore compiler (Wind River and Green Hills)



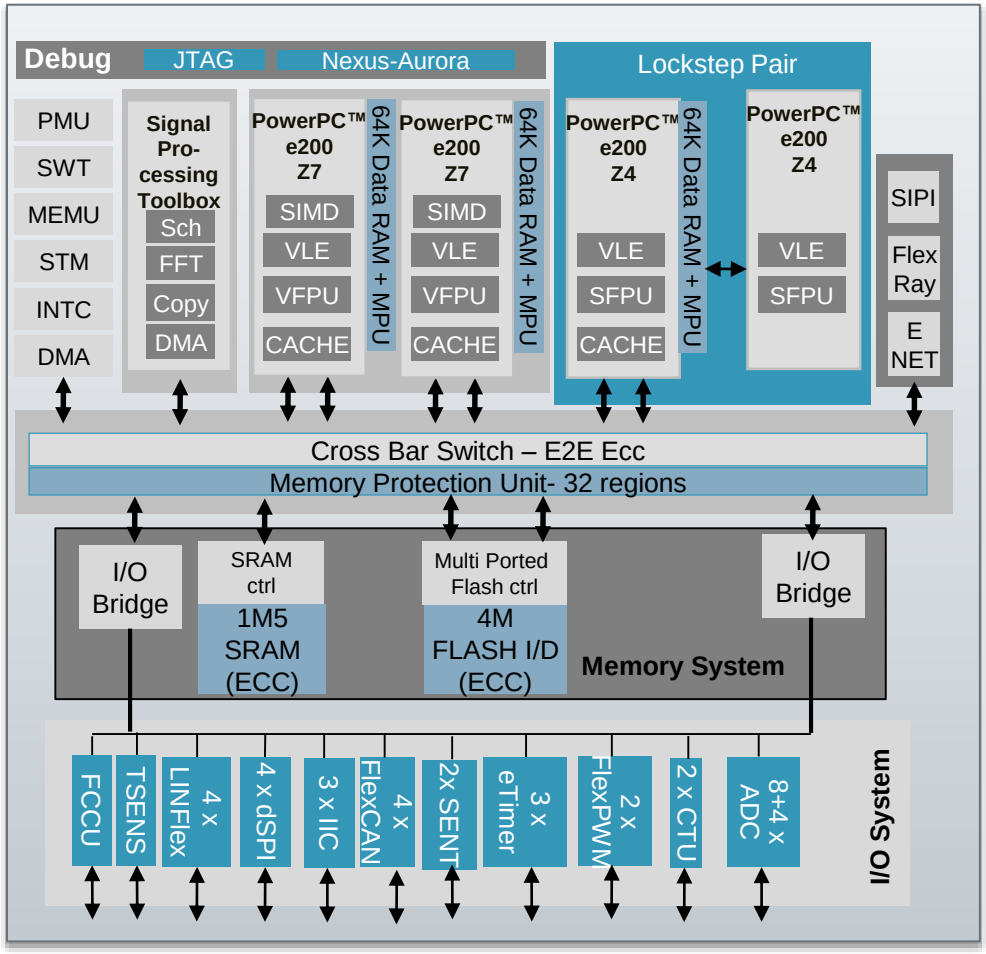
Racerunner

Core
- 260 MHz Power ISA Dual Issue core multi core system
  - Two z4 Cores in permanent delayed Lockstep for high safety integrity level
  - Two z7 cores for application execution
  - I-cache – 16 KB (2 ways) / D-Cache 16 KB (2 ways)
  - Core Local D-memory (64kB at each core) with local MPU
- Vector Floating Point Unit & SIMD (z7)
- 64 bit BIU with E2E ECC
- Signal Processing Toolbox (SPT) FFT accelerator

Memory
- Up to 4 MBytes byte Flash with EE Emulation and ECC
- Up to 1.5 MBytes SRAM with ECC
- Safe Crossbar (E2E ECC) with system MPU

I/O
- 4 x FlexCAN (64 message buffers)
- 1 x FlexRay (Dual Channel 128 msg. buffers)
- 1 x Ethernet Controller (ENET)
- 4 x LINFlex (SCI) & 3x IIC
- 4 x dSPI (4cs std / 8cs in larger v package version only)
- 3 x eTimer
- 2 x FlexPWM (2x 12 channel) & 2x CTU
- Octal A/D (10 M samples/sec) ΣΔ Radar I/F – 5MHz BW + 4x SAR
- 2 x SENT

System
- Highly stable Oscillator for Radar ASIC to A/D synchronization
- SIPI (~300MBaud) for interprocessor or µc to ASIC communication
- Safe DMA Engines
- Autonomous Fault Collection and Control Unit
- CRC computing unit
- Junction temperature sensor
- Nexus Class 3+ debug interface (Aurora extension)
- Low jitter PLL for RADAR
- 3.3 V Single supply (SMPS and/or external supplied)
- 3.3 V I/Os (SAR A/D 5V capable only!)
- 257 (0.8mm pitch) and 473 (0.8mm pitch) BGA , 176LQFP, T_J = 150



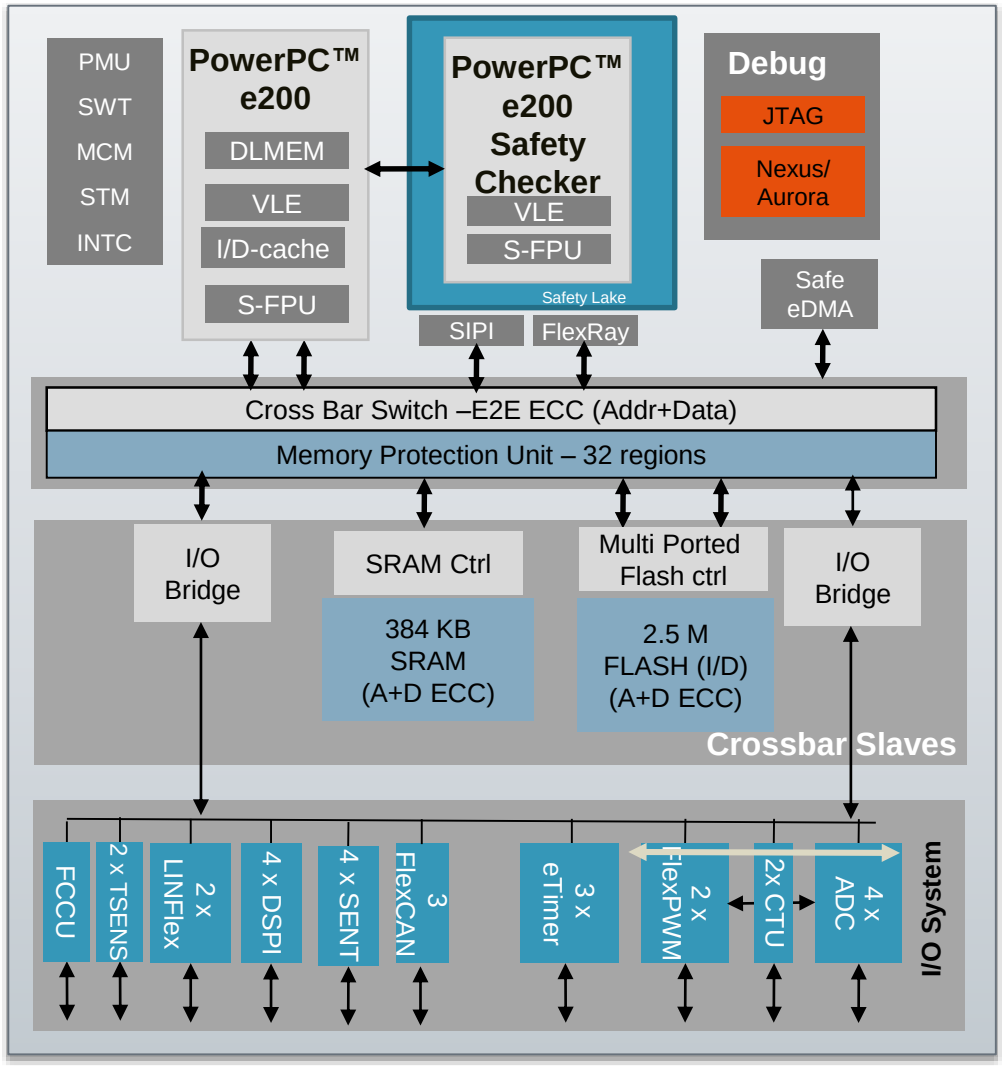
Panther 2.5 MB

Core
- Dual up to 200 MHz Power™ ISA e200 zen4 core (Z420)
- 32 bit Reg File, 64 bit BIU with E2E ECC,
- 64kB RAM of D-LMEM with MPU for fast context switch + local data
- 8KB 2-way I-cache / 4 KB 2-way D-Cache
- 1x Scalar FPU (compiler supported) per core
- Safety enhanced Cores – VLE only
- No signal processing unit (SPE) extension + no MMU
- Delayed Lock Step configuration only

Memory
- 2.5 MBytes NVM with ECC (with add. Safety measure for address).
- 64kB EEE (Data Flash) available incl. ECC
- Up to 384 Kbyte global system SRAM with ECC (Addr + Data)

I/O
- 3 x FlexCAN (64+2x32 message buffers)
- 1 x FlexRay (Dual Channel 64 msg. buffers)
- 2 x LINFlex (Uart/Lin protocol driver)
- 4 x DSPI (4 cs each)
- 2x FlexPWM (2x 12ch for 2 independent motors)
- 3 x eTimer modules (18 channel total)
- 4 x SAR ADC – 1MS/s target 5V input capable
- 2 x Cross-triggering unit for motor control automatism
- 4x SENT

System
- Interprocessor I/F SIPI (– approx 300Mbaud)
- Safe DMA
- Fault Collection unit, WDG, T-sens, & CRC computing unit
- Nexus debug interface – Aurora
- Dual-PLL (Peripheral + System Core)
- 3.3 V Single supply: internal regulator with external power stage or External supply
- 3.3 V I/Os (ADC 5 V capable)
- 144 LQFP-176 LQFP-EP / 257 MAPBGA 0.8 mm pitch
- Tj = 150°C . Extended Temperature at 165°C Option (separate P/N)



Functional Safety

Functional Safety. Simplified.

Simplifies the process of system compliance, with solutions designed to address the requirements of automotive and industrial functional safety standards

Reduces the time and complexity required to develop safety systems that comply with ISO 26262 and IEC 61508 standards

Supports the most stringent Safety Integrity Levels (SILs), enabling designers to build with confidence

Zero defect methodology from design to manufacturing to ensure our products meet the stringent demands of safety applications

The Four Pillars

Safety process

- Integrating functional safety into product development process
- Select products defined and designed from the ground up to comply with the standards

Safety hardware

- Built-in safety functions (self-testing, monitoring and hardware-based redundancy) in Freescale microcontrollers (MCUs), power management ICs and sensors
- Additional system-level safety functionality from Freescale analog solutions (checking MCU timing, voltages and error management)

Safety software

- A comprehensive set of automotive functional safety software, including AUTOSAR OS and associated microcontroller abstraction layer (MCAL) drivers, as well as core self-test capabilities
- Partnerships with leading third-party software providers for additional safety software solutions

Safety support

- From customer-specific training and system design reviews to extensive safety documentation and technical support

ISO26262 – Introduction to the Basics

- ISO 26262 is the new *functional safety standard* for series production passenger cars
- It is applicable to electric / electronic systems where malfunctioning behavior of such systems can cause harm
- The standard focuses on systems (“items”) consisting of sensors, microprocessors and actuators
- Four Automotive Safety Integrity Levels (ASIL A to D) determined through hazard analysis and risk assessment at vehicle level
- The ASILs imply a specific set of requirements and safety measures to be applied for avoiding an unreasonable residual risk
- Smart microprocessor solutions & collateral can significantly reduce the effort required to build functional safe systems complying with ISO26262

The SafeAssure Experience - *Simplicity*

- Functional safety is complex

- SafeAssure products are conceived to **simplify system-level** functional safety **design** and cut down time to **compliance**

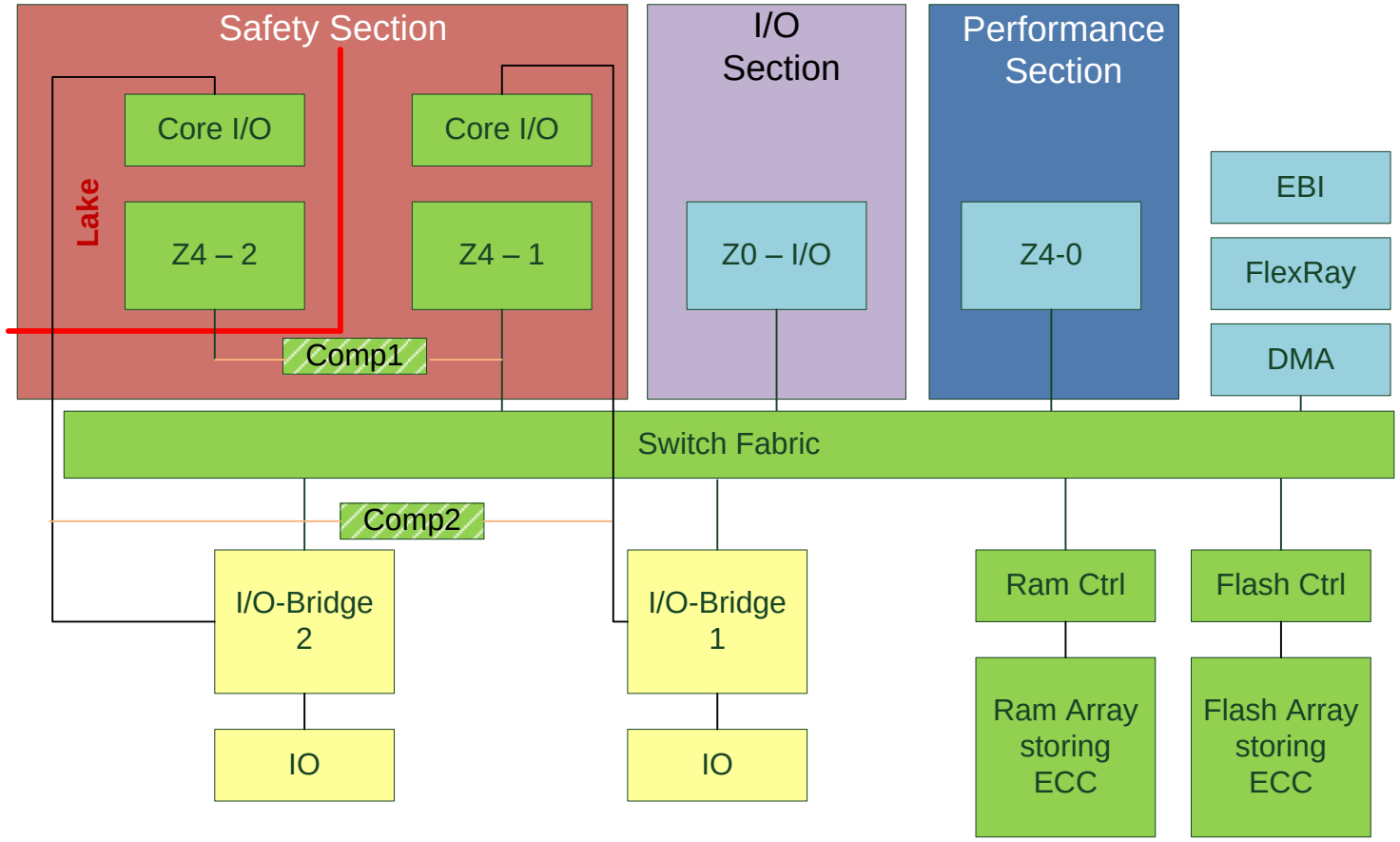
- Key functional safety activities addressed
  - Failure analysis
  - Hardware integration
  - Software integration
  - Support Interface

Safety Concept Summary for 55 nm

- Measures against single point faults
  - Replication only of Cores & attached periphery
  - End-2-End protection of data paths (ECC)
  - ECC on all RAMs (System, periphery, Cache, TCM) & Flash
- Measures against latent errors (during boot)
  - Memory BIST
  - LBIST
  - Limited BIST of analog components

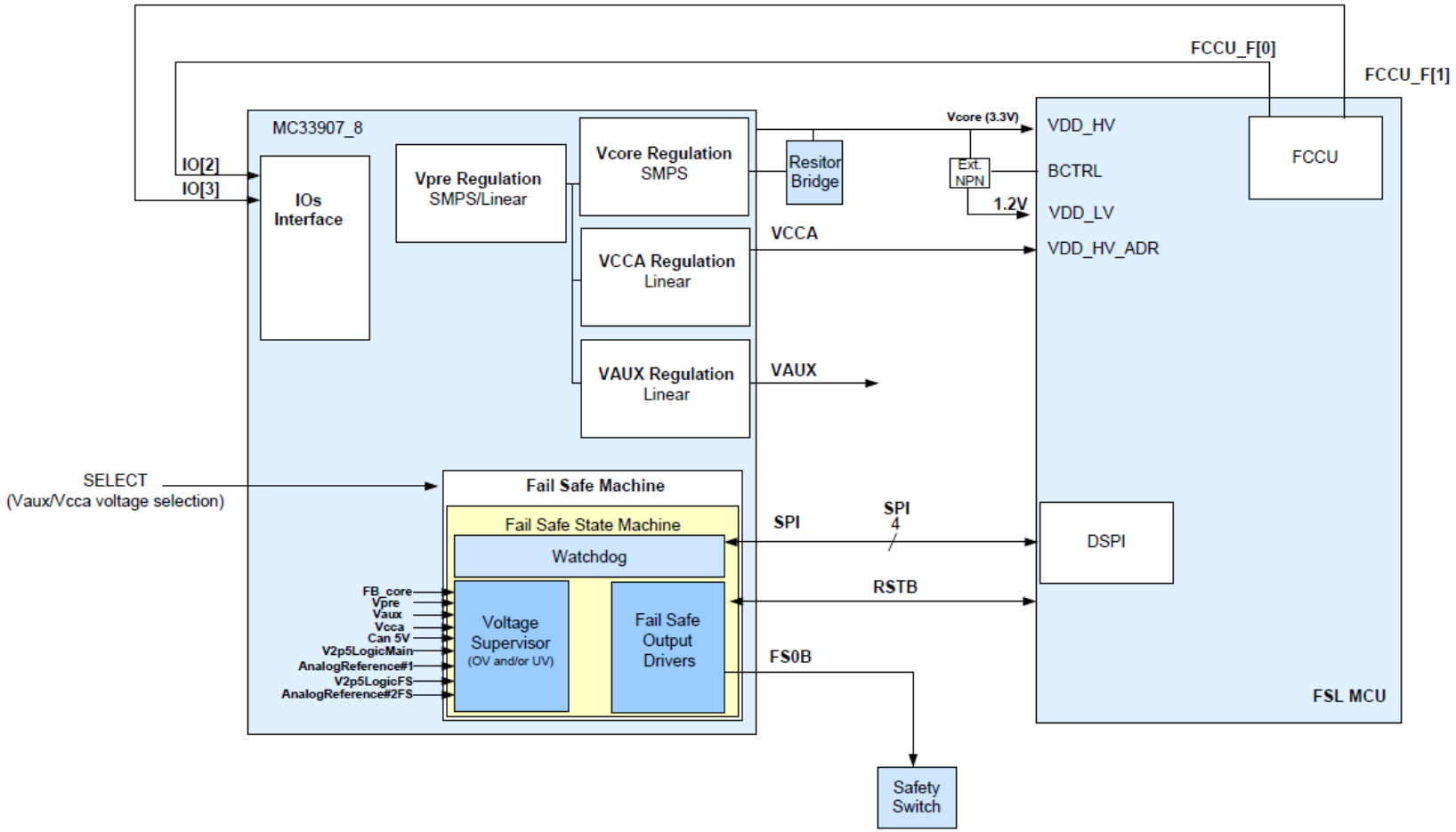
  } < 50ms
- Measures against Common Cause errors
  - Clock & Power Monitors, Monitors of signal lines (debug, test, …)
  - HW-evaluated Temperature Sensors
- Some errors not handled
  - External hardware supervision (Watchdog, Supply Voltage)
  - Redundant usage of I/O by software

General Architecture



- Green: Protected by HW
- Red: Protected by redundant/diverse use by SW
  - (HW replication but not checkers)
- Blue: Other measures necessary/not safety relevant

Functional Safety Interaction Bletween a MCU and a PowerSBC



Summary

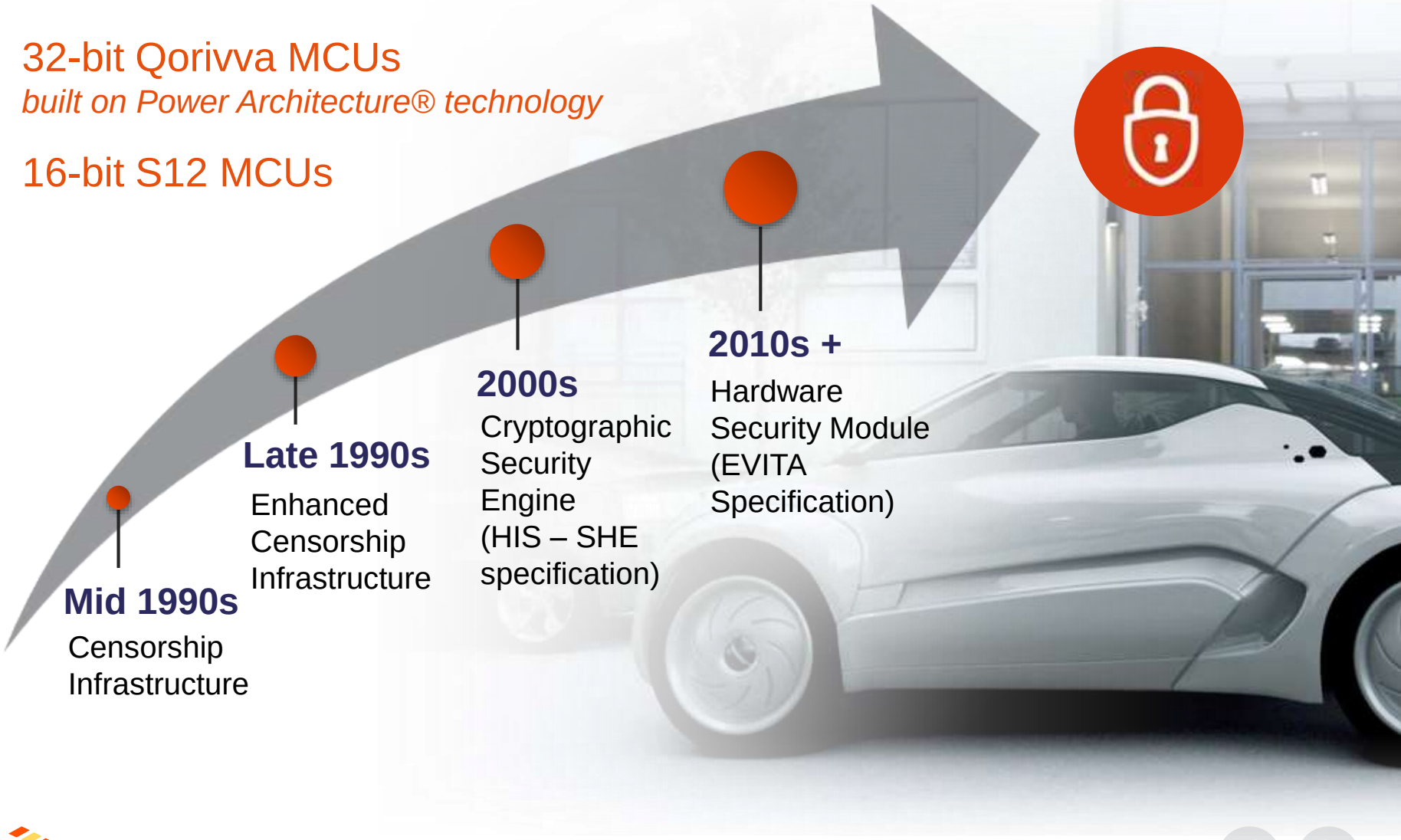
- The automotive and industrial industries are increasingly requiring functional safety solutions.
- Freescale is implementing a **systematic approach** to functional safety that reduces complexity for manufacturers of functional safety systems.
- Freescale's new **SafeAssure** program is built on four strong pillars: *safety process*, *safety hardware*, *safety software* and *safety support*.
- The ultimate goal of the program is to **simplify system compliance** with functional safety standards and, at the end of the day, **keep people safe**.

Security

A Proven History in Driving Automotive Security

32-bit Qorivva MCUs
built on Power Architecture® technology

16-bit S12 MCUs



Mid 1990s
Censorship Infrastructure

Late 1990s
Enhanced Censorship Infrastructure

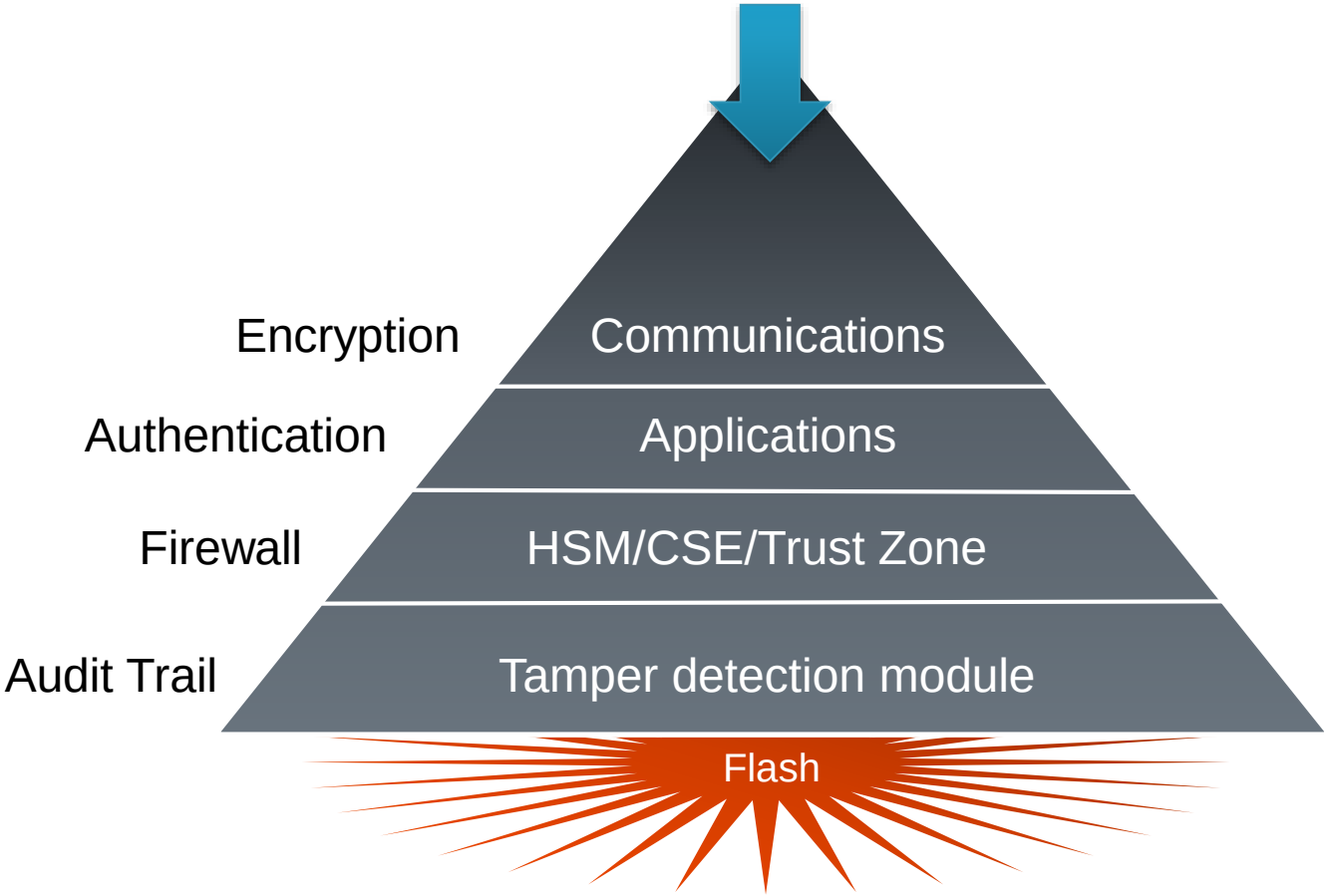
2000s
Cryptographic Security Engine (HIS – SHE specification)

2010s +
Hardware Security Module (EVITA Specification)

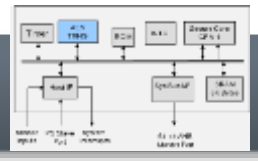
Freescale Security Architecture

Multi-layered approach strengthens overall vehicle security

Protects against HW and SW theft, tuning, parts cloning, mileage manipulation and personal data theft



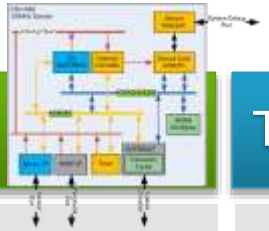
Freescale Qorivva Advantage: Hardware-Enabled Security Options



CSE

Cryptographic Security Engine

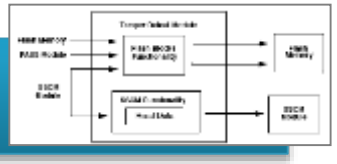
- Turn-key solution that implements SHE specification
- Improves the reliability, maintenance and safety of vehicle
  - Protection against software and hardware theft, tuning, parts cloning, mileage manipulation, personal data theft
  - Allows feature activation to support vehicle upgrades
  - Remote ECU reprogramming
- Enhanced for global OEM security needs



HSM

Hardware Security Module

- User programmable and compliant with EVITA specification
- Secure debug interface protects against malicious attacks on the user program code
- Supports CSE functional requirements
- Additional protection offered through the sensor interface
  - Voltage monitor
  - Temperature monitor
  - Clock monitor



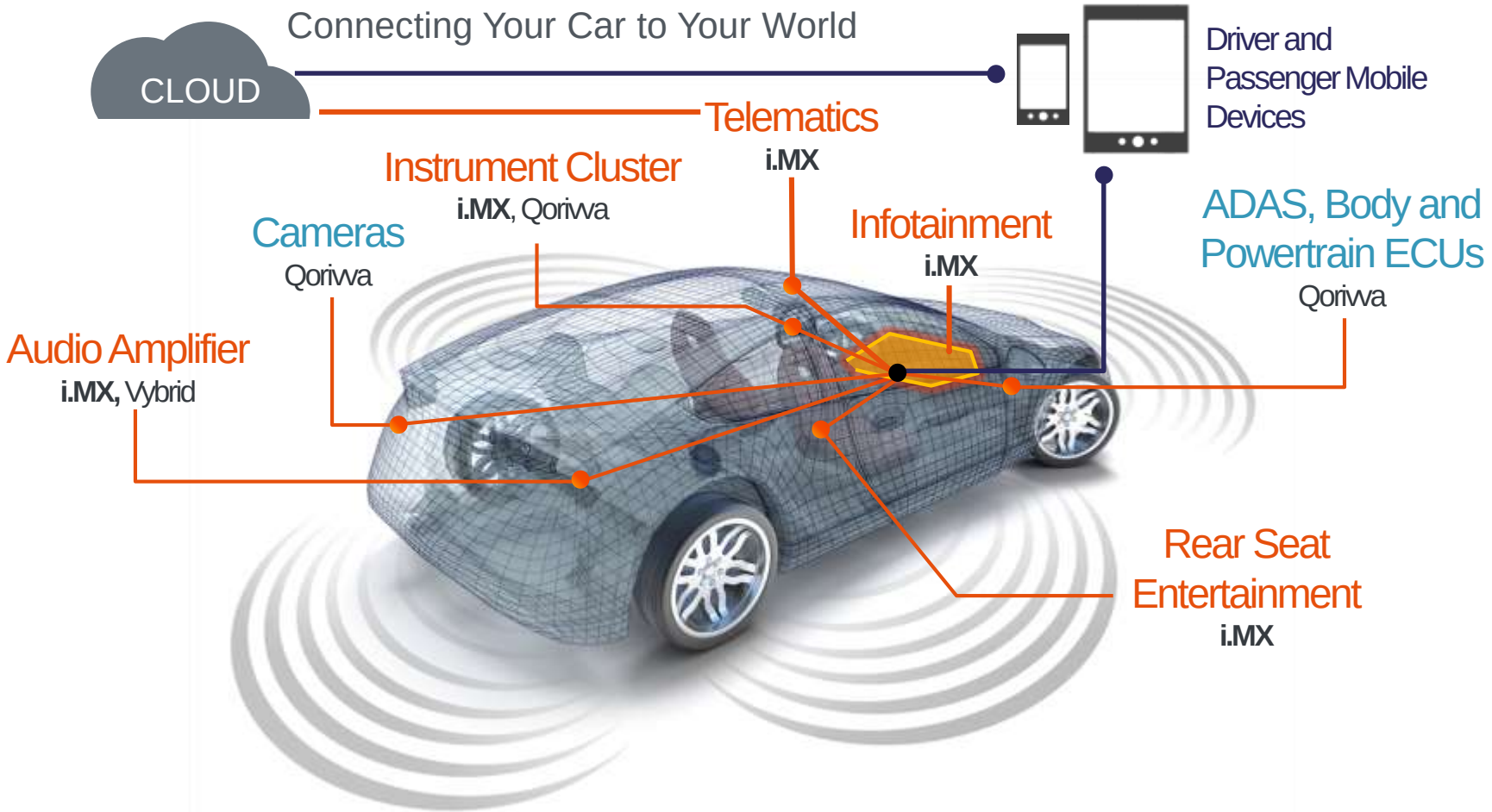
TDM

Tamper Detection Module

- Records all attempts to modify flash memory
- Detects unauthorized re-programming of application code
- Protects manufacturers' investment
- Protected by Patent US8380918 B2, granted Feb 19, 2013

Automotive Infotainment and Instrument Cluster Applications

Automotive Internet of Things



Freescale Connected Vehicle Vision Powered by i.MX

Freescale's Product Longevity Program

- The automotive market requires **long-term product support**
- Freescale has a longstanding track record of **providing long-term production support** for our products
- Freescale is pleased to introduce a **formal product longevity program** for the market segments we serve
  - For the automotive and medical segments, Freescale will make a broad range of solutions available for a minimum of **15 years**
  - For all other market segments in which Freescale participates, Freescale will make a broad range of solutions available for a minimum of **10 years**
  - **Life cycles** begin at the time of launch
- A list of participating products is available at: www.freescale.com/productlongevity

i.MX Applications Processors Automotive Products

All i.MX applications processors automotive products

- Qualified to the AEC-Q100 Grade 3 specification
- PPAP's are available
- Automotive-specific datasheets are available
- Products promoted for automotive applications
  - i.MX25, i.MX28 (ARM926EJ-S CPU)
  - i.MX35 (ARM1136JF-S CPU)
  - i.MX53 (ARM Cortex-A8 CPU)
  - i.MX 6x (ARM Cortex-A9 CPUs)
- All automotive products are rated "Quality Managed" for ASIL level
  - i.MX Automotive products have been used in higher level ASIL solutions where the customer assumes the responsibility for the system level ASIL rating about Quality Managed

*More information see: http://www.aecouncil.com/AECDocuments.html

i.MX 6 Series: Supreme Scalability and Flexibility

Leverage One Design Into Diverse Product Portfolio

Scalable series of **SIX** ARM Cortex-A9-based SoC Families

i.MX	i.MX	i.MX	i.MX	i.MX	i.MX
6SoloLite Family	**6**SoloX Family	**6**Solo Family	**6**DualLite Family	**6**Dual Family	**6**Quad Family

Pin-to-pin Compatible

Software Compatible

Red indicates change from column to the left

i.MX 6 Series At a Glance

Scalable series of six ARM Cortex A9-based SoC families

i.MX 6SoloLite

- Single ARM® Cortex™- A9 at 1GHz
- 256KB L2 cache, Neon, VFPvd16, Trustzone
- 2D graphics
- 32-bit DDR3 and LPDDR2 at 400MHz
- 10/100 Ethernet
- EPD controller

i.MX 6SoloX

- Single Cortex™- A9 up to 1GHz
- **Single Cortex-M4 up to 200MHz**
- 256KB L2 cache, Neon, VFP, Trustzone
- **3D** and 2D Graphics
- 32-bit DDR3 and LPDDR2 at 400MHz
- **Dual Gigabit Ethernet**
- **PCIe (x1 lane)**

i.MX 6Solo

- Single ARM Cortex-A9 up to 1GHz
- **512KB** L2 cache, Neon, VFPvd16, Trustzone
- **3D graphics** with **1 shader**
- 2D graphics
- 32-bit DDR3 and LPDDR2 at 400MHz
- **1080p30 video**
- Gigabit Ethernet
- PCIe (x1 lane)
- **EPD controller**

i.MX 6DualLite

- **Dual** ARM Cortex-A9 up to 1GHz
- 512KB L2 cache, Neon, VFPvd16, Trustzone
- 3D graphics with 1 shader
- 2D graphics
- **64-bit** DDR3 and 2-channel 32-bit LPDDR2 at 400MHz
- 1080p30 video
- Gigabit Ethernet
- PCIe (x1 lane)
- EPD controller

i.MX 6Dual

- Dual ARM Cortex-A9 up to **1.2GHz**
- **1 MB** L2 cache, Neon, VFPvd16, Trustzone
- 3D graphics with **4 shaders**
- **Two** 2D GFX engines
- 64-bit DDR3 and 2-channel 32-bit LPDDR2 at **533MHz**
- **1080p60 video**
- PCIe (x1 lane)
- Gigabit Ethernet
- **SATA-II**

i.MX 6Quad

- **Quad** ARM Cortex-A9 up to 1.2GHz
- 1 MB L2 cache, Neon, VFPvd16, Trustzone
- 3D graphics with 4 shaders
- Two 2D GFX engines
- 64-bit DDR3 and 2-channel 32-bit LPDDR2 at 533MHz
- 1080p60 video
- PCIe (x1 lane)
- Gigabit Ethernet
- SATA-II

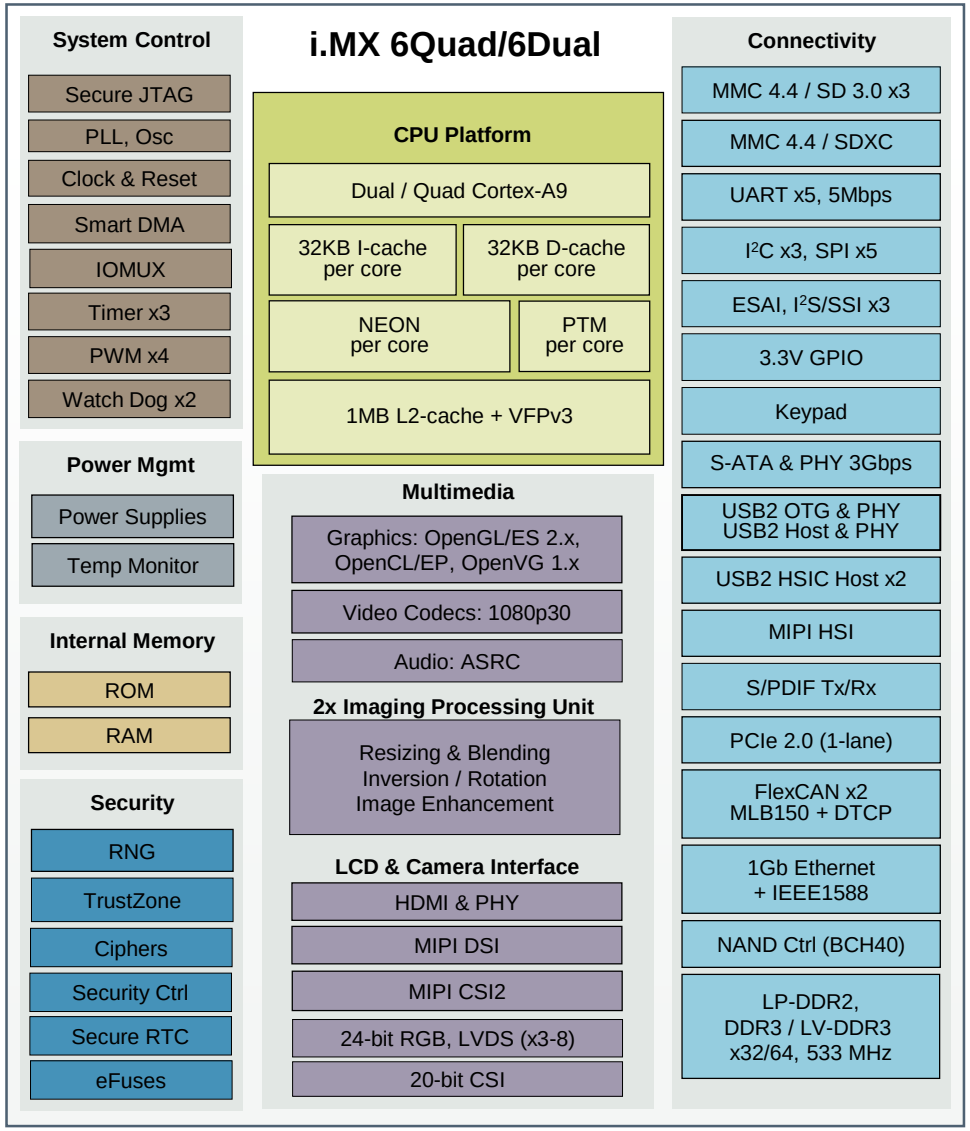
Pin-to-pin and Power Compatible

Software Compatible

- ARM Cortex-A9 based solutions ranging up to 1.2GHz
- HD 1080p encode and decode (except 6SoloLite/6SoloX), 3D video playback in high definition (except 6SoloLite/6SoloX)
- Integrated IO's may include HDMI v1.4, MIPI and LVDS, display ports, MIPI camera, Gigabit Ethernet, multiple USB 2.0, SATA and PCI-Express
- SW support: Google Android™, Linux®, QNX (3rd party), Windows® Embedded CE (3rd party)

i.MX 6Quad/6Dual Applications Processor

- **Specifications:**
  - **CPU:** i.MX6Quad**:** 4x Cortex-A9 @ 850 MHz/1GHz/1.2 GHz
    i.MX6Dual: 2x Cortex-A9 @ 850 MHz/1GHz/1.2 GHz
  - **Process:** 40nm
  - **Package:** 21x21 0.8mm Flip-chip BGA
  - **Temp Range (Tj):** Up to -40 to 125C, AEC-Q100 Grade 3
  - **Qual Tiers:** Commercial, Automotive, Industrial
  - **Pin compatible with i.MX 6DualLite and i.MX 6Solo**
  - **Up to 10000 / 5000 DMIPS**
- **Key Features and Advantages**
  - Multi-core architecture for high performance, 1MB L2 cache
  - 64-bit LP-DDR2, DDR3 and raw / managed NAND
  - S-ATA 3Gbps interface (SSD / HDD)
  - Delivers rich graphics and UI in HW
    - OpenGL/ES 2.x 3D accelerator with OpenCL EP support and OpenVG 1.1 acceleration
    - Drives high resolution video in HW
    - Multi-format HD1080 video decode and encode
    - High quality video processing (resizing, de-interlacing, etc.)
  - Flexible display support
    - Four simultaneous: 2x Parallel, 2x LVDS, MIPI-DSI, or HDMI
    - Dual display up to WUXGA (1920x1200) and HD1080
  - MIPI-CSI2 and HSI
  - Increased analog integration for simplified power supplies
  - Temperature monitor for smart performance control
  - Expansion port support via PCIe 2.0
  - Car network: 2xCAN, MLB25/50/150 with DTCP, 1Gb Ethernet with IEEE1588 time stamping hardware
- **Availability**
  - **Samples:** Now
  - **Production:** Q4 2012



www.Freescale.com