



Freescale Recommendations for **Avionic** and **Defense** **Applications**

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Session Introduction

- Freescale processors have been widely utilized in Aerospace and Defense applications for many generations.
- This two hour session will describe the most commonly selected devices from:
 - i.MX applications processors
 - 32-bit Qorivva microcontrollers built on Power Architecture® technology
 - QorIQ communications platforms
- This presentation will provide examples of successful approaches used on Freescale products for improving robustness and safety and mitigating system failures in aeronautics and defense environments.
- The session will also summarize the design documentation and resources available to support the certification process.



Session Objectives

After completing this session you will be able to:

- Select processors from the Freescale portfolio targeting Aerospace and Defense applications.
- Identify key functions associated with safety.
- Locate essential documentation and collateral.
- Explain the advantages of Freescale devices to support safety.
- Describe the capabilities of the products that will help you meet your design challenges for Aerospace and Defense applications and how they can provide you a with a competitive and differentiating advantage.



Agenda

- Freescale experience in Aerospace and Defense applications
- Key factors
- Development Assurance Level (DAL), criticality & Freescale processors
- Freescale processors architectures
- Timing assessment & technical constraints
- QorIQ "System On Chip" evolution
- System control & configuration
- Memory protection
- Freescale processors - design for SEU robustness
- Freescale implementation advantages
- Certification & regulation considerations
- Summary of the documentation available for Freescale processors
- Export control
- Session summary
- Q&A

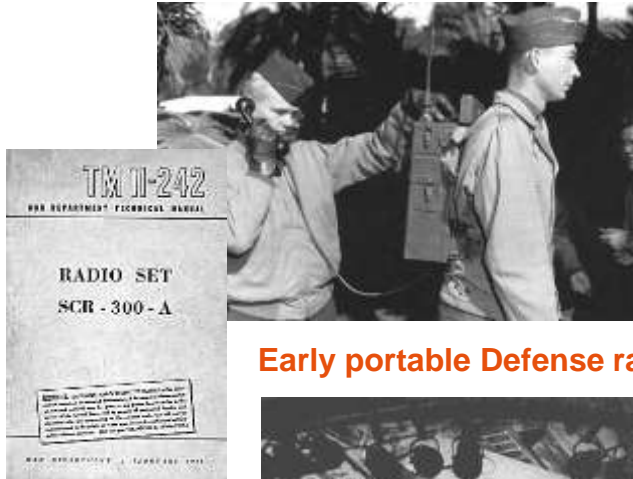


DRADA

Design Recommendations for Aerospace and Defense Applications



Freescale is part of Aerospace and Defense history



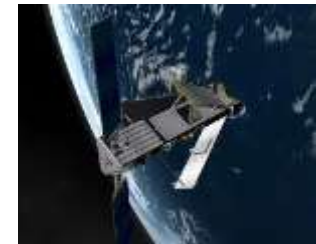
Early portable Defense radio



A Shuttle main engine in a ground test. The Controller can be seen mounted on the left side of the combustion chamber. (NASA photo 885338)
The revised computer uses a Motorola 68000 32-bit microprocessor
(credit : <http://history.nasa.gov/computers/Ch4-8.html>)



Supplier of space applications from ground to sky !



2012

BAE Systems licenses Freescale's technology

BAE Systems licenses Freescale's power architecture technology to develop processors for space missions

BAE Systems is developing fourth generation radiation hardened computers for space applications through a license announced today for Power Architecture® processor cores from Freescale.



Freescale experience in Aerospace and Defense applications



Tactical gear with i.MX



Avionic, flight computers and engine management systems with QorIQ and Qoriva



Since 1953, Motorola semiconductors, and now Freescale Semiconductor has supplied electronics products for Aerospace and Defense applications.

- #1 supplier of 32-bit processors to this industry
- We understand that “time-in-market” is as important as “time-to-market”
- Semiconductor solutions that:
 - Deliver performance
 - Meet embedded power budgets
 - Offer high levels of integration
 - Provide extended qualification
 - Deliver outstanding technical support

Freescale Portfolio Applied in Aeronautic and Defense Applications

The Processors

- Freescale delivers both system-on-a-chip (SoC) based on Power Architecture and ARM® cores.
- Specifically designed for telecom, portable devices, automotive and industrial markets.
- Suitable for the aerospace and defense market, with integrated features that make them suitable for robust applications.
- ECC & parity
- Safety & security blocks
- Manufactured in large volume, providing confidence for "in-service experience"

RF

- Freescale is #1 in RF Power
- Broad portfolio of LDMOS, GaAs and GaN transistors, addressing the complete RF line-up
- High ruggedness, efficiency and thermals
- Strong customer support with applications circuits, reference designs and characterization services

Sensors

- Freescale sensors are designed for automotive applications, human interface and portable terminal. They also fulfill industrial needs.

Analog solution for managing & switching power

- Serve as a companion to processors, addressing complex power-up sequence of multicore. Our solutions offer safety for power supply management



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Key Factors

Key factors for selecting Freescale products for Aerospace & Defense:

- **Quality**
- **Qualification**
 - Application / Qualification Tiers
 - Temperature Range
- **Longevity**
- **Architecture advantage**
 - Safety & Security functions
 - Memory protection
 - Support of Power and ARM cores
- **Documentation & Technical collateral**
- **Technical support**
- **Freescale's commitment to the Aerospace and Defense market**

<http://www.freescale.com/files/32bit/doc/brochure/PWRARBYNDBITSSKD.pdf>



Quality

At Freescale we are committed to being the finest semiconductor company in the world by providing the highest levels of product quality, delivery and service, as viewed through the eyes of our customers.

Freescale is passionate in our relentless pursuit of total customer loyalty by instilling a global high quality culture that results in manufacturing excellence and flawless new products.

- **Freescale Quality home page**
 - http://www.freescale.com/webapp/sps/site/homepage.jsp?code=QUALITY_HOME
- **Quality Policy handbook**
 - http://www.freescale.com/files/abstract/misc/CPA_QA_HANDBOOK.pdf
- **Quality Excellence as Seen Through the Eyes of the Customers**
 - http://www.freescale.com/webapp/sps/site/training_information.jsp?code=WBNR_FTF10_F0861
- **Building Robust Products: Freescale Product Package Mechanical Reliability Testing and Reporting**
 - http://www.freescale.com/webapp/sps/site/training_information.jsp?code=WBNR_FTF11_ENT_F0557



Packaging & Tracing

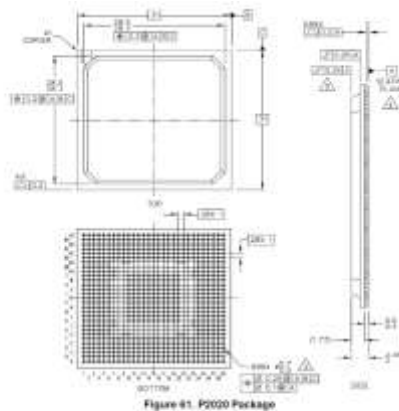


Notes:

ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Product package is marked for tracing

- **Key identification for:**
 - System architecture design
 - Development
 - Debugging
 - Analyzing an issue
 - Identifying silicon related errata
 - Making qualification for a final product



NOTES for Figure 61:
1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to Datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Flatness measurement excludes any effect of mask on top surface of package.

1. **Assembly and tractability**
2. **Country code**
3. **Date code & Mask number**
4. **Part number**

- Processors also offer internal register for content revision and version
- Packaging of products is compliant with JEDEC standards



Application/Qualification Tiers

*Tier	Typical Application Use-Time	Power-On Hours	Examples of Typical Applications
<blank>			No tier level currently defined (to be determined) or tier level not applicable for this product.
Commercial	5 years	Part-time/ Full-time	PCs, consumer electronics, portable telecom products, PDAs, etc.
Industrial	10 years	Part-time/ Full-time	Installed telecom equipment, work stations, servers, routers, etc. Can also be used in Commercial applications.
Automotive	10-20 years	Part-time/ Full-time	"under the hood", drive train control, safety equipment, etc. Can also be used in Commercial and Industrial applications.
* Please refer to product data sheets for operating temperature ranges, since they are independent of tier and will vary per product.			

- i.MX 6Solo/6DualLite Product Usage Lifetime Estimates
- http://www.freescale.com/files/32bit/doc/app_note/AN4725.pdf

Temperature Range #1

Document Number: P1010EC
Rev. 2, 03/2013

QorIQ processing platforms and i.MX application processors support extended temperature range.

P1010

The Freescale documentation refers to junction temperature and provides technical details related to the package that you select.



TePBGA1-425
19 mm x 19 mm

- Operating temperature ($T_a - T_j$) range: 0–105° C (standard) and –40° C to 105° C (extended)

QorIQ

Operating temperature ($T_a - T_j$) range:

0–105° C (standard)

P1010NSE5HHB

–40° C to 105° C (extended)

P1010NXE5DFA

Document Number: IMX6DQIxEC
Rev. 2, 04/2013



i.MX

	Temperature T_j	Code
Consumer	0° C to + 95° C	D
Extended Consumer	-20° C to + 105° C	E
Industrial	-40 ° C to +105° C	C
Auto:	-40° C to + 125° C	A

Table 1. Example Industrial Grade Orderable Part Numbers

Part Number	Quad/Dual CPU	Options	Speed Grade	Temperature Grade	Package
MCIMX6Q7CVT08AC	i.MX 6Quad	With VPU, GPU	800 MHz	Industrial	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D7CVT08AC	i.MX 6Dual	With VPU, GPU	800 MHz	Industrial	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)



Temperature Range

QorIQ processing platforms and i.MX application processors support extended temperature range.

T1040

The Freescale documentation refers to junction temperature and provides technical details related to the package that you select.

QorIQ

Operating temperature (Ta - Tj) range:

0–105° C (standard)

–40° C to 105° C (extended)

Operating temperature range	Normal operation	T _A , T _J	T _A = 0 (min) to T _J = 105(max)	°C	-	-
	Extended Temperature	T _A , T _J	T _A = -40 (min) to T _J = 105(max)	°C	-	-
	Secure boot fuse programming	T _A , T _J	T _A = 0 (min) to T _J = 70 (max)	°C	-	2
Storage temperature range			T _{STG}	-55 to 150	°C	-

T1040NSE7MQB

T1040NxE7MQB



i.MX

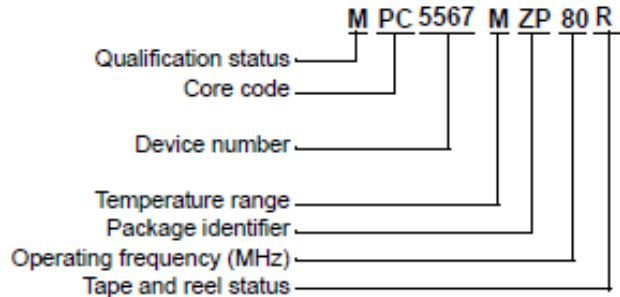
	Temperature Tj	Code
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MCIMX6D7CVT08AC	i.MX 6Dual	With VPU, GPU	800 MHz	Industrial	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)



Temperature Range #2



Example of the Qorivva MPC5567

That document makes reference to ambient temperature

Temperature Range
M = -40° C to 125° C

Package Identifier

- ZP = 416PBGA SnPb
- VR = 416PBGA Pb-free
- ZQ = 324PBGA SnPb
- VZ = 324PBGA Pb-free

Operating Frequency

- 80 = 80 MHz
- 112 = 112 MHz
- 132 = 132 MHz

Tape and Reel Status

- R = Tape and reel
- (blank) = Trays

Qualification Status

- P = Pre qualification
- M = Fully spec. qualified, general market flow
- S = Fully spec. qualified, automotive flow

Note: Not all options are available on all devices. Refer to Table 1.

Figure 1. MPC5500 Family Part Number Example

Unless noted in this data sheet, all specifications apply from T_L to T_H .

Table 1. Orderable Part Numbers

Freescale Part Number ¹	Package Description	Speed (MHz)		Operating Temperature ²	
		Nominal	Max. ³ (f_{MAX})	Min. (T_L)	Max. (T_H)
MPC5567MVR132	MPC5567 416 package Lead-free (PbFree)	132	135	-40° C	125° C
MPC5567MVR112		112	114		
MPC5567MVR80		80	82		



Freescale Longevity Program



- The embedded market needs **long-term product support**
- Freescale has a longstanding track record of **providing long-term production support** for our products
- Freescale is pleased to introduce a **formal product longevity program** for the market segments we serve
 - Automotive and medical segments:
Freescale will make a broad range of program devices available for a minimum of **15 years**
 - All other market segments in which Freescale participates, Freescale will make a broad range of devices available for a minimum of **10 years**
 - **Life cycles** begin at the time of launch
- A list of participating **Freescale products** is available at: www.freescale.com/productlongevity



Recent Product

Category	Family / Series	10-Year	15-Year	Product Launched
Processors	i.MX 6 Series	i.MX 6SoloX	i.MX 6SoloX (Auto)	February 2015
Processors	i.MX 6 Series	i.MX 6Solo	i.MX 6Solo (Auto)	November 2012
Processors	i.MX 6 Series	i.MX 6Dual	i.MX 6Dual (Auto)	November 2012
Processors	i.MX 6 Series	i.MX 6DualLite	i.MX 6DualLite (Auto)	November 2012
Processors	i.MX 6 Series	i.MX 6Quad	i.MX 6Quad (Auto)	November 2012
Processors	QorIQ	-	LS1020A22A	September 2013
Processors	QorIQ	-	LS1021A	September 2013
Processors	QorIQ	-	T1024	April 2014
Processors	QorIQ	-	T1040/42	October 2012
Processors	QorIQ	-	T2080	June 2012
Processors	QorIQ	-	T2081	October 2012
Processors	QorIQ	T4150	-	February 2012
Processors	QorIQ	T4240	-	February 2012



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Development Assurance Level "DAL", Criticality & Freescale Processors

Applications connected to criticality:

Failure conditions	System safety objectives	System DAL (Development Assurance Level)
<p>Catastrophic Multiple deaths, Aircraft lost</p>	<p>Implemented with redundancy and / or diversity</p> <p>$< 10^{-9}$ + Fail Safe Criteria : No single failure can lead to a catastrophic event</p>	A
<p>Hazardous Large reduction in safety margins, serious (potentially fatal) injuries to occupants</p>	<p>Supervised / monitored by MCU or small MPU</p> <p>$< 10^{-7}$</p>	B
<p>Major Significant reduction of safety margins, possible injuries to occupants</p>	<p>All above and MPC8572, MPC7448, P1013, P1010</p> <p>$< 10^{-5}$</p>	C
<p>Minor No significant safety reduction, inconvenience to occupants</p>	<p>All Freescale Portfolio</p> <p>$< 10^{-3}$</p>	D
<p>No safety effect</p>	<p>none</p>	E

MPC8270, MPC8548
MPC8xx, MPC7448,
MPC8610, MPC56xx,
MPC83xx, P1010, P2020
Ongoing on derivative
T1022 and T2080

All above and
MPC8572,
MPC7448
P1013
P1010

All Freescale
Portfolio

Freescale QorIQ Processors for **Aerospace and Defense**

MPC83xx , MPC85xx , MPC86xx

e300 , e500 and e600 cores

800 MHz above 1 GHz

IFF, fuel management, main flight control and secondary flight control, artillery control computer, cockpit display, IMA, airborne computer, rocket navigation system



P1010 , P2020

P3041 , P5020

45nm, e500, e5500 multicore

above 1 GHz

Cockpit display, airborne computer civil and defense, aircraft engine management , communication, government Unified Thread Management (firewall, Gateway) , IMA, rocket navigation system



T4xxx , T1022, T2080

28 nm, e5500 64-bit multicore above 1 GHz

Civil avionic, defense airborne computer, weapon navigation system, UAV flight computer, ground control system



Keys advantages: Low power consumption, single and multi-cores, easy software transition or reuse of previous validation and certification artifacts associated with processors based on Power Architecture

Solutions for Aerospace & Defense Applications

MPC555



Qorivva MPC55xx

Engine management, fuel management, main and secondary flight control



Qorivva MPC56xx

Qorivva MPC57xx

Ongoing transition from above devices to take advantage of hardware safety features



QorIQ Qonverge Platform

Communication system, RADAR , SONAR



i.MX applications processors based on ARM technology

Fingerprint and Retinal Identification System, Sight System, Field Tactical Terminal



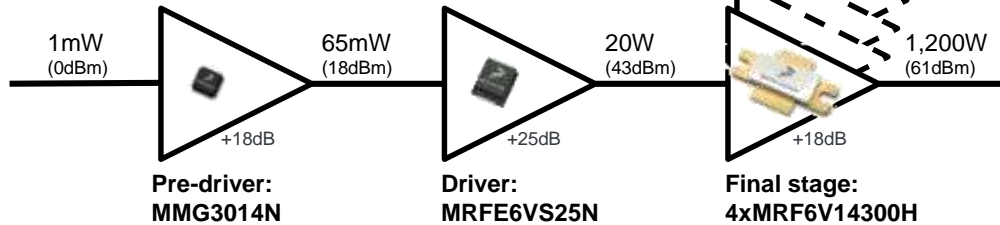
Kinetis MCUs based on ARM Technology

Inertial sensor, Controller for aircraft subsystem



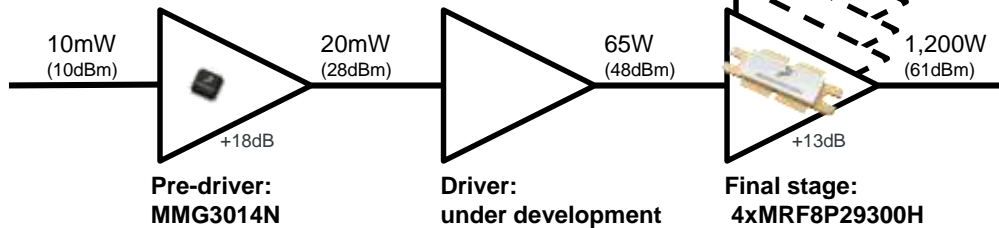
RF Solution for Aerospace & Defense

L-band / 1,300W radar 1.2 to 1.4 GHz



S-ban / 1,300W radar

2.7 to 2.9 GHz (civil), 2.9 to 3.5 GHz (military)



Solution for Radio Applications

- Transponder/Secondary radar
- L-band
- S-band primary radar
- DME
- VOR

- Freescale is the world leader in RF power products in wireless infrastructure, serving macro cells to small cells, land mobile, industrial, scientific, medical and defense applications.
- http://www.freescale.com/webapp/sps/site/homepage.jsp?code=RF_HOME

Safe SBC for Aerospace & Defense

- System Basis Chip (SBC) family provides energy efficient DC/DC power conversion and low voltage operation with advanced functional safety mechanisms

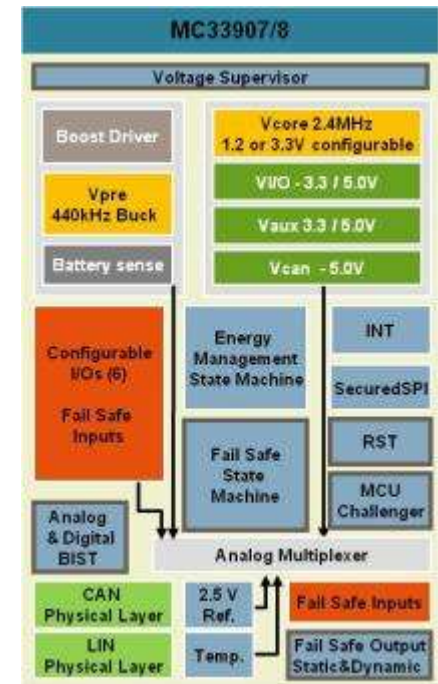
Differentiating Points:

- **Availability** : Ultra low voltage operation **down to 2.7V**
- **Efficiency** of a Dual DC/DC converter topology
- **Safety** : Innovative architecture allowing **independent** monitoring of safety critical parameters
- **Scalable** family of products supporting a wide range of MCU and power segmentation architectures

Product Features:

- Flexible DC/DC Buck pre regulator with optional Boost to fit with **LV124**
- Multiple supplies up to **1.5 A**
- Low Power Modes (**30µA**), -50% versus competition
- Analog Multiplexer & Battery sensing
- **Independent fail safe state machine** supporting functional safety standards
- Secure SPI interface
- Robust physical layers with superior EMI/ESD performance

Typical Block Diagram



PowerSBC Functional Safety Strategy

example of **Power Supply Monitoring**

Single Point Failure (SPF)

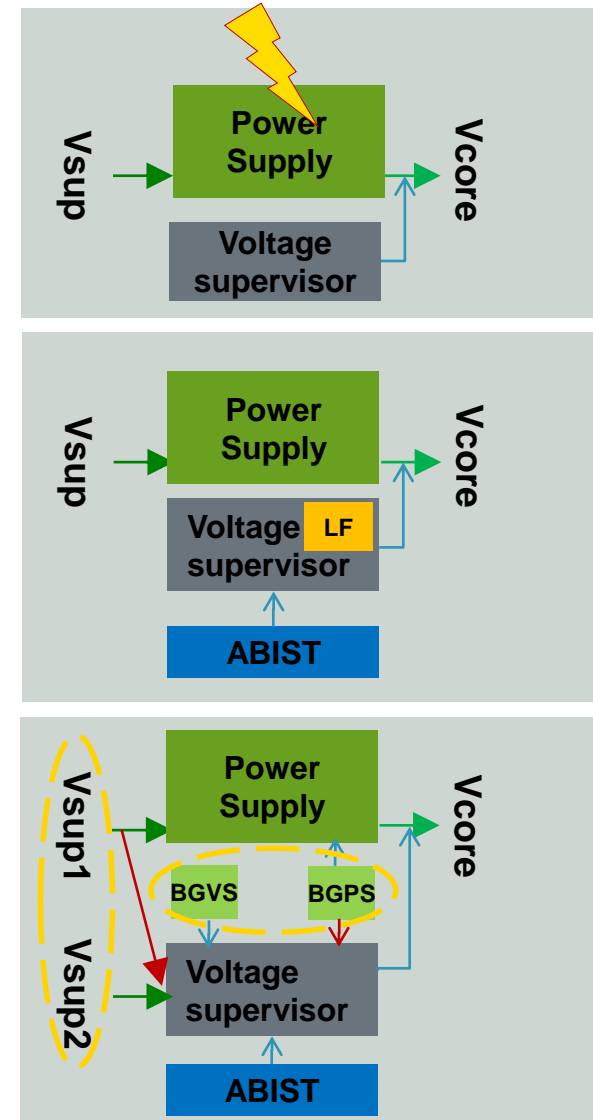
- Fail Safe State Machine as **independent** checker
- Physical and electrical independence
- Own Reference, clock, Supply

Latent Failure (LF)

- **Built-In Self Test**
 - Analog (ABIST)
 - Logic (LBIST) – covering 90%
- Checker activated at each init phase

Common Cause Failure (CCF)

- **Independent** Failure Monitoring Machine covering
 - Independent Vsup, Reference voltage and current, clock
 - Fail-Safe Signal Monitoring
 - Fail-Safe Output Management



SafeAssure HW – Functional Safety Concept



Four PowerSBC **Safety Functions** implemented:

1) Power supply and Supervisor

- Over-voltage detection
- Under-voltage detection
- Voltage supervisor provides **independent supervision of power supply**
- Second power supply not necessary

2) Failsafe inputs

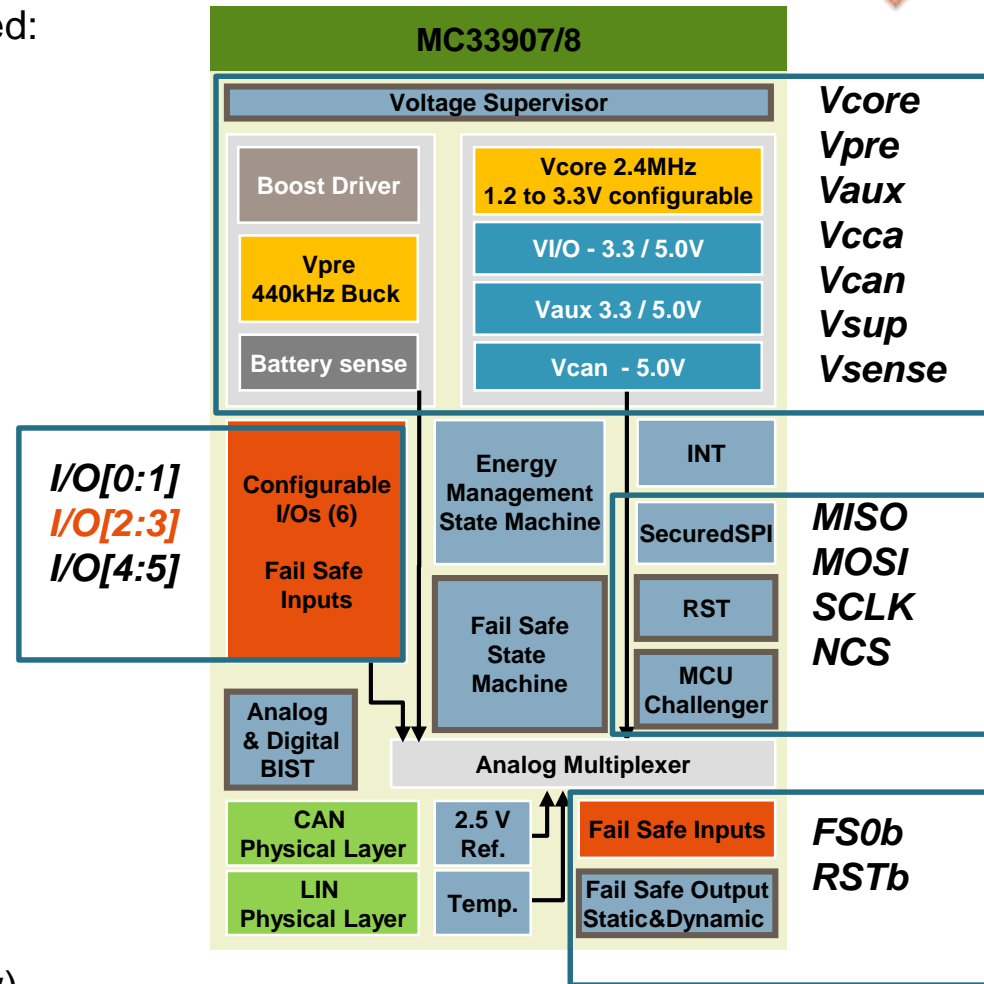
- **MCU error** signal monitoring
- **Analog IC error** signal handling

3) Watchdog

- Windowed watchdog (1ms to 1024ms)
- SPI refresh → Question / Answer principle (8-bits **challenger**)

4) Failsafe outputs

- RSTb → MCU **reset** (active Low)
- FS0b → **System** “deactivation” (active Low)



For more details see back up slides



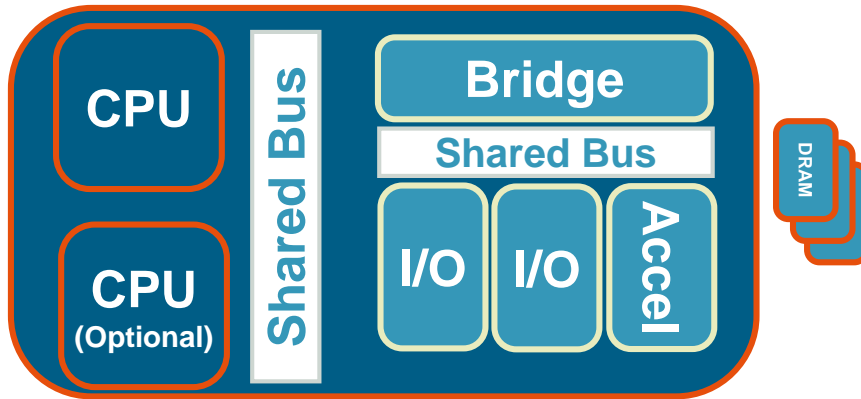
Agenda



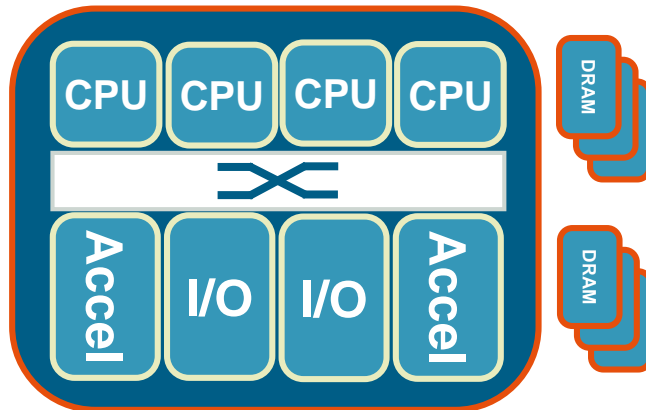
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Freescale Processor Architectures



PQ/P1/P2/Qorivva/ i.MX



P3, P4, P5, T1, T2 & T4

Processors implemented with “shared bus”

- Based on Power Architecture technology
- i.MX applications processors based on ARM technology
- Cores are standard and enable use of standard compilers & development tools
- High integration with: external bus, memory controllers, connectivity
- Omnipresent security functions: ECC, parity, function control, performance monitor, tracing, clock management
- Excellent ratio of performance versus power consumption

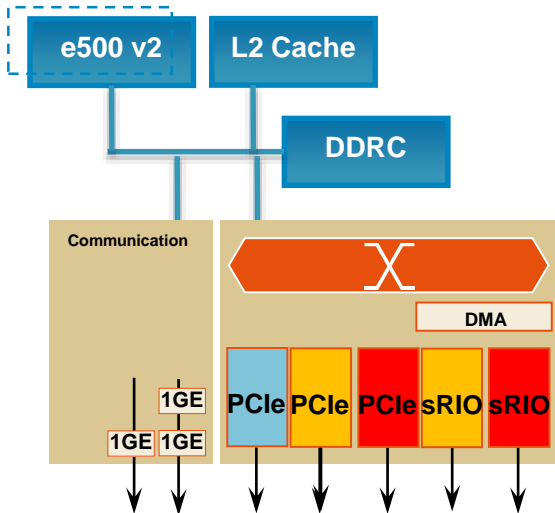
Multicore have all of the above functions and:

- More cores (2, 4, 8 or 12 (24))
- Advanced interconnect
- High performance connectivity
 - up to 10G Ethernet, Multiple PCIe
 - Multiple memory interface with ECC
 - Advance SoC memory mapping supervision (MMU, PAMU, Hypervisor)

Cores & Architecture #1

e500v2 P102x, P202x

- 32-bit Power Architecture Book-E
- Superscalar, OOO, Dual-Issue, 7stage pipeline
- SPE & EFPU
- ECM Bus & Platform L2
- Up to 2 cores, 1.5GHz nominal



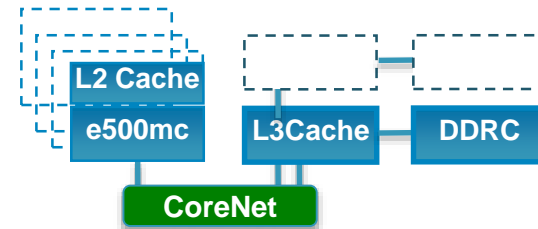
“Classic” processor architecture:

- Available version with only one core
- Integration of bus (DDR, PCIe ...)
- Integration of communication

e500mc

e500v2 enhanced for multicore:

- Hypervisor, MMU TLB w/64 variable size entries
- DP FPU (classic), decorated L/S instructions
- CoreNet Coherency Fabric (2x snoop BW), L3 cache
- Up to 8 cores, 1.5GHz nominal



P40xx, P30xx, P204x

“Interconnect ” processor architecture:

- Implementation with interconnect switch fabric
- Implementation of advance platform safety function (PAMU)

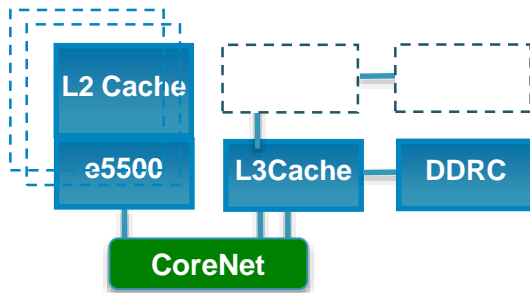
Cores & Architecture #2

64-bit processor architecture

e5500 P50xx, T1xxx

e500mc plus:

- 64b ISA 2.06, 36b (64GB) per process
- Extended Branch Predictor
- Full speed DP FPU (classic)
- Larger L2 (512KB)
- Additional Integer/FP instructions
- Supports 32-bit mode for software legacy
- Up to 4 cores, 2.2GHz in 45SOI

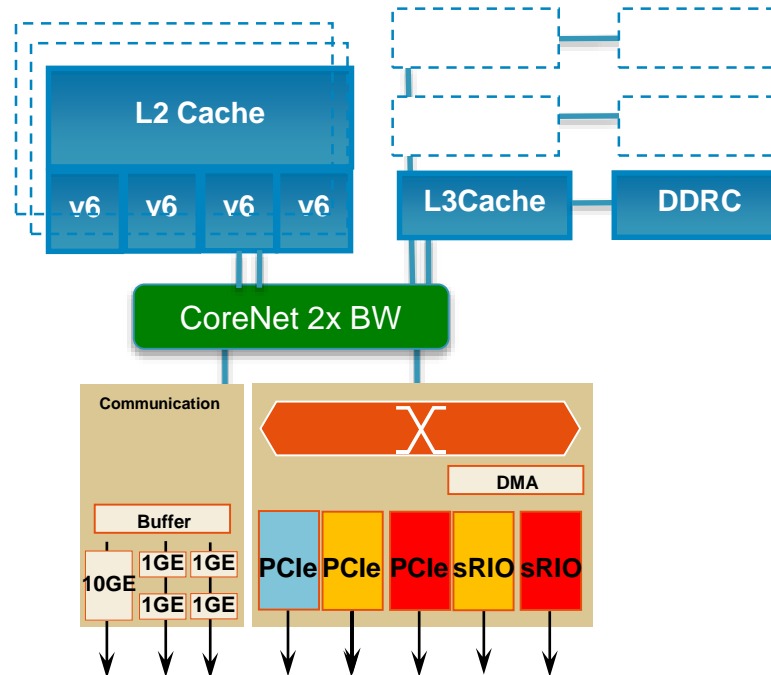


- “28 nm” processors architecture
- High Performance & Low-Power
 - Up to 12 Cores Dual Thread (24 cores)
 - Large surface of internal caches

e6500 T4xxx, T2xxx, B4

e5500 plus:

- Dual SMT Thread
- Clustered architecture with Banked L2 , up to 256-512KB L2 per core
- AltiVec
- 40-bit real address
- Optimized power management
- HW MMU-PTW + LRAT for improved OS/HV performance
- 2.0GHz in 28nm many core



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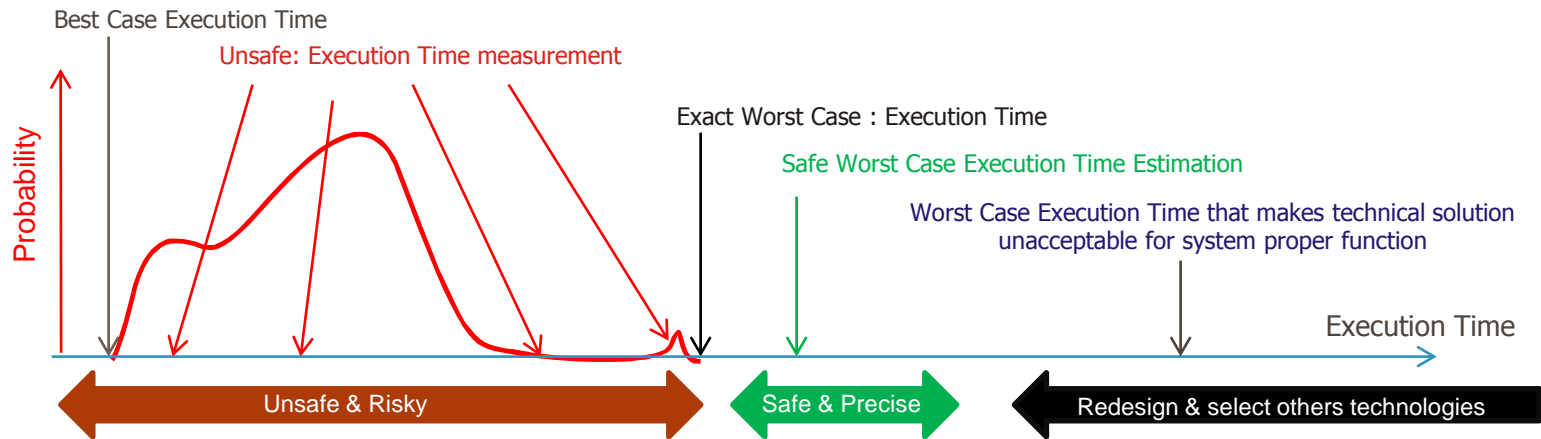
Timing Assessment & Technical Constraints

WCET: “*Worst Case Execution Time*. It consists of determining a safe and precise bound on execution times of all possible runs of a system “.

Applied to a safety computer, a “faster” execution time and “slower” execution time are serious concerns that could lead to serious failure .

“If you move the control stick to left to turn left, it should turn left and not right and it should start right away !”

Several ways to compute that time: simulation, in-deep analysis of chipset specification with available architecture.

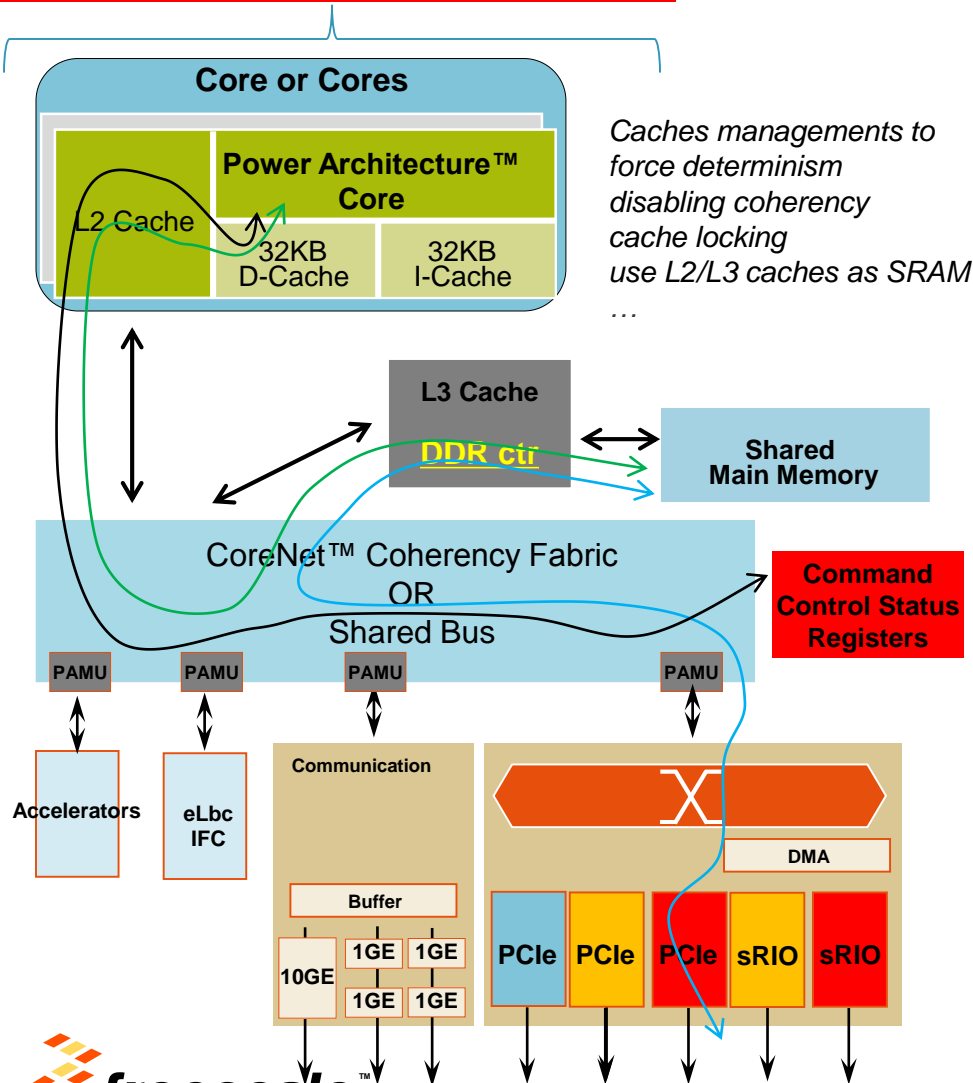


- Evaluation of execution time is extremely complex due to multiple functional blocks that can behave as masters inside the processors.
- Recommended approach is to focus on simplified architecture with bounded use cases.

Timing Evaluation on Multicore Solutions

Peripheral Access Mgmt Units (High-End QorIQ) PAMU

Debug Tools / Performance Management



*Caches managements to force determinism
disabling coherency
cache locking
use L2/L3 caches as SRAM
...*

The simulation option requests a “simulator cycle accurate”. That solution was available on previous processors MPC7xx(x). Not available for complex SOC due technical complexity and support.

The alternative solution is:

- The measurement on real hardware evaluation platform with a bounded, simplified use case that answers to WCET convergence with the support of a theoretical analysis

For example:

- Focus on independent use cases.
- If multiple use cases are required to achieve system targets, the occurrence should be managed by implementation (HW + SF) that enforces the above use cases.

**CORE <> MEMORY
IO <> DMA <> MEMORY
CORE <> SYSTEM CONTROL**

Deliverable is a well-known, fully evaluated bandwidth understanding and execution time behavior.

Key factors that increase complexity:

- Simultaneous access to different functional blocks
- Access to control block
- Multiple DDR controllers
- Assuming multiple cores



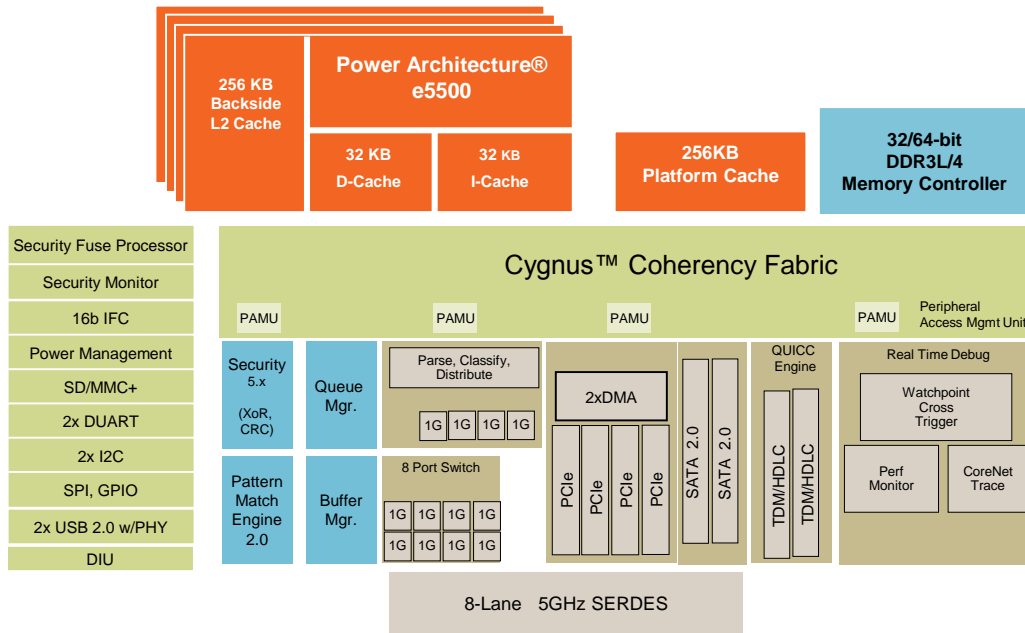
Agenda



- Freescale experience in Aerospace and Defense applications
- Key factors
- Development Assurance Level (DAL), criticality & Freescale processors
- Freescale processors architectures
- Timing assessment & technical constraints
- **QorIQ "System On Chip" evolution**
- System control & configuration
- Memory protection
- Freescale processors - design for SEU robustness
- Freescale implementation advantages
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QorIQ Processors "System On Chip" Evolution



QorIQ Processors

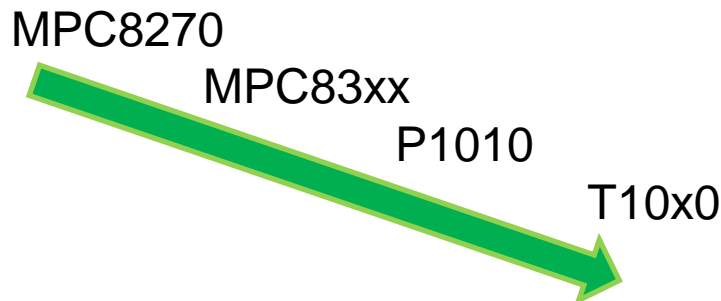
Protection and supervision

- System supervision
- MMU
- PAMU
- Performance monitor
- Global switch controlling functional block
- Memory protection
- ECC on DDR
- Local bus with parity

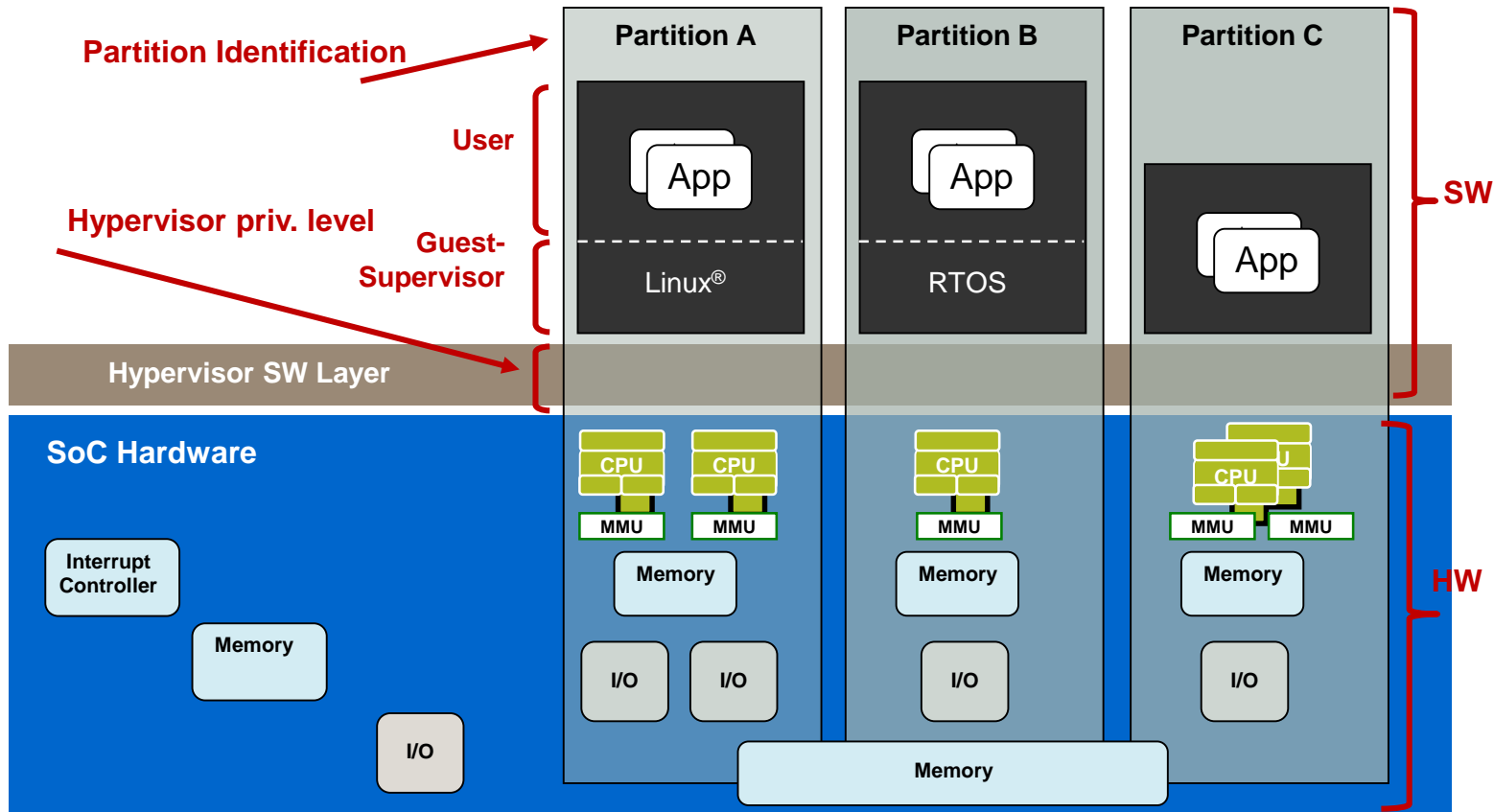
Embedded communication interfaces

- PCIe
- SRIO
- Ethernet 1G / 10G
- Switch
- SATA
- Trace & Debug

Migration path for previous design evolution



“Robust” Partitioning for Flight Computers



White Paper (QORIQHSRPWP) is the main reference for QorIQ partitioning:

Hardware Support for Robust Partitioning in Freescale QorIQ Multicore SoCs (P4080 and derivatives)

http://www.freescale.com/files/32bit/doc/white_paper/QORIQHSRPWP.pdf

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Software “Understanding” of the Hardware

P2020 QorIQ Integrated Processor Reference Manual, Rev. 2, 12/2012

E_00A0	Processor version register (GUTS_PVR)	32	R	8021_1051h	21.4.15/ 1812
--------	---------------------------------------	----	---	------------	------------------

SoC revision	Core revision	Processor version register (PVR)	System version register (SVR)
1.0	4.0	0x8021_1040	System version register (GUTS_SVR)
2.0	5.0	0x8021_1050	System version register (GUTS_SVR)
2.1	5.1	0x8021_1051	System version register (GUTS_SVR)

2BF8	DDR IP block revision 1 (DDR_DDR_IP_REV1)	32	R	See section	8.4.31/323
------	---	----	---	-------------	------------

Field	Description
0–15 IP_ID	IP block ID. For the DDR controller, this value is 0x0002.
16–23 IP_MJ	Major revision. This is currently set to 0x04.
24–31 IP_MN	Minor revision. This is currently set to 0x03.

9BF8	IP block revision register 1 (PEX2_PEX_IP_BLK_REV1)	32	R	0208_0101h	16.6.10/ 1344
9BFC	IP block revision register 2 (PEX2_PEX_IP_BLK_REV2)	32	R	0000_0000h	16.6.11/ 1344

Field	Description
0–15 IP_ID	Block ID
16–23 IP_MJ	Block Major Revision
24–31 IP_MN	Block Minor Revision

QorIQ Processors contain registers that enable identification by software of the silicon version and functional blocks version.

Example: P2020

QorIQ type and version

DDR controller

PCIE controller

....

QorIQ Processors Memory Map

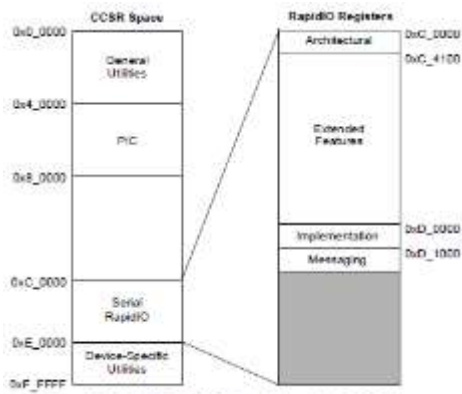


Figure 2-5. Serial RapidIO Register Map within CCSR Space

The Power Architecture core used in QorIQ processors have an MMU to protect the memory map.

QorIQ processors based on e500mc, e5500 and e6500 offer hypervisor functions that can centralize platform configuration and help to identify default and violation.

2.3.1.1 Local Access Window n Base Address Registers (LAWBAR0-LAWBAR11)

The LAWBAR_n registers define the 24 high-order address bits that fixes the location of each window in the local address space. Note that the minimum size of any LAW is 4 Kbytes, so the 12 lowest-order bits of the base address cannot be specified. Figure 2-7 shows the bit fields of the LAWBAR_n registers.

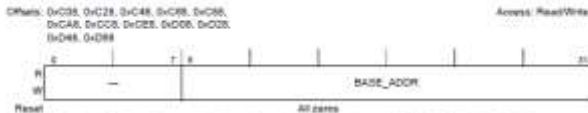


Figure 2-7. Local Access Window Base Address Registers (LAWBAR0 to LAWBAR11)

The memory map can be protected by a window (cumulative function with MMU).

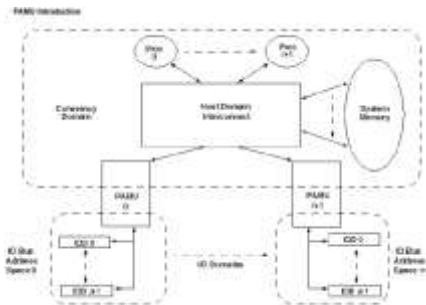


Figure 10-1. Illustration of a Multicore System

The QorIQ processors based on interconnect have a function block (PAMU) that can prevent masters, other than cores (PCIe, DMA, Ethernet ...) from accessing unauthorized memory location.

System Control & Configuration #1

Table 1. P2010 Pinout Listing (continued)¹

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
DFT					
SCAN_MODE	Scan Mode	W27	I	OVDD	33
TEST_SEL	Test Select	AA28	I	OVDD	30

P2010

33. This pin requires a 1 kΩ pull up to OVDD.
30. Requires a pull down with 100~1K to GND

Table 1. P2020 Pinout Listing (continued)¹

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
DFT					
SCAN_MODE	Scan Mode	W27	I	OVDD	33
TEST_SEL	Test Select	AA28	I	OVDD	29

P2020

33. This pin requires a 1 kΩ pull up to OVDD.
29. Pull up with a 4.7 kΩ resistor to OVDD

Table 4-12. Boot ROM location

Functional Signals	Reset Configuration Name	Value (Binary)	Meaning
TBECT_TXD[6:4], TBECT_TX_ER Default: 1111	cfg_rom_loc[0:3]	0000	PCI Express 1
		0001	PCI Express 2
		0010	Serial RapidIO 1
		1111	Local bus GPCM-16-bit ROM

Functional signal	Reset configuration name	Value (Binary)	Meaning
LA27, LA16 No Default	cfg_cpu0_boot, cfg_cpu1_boot	00	CPU boot holdoff mode for both cores. The e500 cores are prevented from booting until configured by an external master.
		01	e500 core 1 is allowed to boot without waiting for configuration by an external master, while e500 core 0 is prevented from booting until configured by an external master or the other core.
		10	e500 core 0 is allowed to boot without waiting for configuration by an external master, while e500 core 1 is prevented from booting until configured by an external master or the other core.
		11	Both e500 cores are allowed to boot without waiting for configuration by an external master.

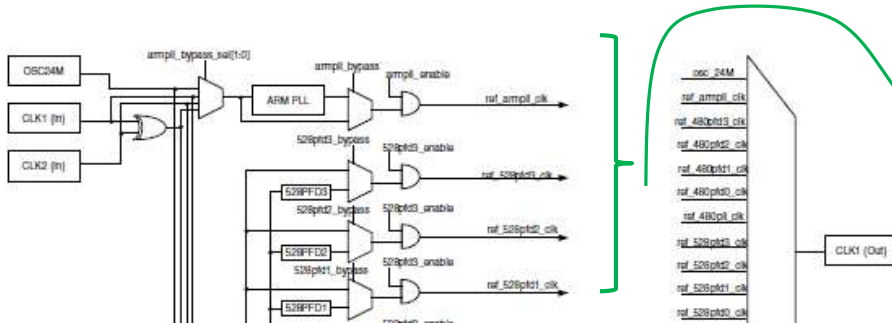
QorIQ processors offer a hard boot configuration or a reset configuration word loaded from memory.

For example, the P2020 and P2010 have a hard selection for one or dual core use. Then a P2020 can be used as a P2010.

Note: It is unsafe to use a P2010 as a P2020. If you use a P2010 as a dual core P2020, “you do that at your own risk”.

Essential boot, configuration and clock are done in hardware or loaded from a specific memory section that could be designed with QCS (QorIQ Configuration Tool).

System Control & Configuration #2



All Freescale processors offer enable bit in each functional block (UART, SPI, external bus ...)

The Freescale processors offer what we call a “clock tree” that supports functions to setup clocks by enabling sub-branch and changing dividers.

Several functional blocks offer a second level to deal with clock issues from a clock tree.

Devices offer internal clock output that can be programmed to export outside of device the internal clocks (DDR, core, bus ...). One best practice is to “PWM” those clock depending of software states to export system functional states and trig deviation with external hardware (FPGA, other SOC ...). Special care should be observed with the EMC.

QorIQ processors offer centralized registers to enable and disable embedded functional blocks.

That is the “Configuration Registers Device Disable Register” (DEVDISR).

22.4.1.8 Device Disable Register (DEVDISR)

DEVDISR, shown in Figure 22-8, contains disable bits for various functional blocks.

Offset 0xE_0070 Access: Read/Write

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
W	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
W	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 22-8. Device Disable Register (DEVDISR)

Table 22-11. DEVDISR Field Descriptions

Bits	Name	Description
0-1	—	Reserved
2	PCIE1	PCI Express 1 controller disable 0 PCI Express 1 controller enable 1 PCI Express 1 controller disable
3	—	Reserved
4	eLBC	Local bus controller disable 0 Local bus controller enable 1 Local bus controller disable
5	PCIE2	PCI Express 2 controller disable 0 PCI Express 2 controller enable 1 PCI Express 2 controller disable



Performance Monitors

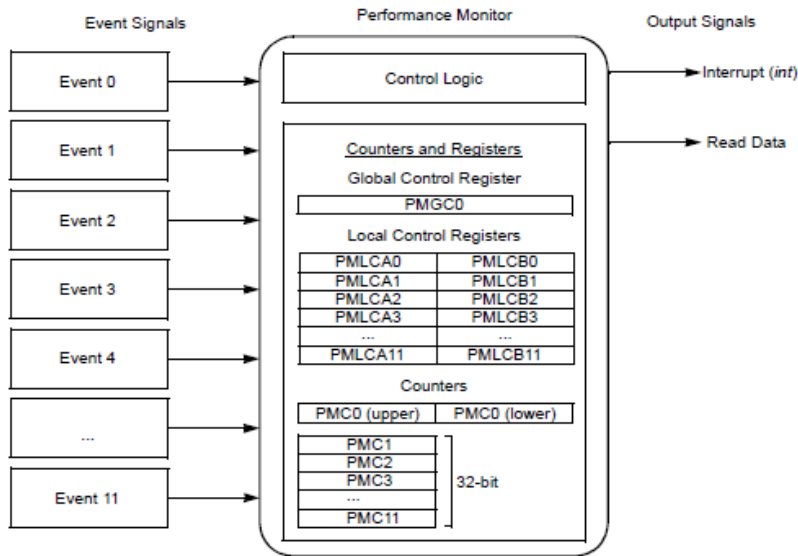


Figure 23-1. Performance Monitor Block Diagram

- Performance monitor can be used to survey activities of the processors functional blocks or behaviors.
- The use of selected performance monitor counters can highlight deviation and unveil software failure like deadlock, DMA misuse and performance change.

Event Counted	Number	Description of Event Counted
Channel 3 read DW or less	C4-72 and C8-118	DMA channel 3 read double word valid
Channel 0 write DW or less	C1-89	DMA channel 0 write double word valid
Channel 1 write DW or less	C2-72	DMA channel 1 write double word valid
Channel 2 write DW or less	C3-71	DMA channel 2 write double word valid
Channel 3 write DW or less	C4-73	DMA channel 3 write double word valid
DMA Controller 2 Events		
Channel 0 read request	C8-88	DMA channel 0 read request active in the system
Channel 1 read request	C5-94	DMA channel 1 read request active in the system
Channel 2 read request	C10-75	DMA channel 2 read request active in the system
Channel 3 read request	C11-73	DMA channel 3 read request active in the system

Event Counted
Cycles a read is returning data from DRAM
Cycles a read or write transfers data from (or to) DRAM
Pipelined read misses in the row open table
Pipelined read or write misses in the row open table
Non-pipelined read misses in the row open table

Freescale solution for "System On Chip" safety

- Qorivva 32-bit MCUs based on Power Architecture® Technology offer advantages for safety built on specialized hardware blocks
- SafeAssure Functional Safety Program
- The Freescale SafeAssure program supports the most stringent Safety Integrity Levels (SILs) to help developers more easily attain system compliance. Whether your need is to attain ASIL-A to D or SIL- 1 to 4 system compliance, the SafeAssure program identifies products that are targeted for use in the effective implementation of functional safety technologies.

<http://www.freescale.com/webapp/sps/site/homepage.jsp?code=SAFETYPRGRM>

Safety process

Integrating functional safety into product development process

Select products defined and designed from the ground up to comply with the standards

Safety hardware

Built-in safety functions (self-testing, monitoring and hardware-based redundancy) in Freescale microcontrollers (MCUs), power management ICs and sensors

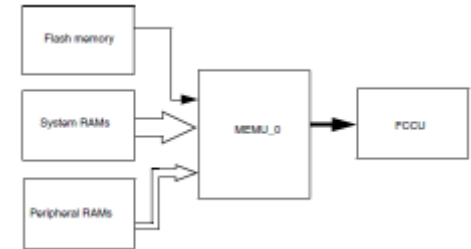
Additional system-level safety functionality from Freescale analog solutions (checking MCU timing, voltages and error management)

Safety software

A comprehensive set of automotive functional safety software, including AUTOSAR OS and associated microcontroller abstraction layer (MCAL) drivers, as well as core self-test capabilities
Partnerships with leading third-party software providers for additional safety software solutions

Safety support

From customer-specific training and system design reviews to extensive safety documentation and technical support



Error Correction Status Module (ECSM)

Memory Error Management Unit (MEMU)

Fault Collection and Control Unit (FCCU)

Self-Test Control Unit (STCU2)

Cyclic Redundancy Check (CRC) Unit



Qorivva MPC5744P & SafeAssure

ISO 26262 ASIL D

- Safety assessment of MCU architecture and development process (ISO 26262)
- helps to reduce effort and time on ECU functional safety assessment

Integrated Safety Architecture (ISA)

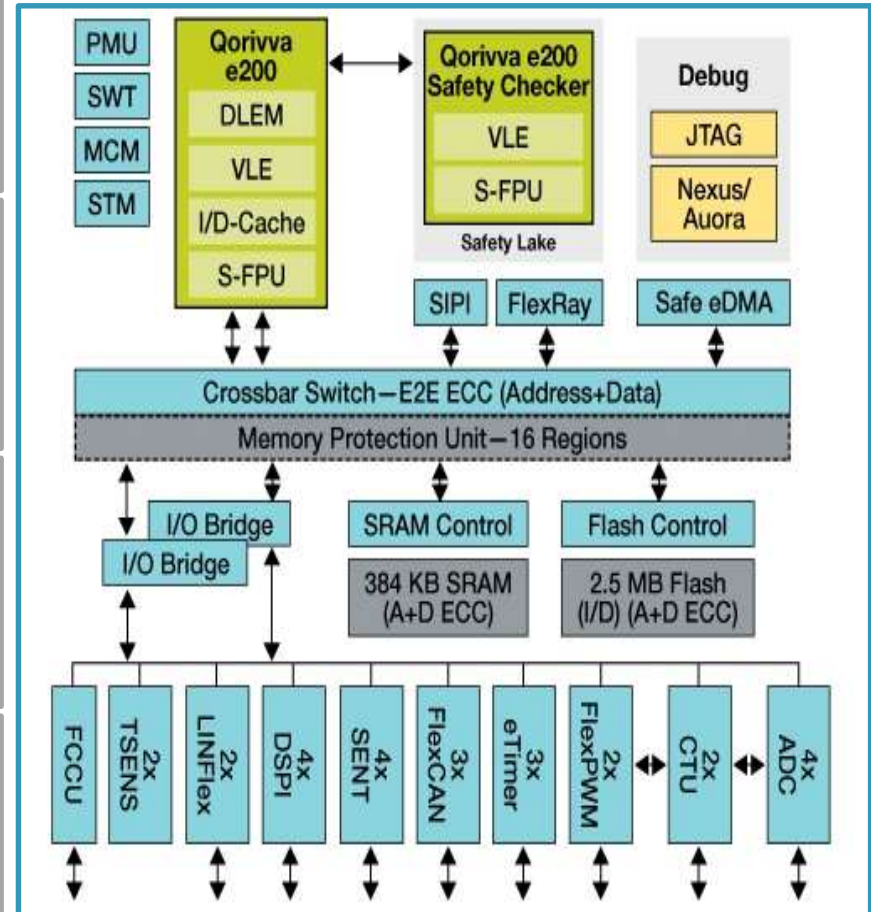
- Saves development effort and time as no complex diagnostic SW required
- CPU processing power available for running applications
- High diagnostic coverage in HW to detect random faults

SW deliverables provided by Freescale and partners

- Enable support for ASIL D applications with minimized performance degradation
- sMCAL & sOS, Selftests, SW Safety Manual

Safety enablement provided by Freescale

- Safety Manual
- FMEDA
- System Level Application Note



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Memory protection

Functional blocks that use memory are protected by parity or ECC.

P1 and P2

L1-cache: parity on data and tag

L2-cache: ECC or parity on data, parity on tag

Local Bus (eLBC) controller: parity on data, ECC on FCM (NAND Flash controller)

P3, P4, P5 and T1, T2, T4

CPC/L3-Cache: ECC on data, tag and status

DDR Controller: ECC on data

PAMU (IO master MMU): ECC on both PAMU Look-aside caches
(Primary PAACT cache and Secondary PAACT cache)

DPAA functions for communication: ECC on QMan, BMan, FMan and 10G-MAC internal memories

LS1

ECC protection on both L1 and L2 caches

DDR3L/DDR4 with ECC and interleaving support

Refer to device specific documentation for details and variation depending of selected device

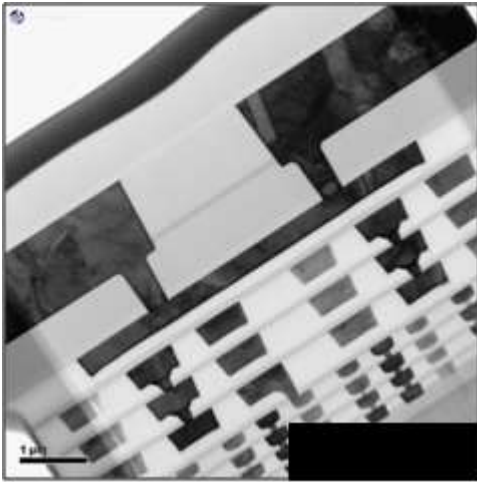
Agenda



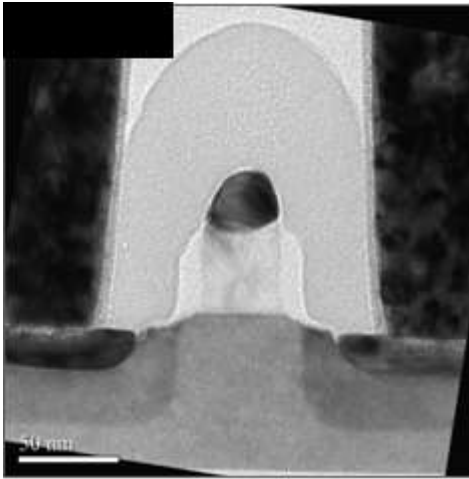
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Freescale Technology Advantage



- Example of 45 nm SOI, delivers on its promise!
- Standard semiconductor technology platform for long-term manufacturing



- Active & Static power improvement
 - Delivered frequency performance
 - Scaling for unparalleled packaged performance-power ratio
- *And retains its strong SER reliability advantage*

Contact Freescale Sales for details, collateral documentation may require a NDA

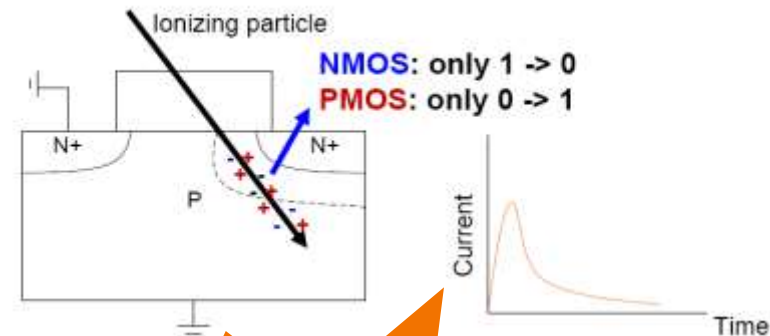
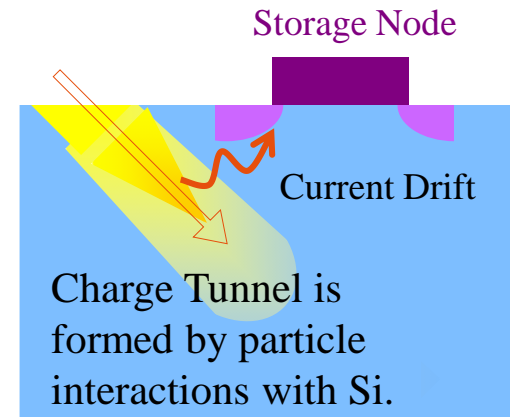
SEU & SEGR

SEU Radiation Events generate Soft Errors

- Neutrons:
 - Background Cosmic Ray flux
 - Depends on location, altitude and atmospheric conditions
 - Difficult to shield
- Alpha Particles:
 - Easily shielded thus only concerned with internal alpha sources
 - Impurities in packaging materials.
 - Contamination of fab. process.
- **Solution is an adapted software and a “system” hardware design**

Single Event Gate Rupture (SEGR)

- Single-ion induced dielectric failure
- MOSFETs, Capacitors, FG Devices
- Difficult to mitigate
- **Solution is redundancy by using multiple processors with eventually multiple cores**
 - By developing survey software that monitor systems. The system architecture should support degraded performance response. The primary target is to discover the fault. On a Freescale processor, it could be based on systematic analysis of all processor exceptions and faults.



Freescale devices are built with ruggedized technology and designed with rules to mitigate those threats

Freescale Processors - Design for SEU Robustness

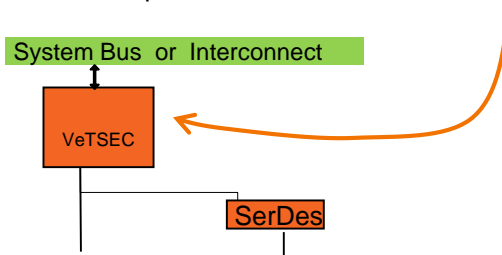
Device		Alpha Flux			Neutron Flux			
Part Number	P2020	Package Type	Wire Bond		Altitude	0 ft		
Technology	C45 SOI	Mold			Neutron	13 n/cm2/hr		
Operating Voltage	1.0V	Compound	0.001	alpha/cm2/hr				
Total Latch Count								
		Package	0.001	alpha/cm2/hr				
Freescale Part Number	Memory Arrays	Bit Cell	Size (Mbits)	ECC	Parity	Column MUX	ECC/Parity Effectiveness	Comments
P2020	L1 Data Cache	608	0.590	no	yes	2	0.00%	
e500v2 core	L1 Inst Cache	608	0.590	no	yes	2	100.00%	
	L1 Dtag	769	0.049	no	yes	1	0.00%	
	L1 Itag	769	0.049	no	yes	1	100.00%	
	L2 Cache	404	4.72	yes	no	4	100.00%	

Internal memory of functional blocks are generally protected (parity or ECC) and memory cell are spread to avoid multiple bit upset.

Contact Freescale Sales for details, collateral documentation may require a NDA

Communication Interfaces Ethernet & QUICC Engine

Enhanced Three-Speed Ethernet Controllers



Examples with QUICC Engine

- P1025/P1016 & LS1021A/LS1020A

Example with Enhanced Three-Speed Ethernet Controllers

- P1010
- P2020

eTSEC & QUICC Engine functional blocks use a memory mapped programming model that enable easy for registers survey.

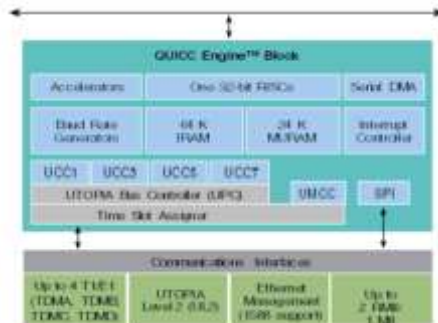
QUICC Engine offer several communication links

Scheduling of communication tasks is based on hardware.

The asynchronous architecture is scalable on RISCs core depending on the device (MPC8569 x 4, P1025 x1, LS1 x 1).

- DMA based communication
- DMA supervision possibility by monitoring each buffers transfers

The memory blocks used by hardware function, eTSEC and QE are protected **ECC or parity**.



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The Advantage of Freescale Security

- i.MX application processors, Vybrid Controller Solutions based on ARM Technology and QorIQ processing platforms offer security functions.
- Secure BOOT
 - It ensures that only software from original manufacturer will run on final products
 - One software could be associated to one special unique final product based on the unique processor serial number.
 - It supports field update and prevents software version downgrade
- eFuse functions
 - Deactivation of functional blocks
 - Defense application like “automatic death” for sensitive equipments
 - Protection again reverse engineering
 - Extreme customization of delivered product by removing function

***Above functions enable the design of systems
with an extremely high security level***



Summary of proposed approach

- Systems based on PowerQUICC integrated communications processors or QorIQ processors are complex and could be supervised by smaller MCU for fault detection for extremely sensitive applications.
- MMUs covers each cores and PAMUs covers “masters” (DMA), either communication devices or bridges (SRio or PCIe).
- Caches are covered respectively by ECC (L2, L3, DDR), parity (L1).
- For devices that don't have a PAMU (P1010, P2020), an alternate solution could be the monitoring of DMA registers and the use of Performance Monitor.
- Internal registers aren't protected and internal memory blocks (FIFO, tables ..) which serve functional blocks are frequently protected by ECC or parity.
- Early detection of failure could be detected with proper heuristic considering error and violation reported by MMU, PAMU, ECC, and parity. The system collapse could be mitigated by monitoring essential registers and adapted measurement with performance monitor. Then performing a Functional Failure Path Analysis (FFPA) could be done at an higher level (reference to MCU that are monitoring one or more multicores).

Freescal Implementation Advantages

Summary of Freescal architecture advantages for Aerospace and Defense

- Multicore architecture
- Supervision function
 - MMU within cores
 - PAMU within platform interconnection
- Memory correction
 - External local bus parity
 - DDR bus with ECC
 - Bus fault monitoring
- Control capability
 - Disabling block

The recommended approach is to implement at the early stage of software development all required handler to catch ALL exceptions including those non-relevant for unused functional blocks.

- QorIQ processors offer an “ultimate” exception “Machine Check” that reports error when “everything goes wrong”. It could be monitored from outside by a microcontroller.

Products Selection Guidelines

- Focus on the product that are labeled as the main device of the family.
- The selected product must be part of the Longevity Program -*not all family members are part of the program.*
- Criteria of package – not all packages for a selected product are part of the Longevity Program.
- Criteria of qualification grade and temperature range
- The low-cost derivatives frequently target specific market. Those markets could be ephemeral.

P1010	i.MX6Q	MPC5567
P2020	i.MX6DL	MPC560xP
P5020	...	MPC574xP
P3041		...

...

T10x0, T20x0 & LS1 should be evaluated. As avionic cycle are long it should be consider to use the latest introduced SOC which will give headroom in term of longevity

E2V Partnership

- Established more than 30 years ago
- Governed by a technology transfer license agreement
- E2V provides services that complement Freescale products:
 - High reliability / hermetic packaging
 - RoHS or lead packaging (eg. QorIQ)
 - Low and high temperature screening
 - Wafer banking, extended life support



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Multicore for Avionics (MCFA) Working Group

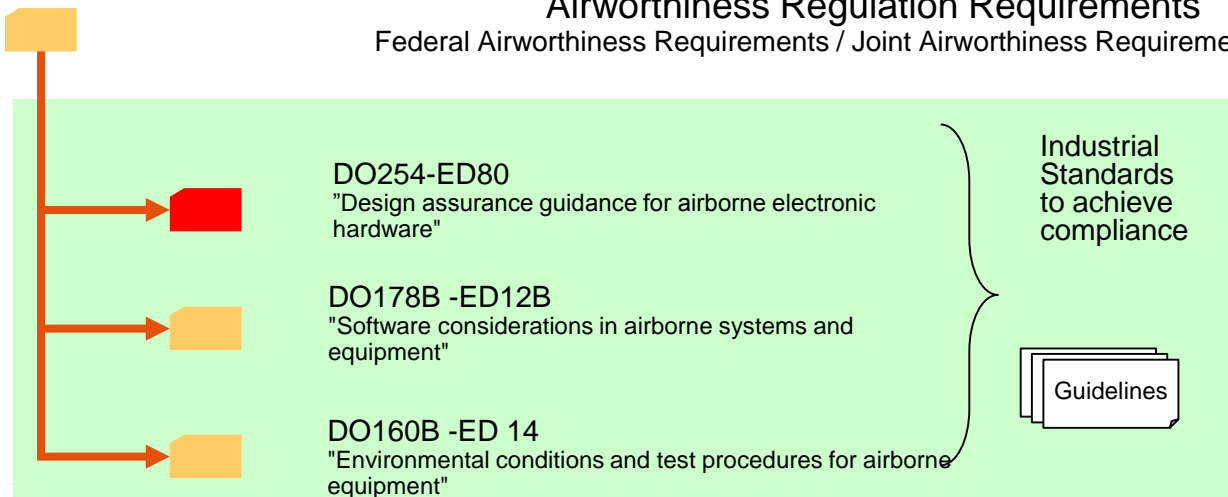
- Assist the industry with the certification of multicore SoC processors in commercial and defense aviation
- In order to better support our avionics customers in evaluating and/or integrating our multicore processors into certified airborne systems, Freescale has initiated a working group named **Multicore for Avionics - (MCFA)**
- **Goals:**
 - Define « **data package** » including necessary data required in the certification process to be made available by Freescale under NDA (Ap.Notes, IP reuse, test/validation, fault-tolerance, service experience ...)
 - Behave as a **forum for exchange** and consolidation of common « Multicore & Certification » issues and guidelines
 - Constructive, collaborative and participative approach
- **Participants** : BAE Systems, BARCO, Boeing, EADS, ELBIT, GE Aviation, Hamilton Sunstrand, Honeywell, Rockwell Collins, Thales and Freescale Semiconductor...
- **News release:**
 - <http://media.freescale.com/phoenix.zhtml?c=196520&p=irol-newsArticle&ID=1606741&highlight=>

Certification & Regulation Considerations

- Freescale has its own development process with robustness and excellence targeting semiconductor design and manufacturing.
- Customers can use the documentation that we deliver for an implementation of the processors, to understand SoC architecture and answer certification steps of DO254.
- Freescale provides online software examples of drivers for i.MX, Qorivva and QorIQ for their functional blocks (Ethernet, DDR, PCIe ...). Customers can use examples to develop DO-178 compliant software (depending on associated license).
- Freescale partners that supply emulators offer tools dedicated for production test and validation.

Airworthiness Regulation Requirements

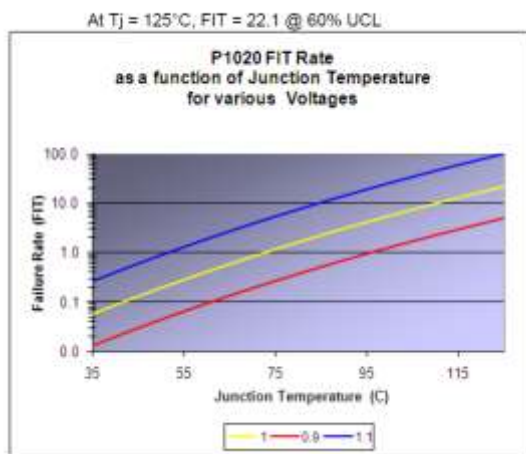
Federal Airworthiness Requirements / Joint Airworthiness Requirements (EASA)



“In Service Experience”

Freescale offers detailed qualification reports that provide details on numbers of devices tested and associated results.

QorIQ P1020 Product Fit Rate and MTTF Derate Curves



Qualification profiles frequently selected are :

- Industrial
 - 10 years
 - Part-time/ Full-time
 - Installed telecom equipment, work stations, servers, routers, etc.
Can also be used in Commercial applications.
- Automotive
 - 10-20 years
 - Part-time/ Full-time
 - "under the hood", drive train control, safety equipment, etc.
Can also be used in Commercial and Industrial applications.
- Others collaterals are available:
 - i.MX 6Solo/6DualLite Product Usage Lifetime Estimates
 - http://www.freescale.com/files/32bit/doc/app_note/AN4725.pdf

Agenda



- Freescale experience in Aerospace and Defense applications
- Key factors
- Development Assurance Level (DAL), criticality & Freescale processors
- Freescale processor architectures
- Timing assessment & technical constraints
- QorIQ "System On Chip" evolution
- System control & configuration
- Memory protection
- Freescale processors - design for SEU robustness
- Freescale implementation advantages
- Certification & regulation considerations
- **Summary of the documentation available for Freescale processors**
- Export control
- Session summary
- Q&A



Summary of the Documents Available for Freescale Processors - *Example of P2020*

Electrical specification “P2020EC” - Parametric specification (timing, voltage ...)

User’s Manual “P2020RM” - Functional specification (how it works)

Errata’s “P2020CE” - **Only available, under NDA for some devices**

Qualification Report - **Only available, under NDA for some devices**

http://www.freescale.com/docs/pcn_attachments/14985_P1020_P1025_SCK_Qual_Reports.pdf

SEU Report – **Only available, under NDA**

Evaluation board “P2020-RDB” - Documentation, schematics, Layout

Applications notes:

- How to implement: DDRs memory, layout rules, software configuration

Example : QORIQHSRPWP // Hardware Support for Robust Partitioning in Freescale QorIQ Multicore SoCs (P4080 and derivatives)

http://www.freescale.com/files/32bit/doc/white_paper/QORIQHSRPWP.pdf

- Clock & Performance Calculators (Availability depends on selected target processor)
- Pins configuration tools (Availability depends on selected target processor)

Summary of the Documents Available for Freescale Processors - *Example of T1040 family product (T1020/22/40/42)*

Electrical specification “T1040” - Parametric specification (timing, voltage ...)

User’s Manual “T1040RM” - Functional specification (how it works)

Errata’s “T1040CE” - **Only available, under NDA for some devices**

Qualification Report (T1040) - **Only available, under NDA for some devices**

http://www.freescale.com/docs/pcn_attachments/14985_P1020_P1025_SCK_Qual_Reports.pdf

SEU Report – **Only available, under NDA**

Evaluation board “T1040RDB” – Documentation
schematics, Layout - **Only available, under NDA**

Applications notes:

- How to implement: DDRs memory, layout rules, software configuration

Example : QORIQHSRPWP // Hardware Support for Robust Partitioning in Freescale QorIQ Multicore SoCs (P4080 and derivatives)

http://www.freescale.com/files/32bit/doc/white_paper/QORIQHSRPWP.pdf

- Clock & Performance Calculators (Availability depends on selected target processor)
- Pins configuration tools (Availability depends on selected target processor)

CodeWarrior Development Studio



Development Phase	Tool Capability
Development / Project Management	Eclipse IDE
Board Bring Up	Memory / Register Visibility, Bare-metal run-control, Memory testing
Deployment	Flash Programmer
Functional Debug of OS / HV	Kernel Debugger
OS Application Development	Application Debugger
Performance Tuning of OS and Application	Performance Analysis Profiling
Advanced Debugging Techniques	Trace Analysis



CodeWarrior Run Control Tools

Planning, &
Simulation

Hardware
Designs

Board
Bring-up

Kernel &
Driver Dev

Application
Development

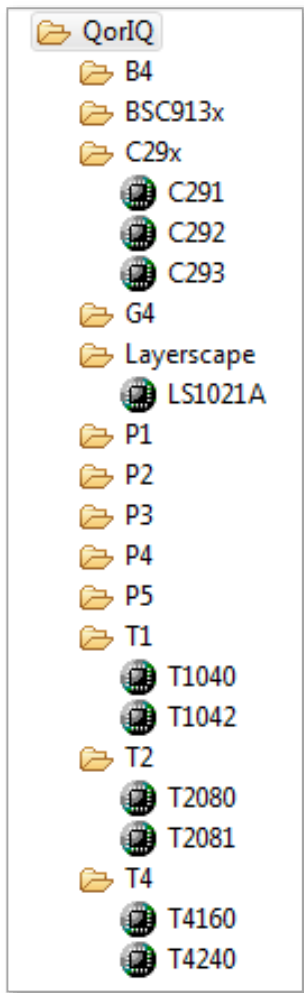
System Analysis
& Test



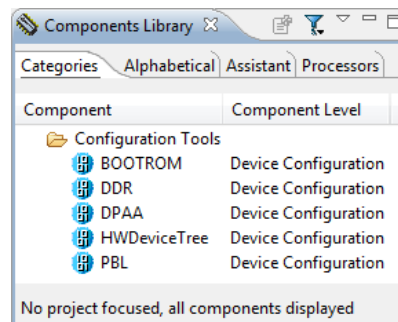
- CodeWarriorTAP :
 - Supports all PQ2Pro, PQ3 + QorIQ P1-5/T1/T4 + LS1
- Gigabit TAP :
 - Supports all PQ2Pro, PQ3 + QorIQ P1-5/T1/T4 + LS1
 - Optional Trace module with Aurora interface

CodeWarrior Development Studio & CodeWarrior Run Control Tools are essential tools for software development, architecture analysis and validation

QorIQ Configuration Suite



- No-cost configuration tool for QorIQ SoC platforms
- Generates source files for use in board initialization code
 - BOOTROM : platform configuration
 - DDR : DDR controller configuration
 - DPAA: graphical configuration of PCD alternate flow processing
 - HWDeviceTree : ePAPR device tree editor
 - PBL: Pre-Boot Loader configuration



QorIQ Optimization Suite - QoS

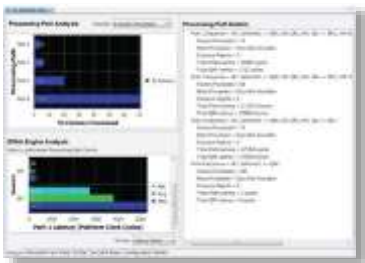
www.freescale.com/qos



- **DDR Validation Tool :**
Optimizes DDR controller configuration by automated memory testing with incrementally adjusted timings settings



- **Scenarios Tool :**
System level performance analysis using on-chip performance counters for DDR traffic, DMA performance, cache hits/misses,...



- **DPAA Packet Tool :**
Packet processing visualization based on data captured from DPAA IP blocks (FMan, QMan,...)

Technical Support



- Web based from
 - www.freescale.com
- Community from
 - community.freescale.com
- Distributors and Representative
- Local Freescale sales representative

Freescale provides custom support under contract

- Software Service
- Engineering Services
 - Schematic review
 - Software drivers port
 - Software optimization



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Export Control



All Freescale products are subject to the export control laws of the United States and the country from which the products are being exported.

Export classifications for Freescale products can be obtained on Freescale.com

http://www.freescale.com/files/corporate/doc/support_info/USER_CERT_2011_ECCN.pdf

Cryptography Export Control

http://www.freescale.com/webapp/sps/site/overview.jsp?code=NETWORK_SECURITY_EXPORT

If additional export information is needed please contact:
iecgrp1@freescale.com



Summary

- Freescale stands by a proven track record in Aerospace and Defense applications
- Freescale guarantees long term product supply
- Freescale offers technical support and design documentation for a variety of applications
- Freescale offers the broadest portfolio of solutions from microcontrollers to super computer-type processors
- Freescale is a “Best in Class” supplier for Aerospace and Defense applications





www.Freescale.com