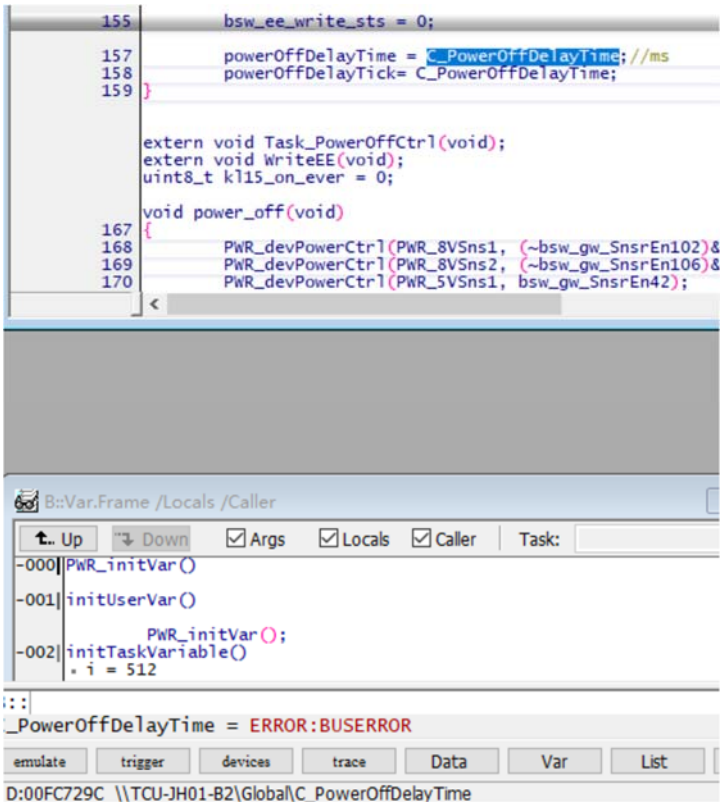
MPC5744P 标定区域读数据错误

问题：程序中读取 C_PowerOffDelayTime，其放在 FLASH 区域 cali_flash，在使用 smpu 配置后，出现 bus_error 错误，请问哪里设置有问题？

1. 程序



2. FLASH 分区

```
MEMORY
{
    flash_rchw        : org = 0x00FA0000,   len = 0x4
    cpu0_reset_vec    : org = 0x00FA0004,   len = 0x4

    eeprom_flash_bsw1 : org = 0x00800000, len = 16K     /*16KB,EEPROM-low block0, RWW_P:0*/
    eeprom_flash_bsw2 : org = 0x00804000, len = 16K     /*16KB,EEPROM-low block1, RWW_P:0*/
    eeprom_flash_boot : org = 0x00808000, len = 32K     /*32KB,EEPROM-mid block0, RWW_P:2*/
    eeprom_flash_asw  : org = 0x00810000, len = 4K      /*32KB,EEPROM-mid block1, RWW_P:3*/

    cali_flash        : org = 0x08FB0000, len = 128K        /*0x00FB_0000~0x00FC_FFFF*/

    cali_bsw          : org = 0x08FF0000, len = 64K     /*0x00FF_0000~0x00FF_FFFF*/
    m_text            : org = 0x01000000, len = 2048K   /*0x0100_0000~0x011F_FFFF*/
```

3. smpu 设置

```
void smpu_config(void) {

    SMPU_0.CESR0.B.GVLD = 0;                        // First ensure module disabled before confi

    // Configure Flash region
    SMPU_0.RGD[0].WORD0.R = 0x40000000;             // start address
    SMPU_0.RGD[0].WORD1.R = 0x4005FFFF;             // end address
    SMPU_0.RGD[0].WORD2.R = 0xFFFFFFFF;             // access control - all bus masters have RW a
    SMPU_0.RGD[0].WORD3.B.CI = 1;                   // Inhibit cache for this memory region
    SMPU_0.RGD[0].WORD3.B.VLD = 1;                  // region descriptor valid

    /* After SMPU initialization, any memory access to a location that is not protected by SMPU w
     * This inlcudes peripheral spaces, RAM, FLASH, everything that is used.
     * Demo uses SIUL2, MC_ME, PLLDIG, MC_CGM, DMA, and FLASH after this function is executed.
     * All these regions must be protected. Refer to memory map chapter of MPC574xP RM for more i
     * However, it is common practice to configure a region for the entire flash block and one fo
     * peripheral space.
     */
#if 1
    /* Configure large flash */
    SMPU_0.RGD[1].WORD0.R = 0x01000000;             //start address
    SMPU_0.RGD[1].WORD1.R = 0x01FFFFFF;             //end address
    SMPU_0.RGD[1].WORD2.R = 0xFFFFFFFF;             // all bus masters have RW control
    SMPU_0.RGD[1].WORD3.B.VLD = 1;                  // Cache init = 0. region descriptor valid
#endif

#if 1
    /* Configure peripheral space */
    SMPU_0.RGD[2].WORD0.R = 0x08FB0000;//0xF8000000;        //Start address of peripheral space
    SMPU_0.RGD[2].WORD1.R = 0x00020000;     //0xFFFFFFFF//End Address of peripheral space
    SMPU_0.RGD[2].WORD2.R = 0xFFFFFFFF;     //all bus masters have RW access to the region
    SMPU_0.RGD[2].WORD3.B.VLD = 1;          //Cache init = 0. Region is valid
#endif
    SMPU_0.CESR0.B.GVLD = 1;                        // Enable the module

}
```