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# MPC5777C-516DS

**Revisions**

Rev	Description	Date	Approved
X1	Initial Draft	09/18/13	David Erazmus
X2	Memory section updated (A070 release)	09/24/13	David Erazmus
X3	1. J23 changed as 1X2 header to sel only 3.3V 2. Transistor:Diode, changed from SQ2301 & SS8P3L to PMV65XP & STPS8L30B in 1.25V onboard reg section	09/26/13	David Erazmus
X4	1. Reset Section buffer updated and circuit modified to reduce a jumper	10/07/13	David Erazmus
X5	1. extra TP on net 1.25V_SR removed	10/14/13	David Erazmus
A	1. Back Annatated 2. A085 release	10/16/13	David Erazmus
AX1	1. Added SBC controller 2. Added 50Mhz clock 3. removed EBI group from MB conn 4. other small fixes	02/23/15	David Erazmus
B	Updated SBC to MC33908LAE Routed 50MHz CLK to MB, J501.20 Released to Agile, A085 Changed PN for C9 to 150-77590	04/07/15	David Erazmus
B1	Change R549 to 4.53K	07/13/15	Steve Harrington
B2	Updated Jumper defaults for J510 and J512 Cleaned up text for visibility	08/24/15	Ugarte Manuel
C	- changed J513 to a 2X3 type - added J13 between SBC_1V25 and 1.25V_SR - added note for C619.1 and R550.1 vs J13.1	08/27/15	Ugarte Manuel
C1	Updated info (schematic and/or tables) for: J504, J505, J511, J513, J523, J524	10/28/15	Catalin Neacsu
C2	Changed J13, J504, J511 to 100MIL type	10/28/15	Catalin Neacsu
C3	- Added J14 - Disconnected J501.30, J501.31, J501.32, J501.139 - Added R9, R11, TP1, TP2, TP32 and TP33	12/16/15	Catalin Neacsu
D	Updated with NXP logos	12/23/15	Catalin Neacsu

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ICAP Classification:		CP:	IUC: X PUBI:
Designer: Catalin Neacsu [nPro]	Drawing Title: <b>MPC5777C-516DS</b>		
Drawn by: Catalin Neacsu [nPro]	Page Title: <b>Table of Contents/Revisions</b>		
Approved: Manuel Ugarte	Size C	Document Number SCH-28088 PDF: SPF-28088	Rev D
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1. Unless Otherwise Specified:
  - All resistors are in ohms, 5%, 1/8 Watt
  - All capacitors are in uF, 20%, 50V
  - All voltages are DC
  - All polarized capacitors are aluminum electrolytic
2. Intruded lines coded with the same letter or letter combinations are electrically connected.
3. Device type number is for reference only. The number varies with the manufacturer.
4. Special signal usage:
  - \_B Denotes - Active-Low Signal
  - <> or [] Denotes - Vectored Signals
5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology

## DEFAULT JUMPER SETTINGS

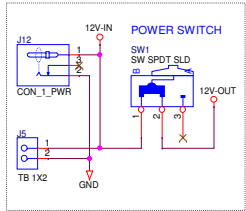
REFDES	Default settings	Description	Header	Jumper Type	Page
J1	2 & 3 (3.3V_MB)	3.3V SR Selection	HDR 1X3	2MM	3
J2	2 & 3 (5.0V_MB)	5V SR Selection	HDR 1X3	2MM	3
J18	2 & 3 (GND)	REGSEL to GND	HDR 1X3	2MM	5
J26	2 & 3	PM4 as PCSA2	HDR 1X3	2MM	5
J27	1 & 2	Reset Enable	HDR 1X2	2MM	7
J31	1 & 2 (3.3V)	JTAG VDD Selection	HDR 1X3	2MM	7
J32	2 & 3 (5.0V)	VDD_HV_IO_MAIN	HDR 1X3	2MM	8
J512	1 - 2	DEBUG PULL-UP	HDR 1X2	2MM	3
J502	1 & 2	LIN Master/Slave	HDR 1X2	2MM	3
J504	2 & 3	VCCA	HDR 1X3	2MM	3
J505	1 & 2	VCCA	HDR 1X2	2MM	3
J506	2 & 3	CAN RX	HDR 3X4	100MIL	3
	5 & 6	CAN TX			
	8 & 9	LIN RX			
	11 & 12	LIN TX			
J507	1 & 3	CAN	HDR 2X2	100MIL	3
	2 & 4	CAN			
J510	1 - 2	CLK SELECTION	HDR 1X3	2MM	5
J511	2 & 3	VDDIO	HDR 1X3	2MM	3
J517	2 - 3	SOUTB	HDR 3X6	100MIL	3
	5 - 6	SINB			
	8 - 9	SCKB			
	11 - 12	PCSB0			
	14 - 15	ANA4			
	16, 17, 18 OPEN	ETPUA10			
J518	OPEN	IO_[0:5]	HDR 2X6	100MIL	3
J519	OPEN	IO_1_PD	HDR 1X2	2MM	3
J520	1 - 2	LED En ETPUA0	HDR 1X2	2MM	5
J521	1 - 2	LED En ETPUA1	HDR 1X2	2MM	5
J523	OPEN	SBC_INT	HDR 2X2	100MIL	3
	OPEN	SBC_RST			
J524	2 & 3	CLOCK	HDR 1X3	2MM	3



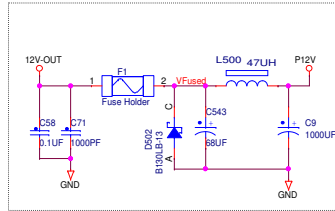
# Power supply : Connectors and Regulators

## Test and reference points

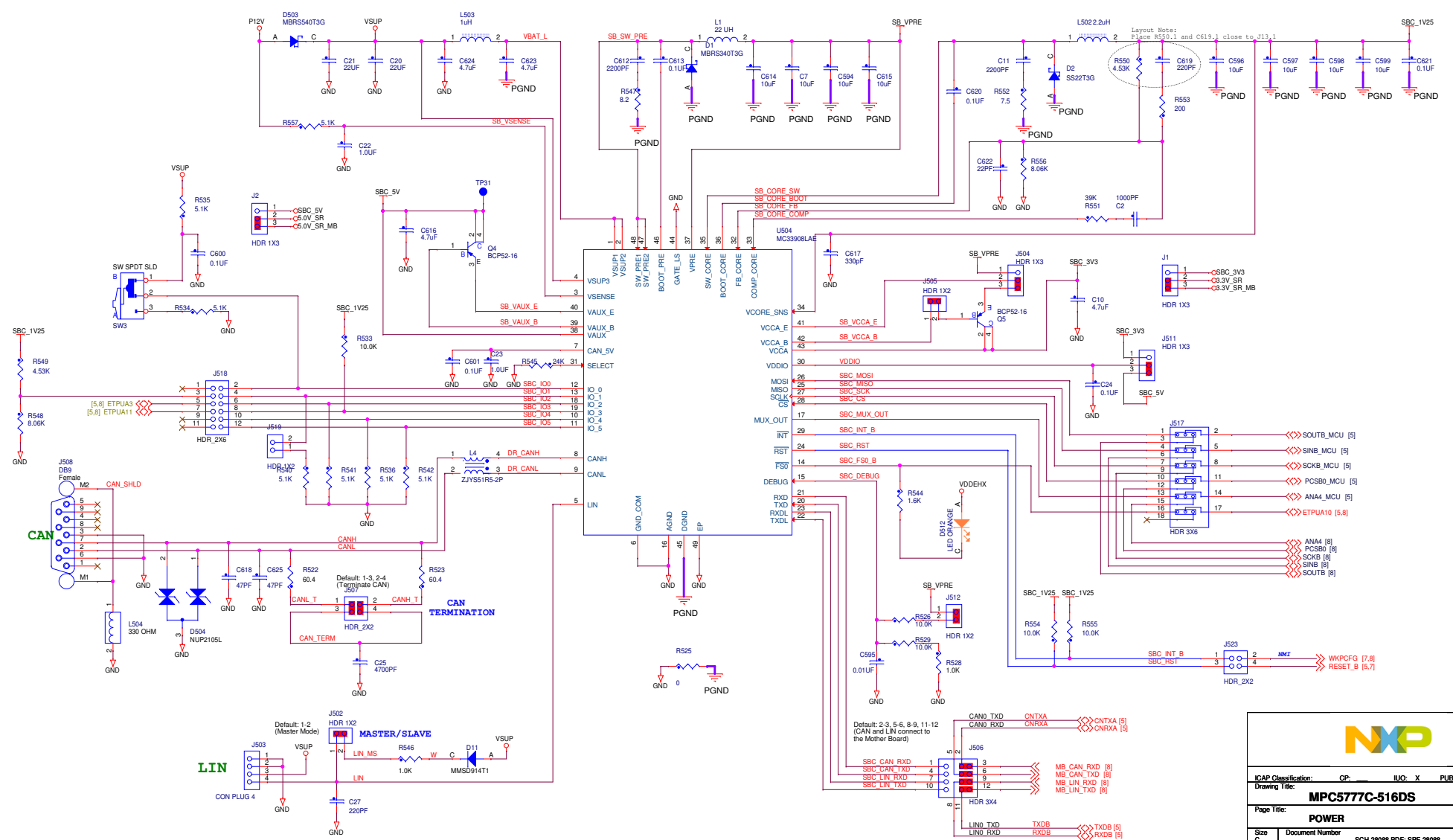
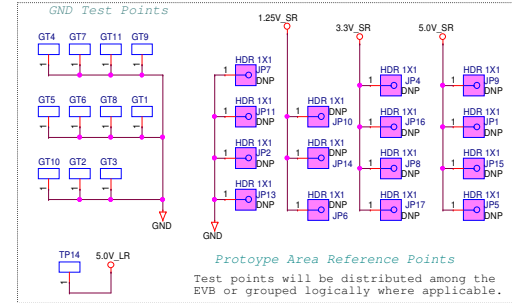
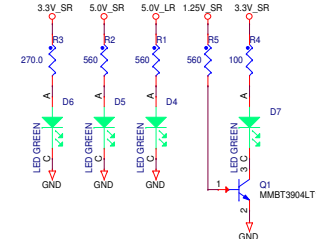
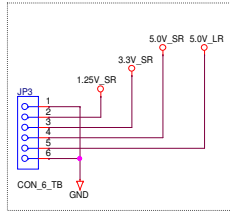
### Input Power Connectors



### Power supply input and filter



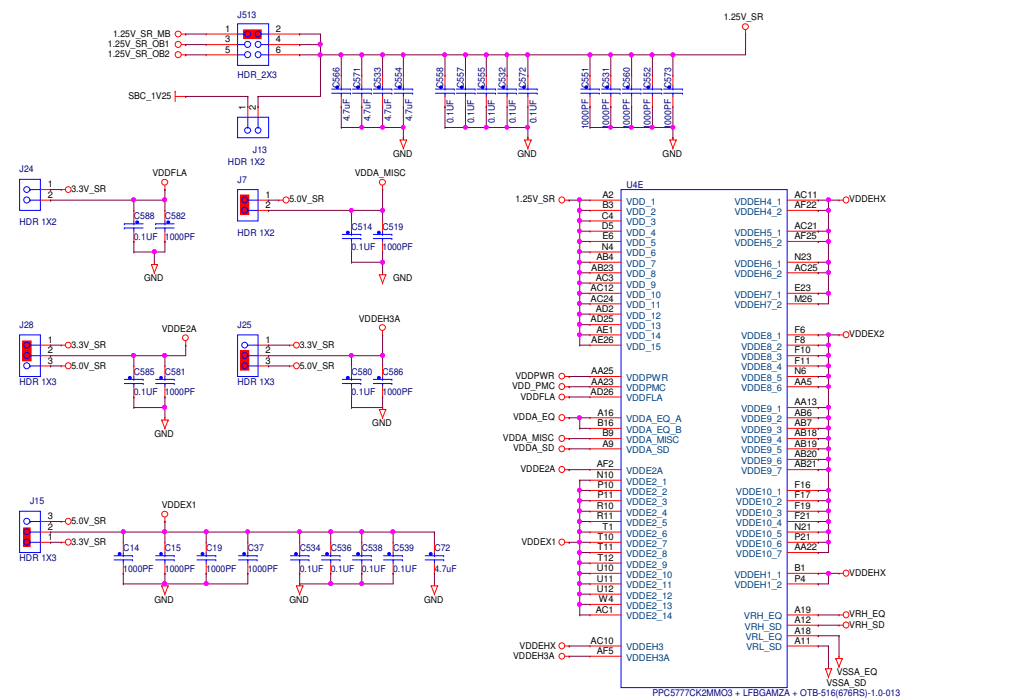
### External Power feed



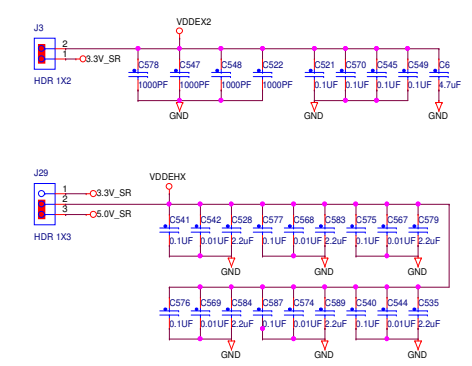
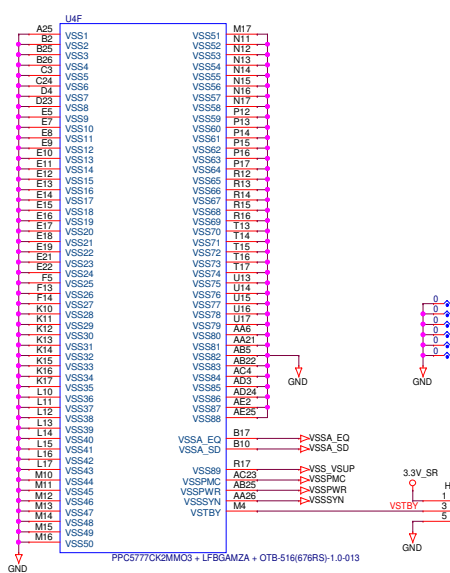
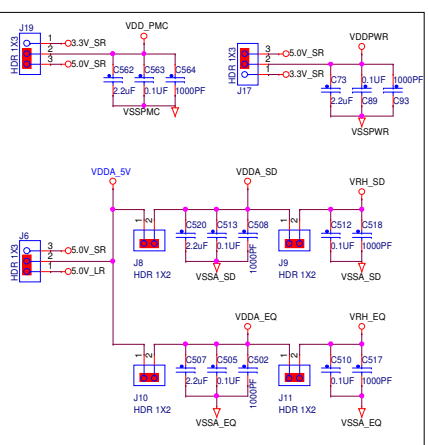
ICAP Classification: CP: IUC: X PUB:	
<b>Drawing Title:</b>	
<b>MPC577C-516DS</b>	
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<b>POWER</b>	
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# MCU Power and 1.2V Regulator

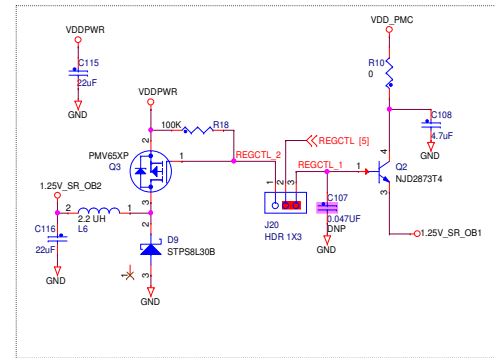
## DEFAULT JUMPER SETTINGS



REFDES	Default settings	Description	Header	Jumper Type	Page
J3	1 & 2	VDDDE8,9,10 Select	HDR 1X2	2MM	4
J4	2 & 3 (CS#1)	SRAM Chip Select	HDR 1X3	2MM	4
J6	1 & 2 (5.0V_LR)	VDDA Selection	HDR 1X3	2MM	4
J7	1 & 2 (5.0V)	VDDA_MISC Select	HDR 1X2	2MM	4
J8	1 & 2	VDDA_SD Selection	HDR 1X2	2MM	4
J9	1 & 2	VRH_SD Selection	HDR 1X2	2MM	4
J10	1 & 2	VDDA_EQ Selection	HDR 1X2	2MM	4
J11	1 & 2	VRH_EQ Selection	HDR 1X2	2MM	4
J13	OPEN	SBC_1V25<->1.25V_SR	HDR 1X2	100MIL	4
J15	1 & 2 (3.3V)	VDDDE2 Selection	HDR 1X3	2MM	4
J16	3 & 5 (GND)	VSTBY Selection	HDR 2X3	2MM	4
J17	2 & 3 (5V)	VDDPWR Selection	HDR 1X3	2MM	4
J19	2 & 3 (5.0V)	VDDPMC Selection	HDR 1X3	2MM	4
J20	2 & 3	REGCTL-1.25V_OB1	HDR 1X3	2MM	4
J24	OPEN	VDDFLA Selection	HDR 1X2	2MM	4
J25	2 & 3 (5.0V)	VDDEH3A Selection	HDR 1X3	2MM	4
J28	1 & 2 (3.3V)	VDDE2A Selection	HDR 1X3	2MM	4
J29	2 & 3 (5.0V)	VDDEHX Selection	HDR 1X3	2MM	4
J513	1 & 2	1.25V_SR_MB	HDR 2X3	100MIL	4



### Onboard 1.25V Switching Regulator



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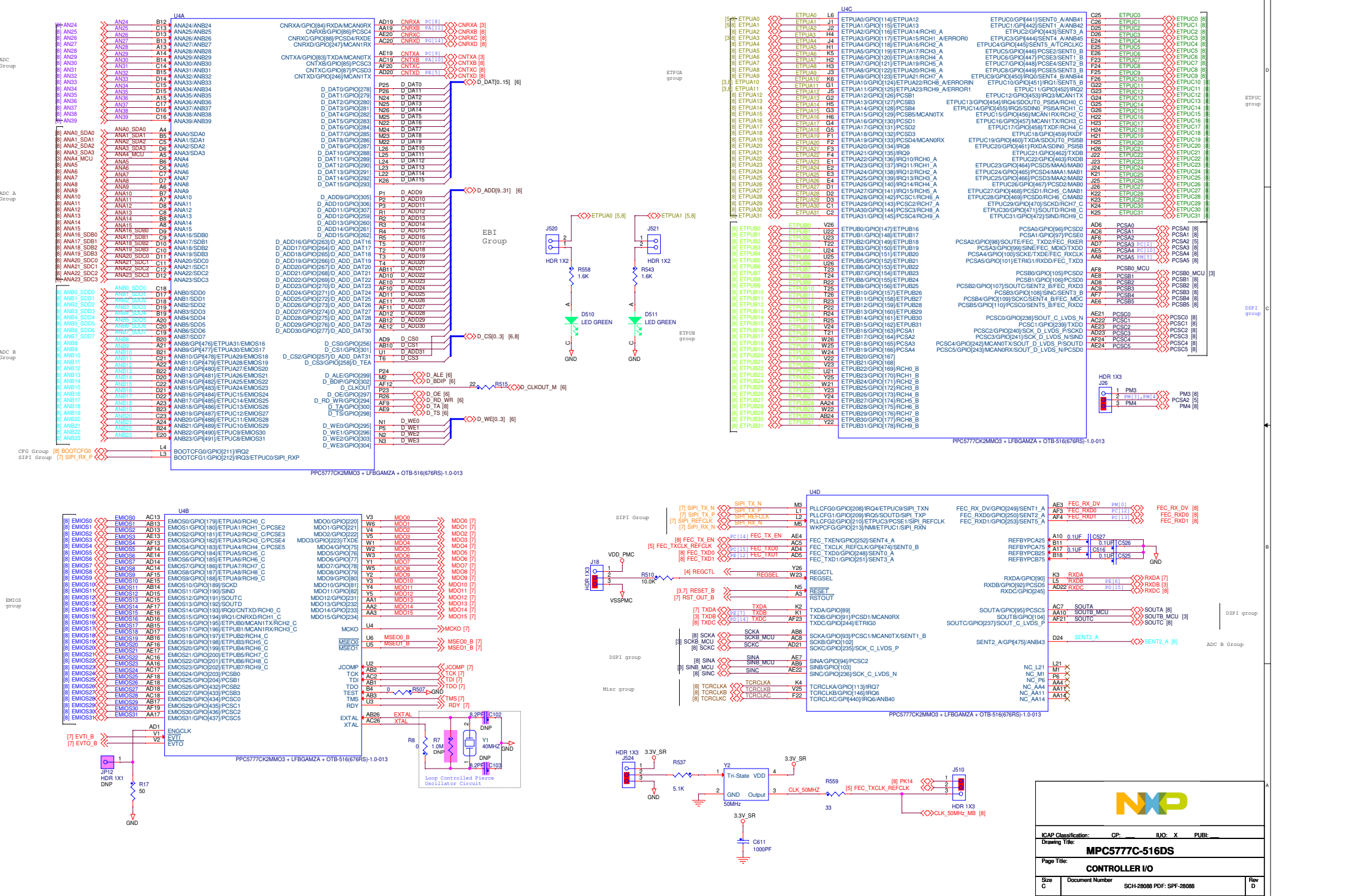
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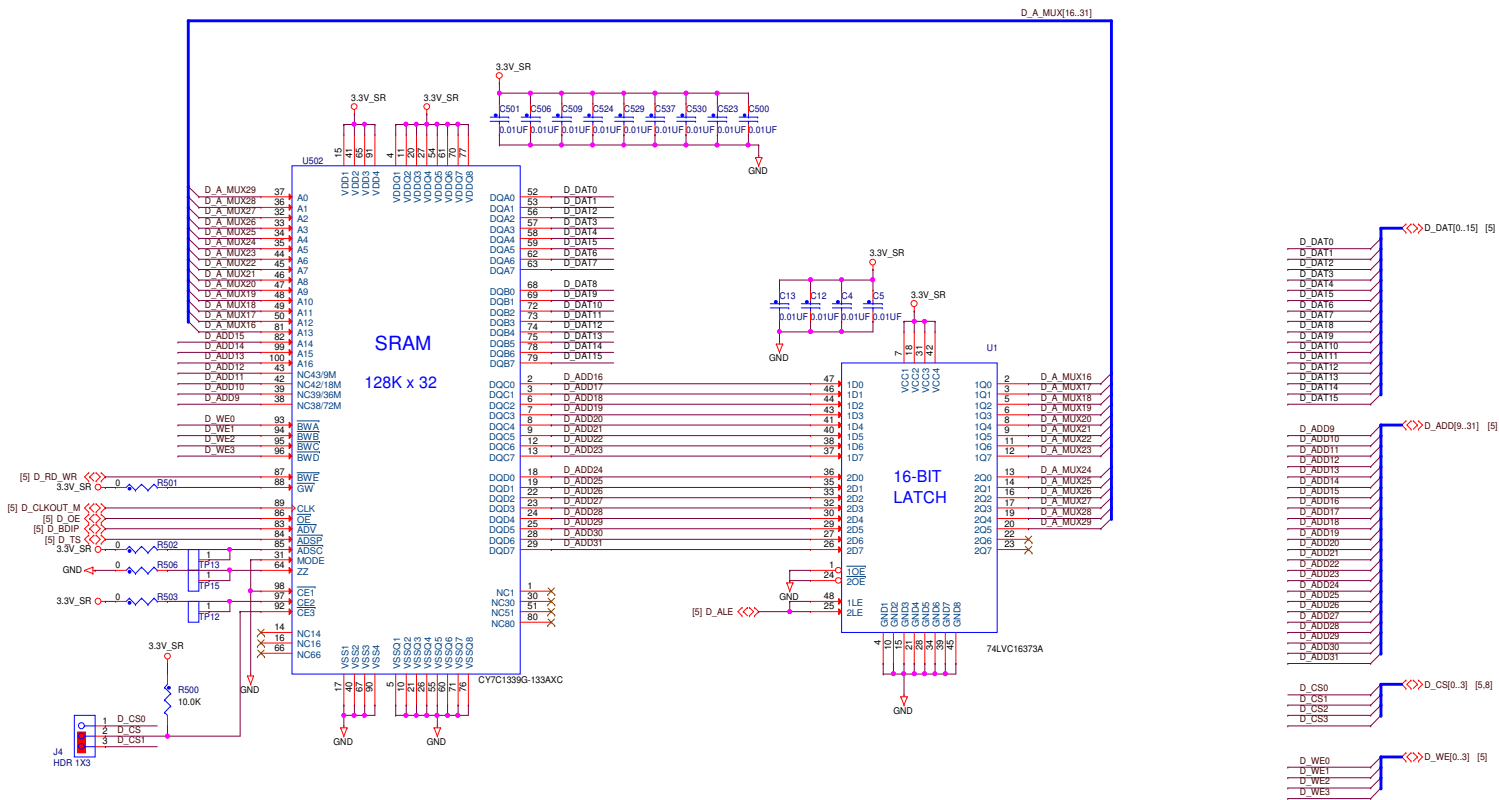
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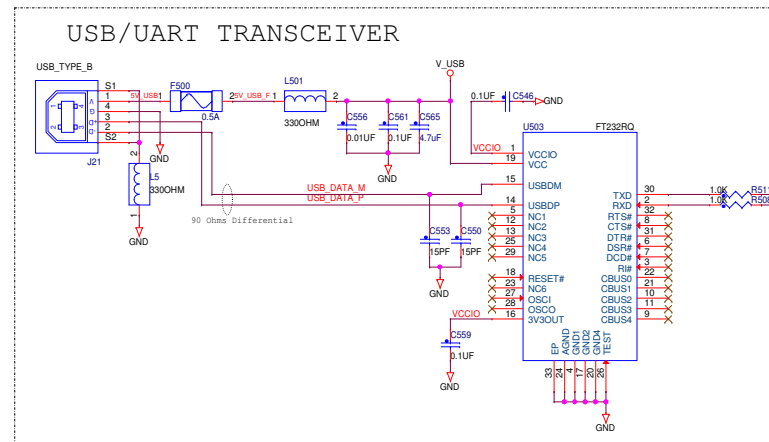
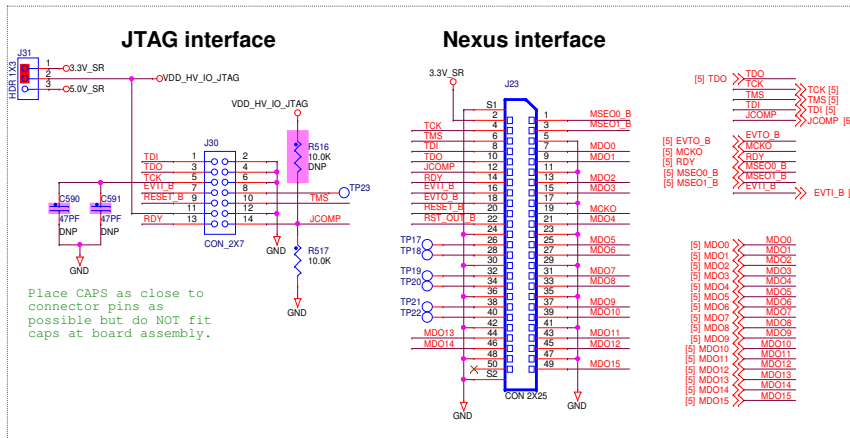
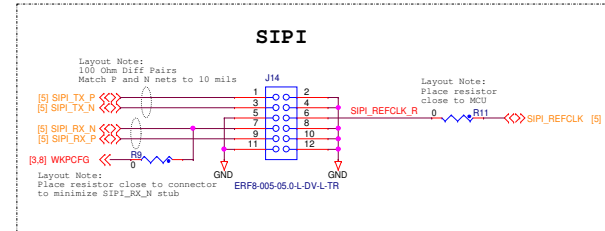
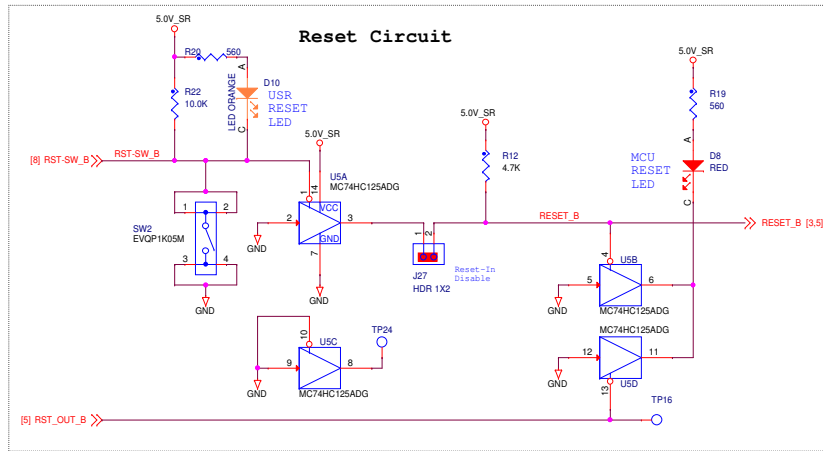
# CONTROLLER I/O



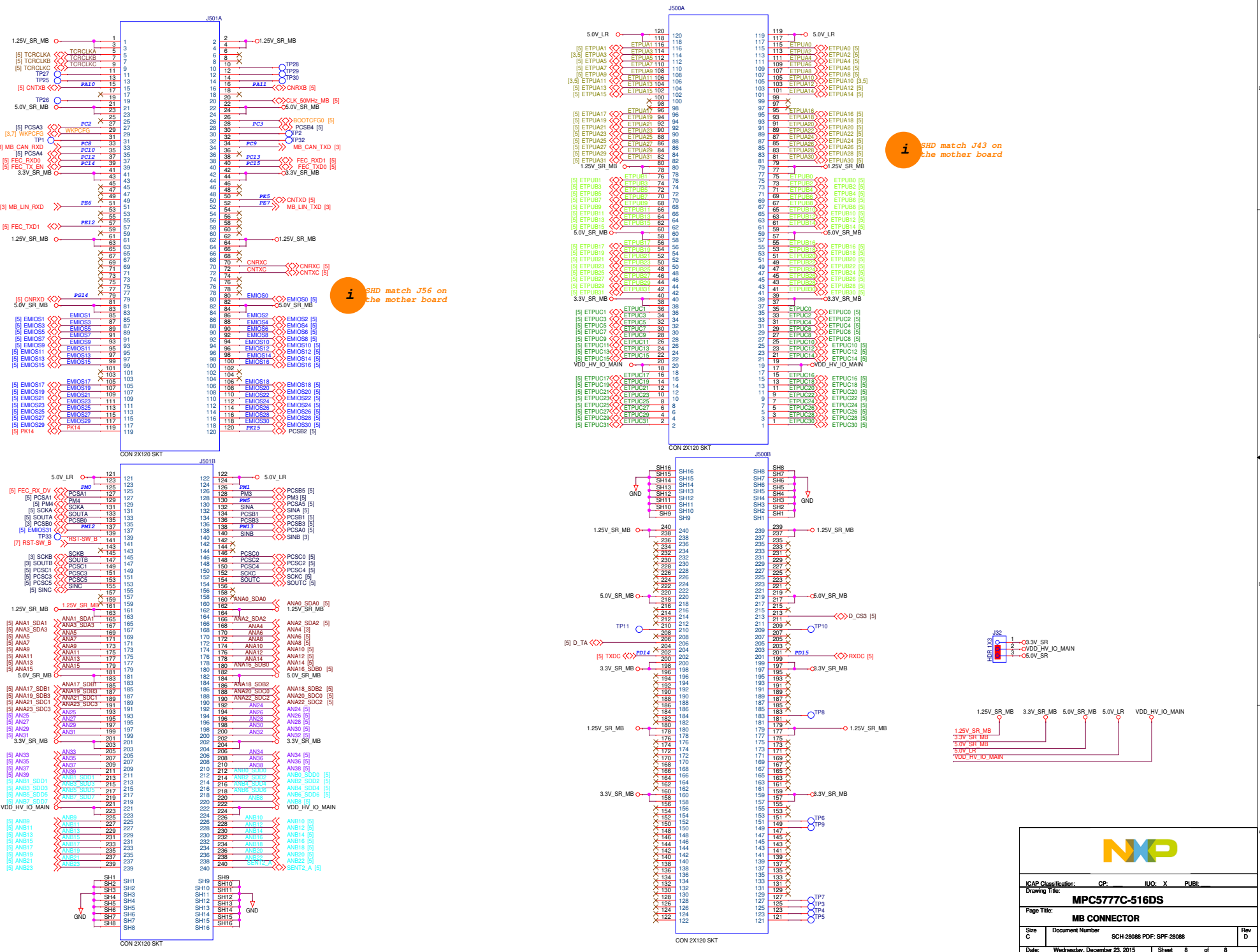
# ON BOARD MEMORY



# RESET, JTAG, NEXUS, SIPI & UART



# DAUGHTER CARD TO MOTHERBOARD CONNECTOR



**i** SHD match J43 on the mother board

**i** SHD match J56 on the mother board

**NXP**

ICAP Classification: CP IUC X PUBL

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Page Title: **MB CONNECTOR**

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