

S32K142EVB-Q100

CUSTOMER EVB

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Revisions				
Rev	Description	Designer	Date	Approved
X1	Draft	J.Sanchez		
C		J.Sanchez	11/09/17	
D	Final Release	J.Sanchez	18/09/17	

CAUTION:

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3 Different test points used in design:

TPVx - Through Hole Pad small

TPHx - Through Hole Pad Large (for standard 0.1" header). Also used on IO Matrix (IOMx)

TPX - Surface Mount Wire Loop

TPV?

TPH5

TP?


Notes:

- All components and board processes are to be ROHS compliant
- All connectors and headers are denoted Jx/Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2.
- 2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

Signals (ports) have not been routed via busses as this makes it harder to determine where each signal goes.

User notes are given throughout the schematics.

Specific PCB LAYOUT notes are detailed in *ITALICS*

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Designer: Jesus Sanchez		Drawing Title: S32K142EVB-Q100	
Drawn by: Jesus Sanchez		Page Title: TITLE PAGE	
Approved: Ricardo Olivares	Size B	Document Number SCH-29701 PDF: SPF-29701	Rev D
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1. Unless Otherwise Specified:

- All resistors are in ohms, 1% and 5 %
- All capacitors are in uF, 10% , 20 % and 5%
- All voltages are DC
- All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:

- _B Denotes - Active-Low Signal
- <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.



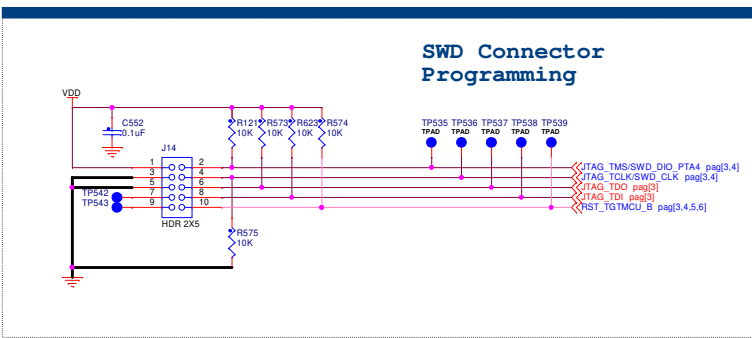
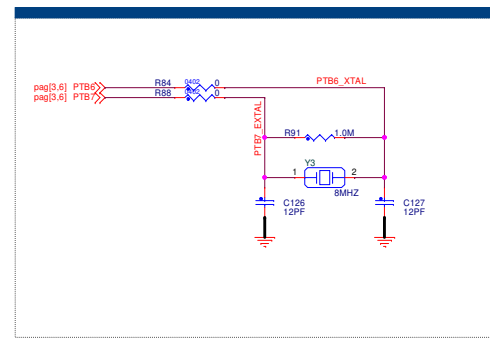
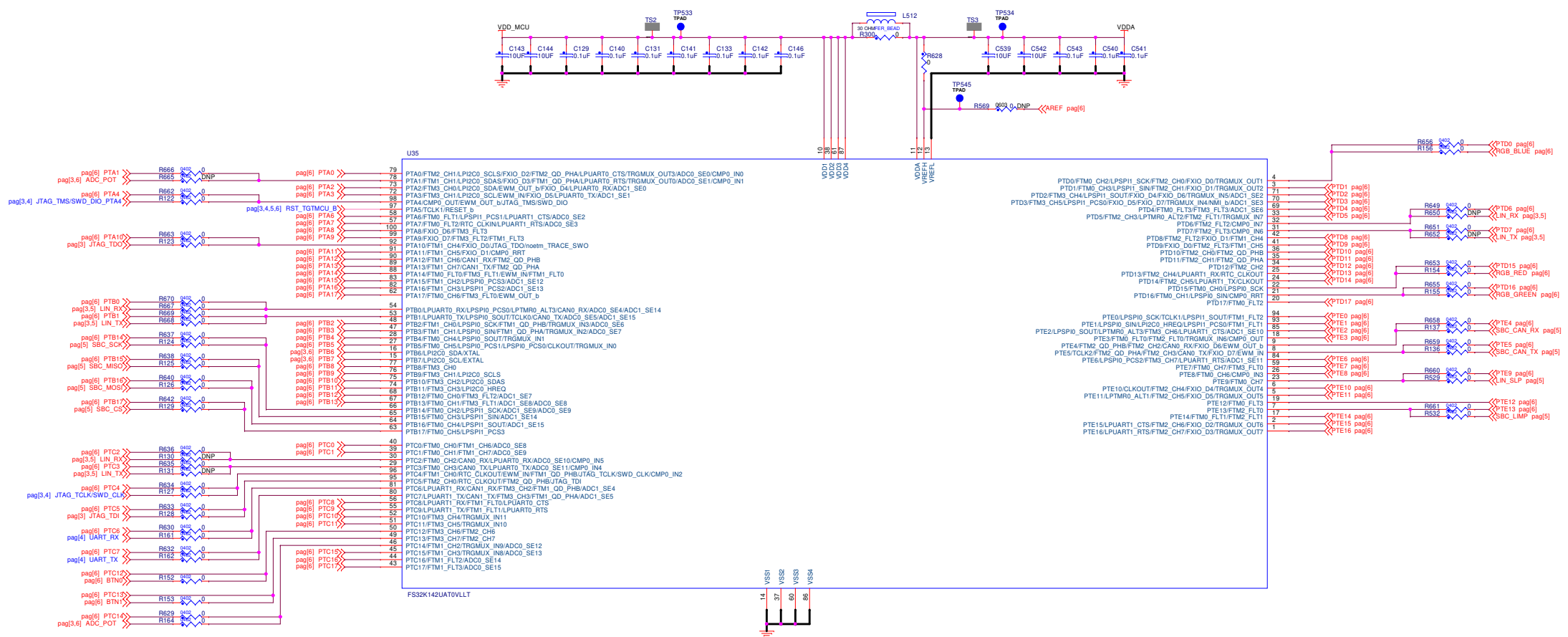
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S32K142EVB-Q100

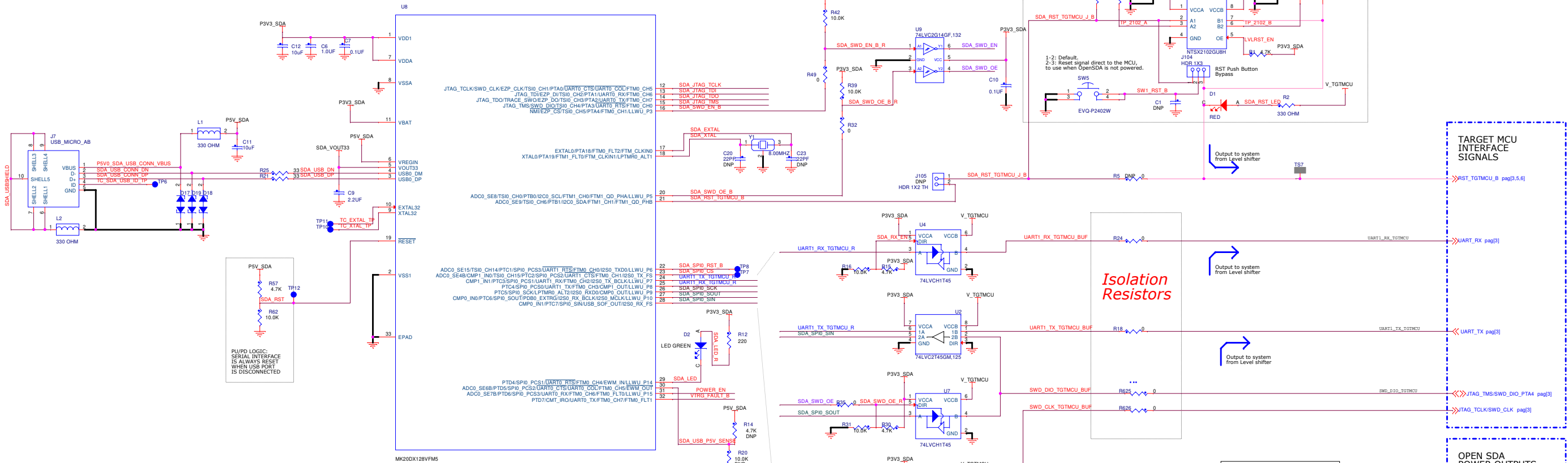
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Notes and Block Diagram

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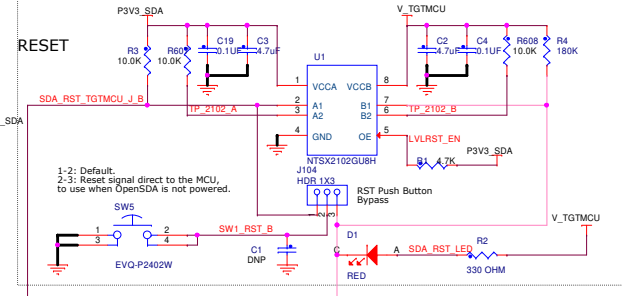
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OpenSDA Interface



PLUPD LOGIC: SERIAL INTERFACE IS ALWAYS RESET WHEN USB PORT IS DISCONNECTED



Isolation Resistors

OPEN SDA INPUT POWER

P3V3_SDA ← i path

3.3VDC, 10mA should be provided to this rail (P3V3_SDA) in order to power openSDA module

OPEN SDA POWER OUTPUTS

SDA_VOUT33 ← i path

PSV_SDA_PSW ← i path

Note: You can power openSDA with your own power supplies by replacing this rail (SDA_VOUT33) with your 3.3V power supply rail

SDA_VOUT33 can provide up to 120mA of power at 3.3VDC to your system

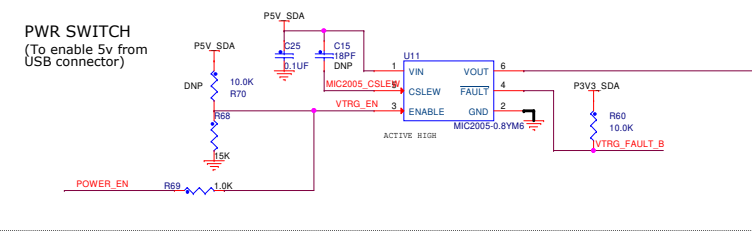
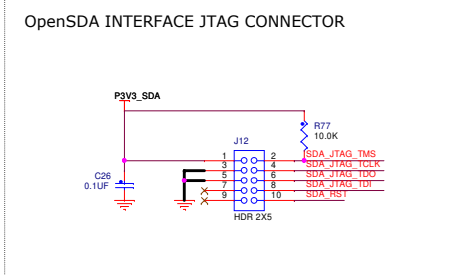
PSV_SDA_PSW can provide up to 450mA (per USB spec) of power at 5VDC to your system

I/O POWER INPUT

V_TGTMCU ← i path

V_BRD is supported from 1.8V to 5V

Power should be provided to this rail for the logic related to your platform I/O

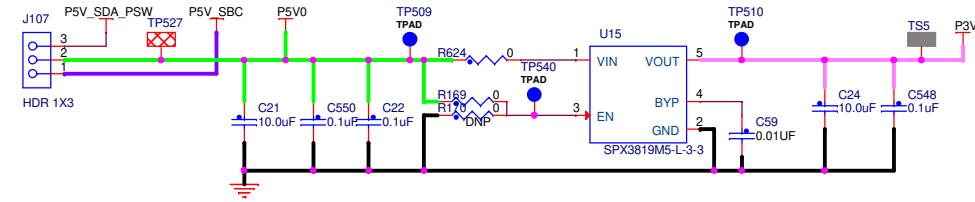


Isolation and level shift stage (for 1.8 to 5V compatibility)

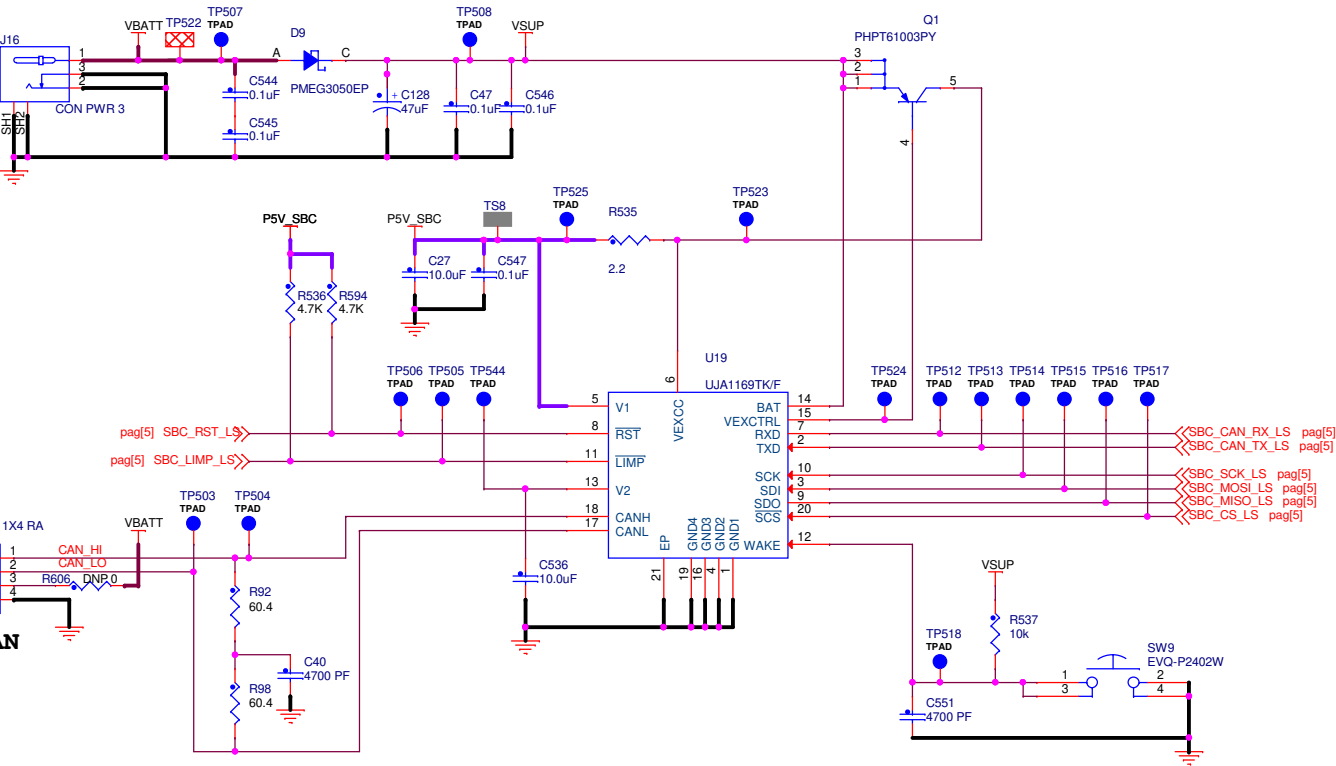
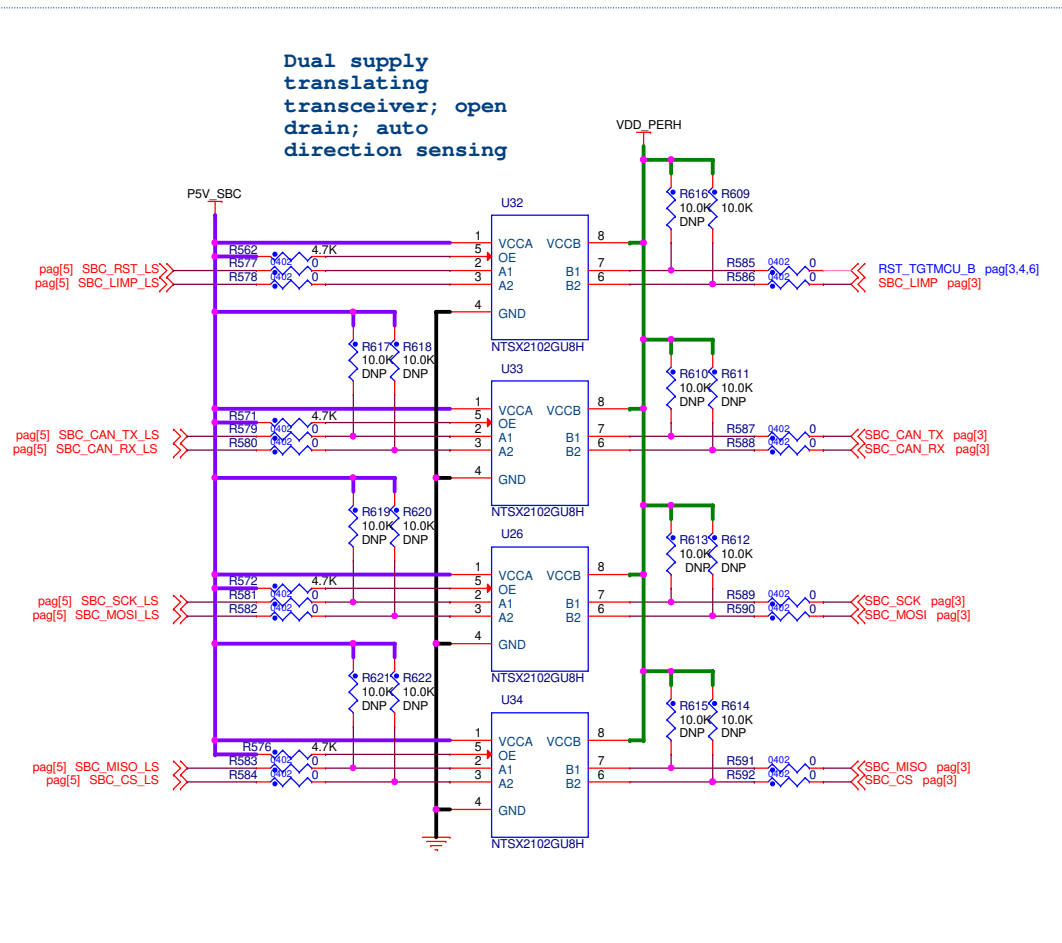
SDA_SPI0_RST_B R41 DNP 0 SDA_SWD_EN
SDA_SPI0_CS R38 DNP 0 SDA_SWD_OE

{For enablement purposes only}

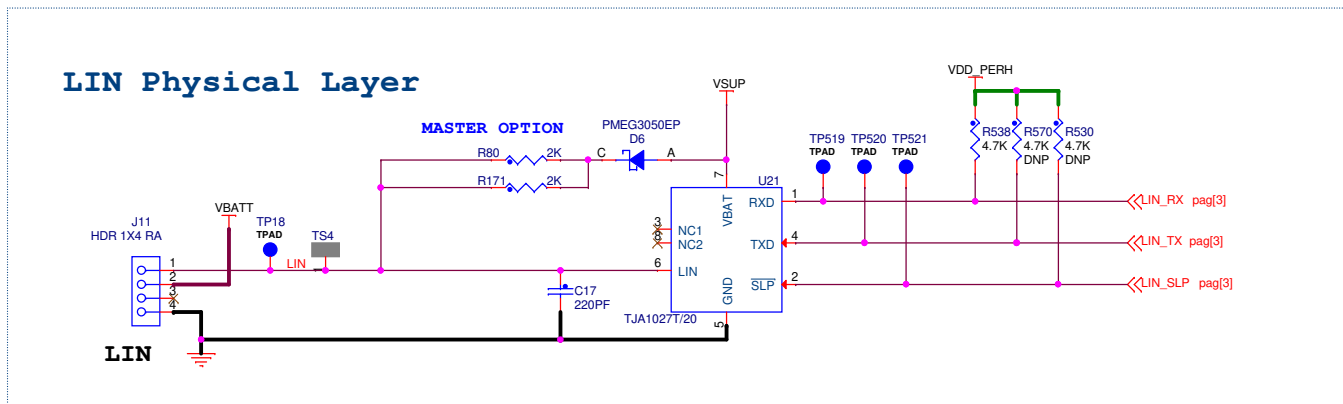
3.3V LDO Power Supply



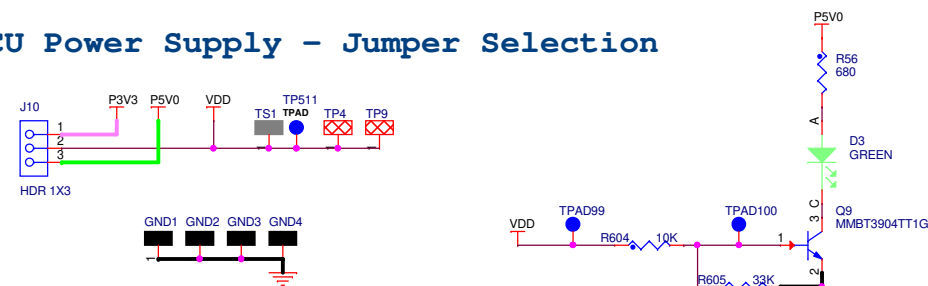
Dual supply translating transceiver; open drain; auto direction sensing



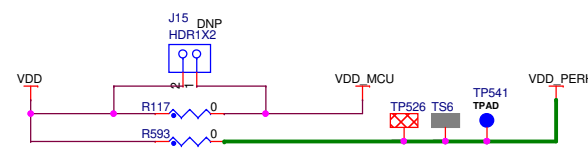
LIN Physical Layer



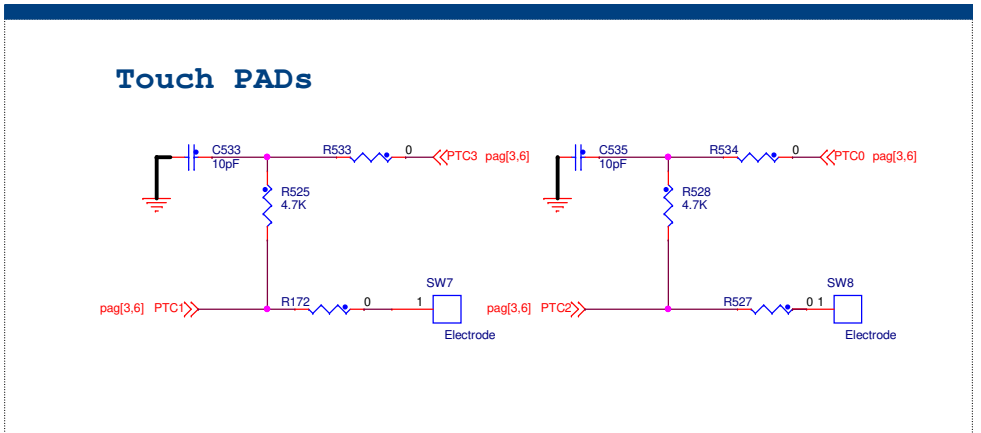
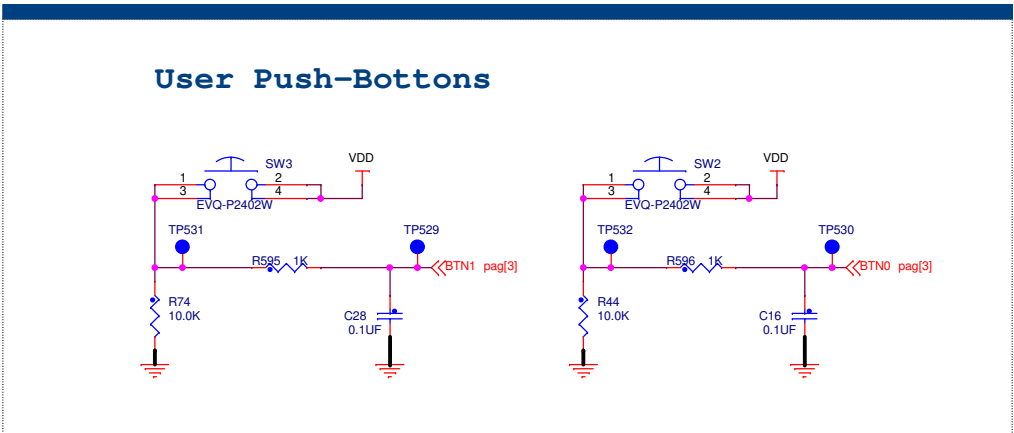
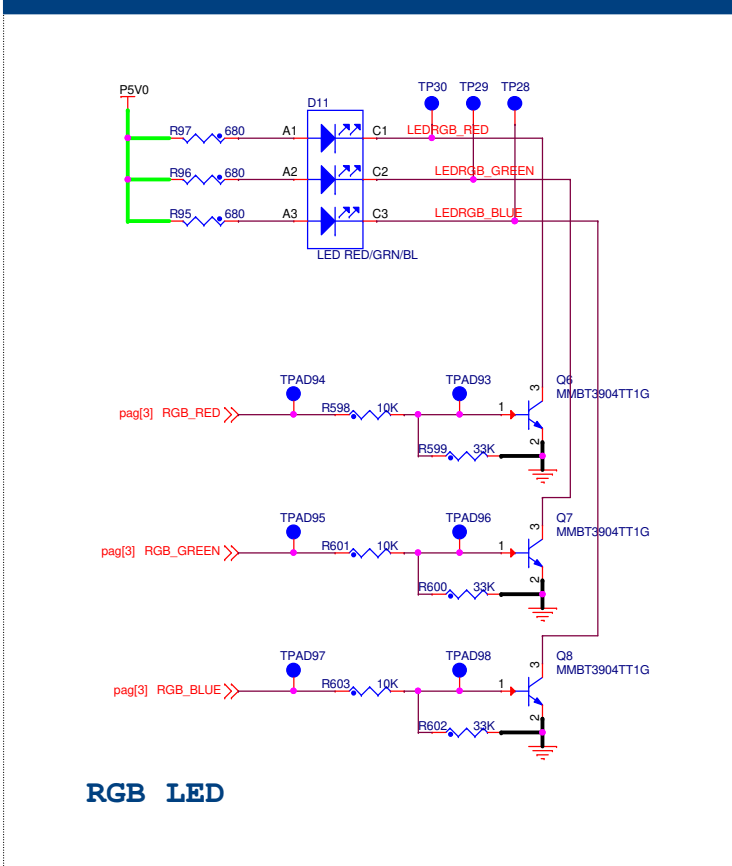
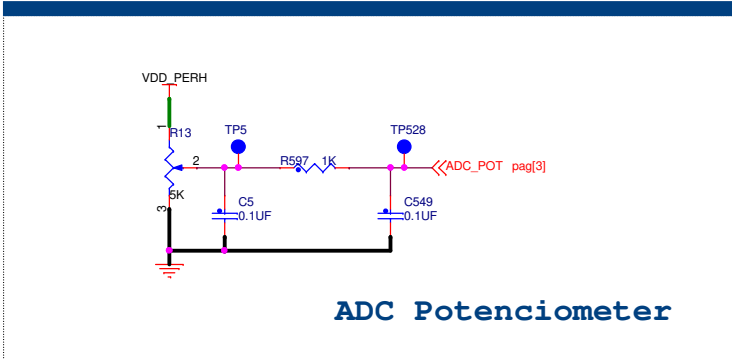
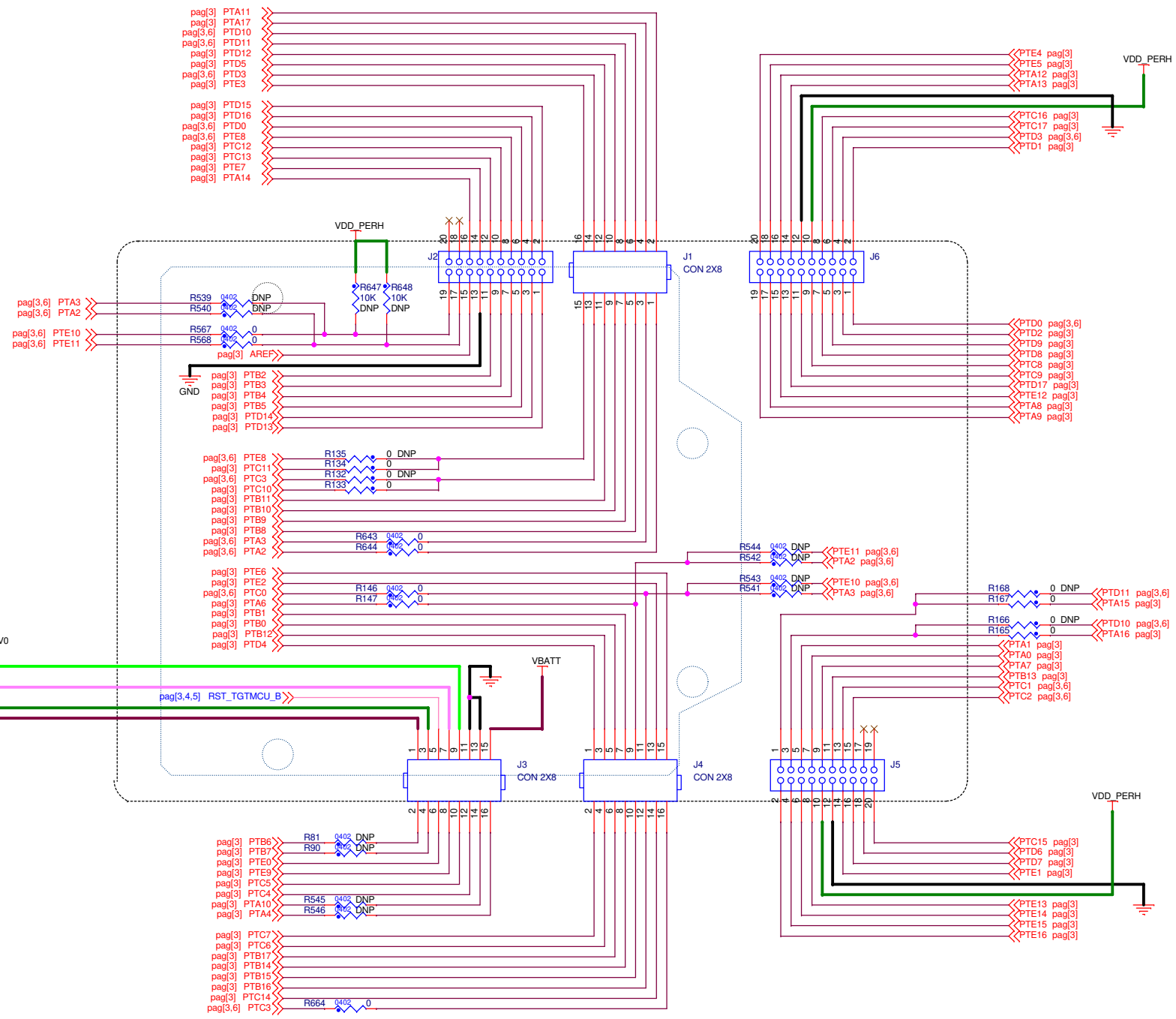
MCU Power Supply - Jumper Selection



MCU Current Measurement



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