

Revision History		
Rev. Code	Date	Description
E	03/30/2018	Preliminary Conversion from Mentor Design Capture

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**LPC546xx/540xx Development brd**

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San Jose, CA 95134

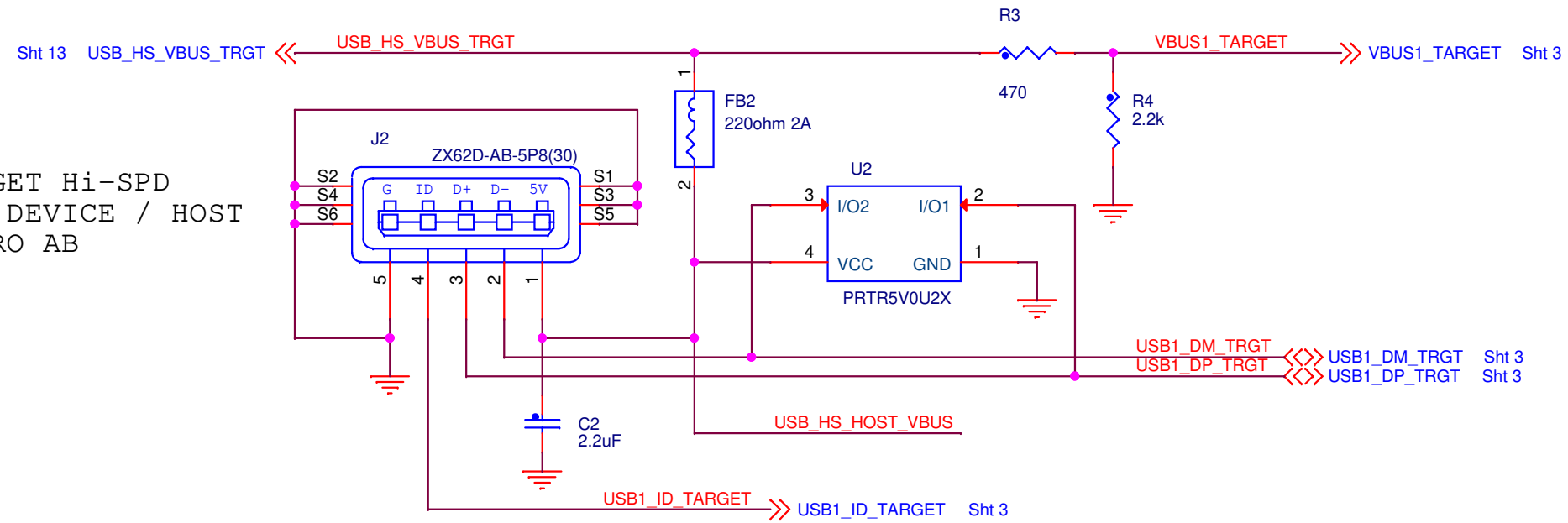
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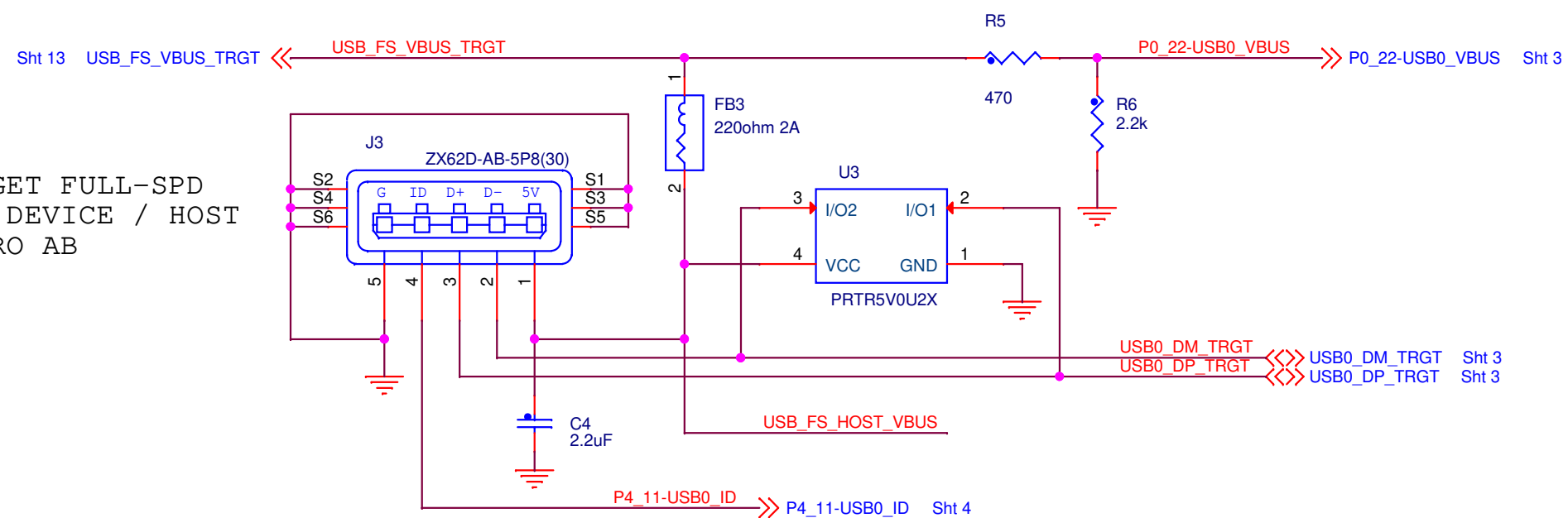
Designer: <Designer>	Drawing Title: <b>LPC546XX / LPC540XX BRD</b>
Drawn by: <DrawnBy>	Page Title: <b>BLOCK DIAGRAM</b>
Approved: <Approver>	Size C Document Number SCHM-LPC546/540XX
Date: Monday, April 02, 2018	Rev E

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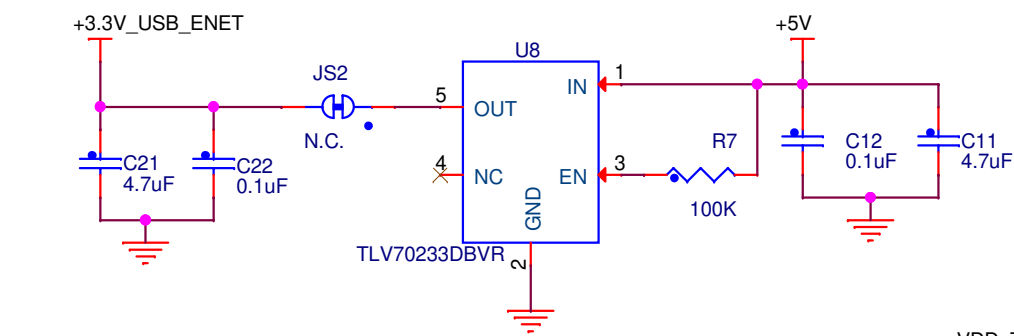
TARGET Hi-SPD  
USB DEVICE / HOST  
MICRO AB



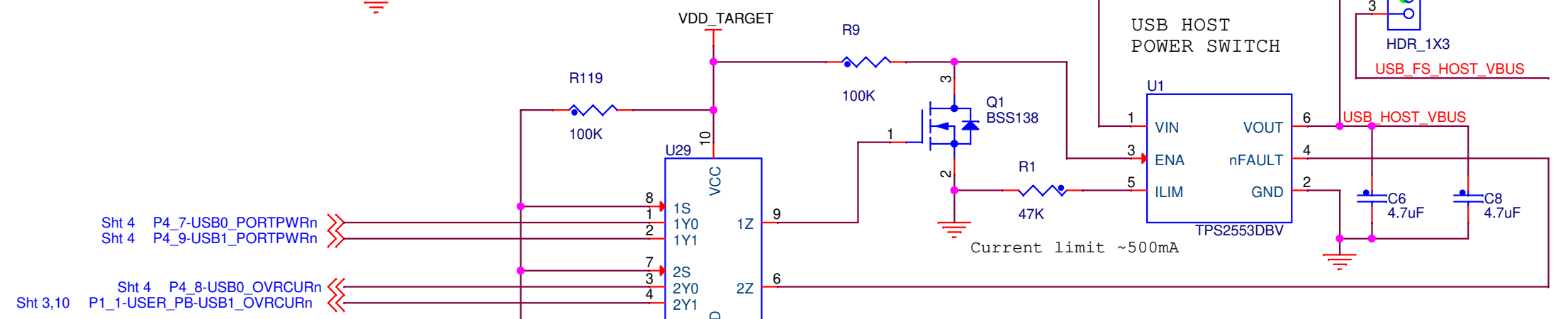
TARGET FULL-SPD  
USB DEVICE / HOST  
MICRO AB



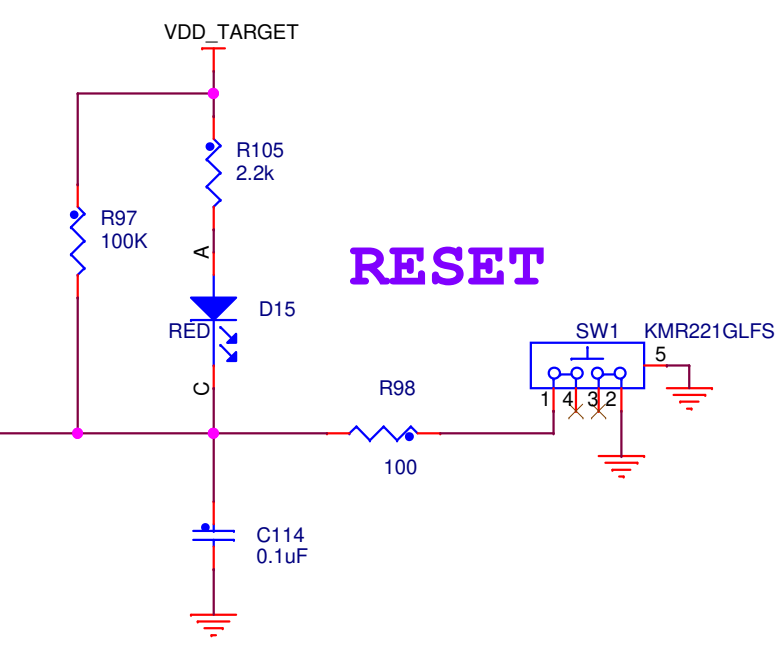
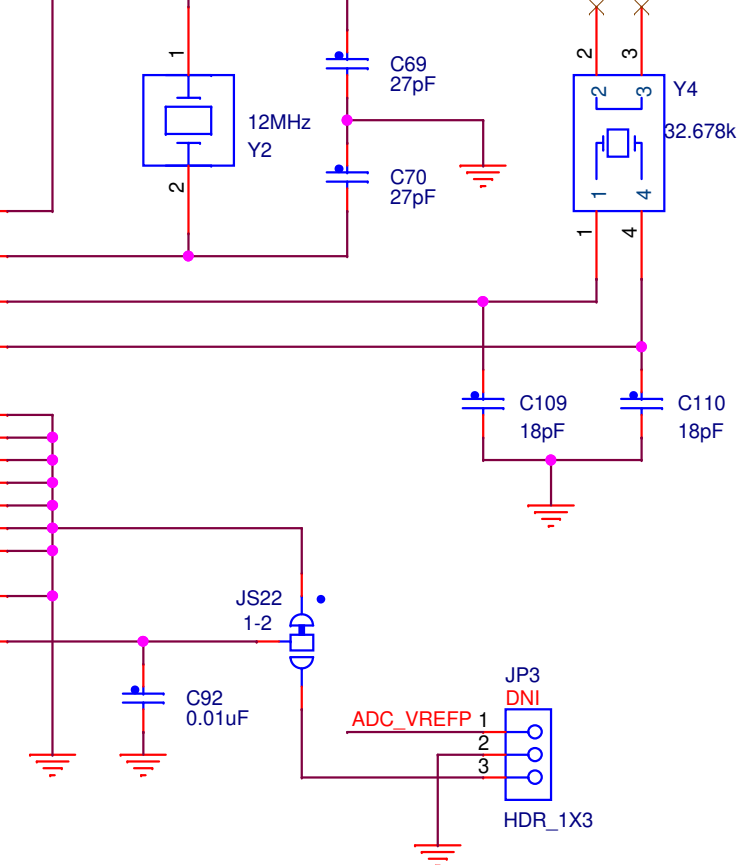
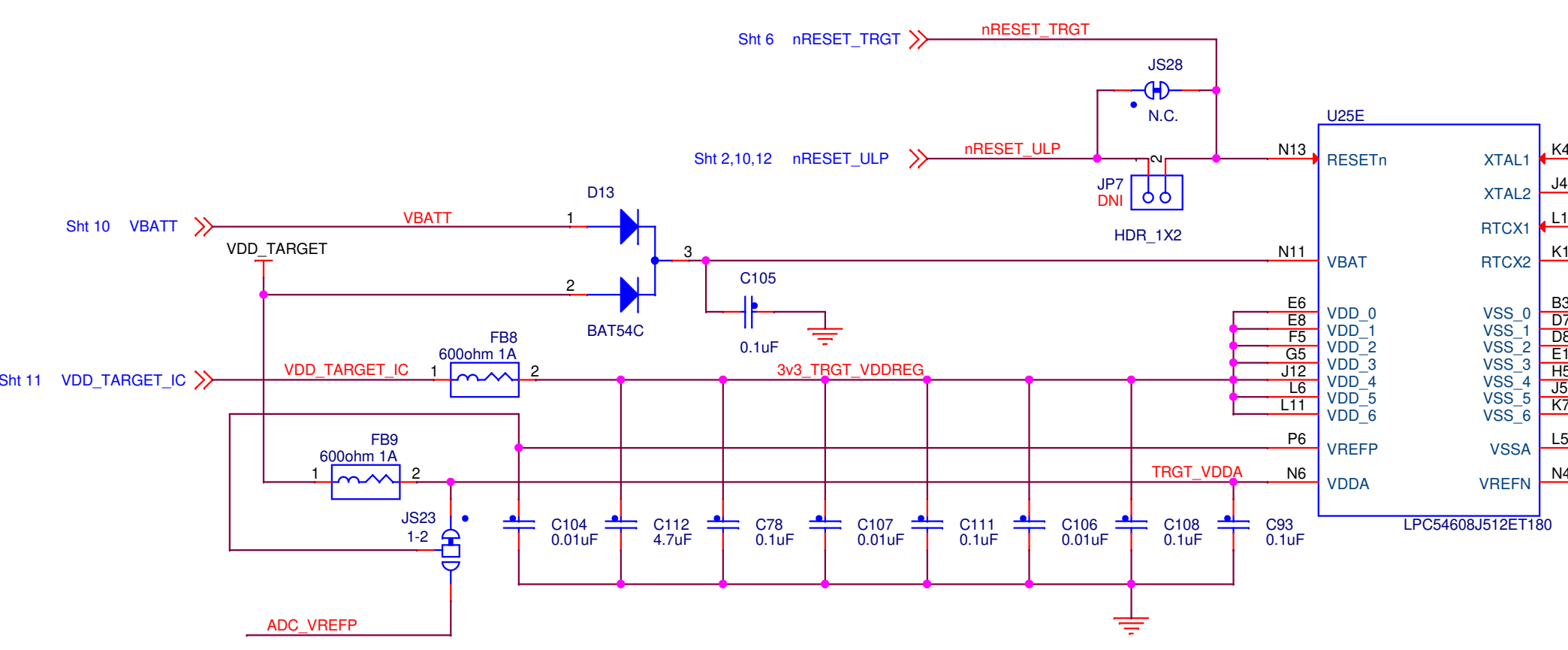
TARGET USB HS / ENET +3.3V POWER



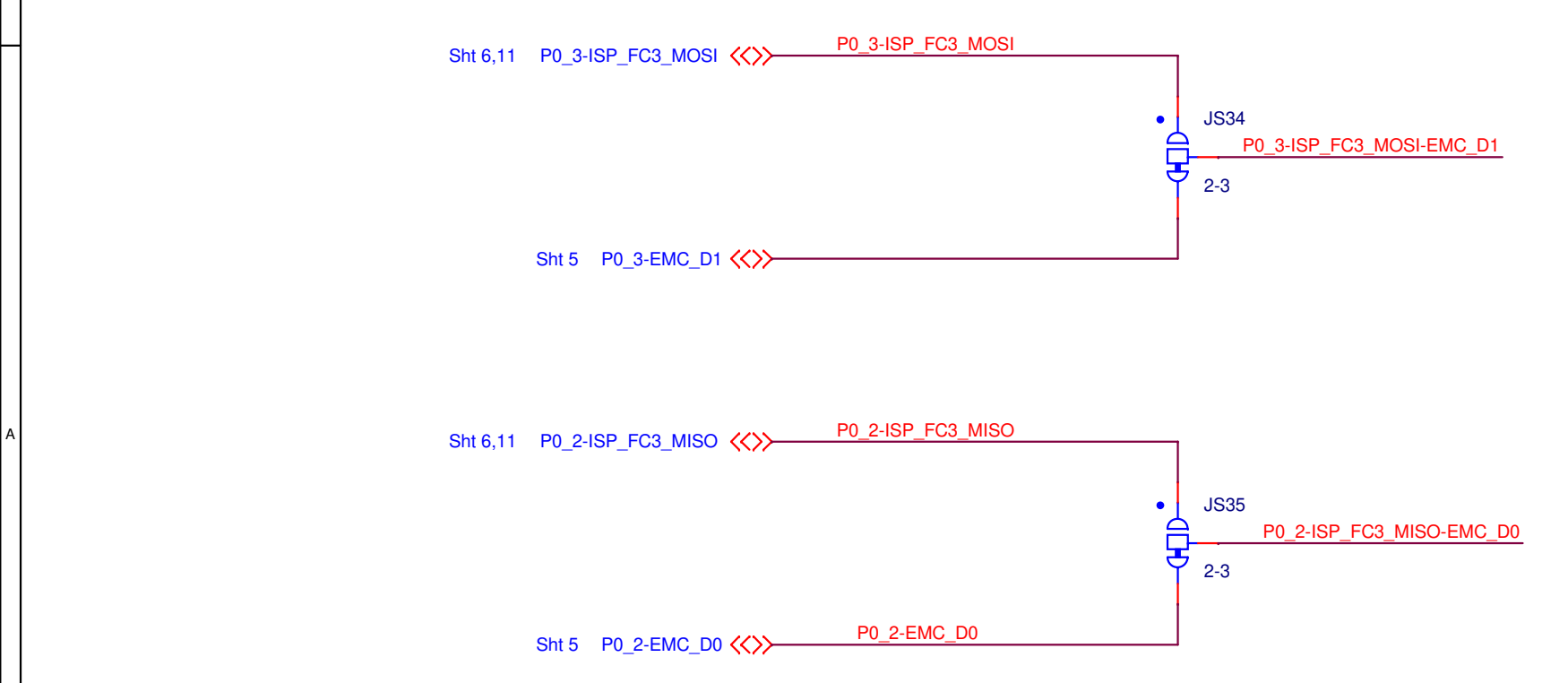
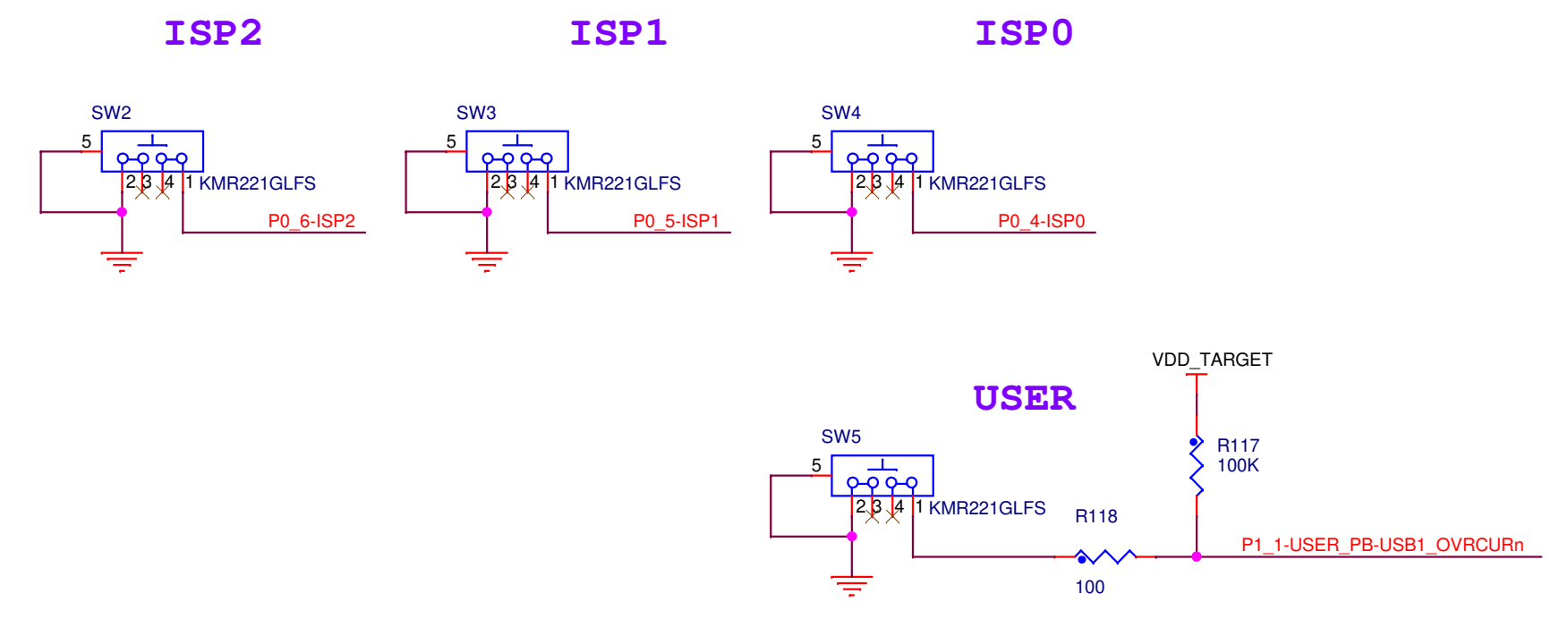
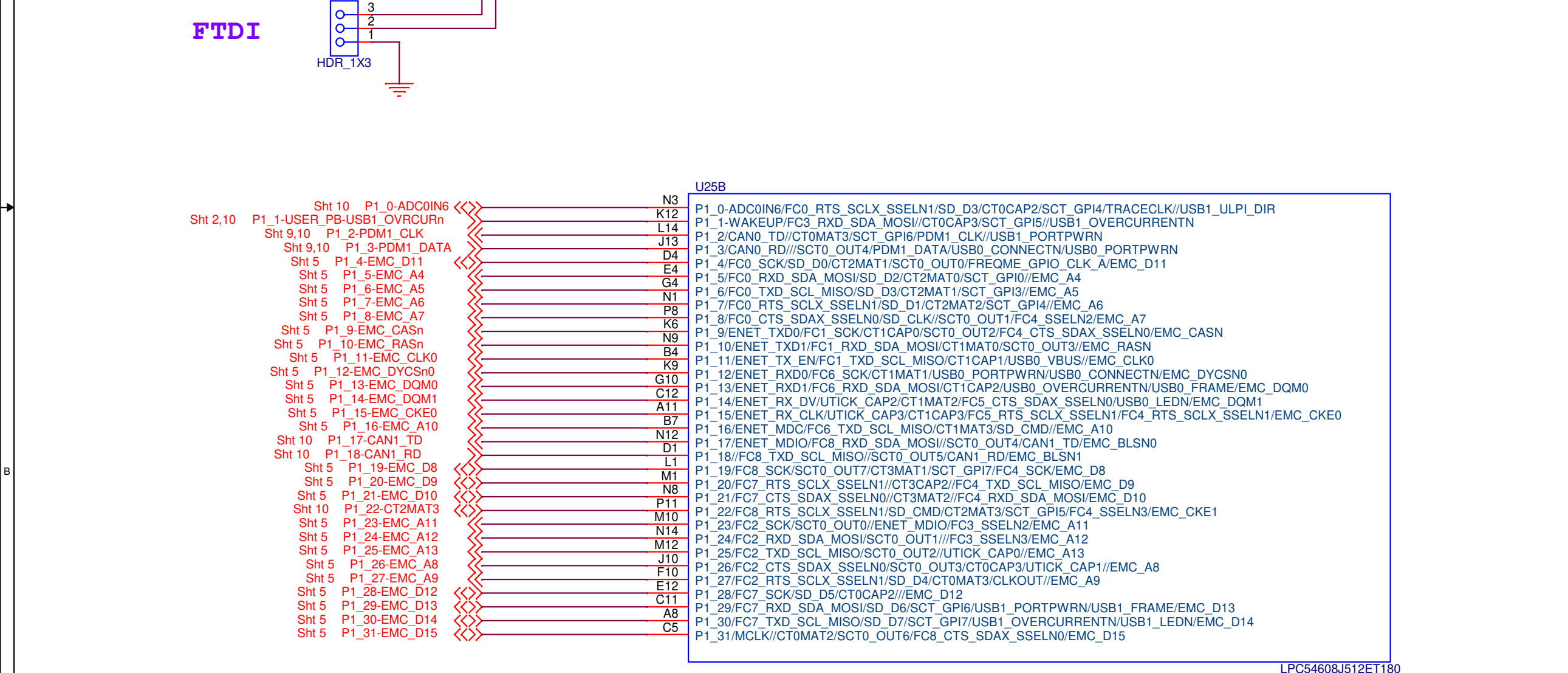
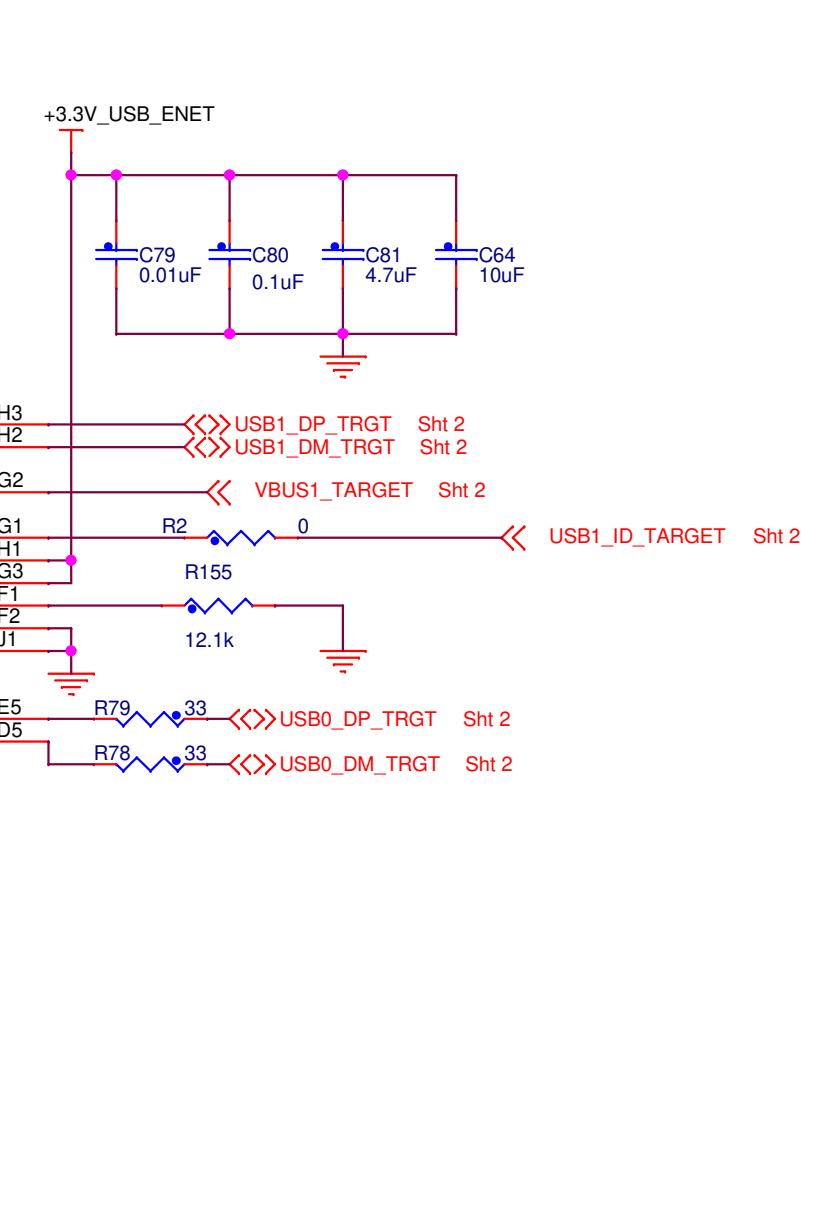
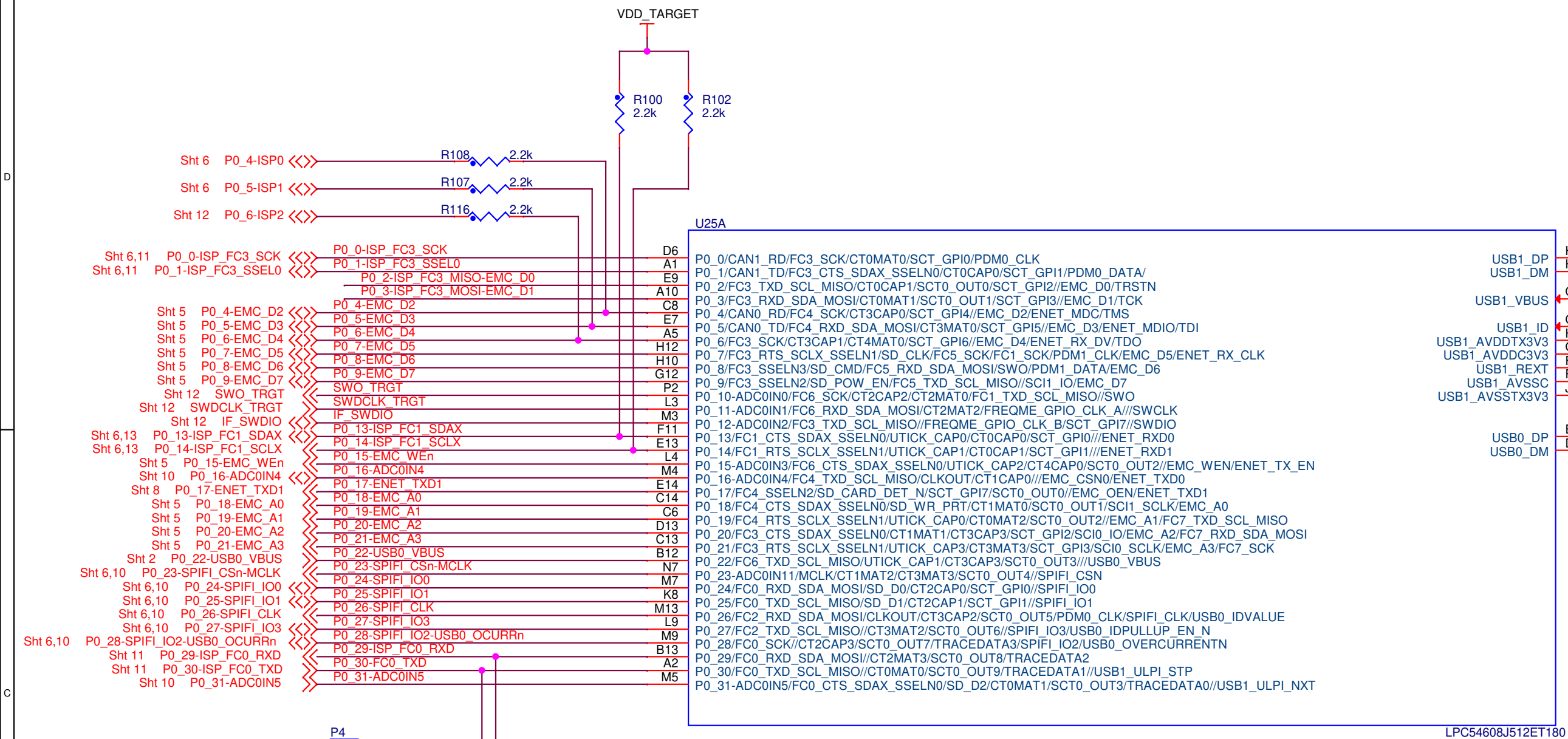
JP9 SETTINGS  
USBX Host VBUS  
USB1 High Spd - shunt 1 - 2 (default)  
USB0 Full Spd - shunt 2 - 3



JP10 SETTINGS  
USBX Host Power Control Select  
USB0 Full Spd --- shunt installed  
USB1 High Spd -- open (default)



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Drawn by: <DrawnBy> Approved: <Approver>		Page Title: <b>LPC546XX/540XX POWER / USB</b> Document Number: SCHM-LPC546/540XX Rev: E	
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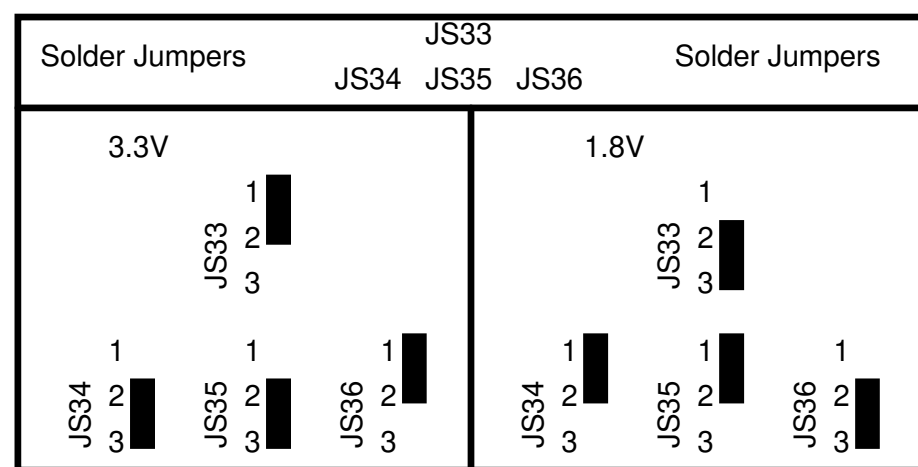
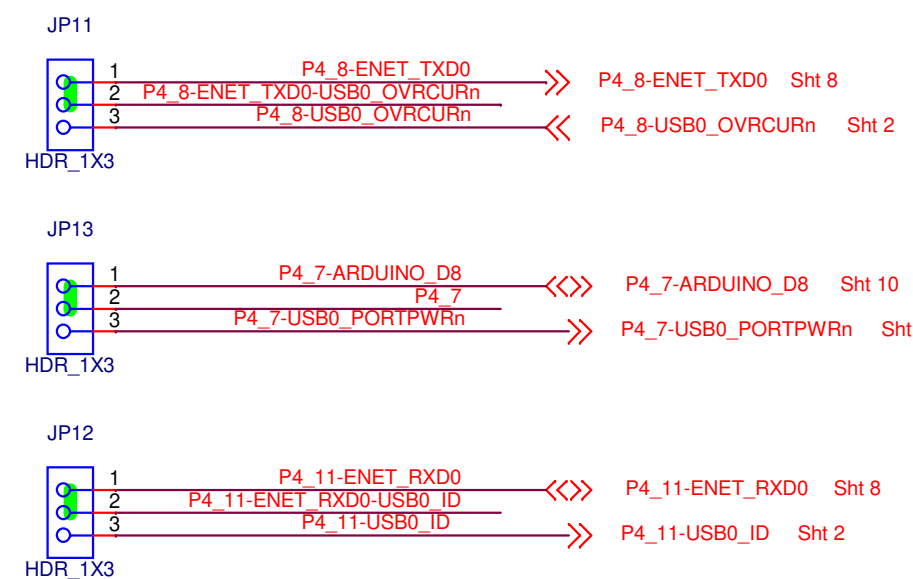
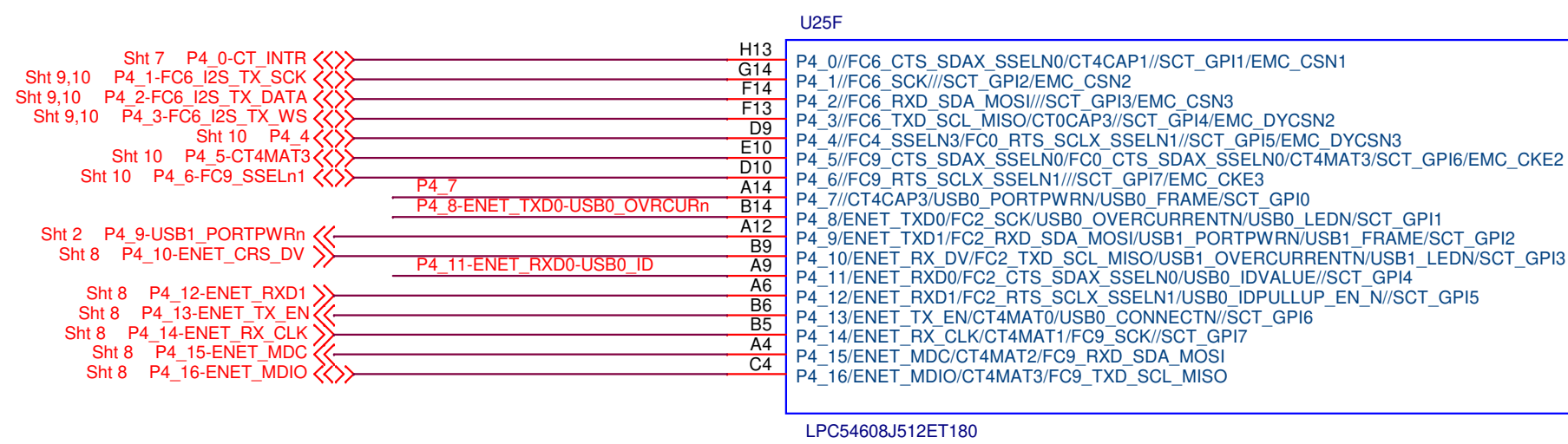
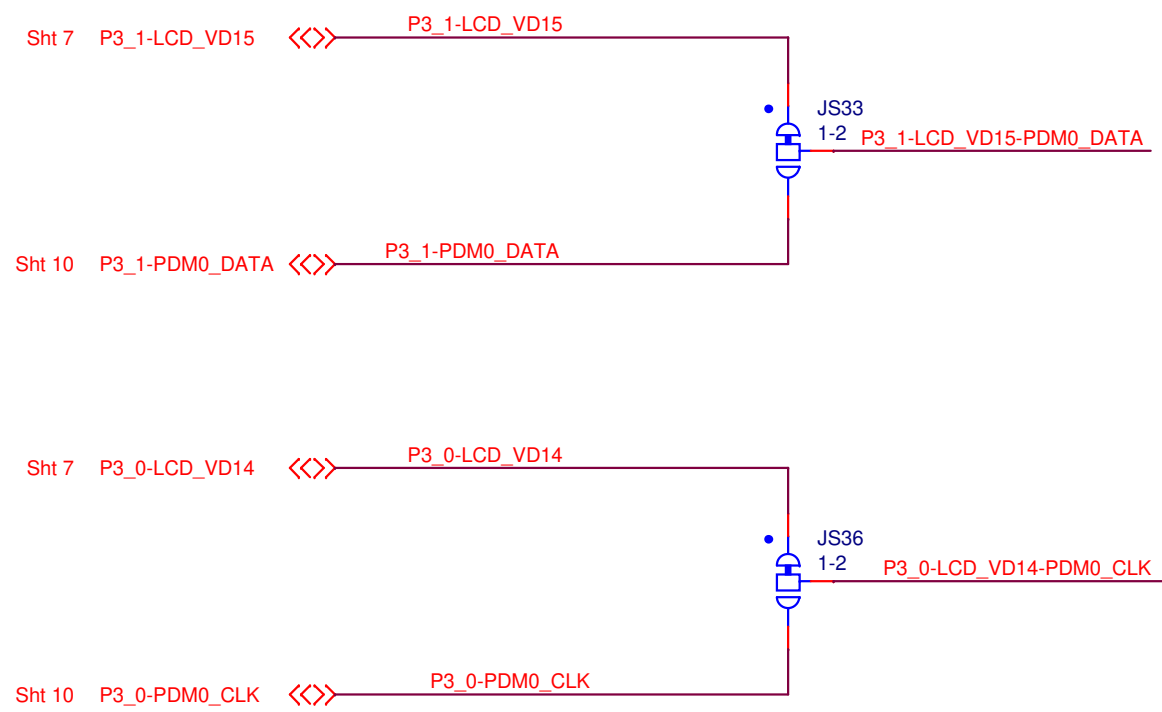
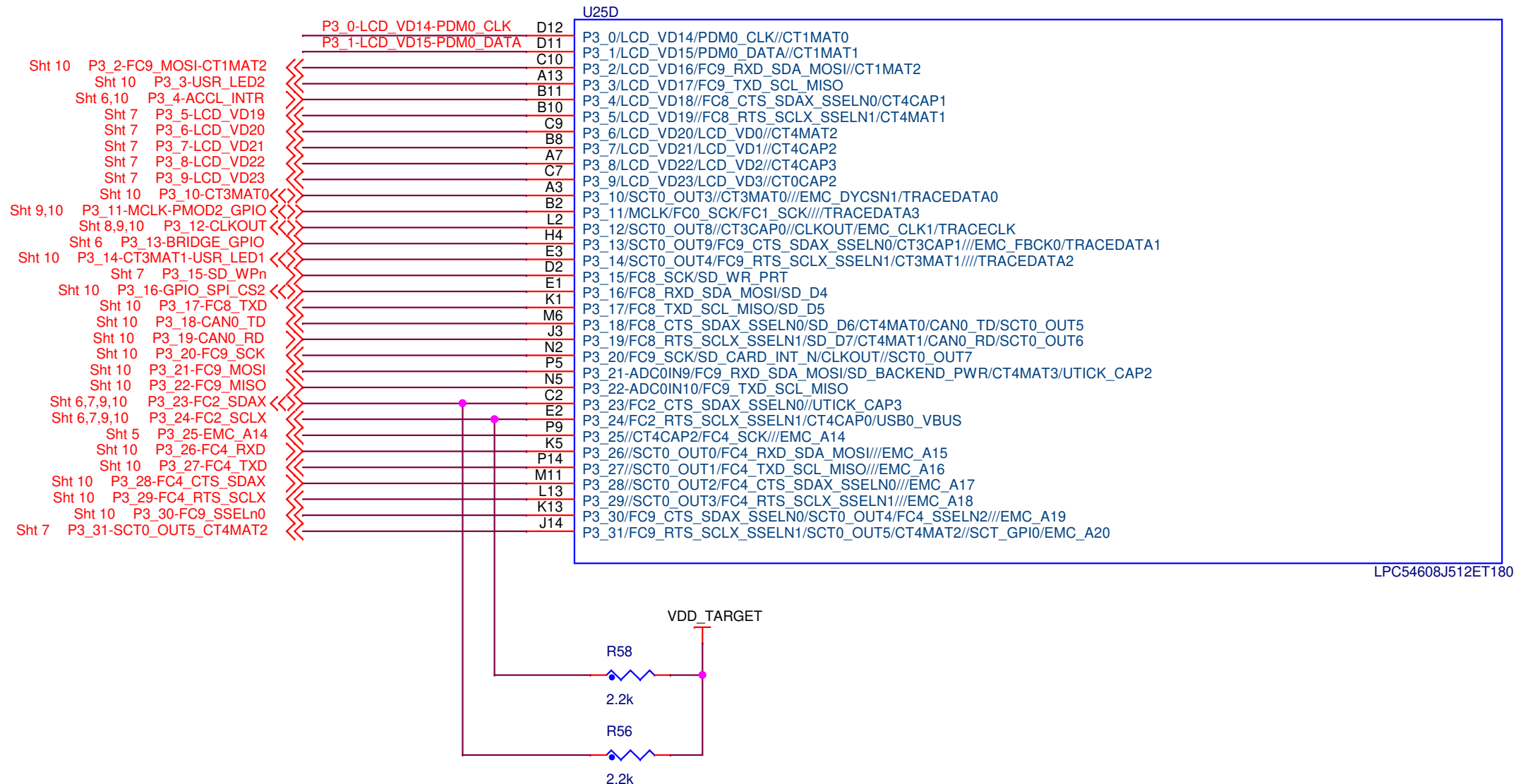
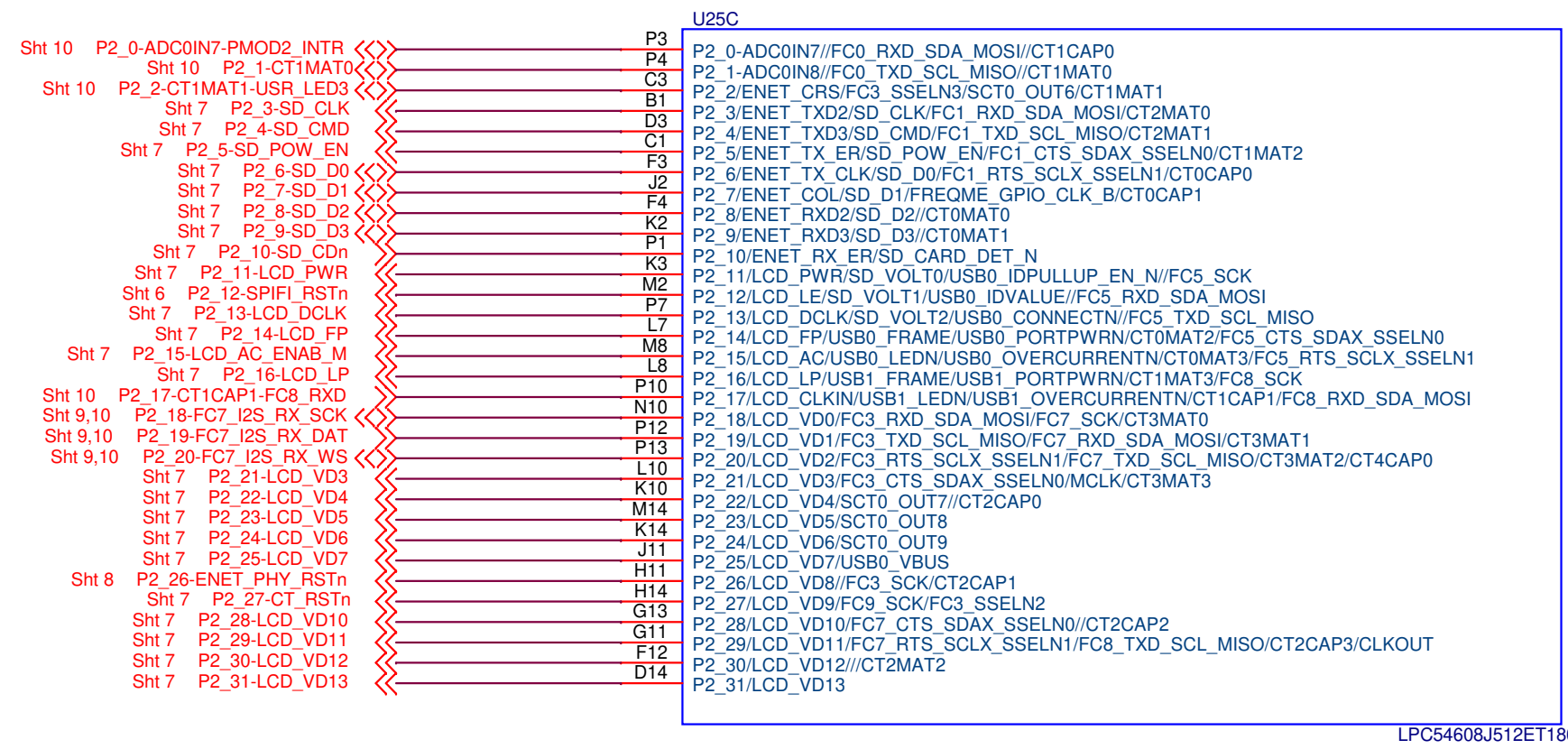
Solder Jumpers		JS33			Solder Jumpers		
		JS34	JS35	JS36			
3.3V		1	2	3	1.8V		
		1	2	3	1	2	3
		2	3	1	2	3	1
		3	1	2	3	1	2

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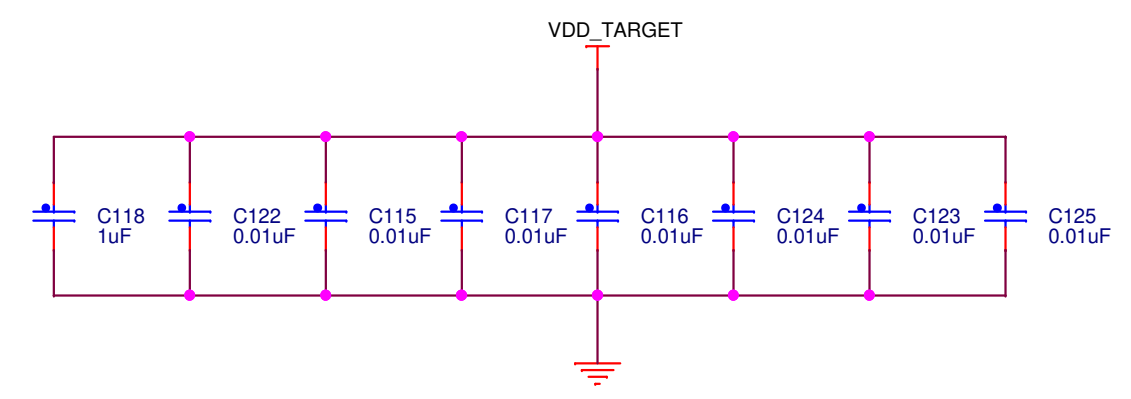
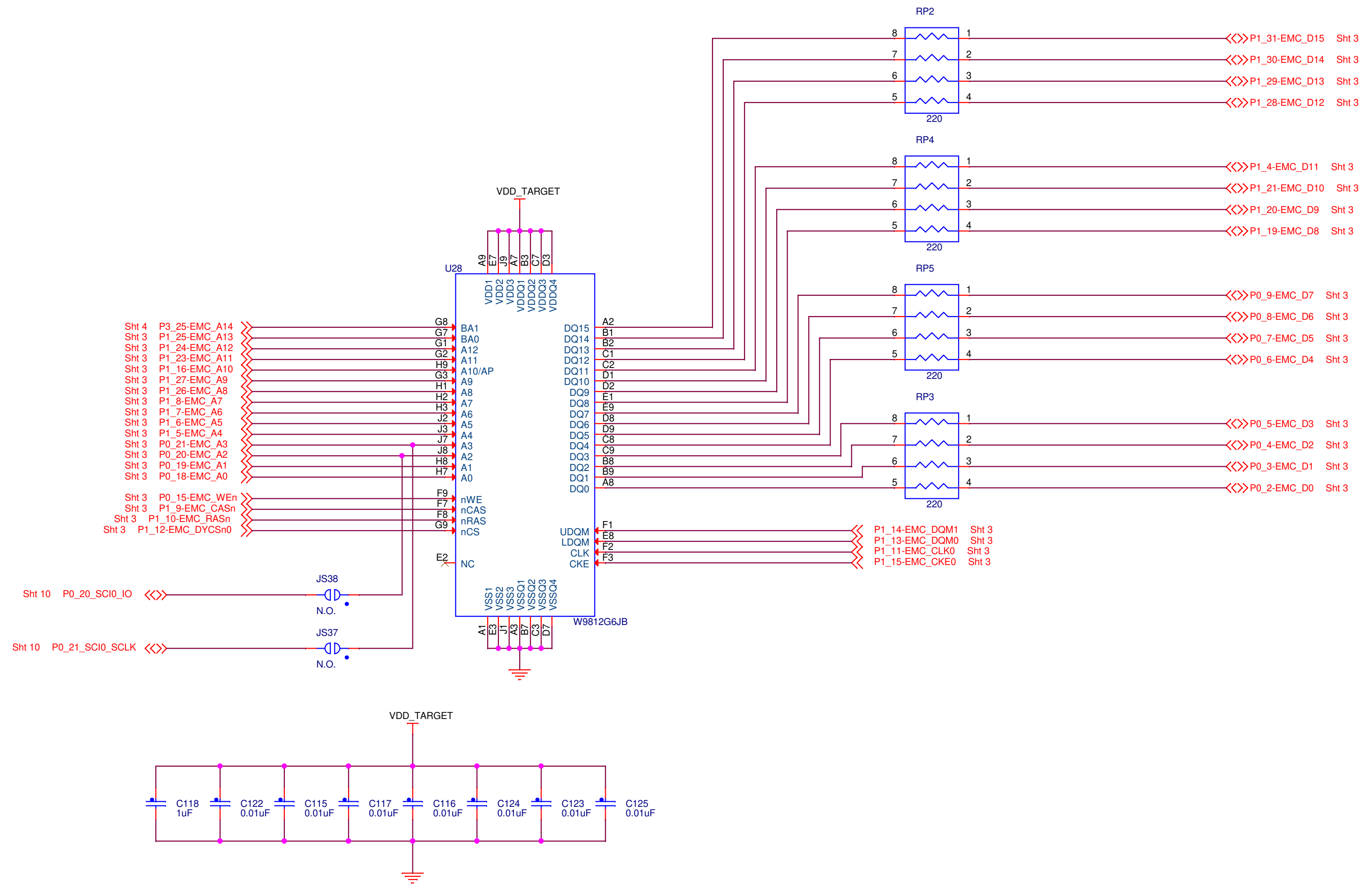
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Drawn by: <DrawnBy>	Page Title: <b>LPC54XXX PORT 0,1 / BOOT SEL</b>		
Approved: <Approver>	Size C	Document Number SCHM-LPC546/540XX	Rev E
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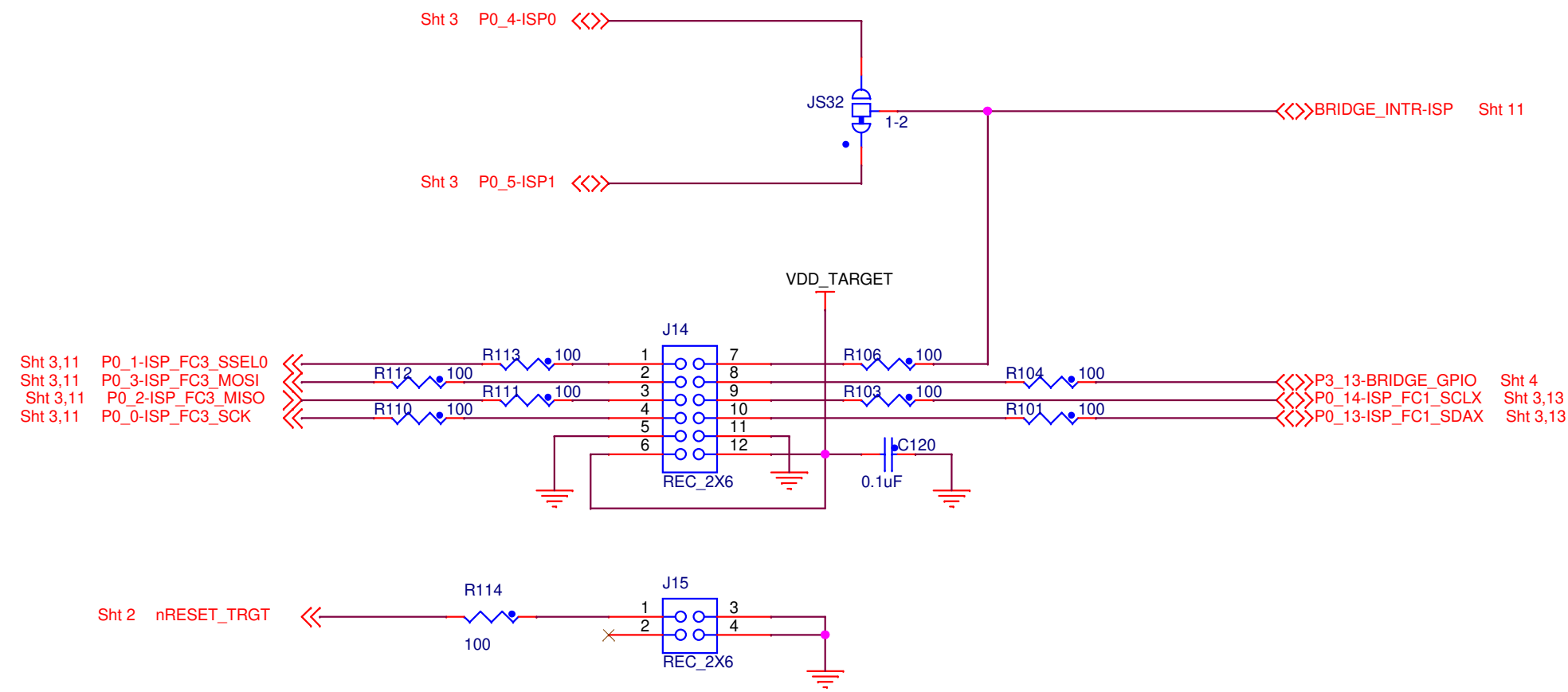


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Drawn by: <DrawnBy>	Page Title: <b>LPC54XX/540XX PORT 2,3,4</b>		
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Drawn by: <DrawnBy>	Page Title: <b>TARGET EMC_RAM</b>		
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SPI / I2C header (PMOD compatible) Host interface



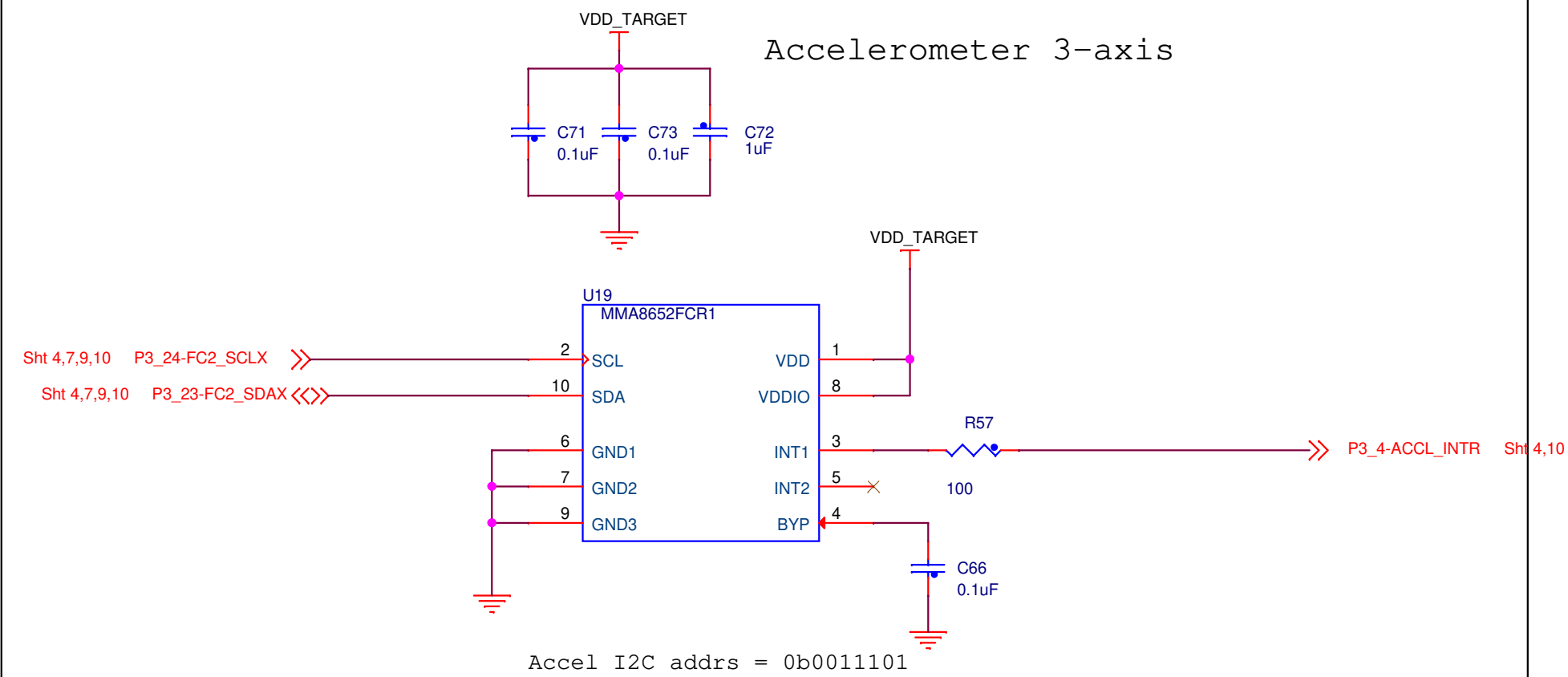
PMOD PIN FUNCTION

Pin 1: GPIO/SPI-SSEL(out)/UART-CTS(in)  
 Pin 2: GPIO/SPI-MOSI(out)/UART-TXD(out)  
 Pin 3: GPIO/SPI-MISO(in)/UART-RXD(in)  
 Pin 4: GPIO/SPI-SCK(out)/UART-RTS(out)  
 Pin 5: GND  
 Pin 6: VCC (3.3V)  
 Pin 7: GPIO/INT(in)  
 Pin 8: GPIO/RESET(out)  
 Pin 9: GPIO/SCL  
 Pin 10: GPIO/SDA  
 Pin 11: GND  
 Pin 12: VCC (3.3V)

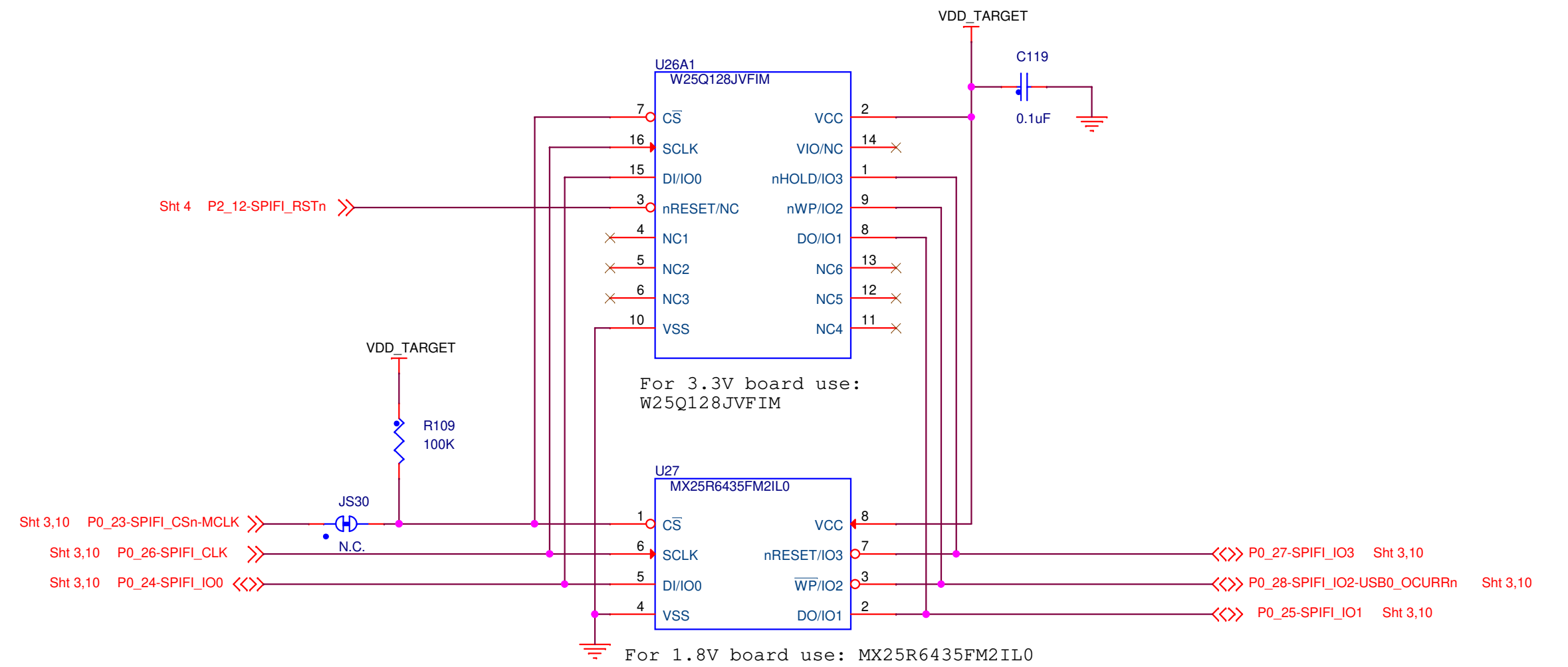
LPC546xx/540xx supported function

Pin 1: GPIO/SPI-SSEL(out/in)  
 Pin 2: GPIO/SPI-MOSI(out/in)  
 Pin 3: GPIO/SPI-MISO(in/out)  
 Pin 4: GPIO/SPI-SCK(out/in)  
 Pin 5: GND  
 Pin 6: VCC (3.3V)  
 Pin 7: GPIO/INT(in/out)  
 Pin 8: GPIO/RESET(out)  
 Pin 9: SCL  
 Pin 10: SDA  
 Pin 11: GND  
 Pin 12: VCC (3.3V)

Accelerometer 3-axis



QSPI (SPIFI) NOR FLASH  
 S016 package / S08 package mutually exclusive

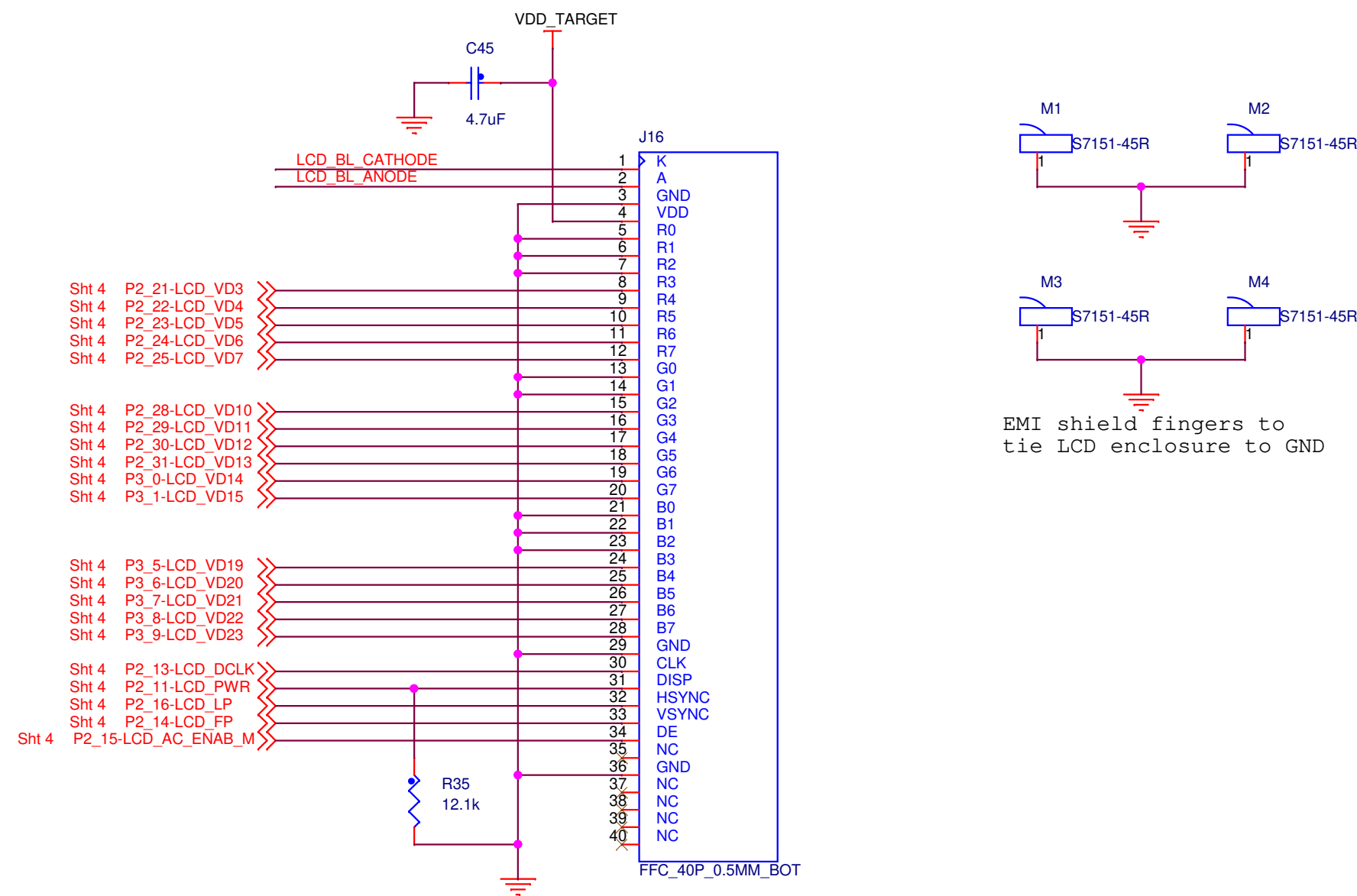


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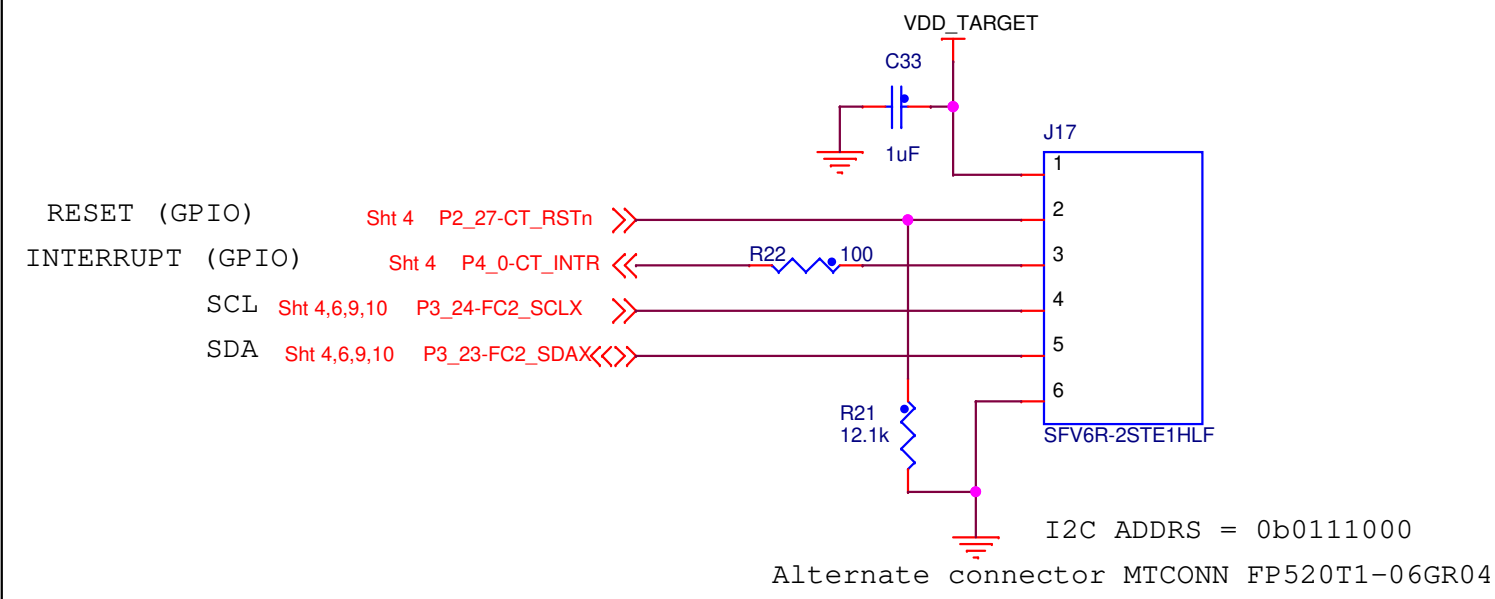
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Approved: <Approver>	Size C Document Number SCHM-LPC546/540XX Rev E
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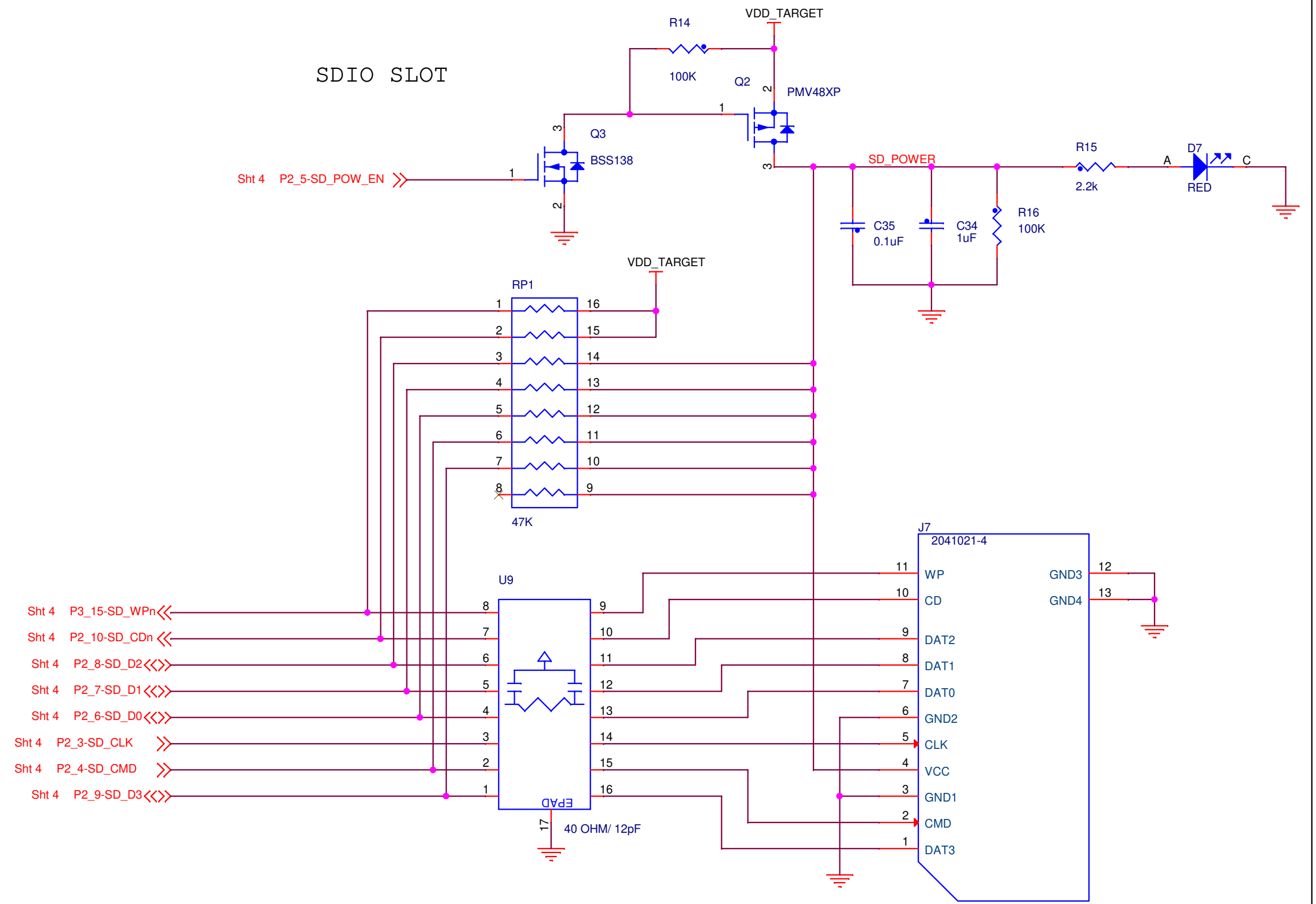
### RK043FN02H-CT LCD display



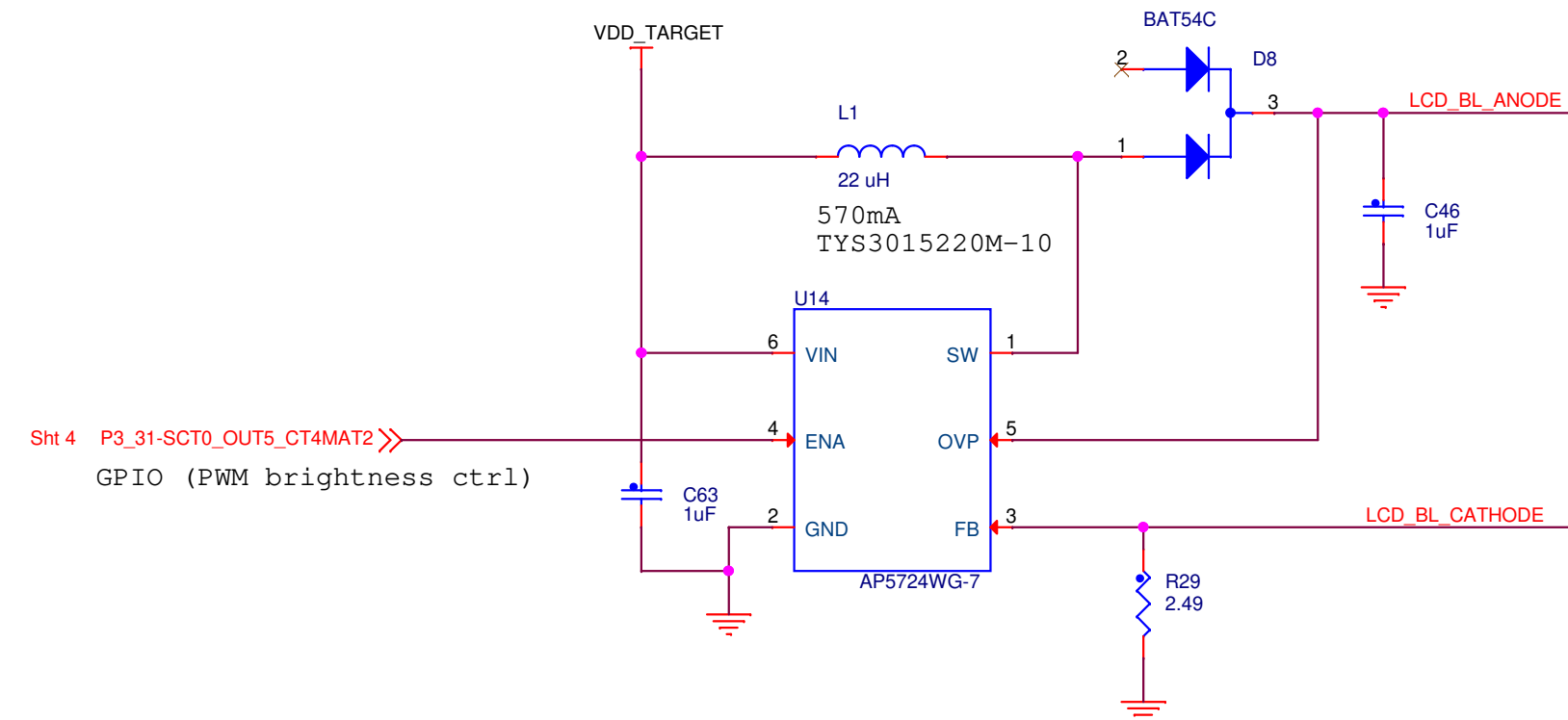
### Cap Touch RK043FN02H-CT LCD display



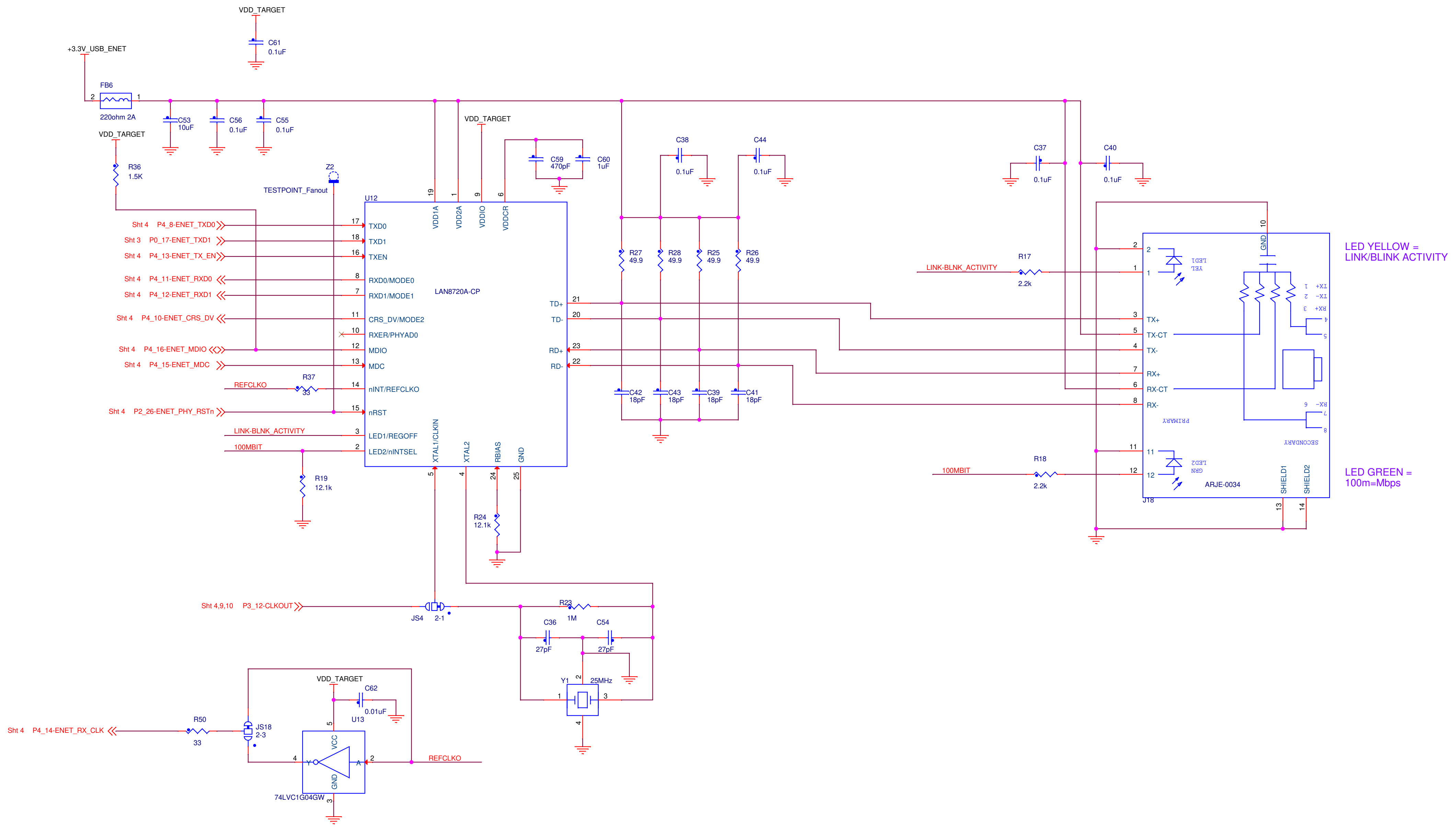
### SDIO SLOT



### LCD Backlight



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Drawn by: <DrawnBy>	Page Title: <b>LCD DISPLAY + CAP TOUCH / SD CARD SLOT</b>		
Approved: <Approver>	Size C	Document Number SCHM-LPC546/540XX	Rev E
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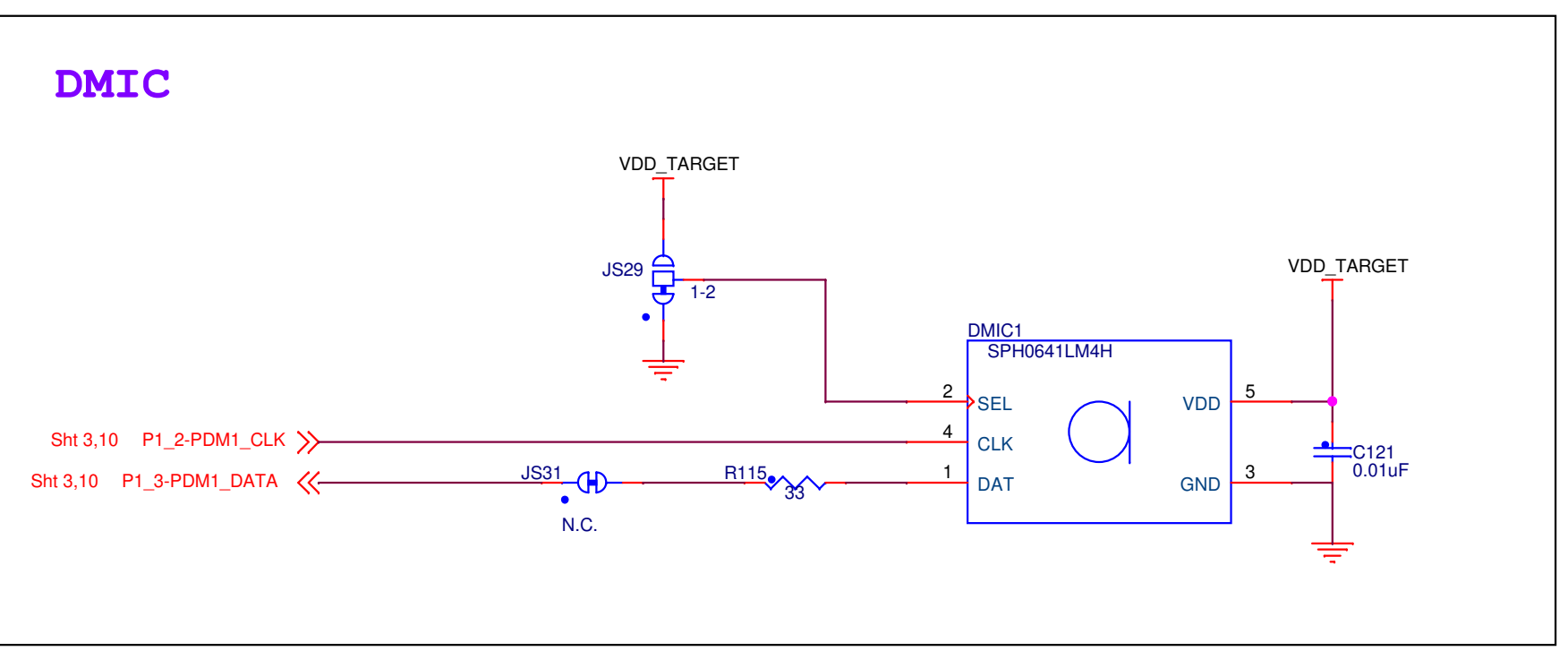
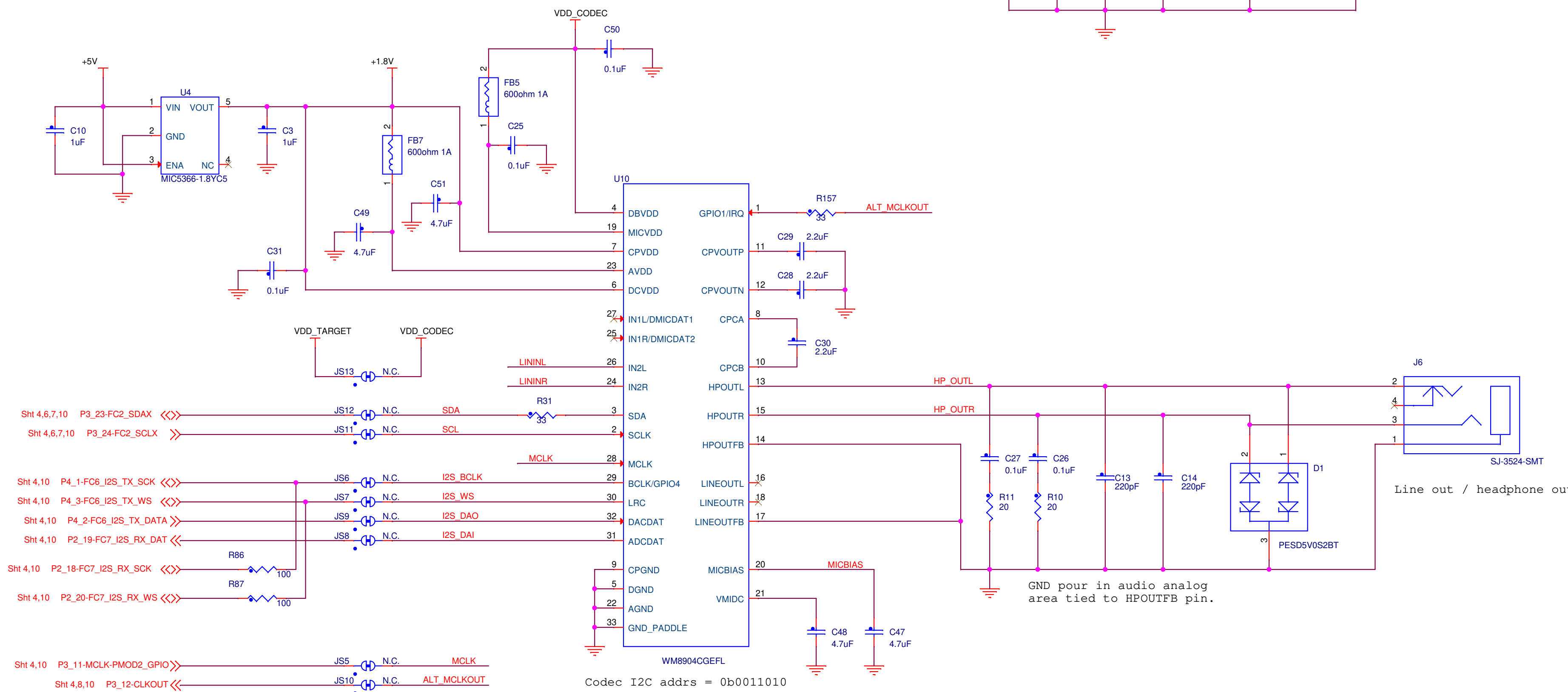


LED YELLOW =  
LINK/BLINK ACTIVITY

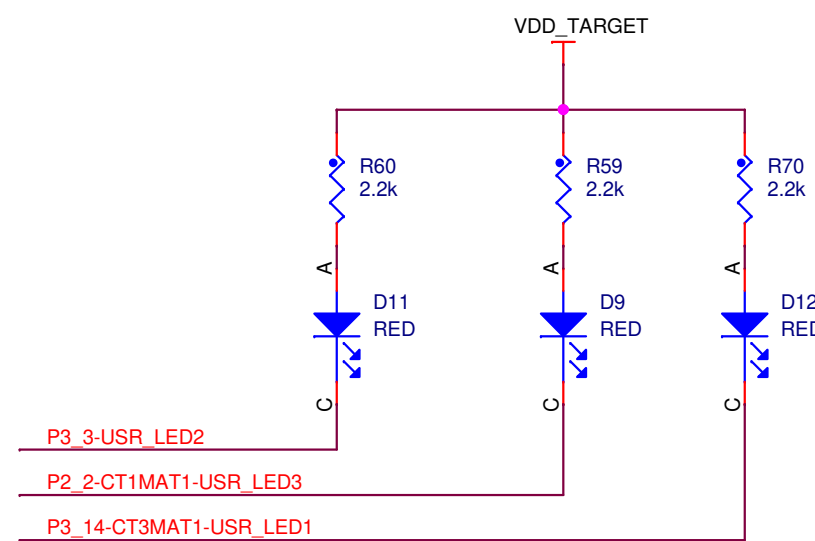
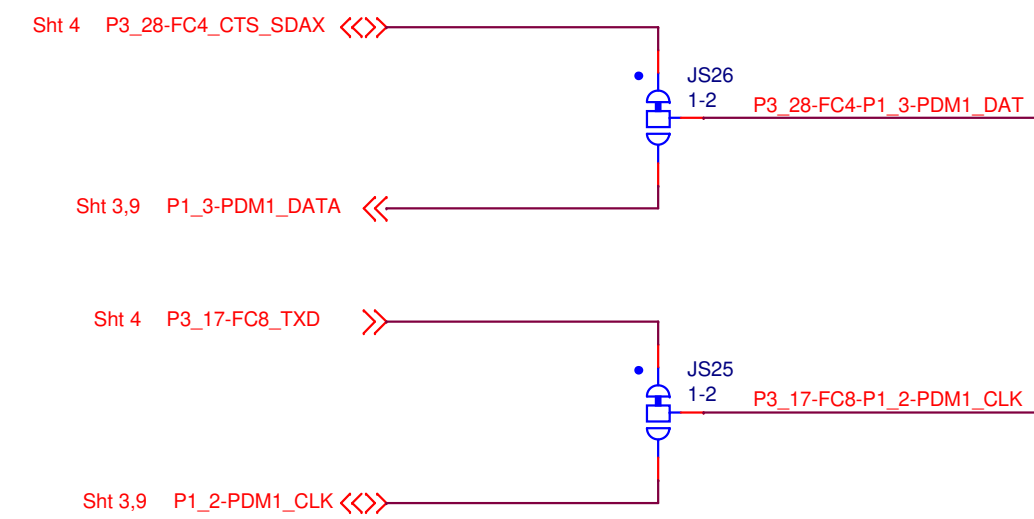
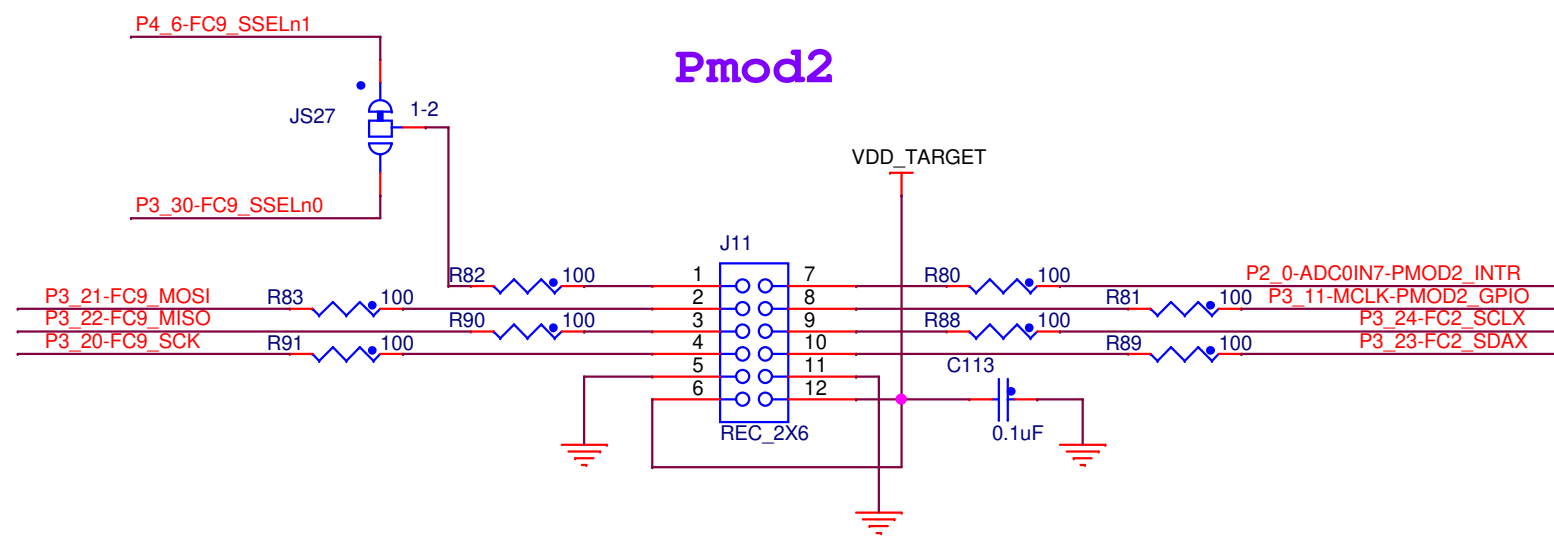
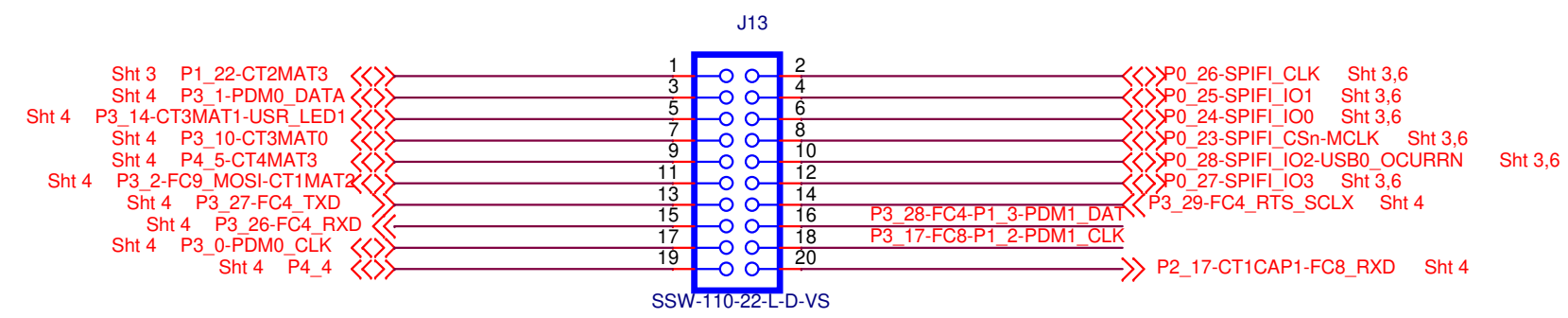
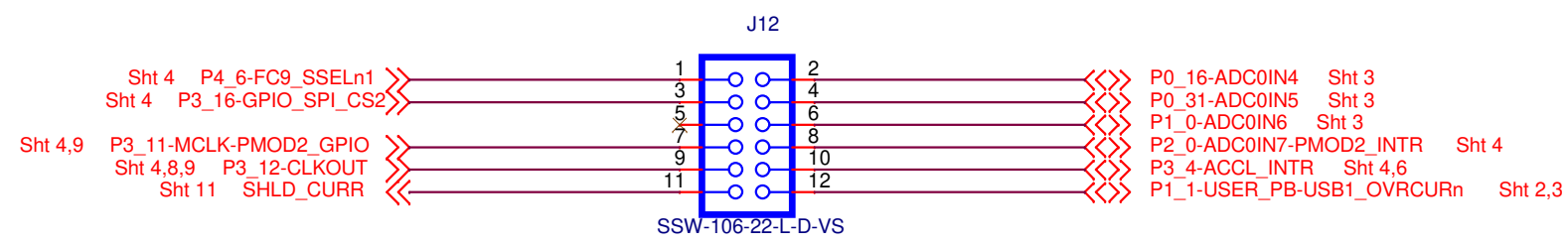
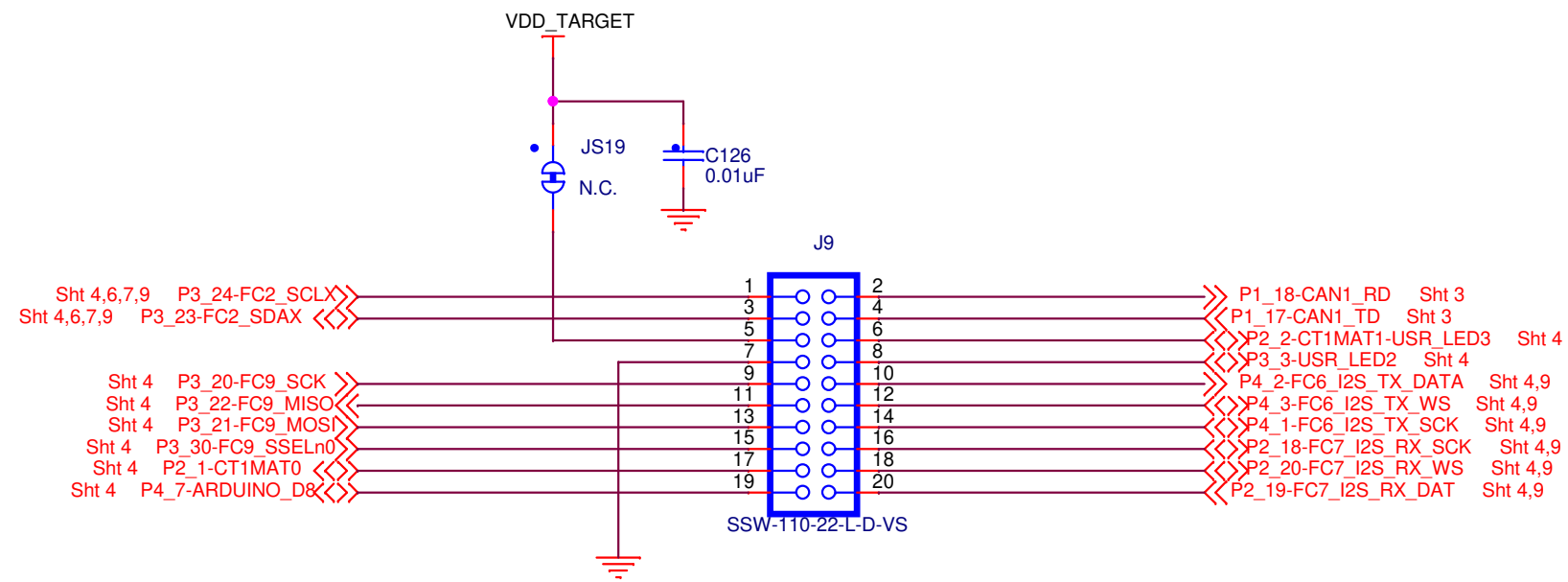
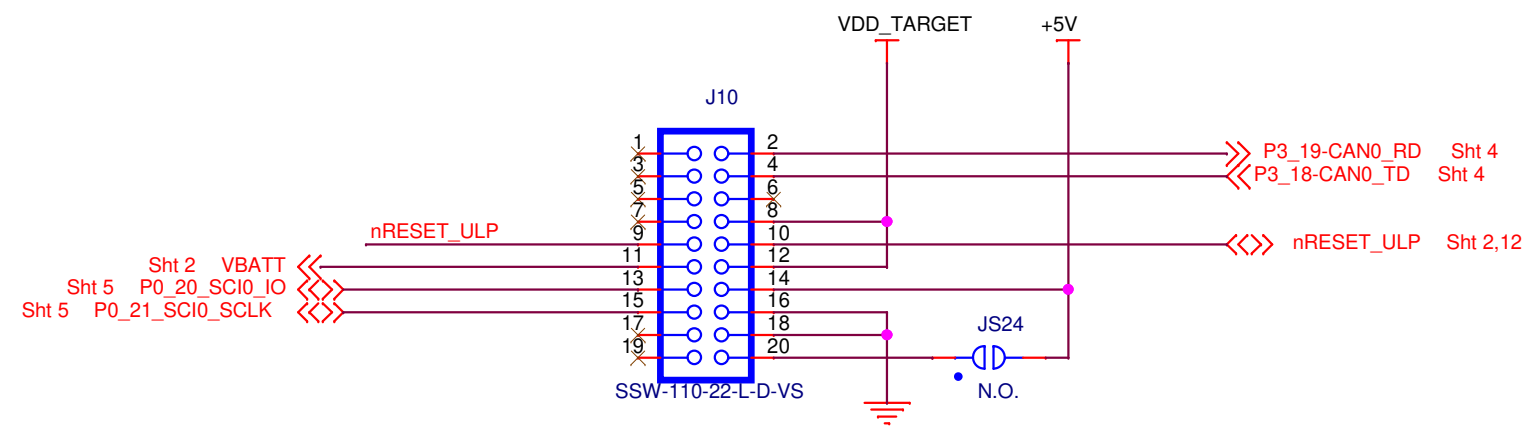
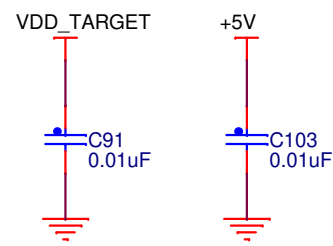
LED GREEN =  
100m=Mbps

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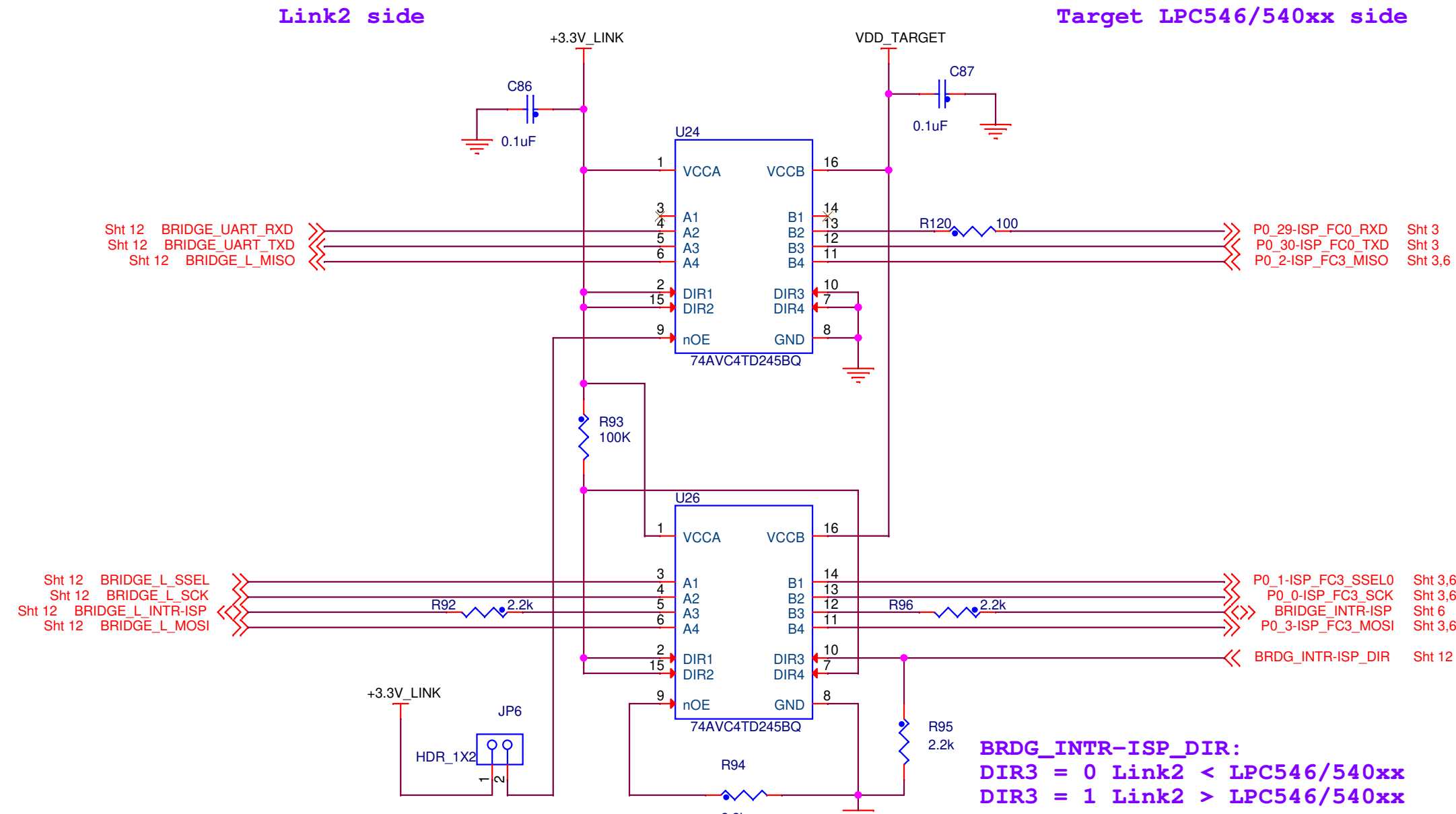


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Approved: <Approver>		<b>SHIELD CONN / PMOD2 / LEDS</b>	
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Short JP6 when using Pmod SPI interface or FC0 UART at P4 (FTDI)



Short JP6 when using Pmod SPI interface or FC0 UART at P4 (FTDI)

BRDG\_INTR-ISP\_DIR:  
DIR3 = 0 Link2 < LPC546/540xx  
DIR3 = 1 Link2 > LPC546/540xx

LPC546XX/540XX VDD Core current measurement

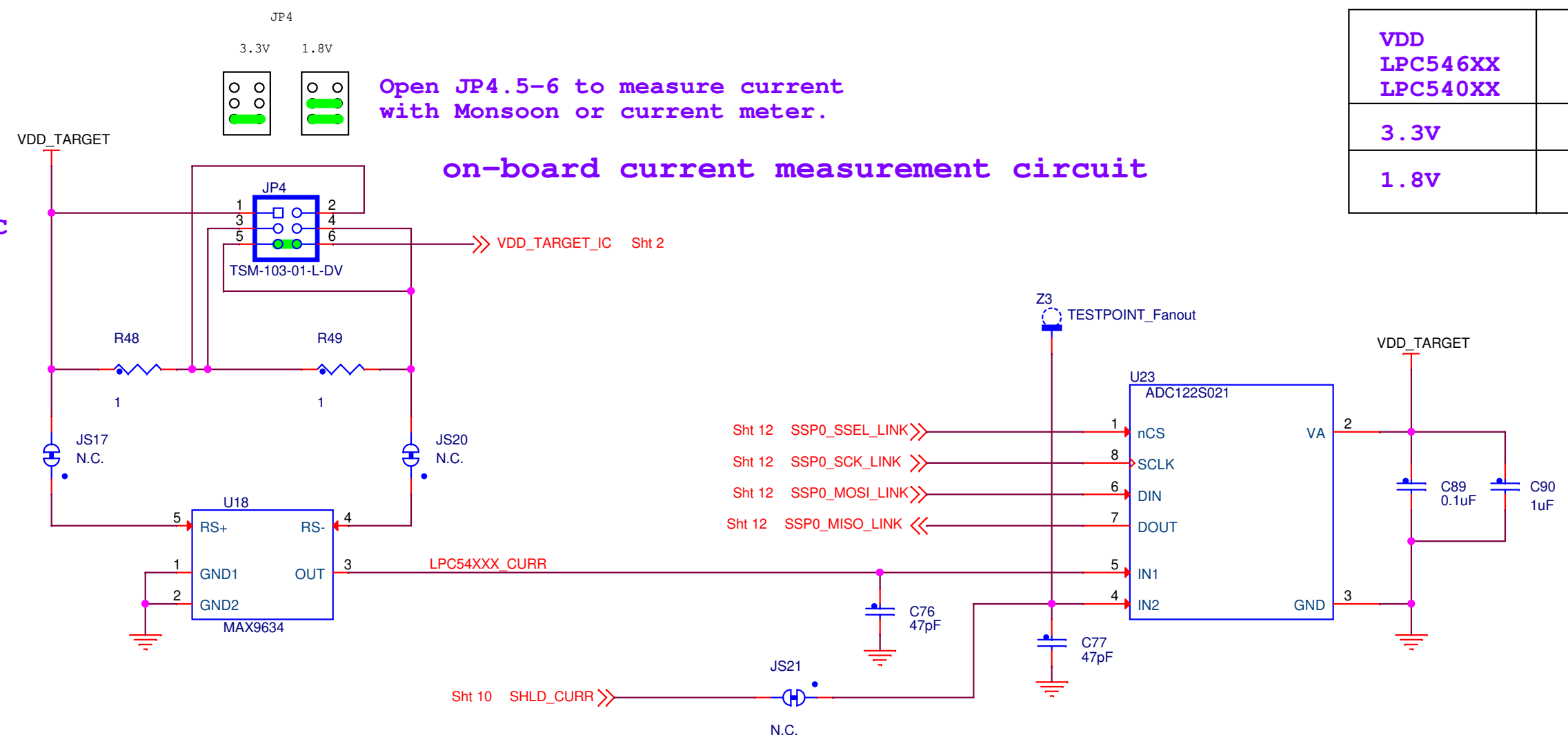
LPC546XX/540XX				ADC122S021 12BIT ADC
Vsense (1) voltage 1-lsb	JP4.3-4 open LPC546xx LPC540xx	JP4.3-4 shunted LPC546xx LPC540xx	maximum current	ADC input 1-lsb 800uV
32uV	16uA minimum	32uA minimum	65mA	

(1) Vsense voltage is beteen U18 RS+ to RS-.  
The total Rvsense = R48 + (R49 || JP4.5-6).

JP4 3-4 setting

VDD LPC546XX LPC540XX	JP4 3-4	Total Rvsense (ohms)
3.3V	open	2
1.8V	shunted	1

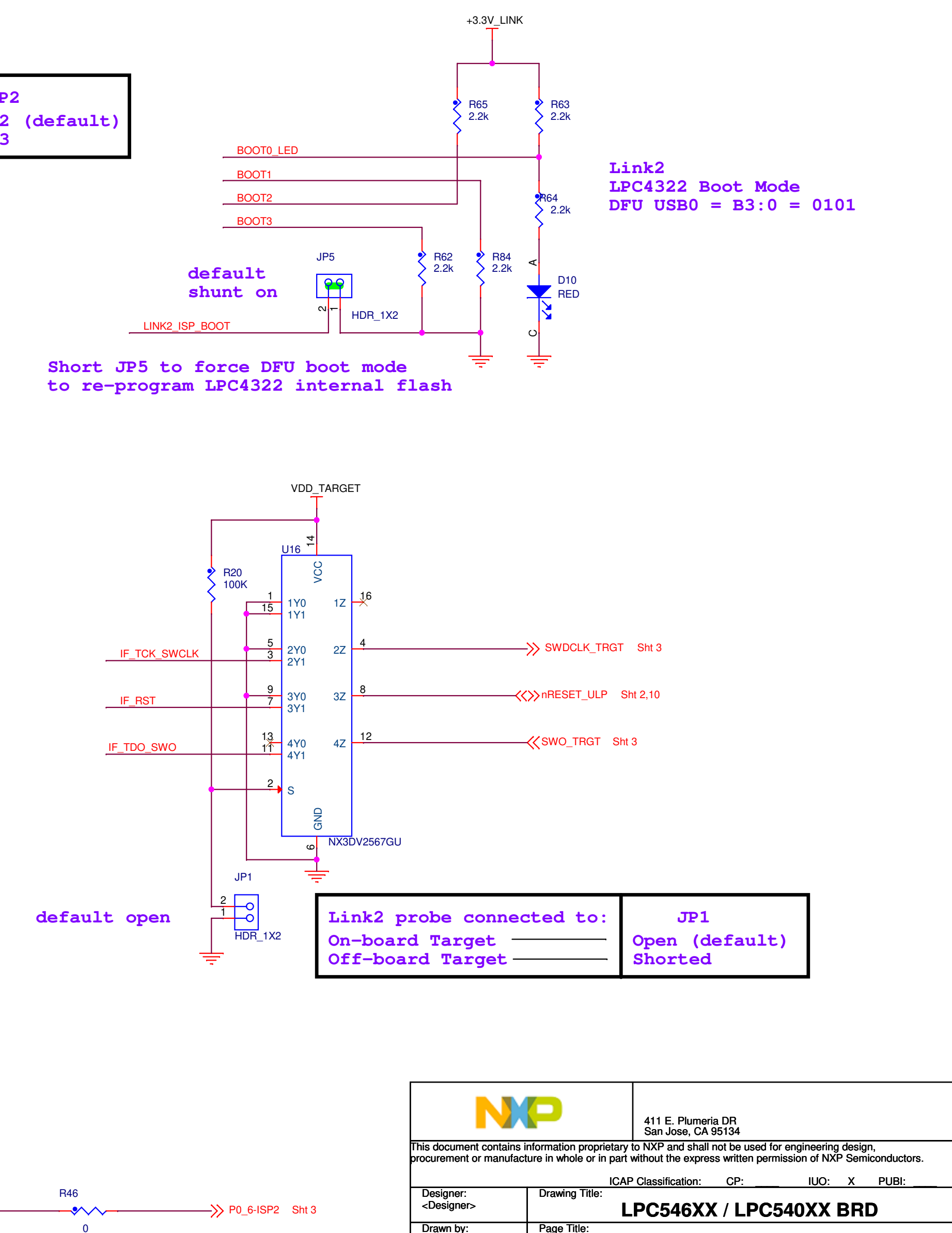
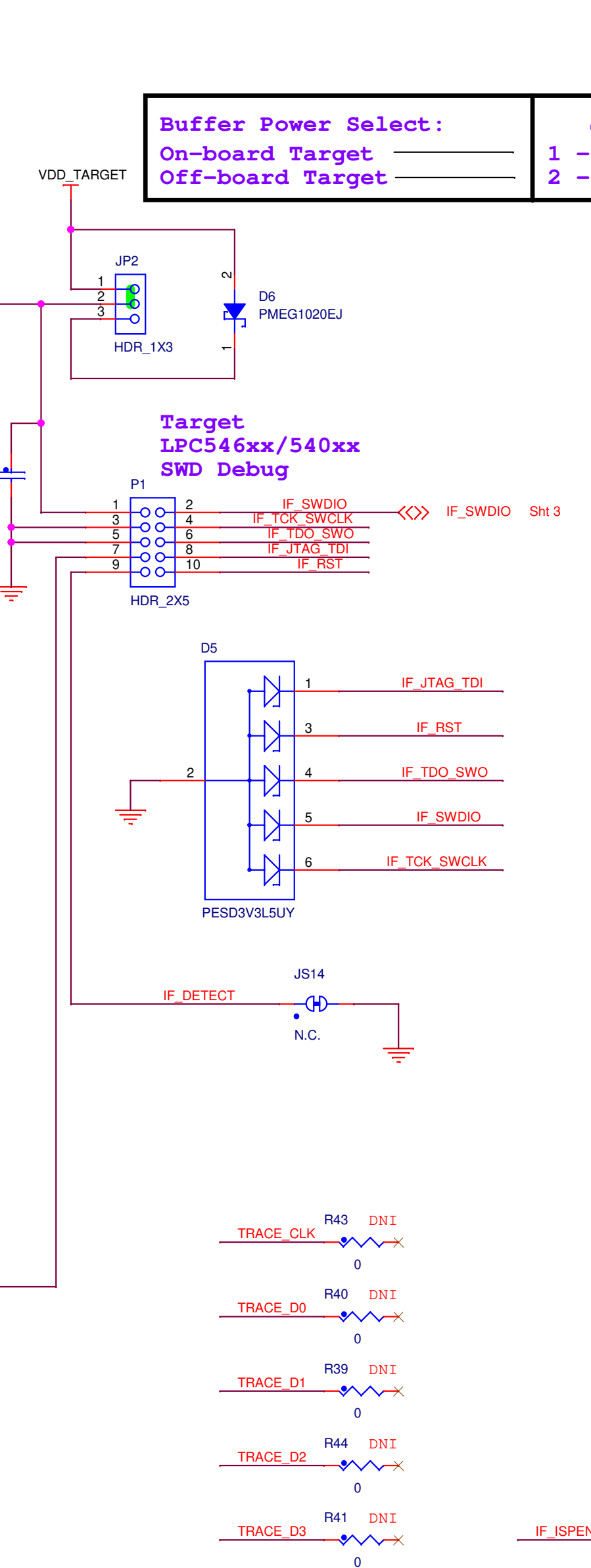
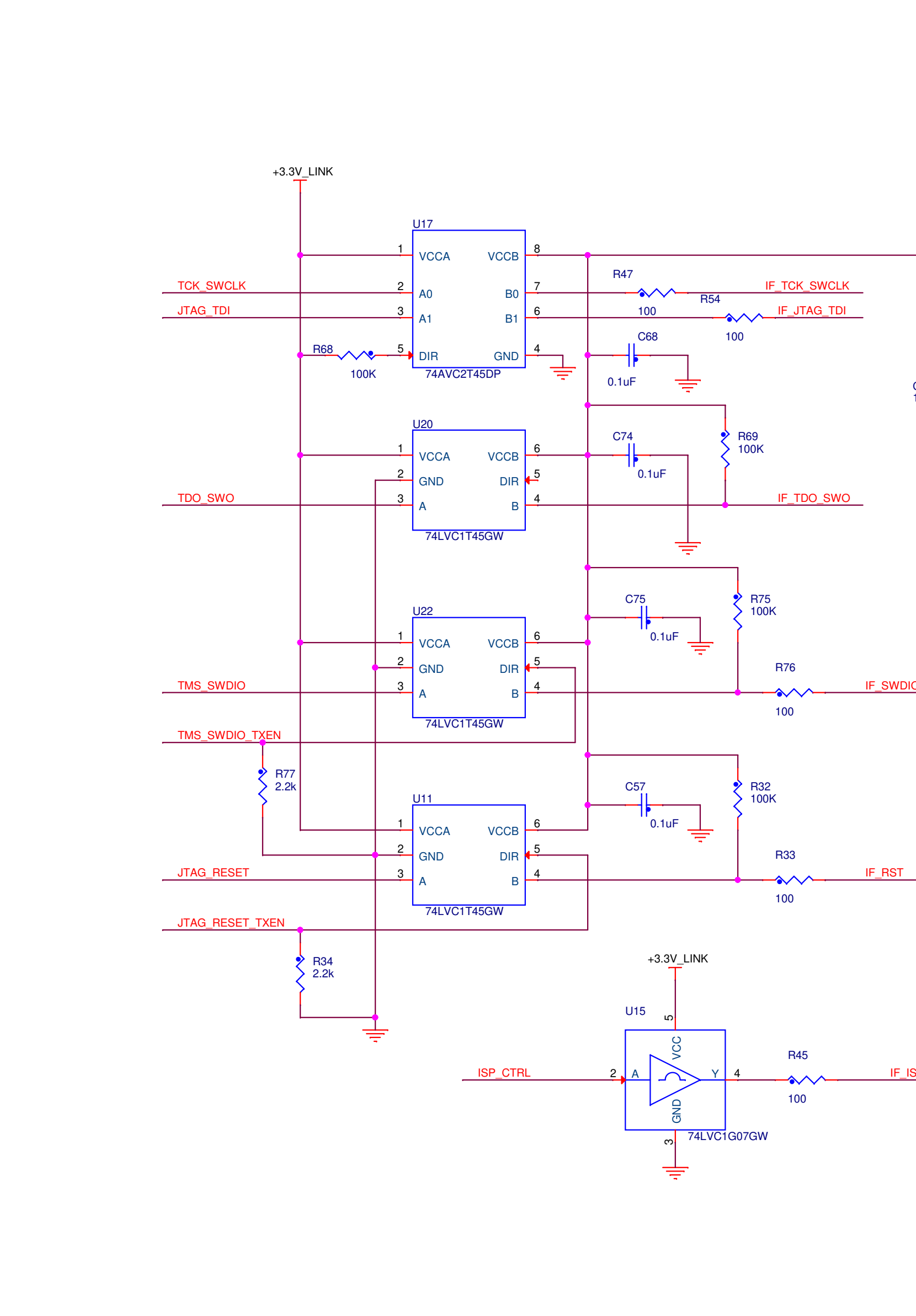
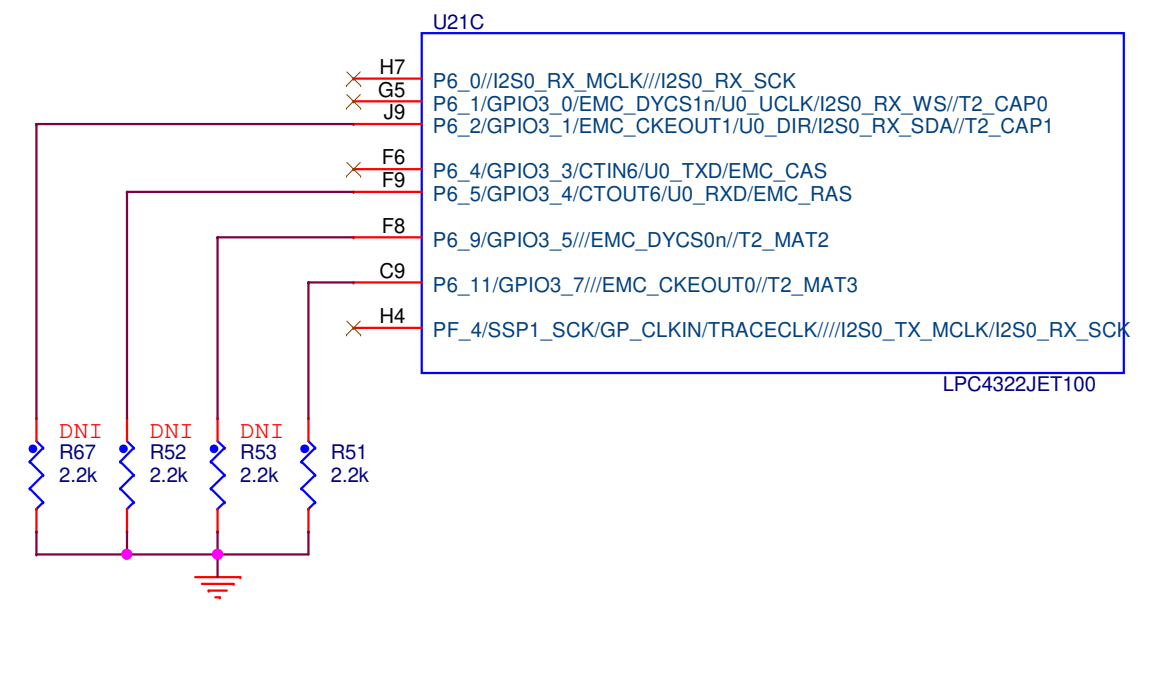
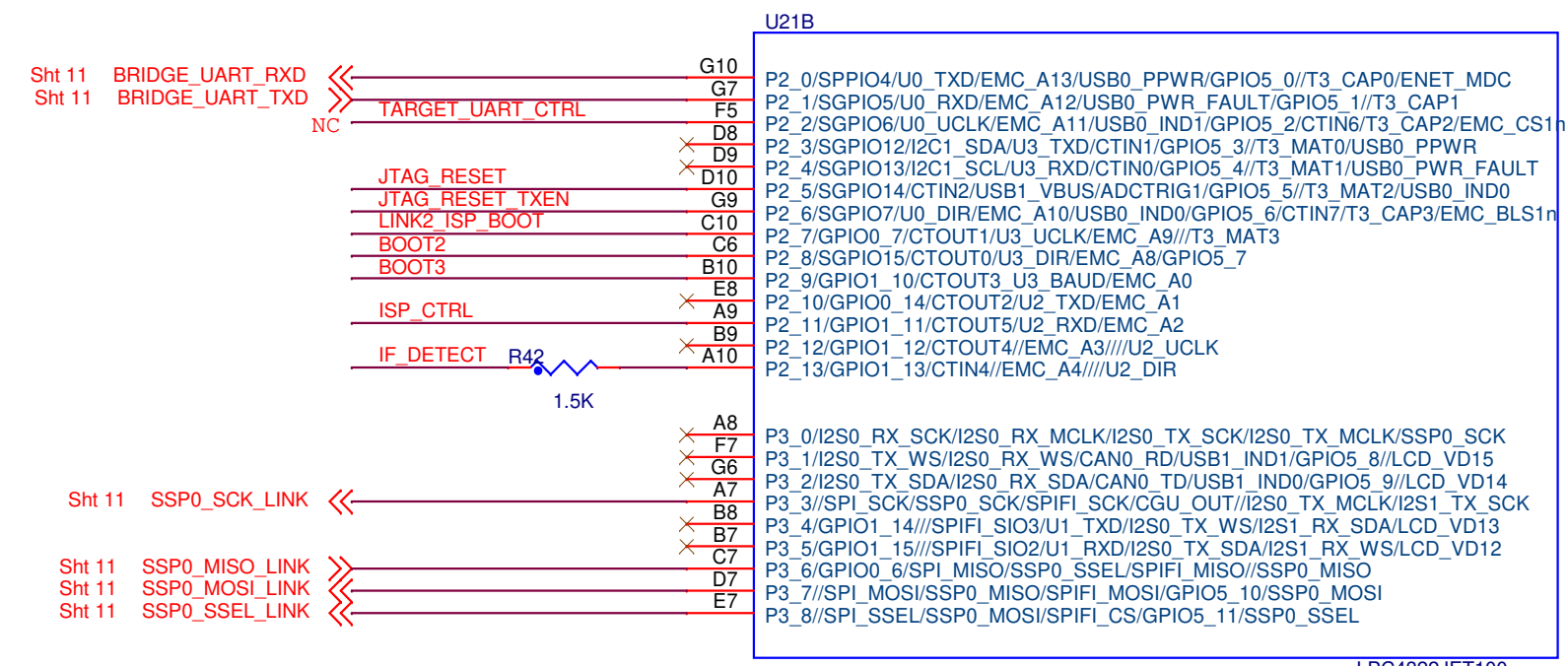
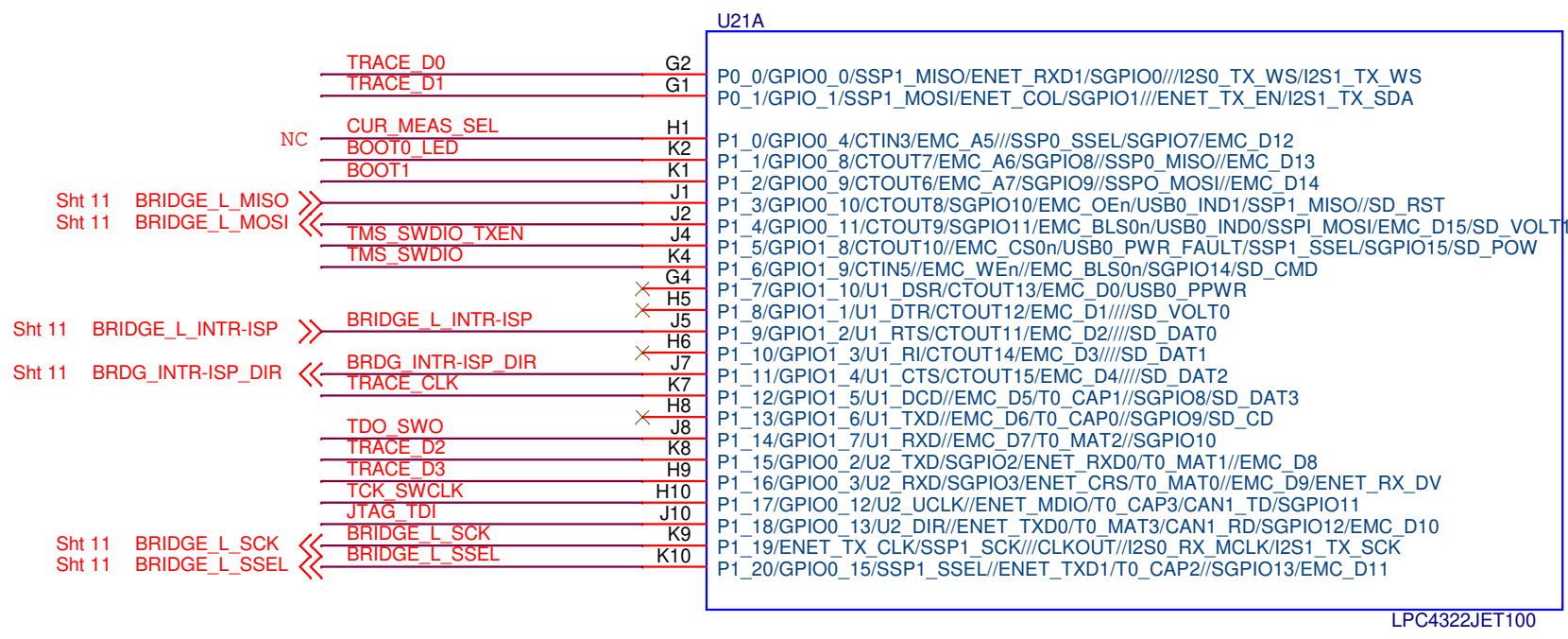
Target LPC54xxx VDDC current measurement

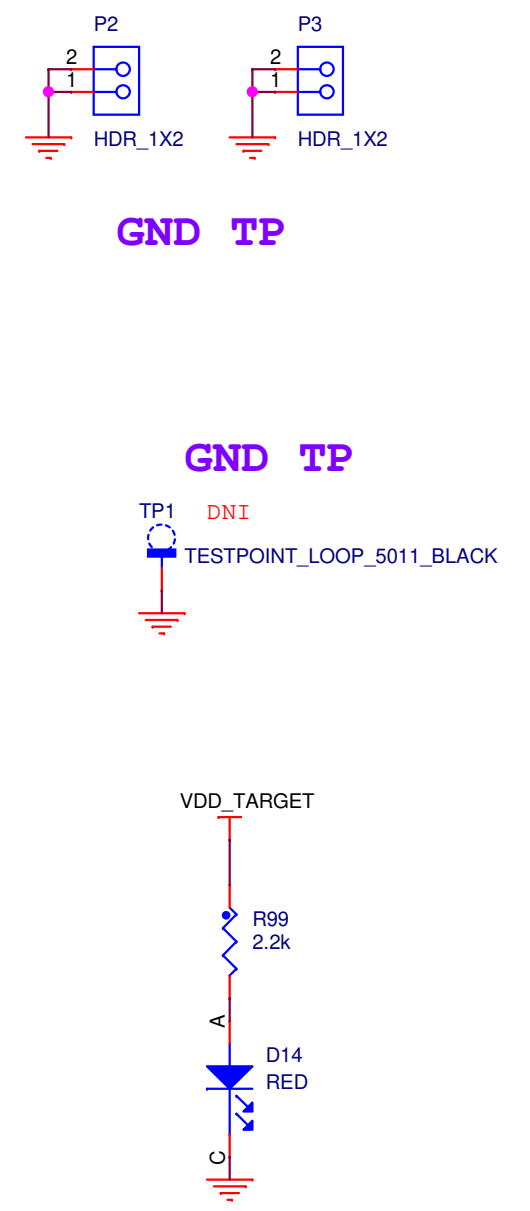
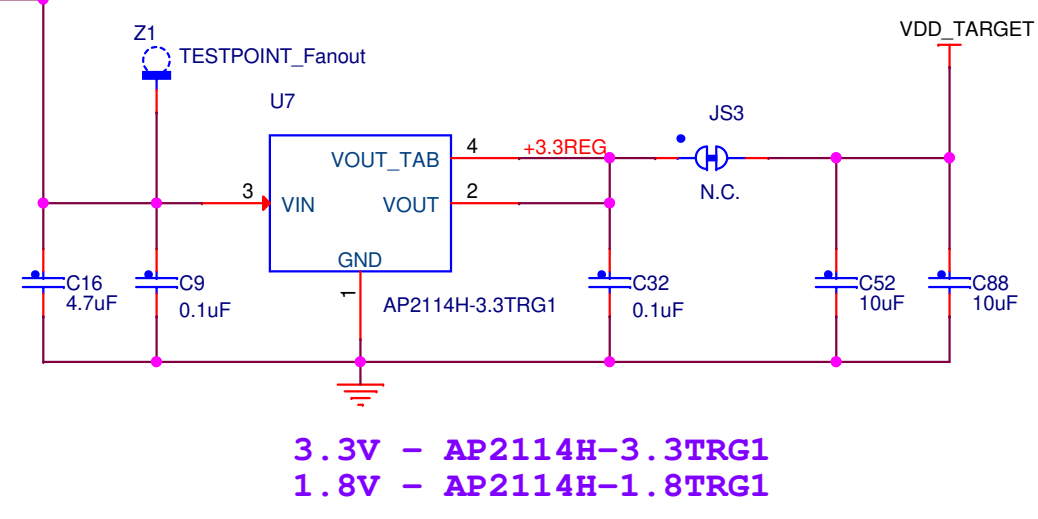
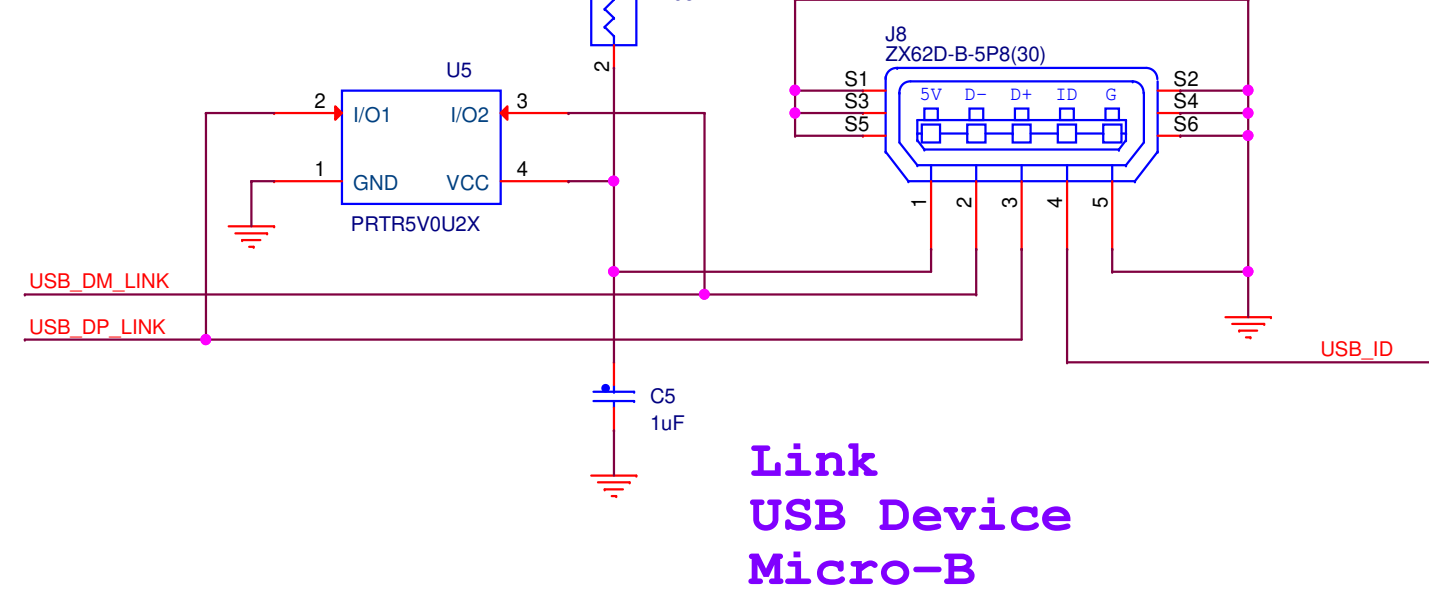
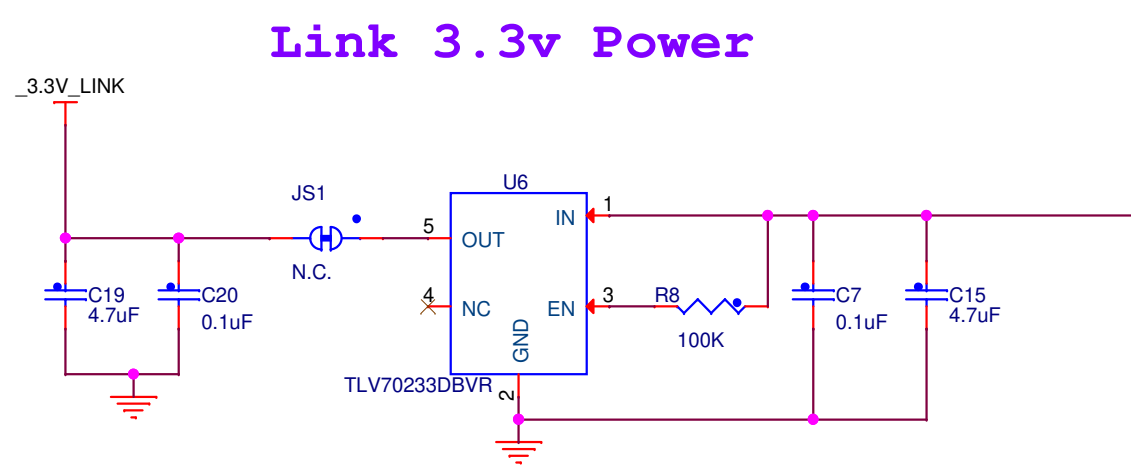
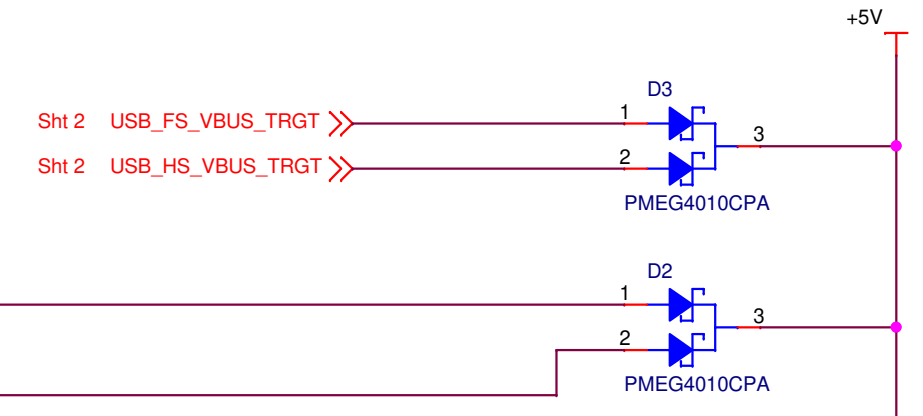
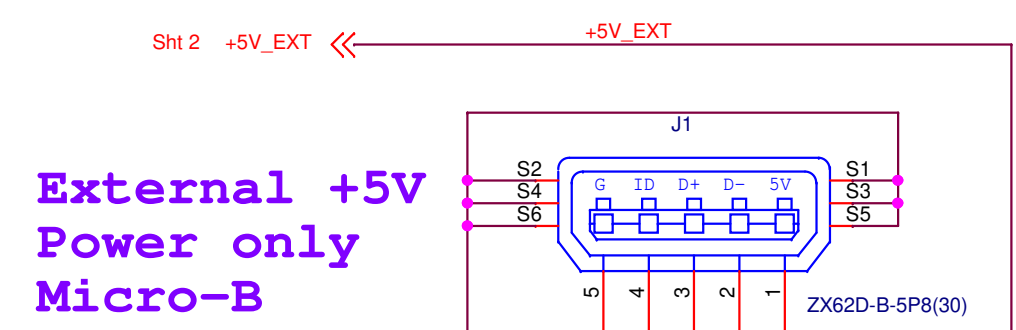
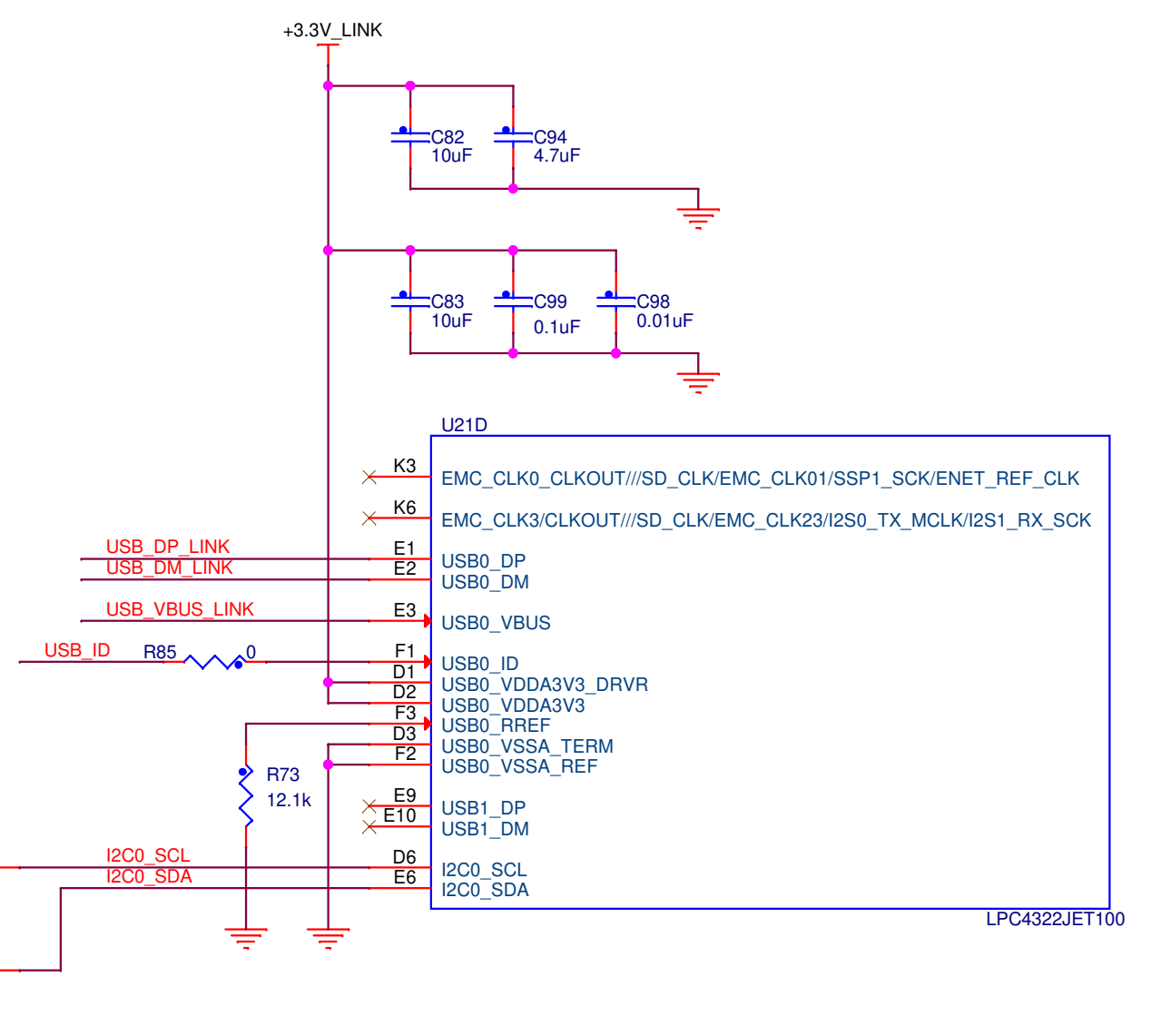
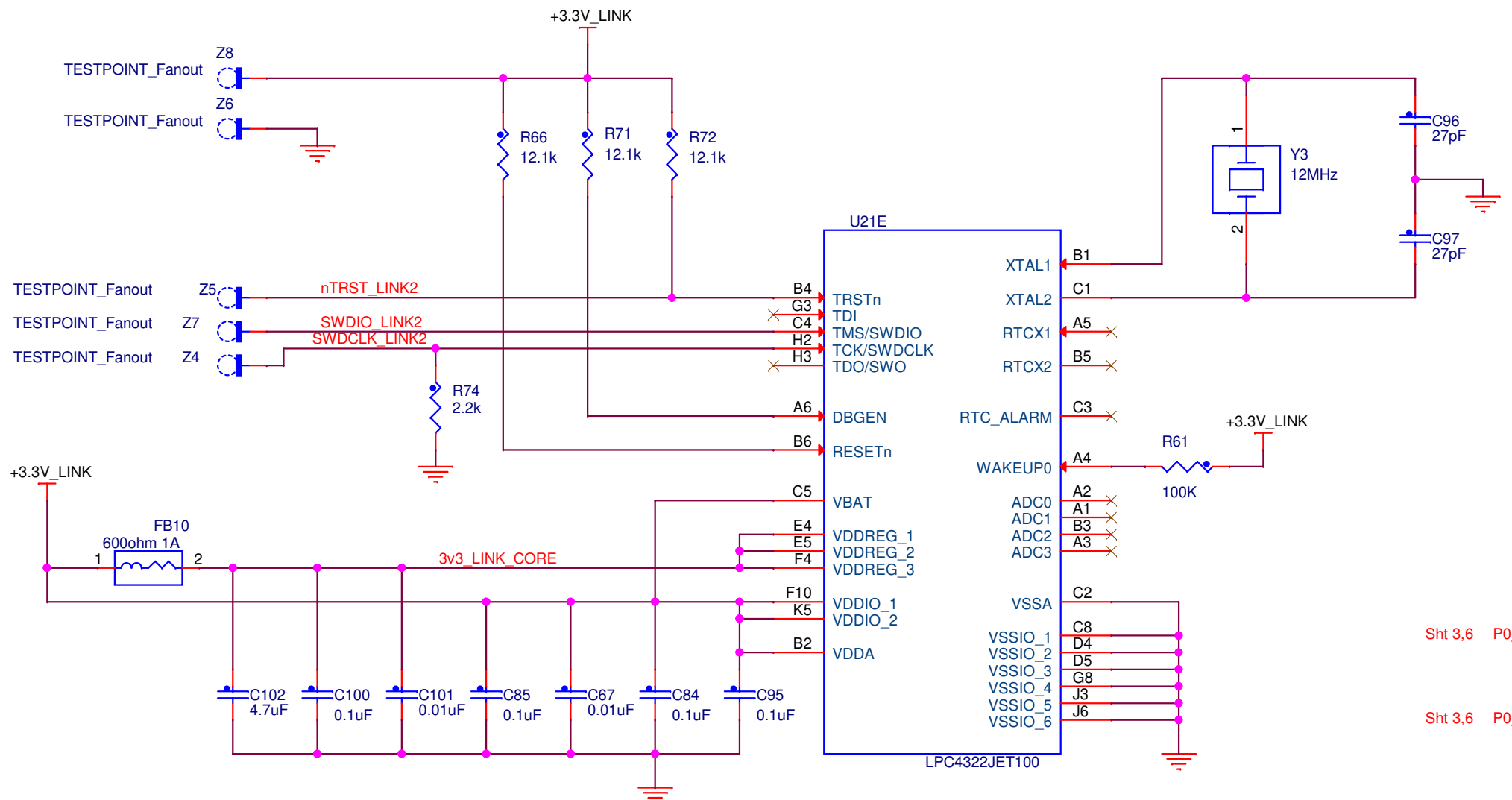


on-board current measurement circuit

Open JP4.5-6 to measure current with Monsoon or current meter.

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Drawn by: <DrawnBy>	Page Title: <b>LPC54XX/540XX CURRENT MONITOR / LINK2 BRIDGE</b>		
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Drawn by: <DrawnBy>	Page Title: <b>LINK2 LPC4322 / LINK2 USB / BOARD POWER</b>		
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