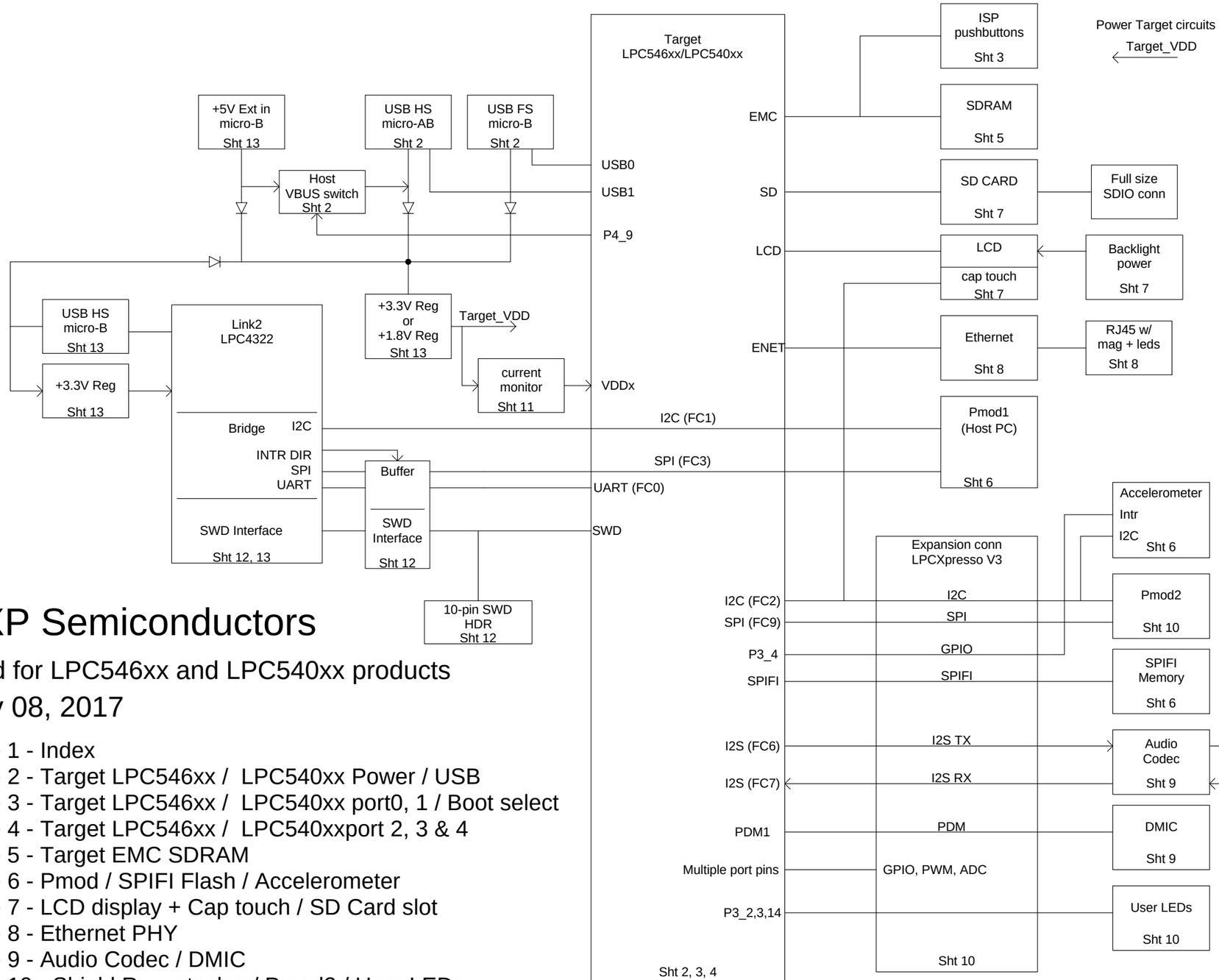

NXP Semiconductors

Used for LPC546xx and LPC540xx products

Nov 08, 2017

DWG. NO. LPC546xx / LPC540xx Brd | SH. 1 | REV E

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
1	PCB Rev 1 release; refdes renumbered	10/05/2015	
1a	U27 changed to MX25L12835FM2I-10G for 1.8V assy; sht 6.	10/14/2015	
1b	C13, C14 changed to 220pF; sht 9.	10/19/2015	
A	PCB Rev A release to production	04/19/2016	
B	Add USB0 FS Host; JP9 - JP13, U29, R119 Sht 2, 3, 4, 9	08/10/2016	
C	Add FC0 Uart to P4; Add R120; replace JP8 with JS33 - JS36. Sht 3, 4, 11	10/31/2016	
D	Correct I2C FC1 SCL, SDA at J14, JS15, JS16. Sht 6, 13 Change D5 to PESD3V3L5UY; Sht 12	06/14/2017	
E	1) Add P0_20 and P0_21 to expansion conn J10; with 0ohm solder jumpers; Sht 5,10 2) JP5 changed to TH; Sht 12	11/08/2017	

Notes:

1) "DNI" = Do Not Install by default
2) "JSx" solder jumpers use 0ohm resistor for default strapping.
3) This board design is used for LPC546xx and LPC540xx products.

CONTRACT NO.		LPC546xx / LPC540xx	
APPROVALS	DATE	**NXP** Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN d.consiglio	11/7/2017		
CHECKED			
ISSUED	11/08/2017	SIZE D / FSCM NO. / DWG. NO. LPC546xx / LPC540xx Brd	REV E
		SCALE	SHEET 1 OF 13

H=8ND; V=4LA

DWG. NO. LPC546xx / LPC540xx Brd | SH. 2 | REV E

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

Target USB HS / ENET+3.3V Power

+3.3V_USB_ENET

SHT 13 USB_HS_VBUS_TRGT — R3 470ohms — VBUS1_TARGET — R4 2.2Kohms — GND

FB2 220ohms

J2 (ZX62D-AB-5P8): SHLD5 SHLD4 SHLD2 SHLD3 SHLD1 SHLD6 — GND ID D+ D- VBUS

U2 (PRTR5V0U2X): I/O2 I/O1 VCC GND

C2 2.2uF 10V — GND

USB_HS_HOST_VBUS

C64 10uF — C81 4.7uF 10v — C80 0.1uF — C79 0.01uF — GND

+5V

+3.3V_USB_ENET — JS2 — C21 4.7uF 10v — C22 0.1uF — GND

U8 (TLV70233DBVR, 300mA): Vout Vin Gnd Ena nc NC — R7 100Kohms — C12 0.1uF — C11 4.7uF 10v — GND

USB_HS_HOST_VBUS — M15 — JP9 — HDR-1x03-SMD — USB_FS_HOST_VBUS

JP9
USBx Host VBUS –
USB1 HS —— shunt 1 - 2 (default)
USB0 FS —— shunt 2 - 3

Target Hi-SpeedUSB Device / Host Micro-AB

U25 LPC54608FET180 LPC54608FET180

USB1_DP_TRGT — USB1_DP (H3)
USB1_DM_TRGT — USB1_DM (H2)
VBUS1_TARGET — USB1_VBUS (G2)
USB1_ID_TRGT — R2 0ohms — USB1_ID (G1)
USB1_AVDDTX3V3 (H1)
USB1_AVDDC3V3 (G3)
R55 12.1Kohms — USB1_REXT (F1)
USB1_AVSSC (F2)
USB1_AVSSTX3V3 (J1)
USB0_DP_TRGT — R79 33ohms — USB0_DP (E5)
USB0_DM_TRGT — R78 33ohms — USB0_DM (D5)

USB Host power switch

VDD_TARGET — R9 100Kohms

SHT 13 +5V_EXT — U1 (NX5P2553GV): VIN VOUT EN nFAULT ILIM GND — USB_HOST_VBUS

Q1 BSS138P,215 — R1 47Kohms — GND

C6 4.7uF 10v — C8 4.7uF 10v

Current limit set to ~500mA.

SHT 13 USB_FS_VBUS_TRGT — R5 470ohms — P0_22-USB0_VBUS — SHT 3

R6 2.2Kohms — GND

FB3 220ohms

J3 (ZX62D-AB-5P8): SHLD5 SHLD4 SHLD2 SHLD3 SHLD1 SHLD6 — GND ID D+ D- VBUS

U3 (PRTR5V0U2X): I/O2 I/O1 VCC GND

C4 2.2uF 10V — GND

USB_FS_HOST_VBUS

P4_11-USB0_ID — SHT 4

Target Full-Speed USB Device / Host Micro-AB

U25 LPC54608FET180 LPC54608FET180

USB0_DP_TRGT — USB0_DP (E5)
USB0_DM_TRGT — USB0_DM (D5)

VDD_TARGET — R119 100Kohms — U29 (NX3L2267GM): VDD 1S 1Y0 1Y1 2S 2Y0 2Y1 GND 1Z 2Z

SHT 4 P4_7-USB0_PORTPWRn — SHT 4 P4_9-USB1_PORTPWRn
SHT 4 P4_8-USB0_OVRCURn — SHT 3, 10 P1_1-USER_PB-USB1_OVRCURn

JP10 HDR-1x02-SMD — M19 — GND

JP10
USBx Host Power Control Select
USB0 FS —— shunt
USB1 HS —— open (default)

ABLS2-12.000MHZ-D4Y-T — Y2 12M — C69 27pF — C70 27pF — GND

SSPT7F-12.5PF20-R — Y4 32.768k — C109 18pF 50V 5% — C110 18pF 50V 5% — GND

XTAL1 (K4) XTAL2 (J4) RTCX1 (L12) RTCX2 (K11)

VSS_0 (B3) VSS_1 (D7) VSS_2 (D8) VSS_3 (E11) VSS_4 (H5) VSS_5 (J5) VSS_6 (K7) VSSA (L5) VREFN (N4)

JS22 — C92 0.01uF — GND

ADC_VREFP — JP3 DNI — HDR-1x03 — GND

SHT 10 VBATT — D13 BAT54C — C105 0.1uF — GND

nRESET_ULP — SHT 2, 10, 12 — JS28 — JP7 DNI — HDR-1x02

SHT 6 nRESET_TRGT — RESETn (N13)

VDD_TARGET — D13 BAT54C — VBAT (N11)

SHT 11 VDD_TARGET_IC — FB8 600ohms — 3v3_TRGT_VDDREG

VDD_0 (E6) VDD_1 (E8) VDD_2 (F5) VDD_3 (G5) VDD_4 (J12) VDD_5 (L6) VDD_6 (L11)

VREFP (P6) VDDA (N6)

TRGT_VDDA — FB9 600ohms — JS23 — ADC_VREFP

C104 0.01uF — C112 4.7uF 10v — C78 0.1uF — C107 0.01uF — C111 0.1uF — C106 0.01uF — C108 0.1uF — C93 0.1uF — GND

RESET

VDD_TARGET — R97 100Kohms — R105 2.2Kohms — D15 (Red) LS Q976-NR-1

SHT 2, 10, 12 nRESET_ULP — R98 100ohms — C114 0.1uF — GND

SW1 KMR221GLFS — Shld — NC NC — GND

CONTRACT NO.		Target LPC54608 / LPC540xx Power / USB
APPROVALS	DATE	**NXP** Semiconductors
DRAWN d.consiglio	11/7/2017	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/
CHECKED		
ISSUED	11/08/2017	

SIZE	FSCM NO.	DWG. NO.	REV
D		LPC546xx / LPC540xx Brd	E

SCALE | SHEET 2 OF 13

H=8ND; V=4LA

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

VDD_TARGET

R100 2.2Kohms

R102 2.2Kohms

SHT 6 — P0_4-ISP0 — R108 2.2Kohms

SHT 6 — P0_5-ISP1 — R107 2.2Kohms

SHT 12 — P0_6-ISP2 — R116 2.2Kohms

U25
LPC54608FET180
LPC54608FET180

SHT 6, 11	P0_0-ISP_FC3_SCK	D6	P0_0/CAN1_RD/FC3_SCK/CT0MAT0/SCT_GPI0/PDM0_CLK
SHT 6, 11	P0_1-ISP_FC3_SSEL0	A1	P0_1/CAN1_TD/FC3_CTS_SDAX_SSELN0/CT0CAP0/SCT_GPI1/PDM0_DATA/
	P0_2-ISP_FC3_MISO-EMC_D0	E9	P0_2/FC3_TXD_SCL_MISO/CT0CAP1/SCT0_OUT0/SCT_GPI2//EMC_D0/TRSTN
	P0_3-ISP_FC3_MOSI-EMC_D1	A10	P0_3/FC3_RXD_SDA_MOSI/CT0MAT1/SCT0_OUT1/SCT_GPI3//EMC_D1/TCK
SHT 5	P0_4-EMC_D2	C8	P0_4/CAN0_RD/FC4_SCK/CT3CAP0/SCT_GPI4//EMC_D2/ENET_MDC/TMS
SHT 5	P0_5-EMC_D3	E7	P0_5/CAN0_TD/FC4_RXD_SDA_MOSI/CT3MAT0/SCT_GPI5//EMC_D3/ENET_MDIO/TDI
SHT 5	P0_6-EMC_D4	A5	P0_6/FC3_SCK/CT3CAP1/CT4MAT0/SCT_GPI6//EMC_D4/ENET_RX_DV/TDO
SHT 5	P0_7-EMC_D5	H12	P0_7/FC3_RTS_SCLX_SSELN1/SD_CLK/FC5_SCK/FC1_SCK/PDM1_CLK/EMC_D5/ENET_RX_CLK
SHT 5	P0_8-EMC_D6	H10	P0_8/FC3_SSELN3/SD_CMD/FC5_RXD_SDA_MOSI/SWO/PDM1_DATA/EMC_D6
SHT 5	P0_9-EMC_D7	G12	P0_9/FC3_SSELN2/SD_POW_EN/FC5_TXD_SCL_MISO//SCI1_IO/EMC_D7
SHT 12	SWO_TRGT	P2	P0_10-ADC0IN0/FC6_SCK/CT2CAP2/CT2MAT0/FC1_TXD_SCL_MISO//SWO
SHT 12	SWDCLK_TRGT	L3	P0_11-ADC0IN1/FC6_RXD_SDA_MOSI/CT2MAT2/FREQME_GPIO_CLK_A///SWCLK
SHT 12	IF_SWDIO	M3	P0_12-ADC0IN2/FC3_TXD_SCL_MISO//FREQME_GPIO_CLK_B/SCT_GPI7//SWDIO
SHT 6, 13	P0_13-ISP_FC1_SDAX	F11	P0_13/FC1_CTS_SDAX_SSELN0/UTICK_CAP0/CT0CAP0/SCT_GPI0///ENET_RXD0
SHT 6, 13	P0_14-ISP_FC1_SCLX	E13	P0_14/FC1_RTS_SCLX_SSELN1/UTICK_CAP1/CT0CAP1/SCT_GPI1///ENET_RXD1
SHT 5	P0_15-EMC_WEn	L4	P0_15-ADC0IN3/FC6_CTS_SDAX_SSELN0/UTICK_CAP2/CT4CAP0/SCT0_OUT2//EMC_WEN/ENET_TX_EN
SHT 10	P0_16-ADC0IN4	M4	P0_16-ADC0IN4/FC4_TXD_SCL_MISO/CLKOUT/CT1CAP0///EMC_CSN0/ENET_TXD0
SHT 8	P0_17-ENET_TXD1	E14	P0_17/FC4_SSELN2/SD_CARD_DET_N/SCT_GPI7/SCT0_OUT0//EMC_OEN/ENET_TXD1
SHT 5	P0_18-EMC_A0	C14	P0_18/FC4_CTS_SDAX_SSELN0/SD_WR_PRT/CT1MAT0/SCT0_OUT1/SCI1_SCLK/EMC_A0
SHT 5	P0_19-EMC_A1	C6	P0_19/FC4_RTS_SCLX_SSELN1/UTICK_CAP0/CT0MAT2/SCT0_OUT2//EMC_A1/FC7_TXD_SCL_MISO
SHT 5	P0_20-EMC_A2	D13	P0_20/FC3_CTS_SDAX_SSELN0/CT1MAT1/CT3CAP3/SCT_GPI2/SCI0_IO/EMC_A2/FC7_RXD_SDA_MOSI
SHT 5	P0_21-EMC_A3	C13	P0_21/FC3_RTS_SCLX_SSELN1/UTICK_CAP3/CT3MAT3/SCT_GPI3/SCI0_SCLK/EMC_A3/FC7_SCK
SHT 2	P0_22-USB0_VBUS	B12	P0_22/FC6_TXD_SCL_MISO/UTICK_CAP1/CT3CAP3/SCT0_OUT3///USB0_VBUS
SHT 6, 10	P0_23-SPIFI_CSn-MCLK	N7	P0_23-ADC0IN11/MCLK/CT1MAT2/CT3MAT3/SCT0_OUT4//SPIFI_CSN
SHT 6, 10	P0_24-SPIFI_IO0	M7	P0_24/FC0_RXD_SDA_MOSI/SD_D0/CT2CAP0/SCT_GPI0//SPIFI_IO0
SHT 6, 10	P0_25-SPIFI_IO1	K8	P0_25/FC0_TXD_SCL_MISO/SD_D1/CT2CAP1/SCT_GPI1//SPIFI_IO1
SHT 6, 10	P0_26-SPIFI_CLK	M13	P0_26/FC2_RXD_SDA_MOSI/CLKOUT/CT3CAP2/SCT0_OUT5/PDM0_CLK/SPIFI_CLK/USB0_IDVALUE
SHT 6, 10	P0_27-SPIFI_IO3	L9	P0_27/FC2_TXD_SCL_MISO//CT3MAT2/SCT0_OUT6//SPIFI_IO3/USB0_IDPULLUP_EN_N
SHT 6, 10	P0_28-SPIFI_IO2-USB0_OCURRn	M9	P0_28/FC0_SCK//CT2CAP3/SCT0_OUT7/TRACEDATA3/SPIFI_IO2/USB0_OVERCURRENTN
SHT 11	P0_29-ISP_FC0_RXD	B13	P0_29/FC0_RXD_SDA_MOSI//CT2MAT3/SCT0_OUT8/TRACEDATA2
SHT 11	P0_30-ISP_FC0_TXD	A2	P0_30/FC0_TXD_SCL_MISO//CT0MAT0/SCT0_OUT9/TRACEDATA1//USB1_ULPI_STP
SHT 10	P0_31-ADC0IN5	M5	P0_31-ADC0IN5/FC0_CTS_SDAX_SSELN0/SD_D2/CT0MAT1/SCT0_OUT3/TRACEDATA0//USB1_ULPI_NXT

P4

HDR-1x03

GND

U25
LPC54608FET180
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SHT 10	P1_0-ADC0IN6	N3	P1_0-ADC0IN6/FC0_RTS_SCLX_SSELN1/SD_D3/CT0CAP2/SCT_GPI4/TRACECLK//USB1_ULPI_DIR
SHT 2, 10	P1_1-USER_PB-USB1_OVRCURn	K12	P1_1-WAKEUP/FC3_RXD_SDA_MOSI//CT0CAP3/SCT_GPI5//USB1_OVERCURRENTN
SHT 9, 10	P1_2-PDM1_CLK	L14	P1_2/CAN0_TD//CT0MAT3/SCT_GPI6/PDM1_CLK//USB1_PORTPWRN
SHT 9, 10	P1_3-PDM1_DATA	J13	P1_3/CAN0_RD///SCT0_OUT4/PDM1_DATA/USB0_CONNECTN/USB0_PORTPWRN
SHT 5	P1_4-EMC_D11	D4	P1_4/FC0_SCK/SD_D0/CT2MAT1/SCT0_OUT0/FREQME_GPIO_CLK_A/EMC_D11
SHT 5	P1_5-EMC_A4	E4	P1_5/FC0_RXD_SDA_MOSI/SD_D2/CT2MAT0/SCT_GPI0//EMC_A4
SHT 5	P1_6-EMC_A5	G4	P1_6/FC0_TXD_SCL_MISO/SD_D3/CT2MAT1/SCT_GPI3//EMC_A5
SHT 5	P1_7-EMC_A6	N1	P1_7/FC0_RTS_SCLX_SSELN1/SD_D1/CT2MAT2/SCT_GPI4//EMC_A6
SHT 5	P1_8-EMC_A7	P8	P1_8/FC0_CTS_SDAX_SSELN0/SD_CLK//SCT0_OUT1/FC4_SSELN2/EMC_A7
SHT 5	P1_9-EMC_CASn	K6	P1_9/ENET_TXD0/FC1_SCK/CT1CAP0/SCT0_OUT2/FC4_CTS_SDAX_SSELN0/EMC_CASN
SHT 5	P1_10-EMC_RASn	N9	P1_10/ENET_TXD1/FC1_RXD_SDA_MOSI/CT1MAT0/SCT0_OUT3//EMC_RASN
SHT 5	P1_11-EMC_CLK0	B4	P1_11/ENET_TX_EN/FC1_TXD_SCL_MISO/CT1CAP1/USB0_VBUS//EMC_CLK0
SHT 5	P1_12-EMC_DYCSn0	K9	P1_12/ENET_RXD0/FC6_SCK/CT1MAT1/USB0_PORTPWRN/USB0_CONNECTN/EMC_DYCSN0
SHT 5	P1_13-EMC_DQM0	G10	P1_13/ENET_RXD1/FC6_RXD_SDA_MOSI/CT1CAP2/USB0_OVERCURRENTN/USB0_FRAME/EMC_DQM0
SHT 5	P1_14-EMC_DQM1	C12	P1_14/ENET_RX_DV/UTICK_CAP2/CT1MAT2/FC5_CTS_SDAX_SSELN0/USB0_LEDN/EMC_DQM1
SHT 5	P1_15-EMC_CKE0	A11	P1_15/ENET_RX_CLK/UTICK_CAP3/CT1CAP3/FC5_RTS_SCLX_SSELN1/FC4_RTS_SCLX_SSELN1/EMC_CKE0
SHT 5	P1_16-EMC_A10	B7	P1_16/ENET_MDC/FC6_TXD_SCL_MISO/CT1MAT3/SD_CMD//EMC_A10
SHT 10	P1_17-CAN1_TD	N12	P1_17/ENET_MDIO/FC6_RXD_SDA_MOSI//SCT0_OUT4/CAN1_TD/EMC_BLSN0
SHT 10	P1_18-CAN1_RD	D1	P1_18//FC8_TXD_SCL_MISO//SCT0_OUT5/CAN1_RD/EMC_BLSN1
SHT 5	P1_19-EMC_D8	L1	P1_19/FC8_SCK/SCT0_OUT7/CT3MAT1/SCT_GPI7/FC4_SCK/EMC_D8
SHT 5	P1_20-EMC_D9	M1	P1_20/FC7_RTS_SCLX_SSELN1//CT3CAP2//FC4_TXD_SCL_MISO/EMC_D9
SHT 5	P1_21-EMC_D10	N8	P1_21/FC7_CTS_SDAX_SSELN0//CT3MAT2//FC4_RXD_SDA_MOSI/EMC_D10
SHT 10	P1_22-CT2MAT3	P11	P1_22/FC8_RTS_SCLX_SSELN1/SD_CMD/CT2MAT3/SCT_GPI5/FC4_SSELN3/EMC_CKE1
SHT 5	P1_23-EMC_A11	M10	P1_23/FC2_SCK/SCT0_OUT0//ENET_MDIO/FC3_SSELN2/EMC_A11
SHT 5	P1_24-EMC_A12	N14	P1_24/FC2_RXD_SDA_MOSI/SCT0_OUT1///FC3_SSELN3/EMC_A12
SHT 5	P1_25-EMC_A13	M12	P1_25/FC2_TXD_SCL_MISO/SCT0_OUT2//UTICK_CAP0//EMC_A13
SHT 5	P1_26-EMC_A8	J10	P1_26/FC2_CTS_SDAX_SSELN0/SCT0_OUT3/CT0CAP3/UTICK_CAP1//EMC_A8
SHT 5	P1_27-EMC_A9	F10	P1_27/FC2_RTS_SCLX_SSELN1/SD_D4/CT0MAT3/CLKOUT//EMC_A9
SHT 5	P1_28-EMC_D12	E12	P1_28/FC7_SCK/SD_D5/CT0CAP2///EMC_D12
SHT 5	P1_29-EMC_D13	C11	P1_29/FC7_RXD_SDA_MOSI/SD_D6/SCT_GPI6/USB1_PORTPWRN/USB1_FRAME/EMC_D13
SHT 5	P1_30-EMC_D14	A8	P1_30/FC7_TXD_SCL_MISO/SD_D7/SCT_GPI7/USB1_OVERCURRENTN/USB1_LEDN/EMC_D14
SHT 5	P1_31-EMC_D15	C5	P1_31/MCLK//CT0MAT2/SCT0_OUT6/FC8_CTS_SDAX_SSELN0/EMC_D15

ISP2

KMR221GLFS SW2

GND — Shld — NC — NC — P0_6-ISP2

ISP1

KMR221GLFS SW3

GND — Shld — NC — NC — P0_5-ISP1

ISP0

KMR221GLFS SW4

GND — Shld — NC — NC — P0_4-ISP0

SHT 6, 11 — P0_3-ISP_FC3_MOSI — JS34 — P0_3-ISP_FC3_MOSI-EMC_D1

SHT 5 — P0_3-EMC_D1

SHT 6, 11 — P0_2-ISP_FC3_MISO — JS35 — P0_2-ISP_FC3_MISO-EMC_D0

SHT 5 — P0_2-EMC_D0

JS33
JS34, JS35, JS36

3.3V	1.8V
JS33 1-2	JS33 2-3
JS34 2-3	JS34 1-2
JS35 2-3	JS35 1-2
JS36 1-2	JS36 2-3

USER

KMR221GLFS SW5

VDD_TARGET

DNI

R117 100Kohms

R118 100ohms

GND — Shld — NC — NC — P1_1-USER_PB-USB1_OVRCURn

CONTRACT NO.		Target LPC546xx / LPC540xx port0, 1 / Boot select	
APPROVALS	DATE	**NXP** Semiconductors	
DRAWN d.consiglio	11/7/2017	411 E. Plumeria Dr	
CHECKED		San Jose, CA 95134	
ISSUED	11/08/2017	www.standardics.nxp.com/microcontrollers/	
SIZE D	FSCM NO.	DWG. NO. LPC546xx / LPC540xx Brd	REV E
SCALE		SHEET 3 OF 13	

H=8ND; V=4LA

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

U25
LPC54608FET180
LPC54608FET180

SHT 10	P2_0-ADC0IN7-PMOD2_INTR	P3
SHT 10	P2_1-CT1MAT0	P4
SHT 10	P2_2-CT1MAT1-USR_LED3	C3
SHT 7	P2_3-SD_CLK	B1
SHT 7	P2_4-SD_CMD	D3
SHT 7	P2_5-SD_POW_EN	C1
SHT 7	P2_6-SD_D0	F3
SHT 7	P2_7-SD_D1	J2
SHT 7	P2_8-SD_D2	F4
SHT 7	P2_9-SD_D3	K2
SHT 7	P2_10-SD_CDn	P1
SHT 7	P2_11-LCD_PWR	K3
SHT 7	P2_12-SPIFI_RSTn	M2
SHT 6	P2_13-LCD_DCLK	P7
SHT 7	P2_14-LCD_FP	L7
SHT 7	P2_15-LCD_AC_ENAB_M	M8
SHT 7	P2_16-LCD_LP	L8
SHT 10	P2_17-CT1CAP1-FC8_RXD	P10
SHT 9, 10	P2_18-FC7_I2S_RX_SCK	N10
SHT 9, 10	P2_19-FC7_I2S_RX_DAT	P12
SHT 9, 10	P2_20-FC7_I2S_RX_WS	P13
SHT 7	P2_21-LCD_VD3	L10
SHT 7	P2_22-LCD_VD4	K10
SHT 7	P2_23-LCD_VD5	M14
SHT 7	P2_24-LCD_VD6	K14
SHT 7	P2_25-LCD_VD7	J11
SHT 8	P2_26-ENET_PHY_RSTn	H11
SHT 7	P2_27-CT_RSTn	H14
SHT 7	P2_28-LCD_VD10	G13
SHT 7	P2_29-LCD_VD11	G11
SHT 7	P2_30-LCD_VD12	F12
SHT 7	P2_31-LCD_VD13	D14

P2_0-ADC0IN7//FC0_RXD_SDA_MOSI//CT1CAP0
P2_1-ADC0IN8//FC0_TXD_SCL_MISO//CT1MAT0
P2_2/ENET_CRS/FC3_SSELN3/SCT0_OUT6/CT1MAT1
P2_3/ENET_TXD2/SD_CLK/FC1_RXD_SDA_MOSI/CT2MAT0
P2_4/ENET_TXD3/SD_CMD/FC1_TXD_SCL_MISO/CT2MAT1
P2_5/ENET_TX_ER/SD_POW_EN/FC1_CTS_SDAX_SSELN0/CT1MAT2
P2_6/ENET_TX_CLK/SD_D0/FC1_RTS_SCLX_SSELN1/CT0CAP0
P2_7/ENET_COL/SD_D1/FREQME_GPIO_CLK_B/CT0CAP1
P2_8/ENET_RXD2/SD_D2//CT0MAT0
P2_9/ENET_RXD3/SD_D3//CT0MAT1
P2_10/ENET_RX_ER/SD_CARD_DET_N
P2_11/LCD_PWR/SD_VOLT0/USB0_IDPULLUP_EN_N//FC5_SCK
P2_12/LCD_LE/SD_VOLT1/USB0_IDVALUE//FC5_RXD_SDA_MOSI
P2_13/LCD_DCLK/SD_VOLT2/USB0_CONNECTN//FC5_TXD_SCL_MISO
P2_14/LCD_FP/USB0_FRAME/USB0_PORTPWRN/CT0MAT2/FC5_CTS_SDAX_SSELN0
P2_15/LCD_AC/USB0_LEDN/USB0_OVERCURRENTN/CT0MAT3/FC5_RTS_SCLX_SSELN1
P2_16/LCD_LP/USB1_FRAME/USB1_PORTPWRN/CT1MAT3/FC8_SCK
P2_17/LCD_CLKIN/USB1_LEDN/USB1_OVERCURRENTN/CT1CAP1/FC8_RXD_SDA_MOSI
P2_18/LCD_VD0/FC3_RXD_SDA_MOSI/FC7_SCK/CT3MAT0
P2_19/LCD_VD1/FC3_TXD_SCL_MISO/FC7_RXD_SDA_MOSI/CT3MAT1
P2_20/LCD_VD2/FC3_RTS_SCLX_SSELN1/FC7_TXD_SCL_MISO/CT3MAT2/CT4CAP0
P2_21/LCD_VD3/FC3_CTS_SDAX_SSELN0/MCLK/CT3MAT3
P2_22/LCD_VD4/SCT0_OUT7//CT2CAP0
P2_23/LCD_VD5/SCT0_OUT8
P2_24/LCD_VD6/SCT0_OUT9
P2_25/LCD_VD7/USB0_VBUS
P2_26/LCD_VD8//FC3_SCK/CT2CAP1
P2_27/LCD_VD9/FC9_SCK/FC3_SSELN2
P2_28/LCD_VD10/FC7_CTS_SDAX_SSELN0//CT2CAP2
P2_29/LCD_VD11/FC7_RTS_SCLX_SSELN1/FC8_TXD_SCL_MISO/CT2CAP3/CLKOUT
P2_30/LCD_VD12///CT2MAT2
P2_31/LCD_VD13

U25
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	P3_0-LCD_VD14-PDM0_CLK	D12
	P3_1-LCD_VD15-PDM0_DATA	D11
SHT 10	P3_2-FC9_MOSI-CT1MAT2	C10
SHT 10	P3_3-USR_LED2	A13
SHT 6, 10	P3_4-ACCL_INTR	B11
SHT 7	P3_5-LCD_VD19	B10
SHT 7	P3_6-LCD_VD20	C9
SHT 7	P3_7-LCD_VD21	B8
SHT 7	P3_8-LCD_VD22	A7
SHT 7	P3_9-LCD_VD23	C7
SHT 10	P3_10-CT3MAT0	A3
SHT 9, 10	P3_11-MCLK-PMOD2_GPIO	B2
SHT 8, 9, 10	P3_12-CLKOUT	L2
SHT 6	P3_13-BRIDGE_GPIO	H4
SHT 10	P3_14-CT3MAT1-USR_LED1	E3
SHT 7	P3_15-SD_WPn	D2
SHT 10	P3_16-GPIO_SPI_CS2	E1
SHT 10	P3_17-FC8_TXD	K1
SHT 10	P3_18-CAN0_TD	M6
SHT 10	P3_19-CAN0_RD	J3
SHT 10	P3_20-FC9_SCK	N2
SHT 10	P3_21-FC9_MOSI	P5
SHT 10	P3_22-FC9_MISO	N5
SHT 6, 7, 9, 10	P3_23-FC2_SDAX	C2
SHT 6, 7, 9, 10	P3_24-FC2_SCLX	E2
SHT 5	P3_25-EMC_A14	P9
SHT 10	P3_26-FC4_RXD	K5
SHT 10	P3_27-FC4_TXD	P14
SHT 10	P3_28-FC4_CTS_SDAX	M11
SHT 10	P3_29-FC4_RTS_SCLX	L13
SHT 10	P3_30-FC9_SSELn0	K13
SHT 7	P3_31-SCT0_OUT5_CT4MAT2	J14

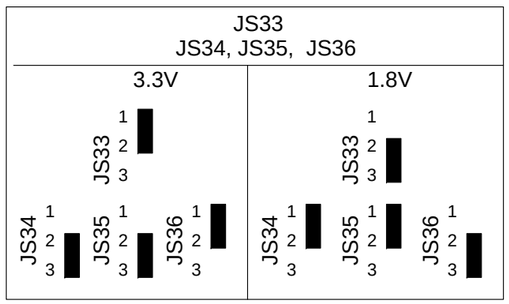
P3_0/LCD_VD14/PDM0_CLK//CT1MAT0
P3_1/LCD_VD15/PDM0_DATA//CT1MAT1
P3_2/LCD_VD16/FC9_RXD_SDA_MOSI//CT1MAT2
P3_3/LCD_VD17/FC9_TXD_SCL_MISO
P3_4/LCD_VD18//FC8_CTS_SDAX_SSELN0/CT4CAP1
P3_5/LCD_VD19//FC8_RTS_SCLX_SSELN1/CT4MAT1
P3_6/LCD_VD20/LCD_VD0//CT4MAT2
P3_7/LCD_VD21/LCD_VD1//CT4CAP2
P3_8/LCD_VD22/LCD_VD2//CT4CAP3
P3_9/LCD_VD23/LCD_VD3//CT0CAP2
P3_10/SCT0_OUT3//CT3MAT0///EMC_DYCSN1/TRACEDATA0
P3_11/MCLK/FC0_SCK/FC1_SCK////TRACEDATA3
P3_12/SCT0_OUT8//CT3CAP0//CLKOUT/EMC_CLK1/TRACECLK
P3_13/SCT0_OUT9/FC9_CTS_SDAX_SSELN0/CT3CAP1///EMC_FBCK0/TRACEDATA1
P3_14/SCT0_OUT4/FC9_RTS_SCLX_SSELN1/CT3MAT1////TRACEDATA2
P3_15/FC8_SCK/SD_WR_PRT
P3_16/FC8_RXD_SDA_MOSI/SD_D4
P3_17/FC8_TXD_SCL_MISO/SD_D5
P3_18/FC8_CTS_SDAX_SSELN0/SD_D6/CT4MAT0/CAN0_TD/SCT0_OUT5
P3_19/FC8_RTS_SCLX_SSELN1/SD_D7/CT4MAT1/CAN0_RD/SCT0_OUT6
P3_20/FC9_SCK/SD_CARD_INT_N/CLKOUT//SCT0_OUT7
P3_21-ADC0IN9/FC9_RXD_SDA_MOSI/SD_BACKEND_PWR/CT4MAT3/UTICK_CAP2
P3_22-ADC0IN10/FC9_TXD_SCL_MISO
P3_23/FC2_CTS_SDAX_SSELN0//UTICK_CAP3
P3_24/FC2_RTS_SCLX_SSELN1/CT4CAP0/USB0_VBUS
P3_25//CT4CAP2/FC4_SCK///EMC_A14
P3_26//SCT0_OUT0/FC4_RXD_SDA_MOSI///EMC_A15
P3_27//SCT0_OUT1/FC4_TXD_SCL_MISO///EMC_A16
P3_28//SCT0_OUT2/FC4_CTS_SDAX_SSELN0///EMC_A17
P3_29//SCT0_OUT3/FC4_RTS_SCLX_SSELN1///EMC_A18
P3_30/FC9_CTS_SDAX_SSELN0/SCT0_OUT4/FC4_SSELN2///EMC_A19
P3_31/FC9_RTS_SCLX_SSELN1/SCT0_OUT5/CT4MAT2//SCT_GPI0/EMC_A20

VDD_TARGET
R58 2.2Kohms
R56 2.2Kohms

SHT 7 P3_1-LCD_VD15 → JS33 pin 1
JS33 pin 2 → P3_1-LCD_VD15-PDM0_DATA
JS33 pin 3 → SHT 10 P3_1-PDM0_DATA

SHT 7 P3_0-LCD_VD14 → JS36 pin 1
JS36 pin 2 → P3_0-LCD_VD14-PDM0_CLK
JS36 pin 3 → SHT 10 P3_0-PDM0_CLK

JS33
JS34, JS35, JS36



SHT 8 P4_8-ENET_TXD0 → M17 pin 1
M17 pin 2 → JP11 pin 2 P4_8-ENET_TXD0-USB0_OVRCURn
JP11 pin 3 → SHT 2 P4_8-USB0_OVRCURn
JP11: HDR-1x03-SMD

P4_7 → JP13 pin 2
JP13 pin 1 → M16 → P4_7-ARDUINO_D8 → SHT 10
JP13 pin 3 → P4_7-USB0_PORTPWRn → SHT 2
JP13: HDR-1x03-SMD

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SHT 7	P4_0-CT_INTR	H13
SHT 9, 10	P4_1-FC6_I2S_TX_SCK	G14
SHT 9, 10	P4_2-FC6_I2S_TX_DATA	F14
SHT 9, 10	P4_3-FC6_I2S_TX_WS	F13
SHT 10	P4_4	D9
SHT 10	P4_5-CT4MAT3	E10
SHT 10	P4_6-FC9_SSELn1	D10
	P4_7	A14
	P4_8-ENET_TXD0-USB0_OVRCURn	B14
SHT 2	P4_9-USB1_PORTPWRn	A12
SHT 8	P4_10-ENET_CRS_DV	B9
	P4_11-ENET_RXD0-USB0_ID	A9
	P4_12-ENET_RXD1	A6
SHT 8	P4_13-ENET_TX_EN	B6
SHT 8	P4_14-ENET_RX_CLK	B5
SHT 8	P4_15-ENET_MDC	A4
SHT 8	P4_16-ENET_MDIO	C4

P4_0//FC6_CTS_SDAX_SSELN0/CT4CAP1//SCT_GPI1/EMC_CSN1
P4_1//FC6_SCK///SCT_GPI2/EMC_CSN2
P4_2//FC6_RXD_SDA_MOSI///SCT_GPI3/EMC_CSN3
P4_3//FC6_TXD_SCL_MISO/CT0CAP3//SCT_GPI4/EMC_DYCSN2
P4_4//FC4_SSELN3/FC0_RTS_SCLX_SSELN1//SCT_GPI5/EMC_DYCSN3
P4_5//FC9_CTS_SDAX_SSELN0/FC0_CTS_SDAX_SSELN0/CT4MAT3/SCT_GPI6/EMC_CKE2
P4_6//FC9_RTS_SCLX_SSELN1///SCT_GPI7/EMC_CKE3
P4_7//CT4CAP3/USB0_PORTPWRN/USB0_FRAME/SCT_GPI0
P4_8/ENET_TXD0/FC2_SCK/USB0_OVERCURRENTN/USB0_LEDN/SCT_GPI1
P4_9/ENET_TXD1/FC2_RXD_SDA_MOSI/USB1_PORTPWRN/USB1_FRAME/SCT_GPI2
P4_10/ENET_RX_DV/FC2_TXD_SCL_MISO/USB1_OVERCURRENTN/USB1_LEDN/SCT_GPI3
P4_11/ENET_RXD0/FC2_CTS_SDAX_SSELN0/USB0_IDVALUE//SCT_GPI4
P4_12/ENET_RXD1/FC2_RTS_SCLX_SSELN1/USB0_IDPULLUP_EN_N//SCT_GPI5
P4_13/ENET_TX_EN/CT4MAT0/USB0_CONNECTN//SCT_GPI6
P4_14/ENET_RX_CLK/CT4MAT1/FC9_SCK//SCT_GPI7
P4_15/ENET_MDC/CT4MAT2/FC9_RXD_SDA_MOSI
P4_16/ENET_MDIO/CT4MAT3/FC9_TXD_SCL_MISO

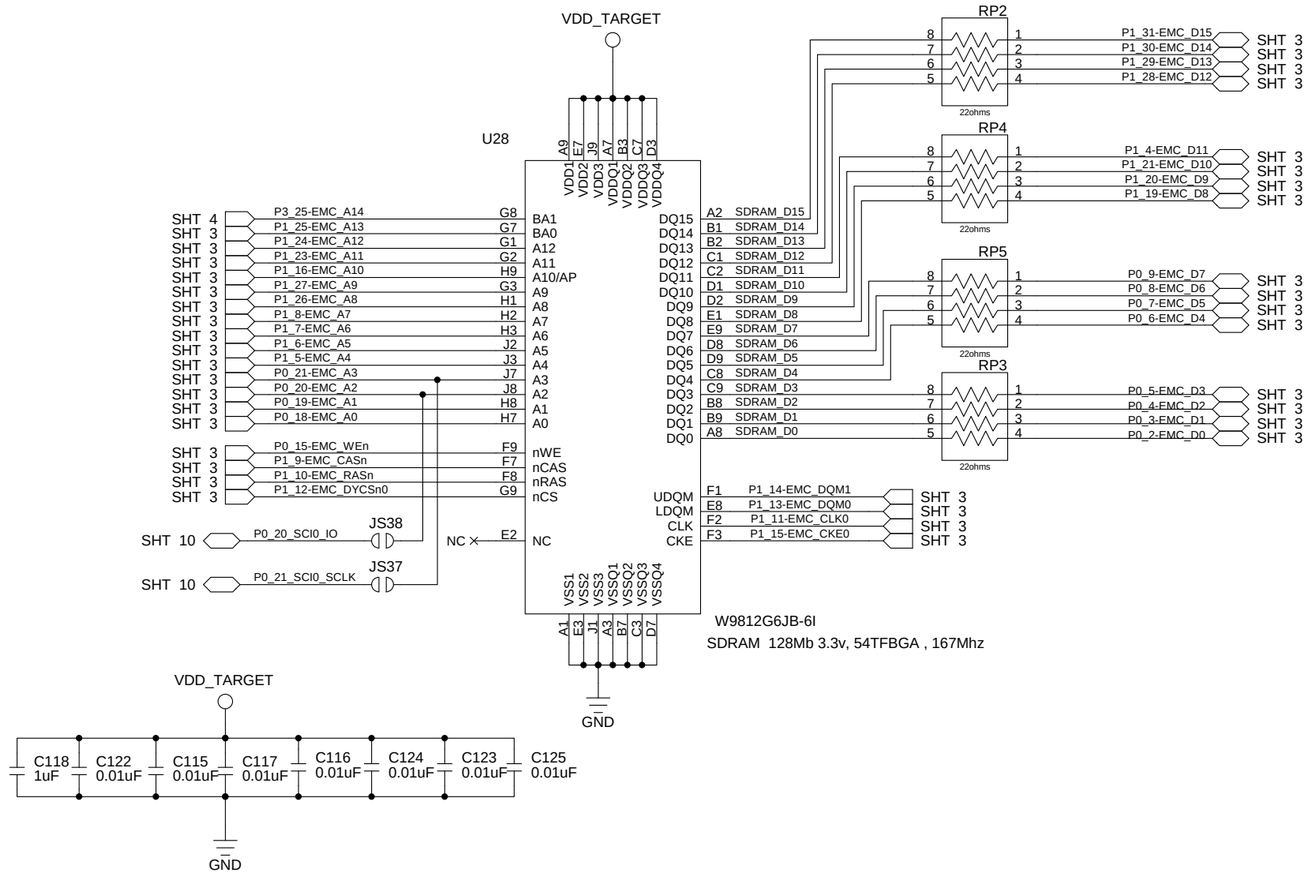
SHT 8 P4_11-ENET_RXD0 → M18 pin 1
M18 pin 2 → JP12 pin 2 P4_11-ENET_RXD0-USB0_ID
JP12 pin 3 → SHT 2 P4_11-USB0_ID
JP12: HDR-1x03-SMD

CONTRACT NO.		Target LPC546xx / LPC540xx port 2, 3 & 4	
APPROVALS	DATE	**NXP** Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN d.consiglio	11/7/2017		
CHECKED			
ISSUED	11/08/2017	SIZE D / FSCM NO. / DWG. NO. LPC546xx / LPC540xx Brd / REV E	
		SCALE	SHEET 4 OF 13

H=8ND; V=4LA

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

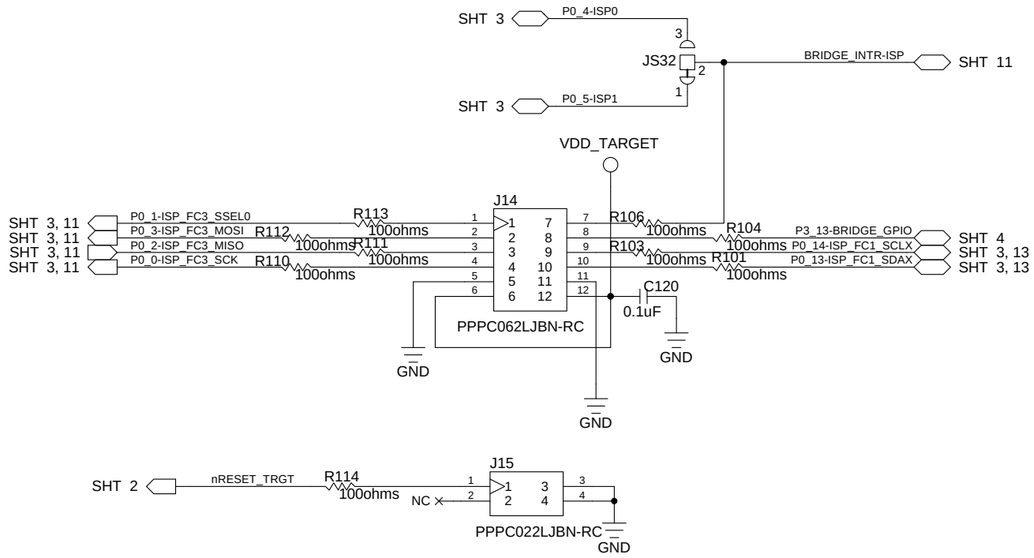


CONTRACT NO.		Target EMC SDRAM
APPROVALS	DATE	**NXP** Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/
DRAWN d.consiglio	11/7/2017	
CHECKED		
ISSUED	11/08/2017	SIZE D | FSCM NO. | DWG. NO. LPC546xx / LPC540xx Brd | REV E
		SCALE | SHEET 5 OF 13

REVISIONS

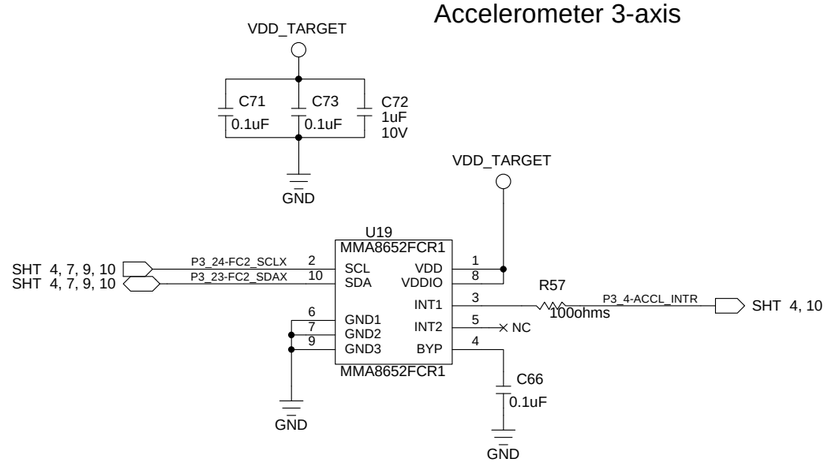
REV	DESCRIPTION	DATE	APPROVED

SPI / I2C header (PMOD compatible) Host interface



PMOD pin function	LPC546xx/540xx supported function
Pin 1: GPIO/SPI-SSEL(out)/UART-CTS(in)	GPIO/SPI-SSEL(in/out)
Pin 2: GPIO/SPI-MOSI(out)/UART-TXD(out)	GPIO/SPI-MOSI(in/out)
Pin 3: GPIO/SPI-MISO(in)/UART-RXD(in)	GPIO/SPI-MISO(out/in)
Pin 4: GPIO/SPI-SCK(out)/UART-RTS(out)	GPIO/SPI-SCK(in/out)
Pin 5: GND	GND
Pin 6: VCC(3.3V)	VCC(3.3V)
Pin 7: GPIO/INT(in)	GPIO/INT(out/in)
Pin 8: GPIO/RESET(out)	GPIO/RESET(out)
Pin 9: GPIO/SCL	SCL
Pin 10:GPIO/SDA	SDA
Pin 11:GND	GND
Pin 12:VCC(3.3V)	VCC(3.3V)

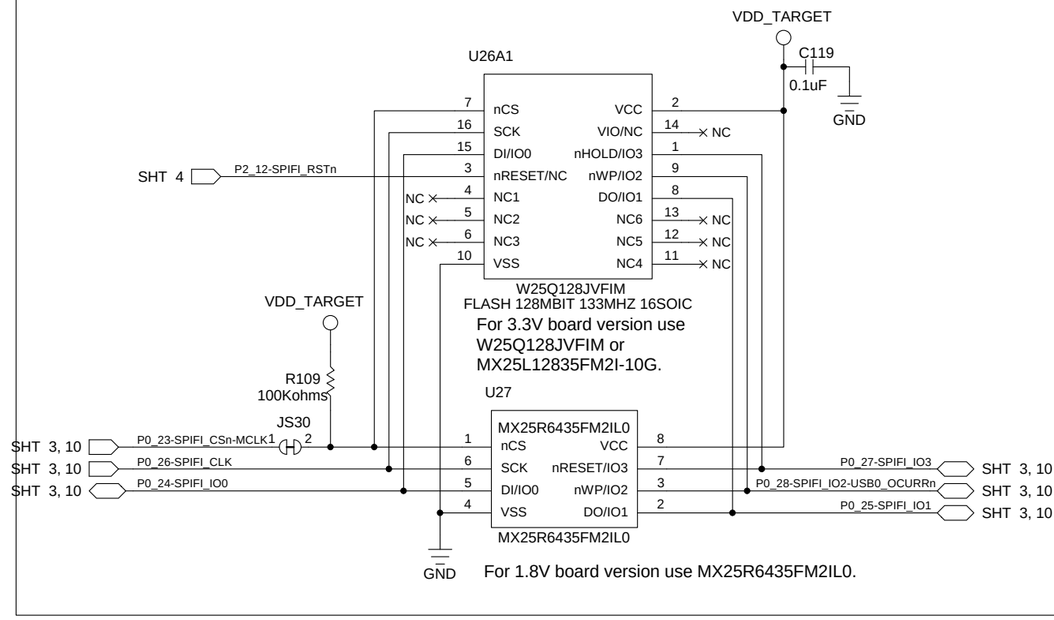
Accelerometer 3-axis



Accel I2C addrs = 0b0011101

QSPI (SPIFI) NOR Flash

SO16 pkg / SO8 pkg mutually exclusive



CONTRACT NO.		Pmod / SPIFI Flash / Accelerometer
APPROVALS	DATE	**NXP** Semiconductors
DRAWN d.consiglio	11/7/2017	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/
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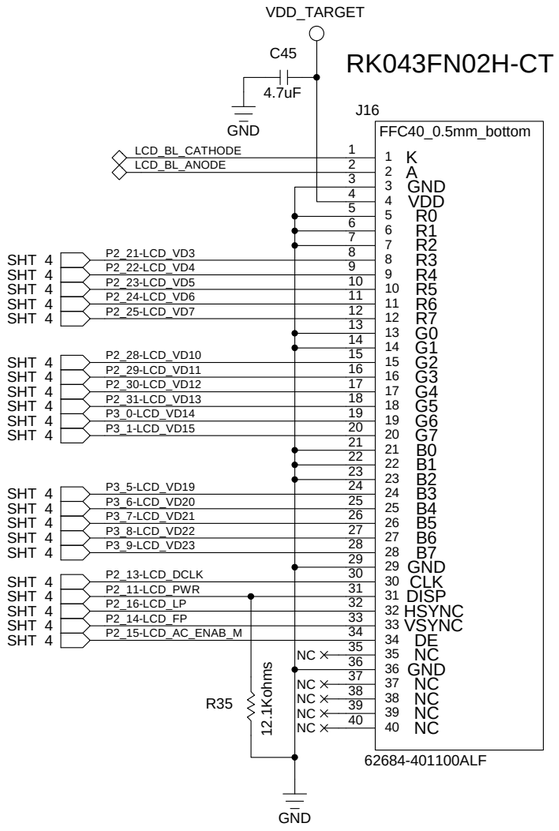
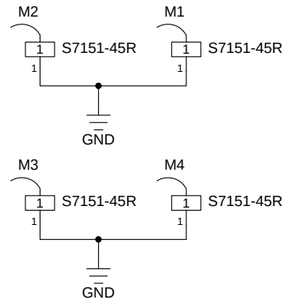
ISSUED	11/08/2017	SIZE D | FSCM NO. | DWG. NO. LPC546xx / LPC540xx Brd | REV E
		SCALE | SHEET 6 OF 13

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

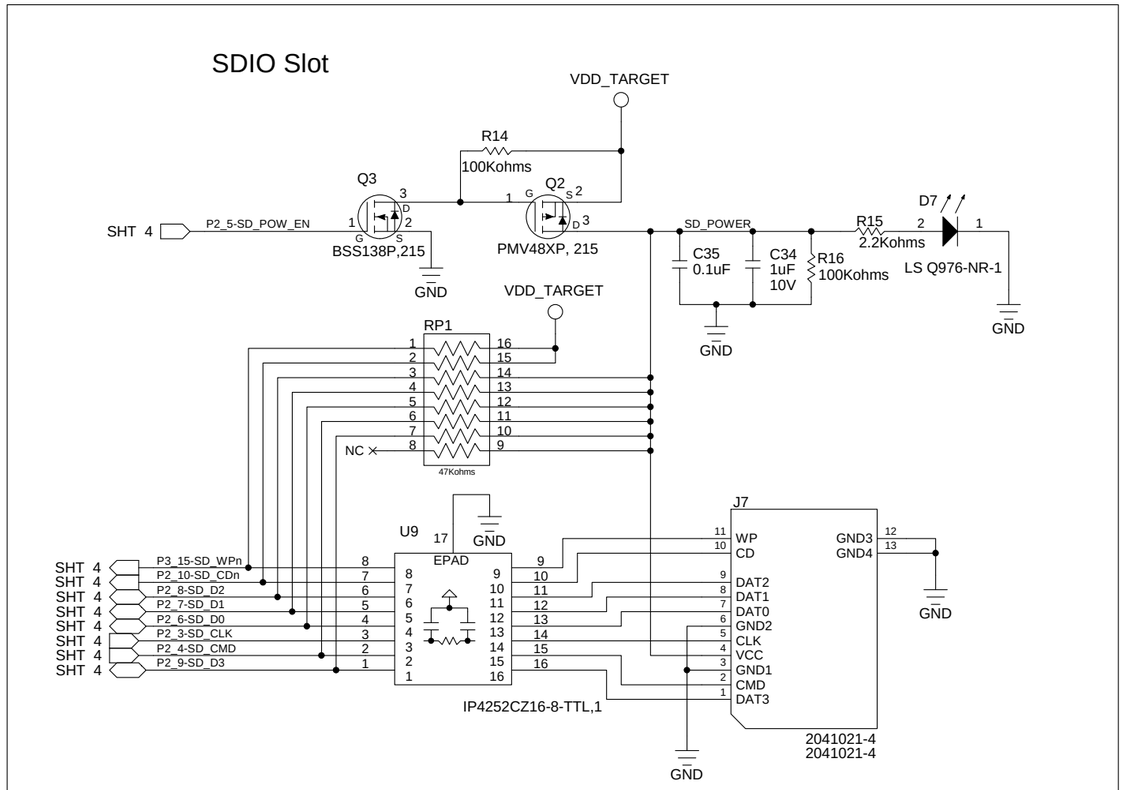
RK043FN02H-CT LCD display



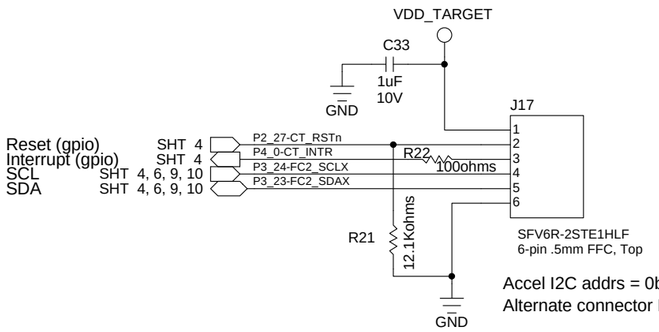


EMI shield fingers to
tie LCD enclosure to GND.

SDIO Slot

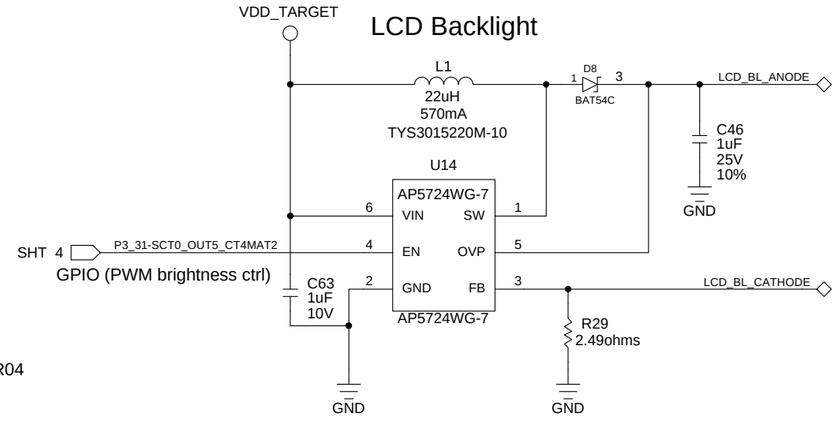


Cap Touch RK043FN02H-CT LCD display

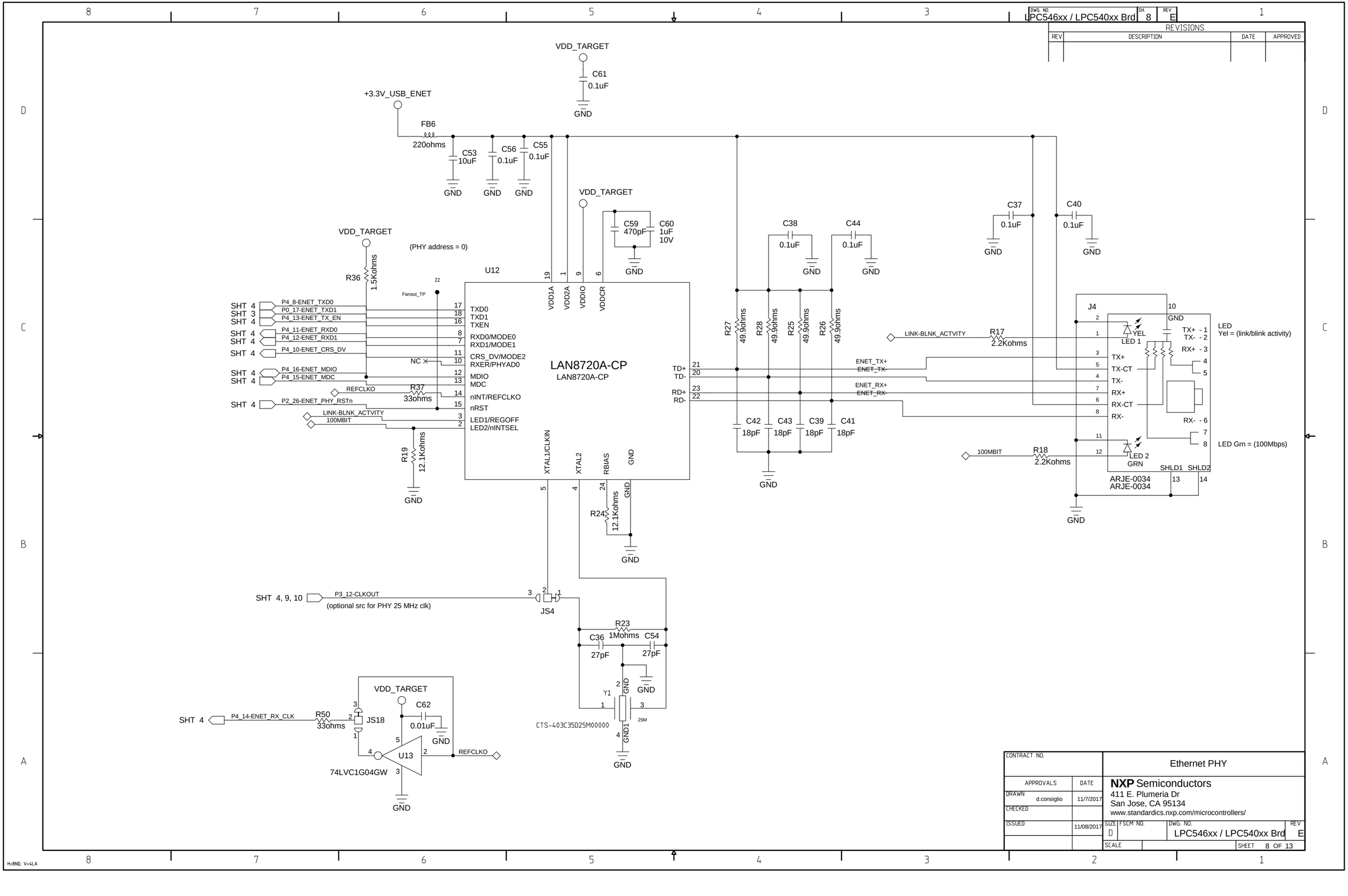


Accel I2C addrs = 0b0111000
Alternate connector MTCONN FP520T1-06GR04

LCD Backlight



CONTRACT NO.		LCD display + Cap touch / SD Card slot	
APPROVALS	DATE	**NXP** Semiconductors	
DRAWN d.consiglio	11/7/2017	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
CHECKED			
ISSUED	11/08/2017	SIZE D	FSCM NO.	DWG. NO. LPC546xx / LPC540xx Brd	REV E
		SCALE		SHEET 7 OF 13	



CONTRACT NO.				Ethernet PHY	
APPROVALS	DATE	**NXP** Semiconductors			
DRAWN d.consiglio	11/7/2017	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/			
CHECKED					
ISSUED	11/08/2017	SIZE: D	FSCM NO.	DWG. NO.: LPC546xx / LPC540xx Brd	REV: E
		SCALE		SHEET 8 OF 13	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

H=8ND; V=4LA

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

+5V

U4

MIC5366-1.8YC5 TR

C10 1uF 10V

C3 1uF 10V

+1.8V

VDD_CODEC

FB7 600ohms

FB5 600ohms

C50 0.1uF

C25 0.1uF

C51 4.7uF

C31 0.1uF

C49 4.7uF

U10

WM8904CGEFL/V

R30 33ohms ALT_MCLKOUT

C29 2.2uF

C28 2.2uF

C30 2.2uF 10V

R31 33ohms

VDD_TARGET

VDD_CODEC

JS13 JS12 JS11 JS6 JS7 JS9 JS8 JS5 JS10

SHT 4, 6, 7, 10 P3_23-FC2_SDAX

SHT 4, 6, 7, 10 P3_24-FC2_SCLX

SHT 4, 10 P4_1-FC6_I2S_TX_SCK

SHT 4, 10 P4_3-FC6_I2S_TX_WS

SHT 4, 10 P4_2-FC6_I2S_TX_DATA

SHT 4, 10 P2_19-FC7_I2S_RX_DAT

SHT 4, 10 P2_18-FC7_I2S_RX_SCK

SHT 4, 10 P2_20-FC7_I2S_RX_WS

R86 100ohms

R87 100ohms

SHT 4, 10 P3_11-MCLK-PMOD2_GPIO

SHT 4, 8, 10 P3_12-CLKOUT

Codec I2C addrs = 0b0011010

Audio Line In

LININL C24 4.7uF

LININR C23 4.7uF

R12 47Kohms

R13 47Kohms

C17 220pF

C18 220pF

D4 PESD5V0S2BT

J5 SJ-3524-SMT

Line out / headphone out

HP_OUTL

HP_OUTR

C27 0.1uF

C26 0.1uF

R11 20ohms

R10 20ohms

C13 220pF

C14 220pF

D1 PESD5V0S2BT

J6 SJ-3524-SMT

GND pour in audio analog area tied to HPOUTFB pin.

DMIC

VDD_TARGET

JS29

DMIC1

SPH0641LM4H

SHT 3, 10 P1_2-PDM1_CLK

SHT 3, 10 P1_3-PDM1_DATA

JS31

R115 33ohms

C121 0.01uF

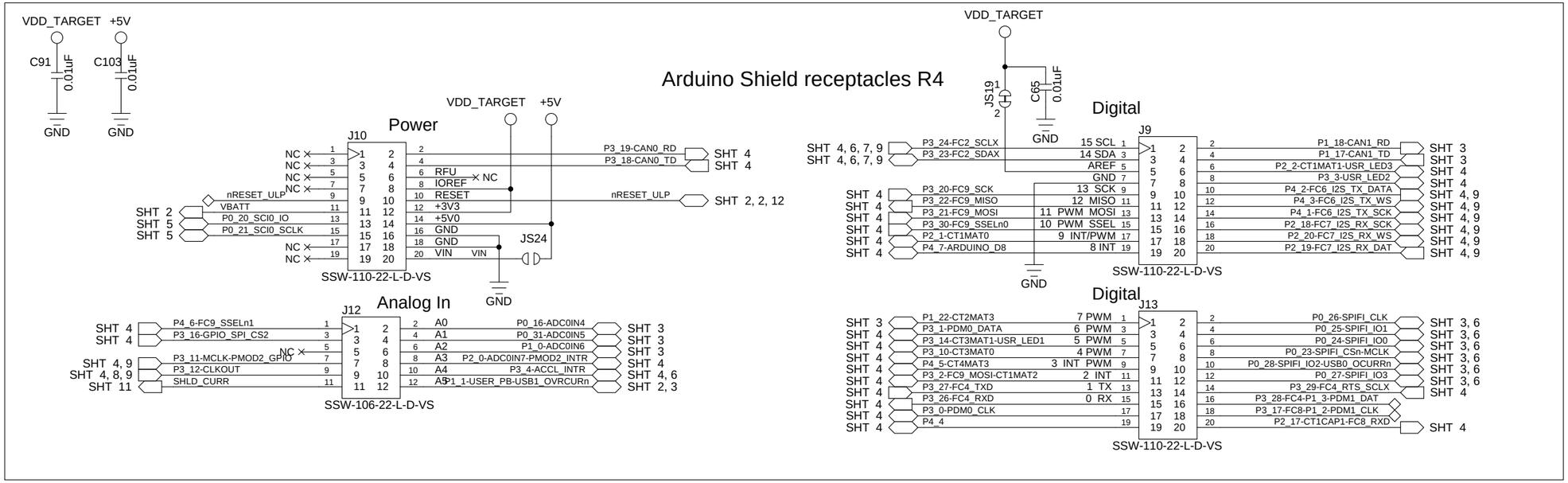
CONTRACT NO.		Audio Codec / DMIC	
APPROVALS	DATE	**NXP** Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN d.consiglio	11/7/2017		
CHECKED			
ISSUED	11/08/2017	SIZE D / FSCM NO. / DWG. NO. LPC546xx / LPC540xx Brd / REV E	
		SCALE / SHEET 9 OF 13	

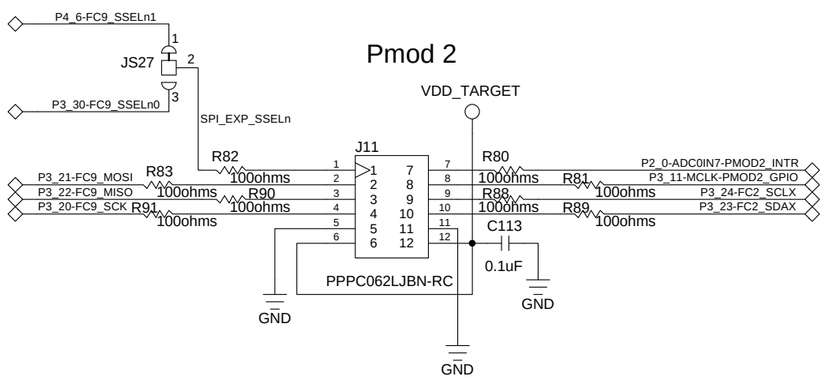
H:8ND; V:4LA

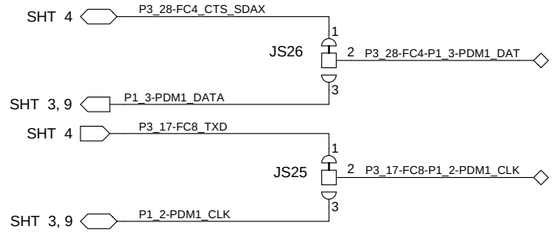
REVISIONS

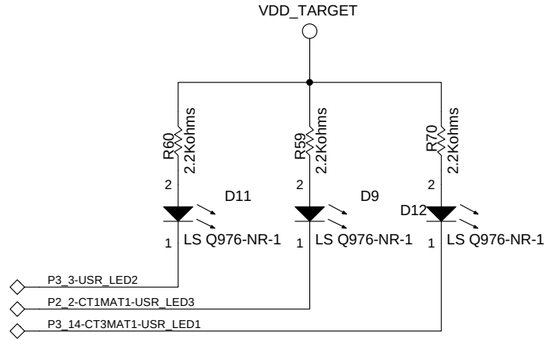
REV	DESCRIPTION	DATE	APPROVED

Arduino Shield receptacles R4







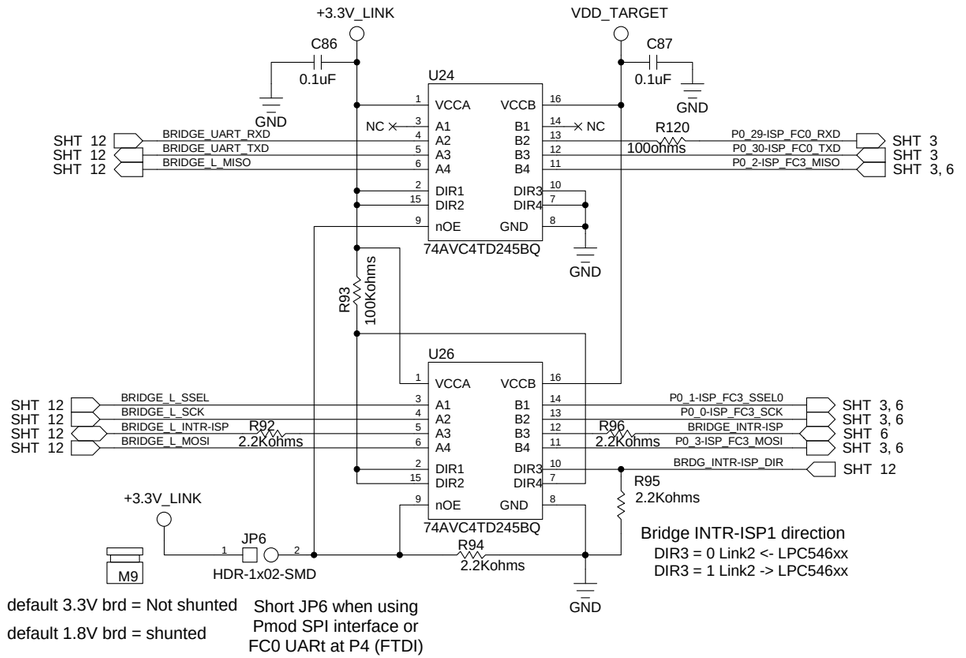


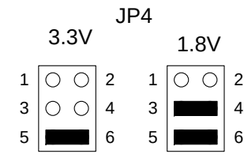
CONTRACT NO.		Shield Receptacles / Pmod2 / User LEDs	
APPROVALS	DATE	**NXP** Semiconductors	
DRAWN d.consiglio	11/7/2017	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
CHECKED			
ISSUED	11/08/2017	SIZE D / FSCM NO. / DWG. NO. LPC546xx / LPC540xx Brd / REV E	
		SCALE / SHEET 10 OF 13	

H=8ND; V=4LA

LPC546xx/540xx				
LPC546xx/540xx				ADC111S021 12bit ADC
Vsense (1) voltage 1-lsb	JP4.3/4 open LPC546xx LPC540xx	JP4.3/4 shunted LPC546xx LPC540xx	maximum current	ADC input 1- lsb 800uV
32uV	16uA	32uA	65mA	

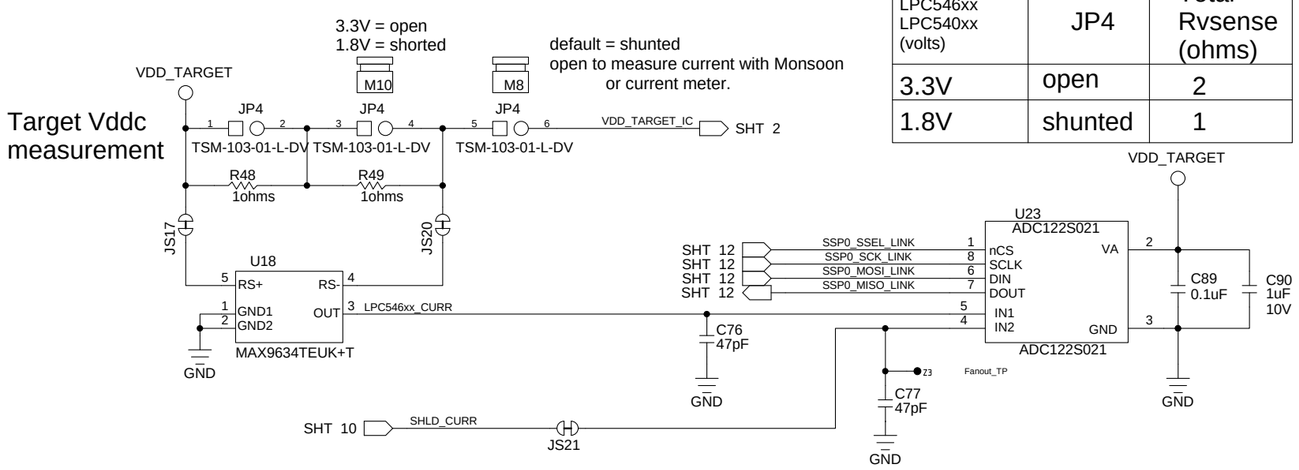
(1) Vsense voltage is between U18 RS+ to RS-. Total Rvsense = R48 + (R49 || JP4.5/6).





JP4 Setting

VDD LPC546xx LPC540xx (volts)	JP4	Total Rvsense (ohms)
3.3V	open	2
1.8V	shunted	1



CONTRACT NO.		LPC546xx / LPC540xx current monitor LINK2 Bridge buffer	
APPROVALS	DATE	**NXP** Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
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REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

H=8ND; V=4LA

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

U21
LPC4322JET100
LPC4322JET100

TRACE_D0 G2
TRACE_D1 G1
P0[0]_/GPIO0[0]/SSP1_MISO/ENET_RXD1/SGPIO0
P0[1]_/GPIO0[1]/SSP1_MOSI/ENET_TXEN/SGPIO1

NC CUR_MEAS_SEL H1
BOOT0_LED K2
BOOT1 K1
SHT 11 BRIDGE_L_MISO J1
SHT 11 BRIDGE_L_MOSI J2
TMS_SWDIO_TXEN J4
TMS_SWDIO K4
G4
NC H5
SHT 11 BRIDGE_L_INTR-ISP J5
H6
NC
SHT 11 BRDG_INTR-ISP_DIR J7
TRACE_CLK K7
H8
NC J8
TDO_SWO
TRACE_D2 K8
TRACE_D3 H9
TCK_SWCLK H10
JTAG_TDI J10
SHT 11 BRIDGE_L_SCK K9
SHT 11 BRIDGE_L_SSEL K10

P1[0]_/GPIO0[4]/CTIN_3/EXTBUS_A5
P1[1]_/GPIO0[8]/CTOUT_7/EXTBUS_A6/SGPIO8
P1[2]_/GPIO0[9]/CTOUT_6/EXTBUS_A7/SGPIO9
P1[3]_/GPIO0[10]/CTOUT_8/SGPIO10/EXTBUS_OE
P1[4]_/GPIO0[11]/CTOUT_9/SGPIO11/EXTBUS_BLS0
P1[5]_/GPIO1[8]/CTOUT_10/NC/EXTBUS_CS0
P1[6]_/GPIO1[9]/CTIN_5/NC/EXTBUS_WE
P1[7]_/GPIO1[0]/U1_DSR/CTOUT_13/EXTBUS_D0
P1[8]_/GPIO1[1]/U1_DTR/CTOUT_12/EXTBUS_D1
P1[9]_/GPIO1[2]/U1_RTS/CTOUT_11/EXTBUS_D2
P1[10]_/GPIO1[3]/U1_RI/CTOUT_14/EXTBUS_D3
P1[11]_/GPIO1[4]/U1_CTS/CTOUT_15/EXTBUS_D4
P1[12]_/GPIO1[5]/U1_DCD/NC/EXTBUS_D5
P1[13]_/GPIO1[6]/U1_TXD/NC/EXTBUS_D6
P1[14]_/GPIO1[7]/U1_RXD/NC/EXTBUS_D7
P1[15]_/GPIO0[2]/U2_TXD/SGPIO2/ENET_RXD0
P1[16]_/GPIO0[3]/U2_RXD/SGPIO3/ENET_RX_DV
P1[17]_/GPIO0[12]/U2_UCLK/NC/ENET_MDIO
P1[18]_/GPIO0[13]/U2_DIR/NC/ENET_TXD0
P1[19]_/ENET_TX_REF_CLK/SSP1_SCK/CLKOUT/I2S1_RX_SCK
P1[20]_/GPIO0[15]/SSP1_SSEL/NC/ENET_TXD1

U21
LPC4322JET100
LPC4322JET100

SHT 11 BRIDGE_UART_RXD G10
SHT 11 BRIDGE_UART_TXD G7
NC TARGET_UART_CTRL F5
NC D8
NC D9
NC D10
JTAG_RESET G9
JTAG_RESET_TXEN C10
Link2_ISP_BOOT C6
BOOT2 B10
BOOT3 E8
NC A9
ISP_CTRL B9
IF_DETECT R42 NC A10
1.5Kohms
NC A8
NC F7
NC G6
NC A7
SHT 11 SSP0_SCK_LINK B8
NC B7
NC C7
SHT 11 SSP0_MISO_LINK D7
SHT 11 SSP0_MOSI_LINK E7
SHT 11 SSP0_SSEL_LINK

P2[0]_/SGPIO4/U0_TXD/EXTBUS_A13/USB0_PWR_EN
P2[1]_/SGPIO5/U0_RXD/EXTBUS_A12/USB0_PWR_FAULT
P2[2]_/SGPIO6/U0_UCLK/EXTBUS_A11/USB0_IND1
P2[3]_/SGPIO12/I2C1_SDA/U3_TXD/CTIN_1
P2[4]_/SGPIO13/I2C1_SCL/U3_RXD/CTIN_0
P2[5]_/SGPIO14/CTIN_2/USB1_VBUS/ADCTRIG1
P2[6]_/SGPIO7/U0_DIR/EXTBUS_A10/USB0_IND0
P2[7]_/GPIO0[7]/CTOUT_1/U3_UCLK/EXTBUS_A9
P2[8]_/SGPIO15/CTOUT_0/U3_DIR/EXTBUS_A8/GPIO5[7]
P2[9]_/GPIO1[10]/CTOUT_3/U3_BAUD3/EXTBUS_A0
P2[10]_/GPIO0[14]/CTOUT_2/U2_TXD/EXTBUS_A1
P2[11]_/GPIO1[11]/CTOUT_5/U2_RXD/EXTBUS_A2
P2[12]_/GPIO1[12]/CTOUT_4/NC/EXTBUS_A3
P2[13]_/GPIO1[13]/CTIN_4/NC/EXTBUS_A4

P3[0]_/I2S0_RX_SCK/I2S0_RX_MCLK/I2S0_TX_SCK/I2S0_TX_MCLK
P3[1]_/I2S0_TX_WS/I2S0_RX_WS/CAN0_RD/USB1_IND1/GPIO5[8]
P3[2]_/I2S0_TX_SDA/I2S0_RX_SDA/CAN0_TD/USB1_IND0/GPIO5[9]
SHT 11 P3[3]_//SPI_SCK/SSP0_SCK/SPIFI_SCK
P3[4]_/GPIO1[14]///SPIFI_SIO3
P3[5]_/GPIO1[15]///SPIFI_SIO2
SHT 11 P3[6]_/GPIO0[6]/SPI_MISO/SSP0_SSEL/SPIFI_MISO
SHT 11 P3[7]_//SPI_MOSI/SSP0_MISO/SPIFI_MOSI
SHT 11 P3[8]_//SPI_SSEL/SSP0_MOSI/SPIFI_CS

U21
LPC4322JET100
LPC4322JET100

NC H7
NC G5
NC J9
NC F6
NC F9
F8
C9
NC H4

P6[0]_/I2S0_RX_MCLK///I2S0_RX_SCK
P6[1]_/GPIO3[0]/EXTBUS_nDYCS1/U0_UCLK/I2S0_RX_WS
P6[2]_/GPIO3[1]/EXTBUS_CKEOUT1/U0_DIR/I2S0_RX_SDA
P6[4]_/GPIO3[3]/CTIN_6/U0_TXD/EXTBUS_nCAS
P6[5]_/GPIO3[4]/CTOUT_6/U0_RXD/EXTBUS_nRAS
P6[9]_/GPIO3[5]/NC/NC/EXTBUS_nDYCS0
P6[11]_/GPIO3[7]/NC/NC/EXTBUS_CKEOUT0
PF[4]_/SSP1_SCK/SPIFI_CLKIN/TRACECLK///I2S_TX_MCLK/I2S_RX_MCLK

R67 DNI 2.2Kohms
R52 DNI 2.2Kohms
R53 DNI 2.2Kohms
R51 2.2Kohms
GND

+3.3V_LINK
R65 2.2Kohms
R63 2.2Kohms
BOOT0_LED
BOOT1
BOOT2
BOOT3
R62 2.2Kohms
R84 2.2Kohms
R64 2.2Kohms
defualt shunt on
M13
JP5
Link2_ISP_BOOT
HDR-1x02
D10
LS Q976-NR-1
GND
GND

Short JP5 to force DFU boot mode to
(re-program LPC4322 internal flash)

Link2
LPC4322 Boot mode
DFU USB0 = B3:0 = 0101

VDD_TARGET
M11
JP2
HDR-1x03-SMD
D6
PMEG1020EJ

Buffer Pwr Select (JP2)
On-board Target 1 - 2 (default)
Off-board Target 2 - 3

+3.3V_LINK
U17
74AVC2T45DP
TCK_SWCLK
JTAG_TDI
R68 100Kohms
R47 100ohms
R54 100ohms
IF_TCK_SWCLK
IF_JTAG_TDI
C68 0.1uF
GND

U20
74LVC1T45GW
TDO_SWO
C74 0.1uF
R69 100Kohms
IF_TDO_SWO

U22
74LVC1T45GW
TMS_SWDIO
C75 0.1uF
R75 100Kohms
R76 100ohms
IF_SWDIO
TMS_SWDIO_TXEN
R77 2.2Kohms

U11
74LVC1T45GW
JTAG_RESET
C57 0.1uF
R32 100Kohms
R33 100ohms
IF_RST
JTAG_RESET_TXEN
R34 2.2Kohms

+3.3V_LINK
U15
74LVC1G07GW
ISP_CTRL
R45 100ohms
IF_ISPEN

Target
LPC546xx/540xx
SWD Debug

C58 10uF
P1
FTSH-105-01-L-DV-K
IF_SWDIO
IF_TCK_SWCLK
IF_TDO_SWO
IF_JTAG_TDI
IF_RST
SHT 3

D5
PESD3V3L5UY
IF_JTAG_TDI
IF_RST
IF_TDO_SWO
IF_SWDIO
IF_TCK_SWCLK
IF_DETECT
JS14

VDD_TARGET
U16
NX3DV2567GU,115
R20 100Kohms
IF_TCK_SWCLK
IF_RST
IF_TDO_SWO
NC
SWDCLK_TRGT
nRESET_ULP
SWO_TRGT
SHT 3
SHT 2, 2, 10
SHT 3
SHT 3
M12
defualt open
JP1
HDR-1x02-SMD

Link2 probe connected to: (JP1)
On-board Target - open (default)
Off-board Target - short

TRACE_CLK R43 DNI 0ohms NC
TRACE_D0 R40 DNI 0ohms NC
TRACE_D1 R39 DNI 0ohms NC
TRACE_D2 R44 DNI 0ohms NC
TRACE_D3 R41 DNI 0ohms NC

LPC546xx/LPC540xx

IF_ISPEN R46 0ohms P0_6-ISP2 SHT 3

CONTRACT NO.		LINK2 LPC4322 Peripherals / debug buffer	
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		SCALE / SHEET 12 OF 13	

H=8ND; V=4LA

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

External +5V Power Micro-B

Link +3.3V Power

LINK USB Device Micro-B

Target Power

3.3V - AP2114H-3.3TRG1

1.8V - AP2114H-1.8TRG1

Power-On LED

GND TP

CONTRACT NO.	LINK2 LPC4322 / LINK2 USB / Board Power
APPROVALS / DATE	**NXP** Semiconductors
DRAWN d.consiglio 11/7/2017	411 E. Plumeria Dr
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SIZE D / FSCM NO. / DWG. NO. LPC546xx / LPC540xx Brd / REV E	
SCALE	SHEET 13 OF 13

H=8ND; V=4LA