9.13.19 Dynamic Memory Configuration registers

The EMCDynamicConfig0-3 registers enable you to program the configuration information for the relevant dynamic memory chip select. These registers are normally only modified during system initialization. These registers are accessed with one wait state.

Table 133 shows the bit assignments for the EMCDynamicConfig0-3 registers.

Table 133. Dynamic Memory Configuration registers (DYNAMICCONFIG[0:3], address 0x2009 C100 (DYNAMICCONFIG0), 0x2009 C120 (DYNAMICCONFIG1), 0x2009 C140 (DYNAMICCONFIG2), 0x2009 C160 (DYNAMICCONFIG3)) bit description

Bit	Symbol	Value	Description	Reset Value
2:0	-		Reserved. Read value is undefined, only zero should be written.	NA
4:3	MD		Memory device.	0
		0x0	SDRAM (POR reset value).	
		0x1	Low-power SDRAM.	
		0x2	Reserved.	
		0x3	Reserved.	
6:5	-		Reserved. Read value is undefined, only zero should be written.	NA
12:7	AM0		See Table 134. 000000 = reset value.[1]	0
13	-		Reserved. Read value is undefined, only zero should be written.	NA
14	AM1		See Table 134. 0 = reset value.	0
18:15	-		Reserved. Read value is undefined, only zero should be written.	NA
19	B		Buffer enable.	0
		0	Buffer disabled for accesses to this chip select (POR reset value).	
		1	Buffer enabled for accesses to this chip select.[2]	
20	P		Write protect.	0
		0	Writes not protected (POR reset value).	
		1	Writes protected.	
31:21	-		Reserved. Read value is undefined, only zero should be written.	NA

[1] The SDRAM column and row width and number of banks are computed automatically from the address mapping.

[2] The buffers must be disabled during SDRAM initialization. The buffers must be enabled during normal operation.

Address mappings that are not shown in Table 134 are reserved.

Table 134. Address mapping

14	12	11:9	8:7	Description
16 bit external bus address mapping (Row, Bank, Column)				
0	0	000	00	16 Mbit (2Mx8), 2 banks, row length = 11, column length = 9
0	0	000	01	16 Mbit (1Mx16), 2 banks, row length = 11, column length = 8
0	0	001	00	64 Mbit (8Mx8), 4 banks, row length = 12, column length = 9
0	0	001	01	64 Mbit (4Mx16), 4 banks, row length = 12, column length = 8
0	0	010	00	128 Mbit (16Mx8), 4 banks, row length = 12, column length = 10
0	0	010	01	128 Mbit (8Mx16), 4 banks, row length = 12, column length = 9
0	0	011	00	256 Mbit (32Mx8), 4 banks, row length = 13, column length = 10

Table 134. Address mapping

14	12	11:9	8:7	Description
0	0	011	01	256 Mbit (16Mx16), 4 banks, row length = 13, column length = 9
0	0	100	00	512 Mbit (64Mx8), 4 banks, row length = 13, column length = 11
0	0	100	01	512 Mbit (32Mx16), 4 banks, row length = 13, column length = 10
16 bit external bus address mapping (Bank, Row, Column)				
0	1	000	00	16 Mbit (2Mx8), 2 banks, row length = 11, column length = 9
0	1	000	01	16 Mbit (1Mx16), 2 banks, row length = 11, column length = 8
0	1	001	00	64 Mbit (8Mx8), 4 banks, row length = 12, column length = 9
0	1	001	01	64 Mbit (4Mx16), 4 banks, row length = 12, column length = 8
0	1	010	00	128 Mbit (16Mx8), 4 banks, row length = 12, column length = 10
0	1	010	01	128 Mbit (8Mx16), 4 banks, row length = 12, column length = 9
0	1	011	00	256 Mbit (32Mx8), 4 banks, row length = 13, column length = 10
0	1	011	01	256 Mbit (16Mx16), 4 banks, row length = 13, column length = 9
0	1	100	00	512 Mbit (64Mx8), 4 banks, row length = 13, column length = 11
0	1	100	01	512 Mbit (32Mx16), 4 banks, row length = 13, column length = 10
32 bit external bus address mapping (Row, Bank, Column)				
1	0	000	00	16 Mbit (2Mx8), 2 banks, row length = 11, column length = 9
1	0	000	01	16 Mbit (1Mx16), 2 banks, row length = 11, column length = 8
1	0	001	00	64 Mbit (8Mx8), 4 banks, row length = 12, column length = 9
1	0	001	01	64 Mbit (4Mx16), 4 banks, row length = 12, column length = 8
1	0	001	10	64 Mbit (2Mx32), 4 banks, row length = 11, column length = 8
1	0	010	00	128 Mbit (16Mx8), 4 banks, row length = 12, column length = 10
1	0	010	01	128 Mbit (8Mx16), 4 banks, row length = 12, column length = 9
1	0	010	10	128 Mbit (4Mx32), 4 banks, row length = 12, column length = 8
1	0	011	00	256 Mbit (32Mx8), 4 banks, row length = 13, column length = 10
1	0	011	01	256 Mbit (16Mx16), 4 banks, row length = 13, column length = 9
1	0	011	10	256 Mbit (8Mx32), 4 banks, row length = 13, column length = 8
1	0	100	00	512 Mbit (64Mx8), 4 banks, row length = 13, column length = 11
1	0	100	01	512 Mbit (32Mx16), 4 banks, row length = 13, column length = 10
32 bit external bus address mapping (Bank, Row, Column)				
1	1	000	00	16 Mbit (2Mx8), 2 banks, row length = 11, column length = 9
1	1	000	01	16 Mbit (1Mx16), 2 banks, row length = 11, column length = 8
1	1	001	00	64 Mbit (8Mx8), 4 banks, row length = 12, column length = 9
1	1	001	01	64 Mbit (4Mx16), 4 banks, row length = 12, column length = 8
1	1	001	10	64 Mbit (2Mx32), 4 banks, row length = 11, column length = 8
1	1	010	00	128 Mbit (16Mx8), 4 banks, row length = 12, column length = 10
1	1	010	01	128 Mbit (8Mx16), 4 banks, row length = 12, column length = 9
1	1	010	10	128 Mbit (4Mx32), 4 banks, row length = 12, column length = 8
1	1	011	00	256 Mbit (32Mx8), 4 banks, row length = 13, column length = 10
1	1	011	01	256 Mbit (16Mx16), 4 banks, row length = 13, column length = 9

Table 134. Address mapping

14	12	11:9	8:7	Description
1	1	011	10	256 Mbit (8Mx32), 4 banks, row length = 13, column length = 8
1	1	100	00	512 Mbit (64Mx8), 4 banks, row length = 13, column length = 11
1	1	100	01	512 Mbit (32Mx16), 4 banks, row length = 13, column length = 10

A chip select can be connected to a single memory device, in this case the chip select data bus width is the same as the device width. Alternatively the chip select can be connected to a number of external devices. In this case the chip select data bus width is the sum of the memory device data bus widths.

For example, for a chip select connected to:

- a 32 bit wide memory device, choose a 32 bit wide address mapping.
- a 16 bit wide memory device, choose a 16 bit wide address mapping.
- four x 8 bit wide memory devices, choose a 32 bit wide address mapping.
- two x 8 bit wide memory devices, choose a 16 bit wide address mapping.

The SDRAM bank select pins BA1 and BA0 are connected to address lines A14 and A13, respectively.