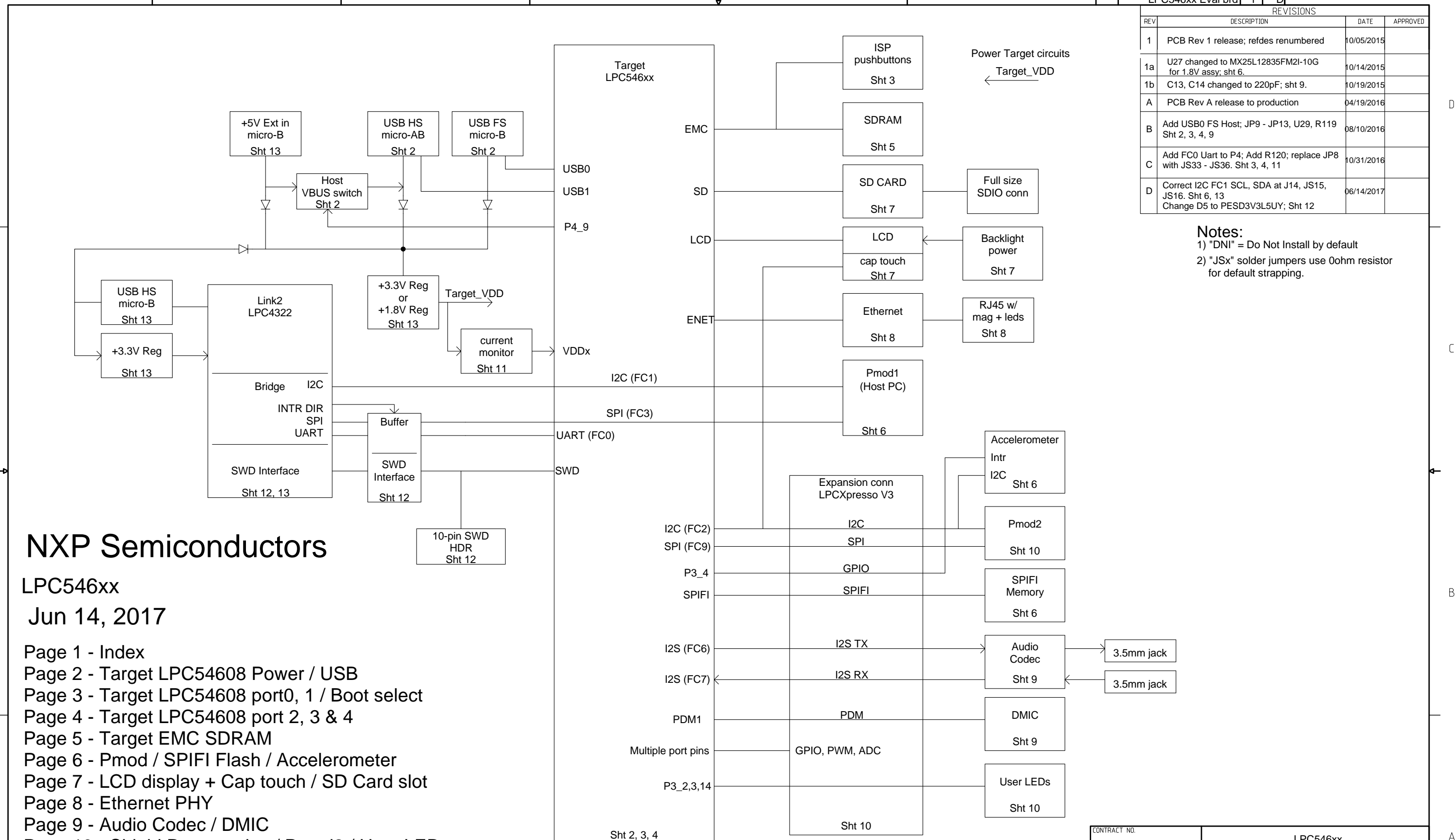


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
1	PCB Rev 1 release; refdes renumbered	10/05/2015	
1a	U27 changed to MX25L12835FM2I-10G for 1.8V assy; sht 6.	10/14/2015	
1b	C13, C14 changed to 220pF; sht 9.	10/19/2015	
A	PCB Rev A release to production	04/19/2016	
B	Add USB0 FS Host; JP9 - JP13, U29, R119 Sht 2, 3, 4, 9	08/10/2016	
C	Add FC0 Uart to P4; Add R120; replace JP8 with JS33 - JS36. Sht 3, 4, 11	10/31/2016	
D	Correct I2C FC1 SCL, SDA at J14, JS15, JS16. Sht 6, 13 Change D5 to PESD3V3L5UY; Sht 12	06/14/2017	

Notes:
 1) "DNI" = Do Not Install by default
 2) "JSx" solder jumpers use 0ohm resistor for default strapping.



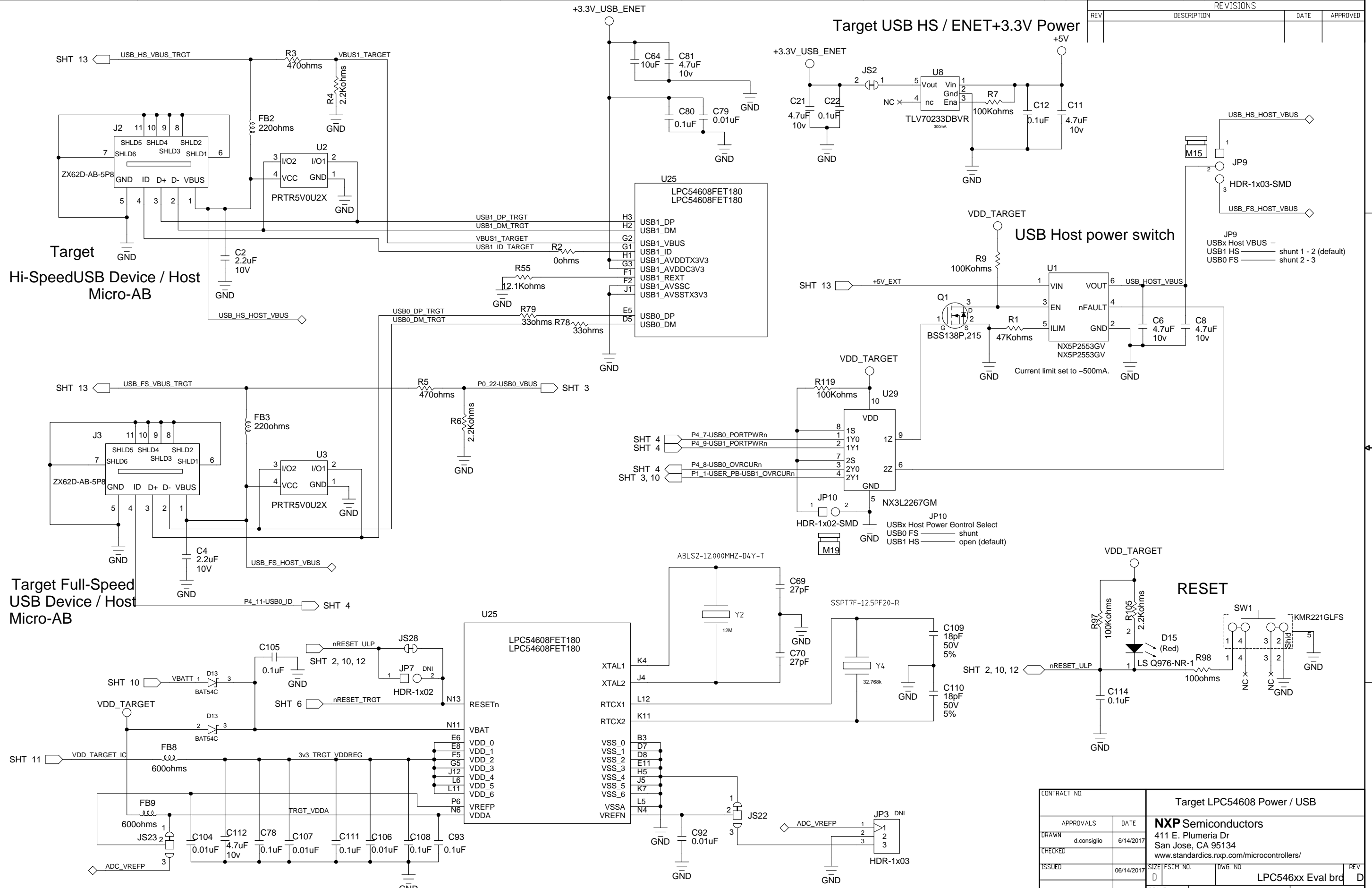
NXP Semiconductors

LPC546xx
 Jun 14, 2017

- Page 1 - Index
- Page 2 - Target LPC54608 Power / USB
- Page 3 - Target LPC54608 port0, 1 / Boot select
- Page 4 - Target LPC54608 port 2, 3 & 4
- Page 5 - Target EMC SDRAM
- Page 6 - Pmod / SPIFI Flash / Accelerometer
- Page 7 - LCD display + Cap touch / SD Card slot
- Page 8 - Ethernet PHY
- Page 9 - Audio Codec / DMIC
- Page 10 - Shield Receptacles / Pmod2 / User LEDs
- Page 11 - LPC54608 current monitor; LINK2 Bridge buffer
- Page 12 - Debug LINK2 LPC4322 Peripherals / debug buffer
- Page 13 - Debug LINK2 LPC4322 / LINK2 USB / Board Power

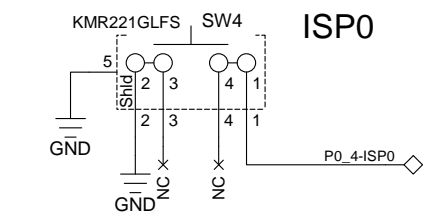
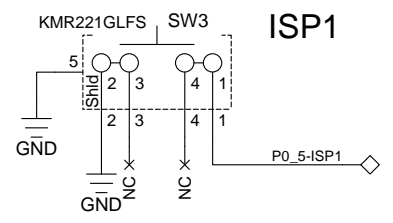
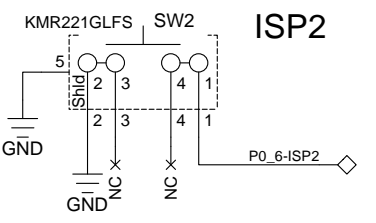
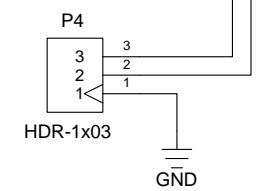
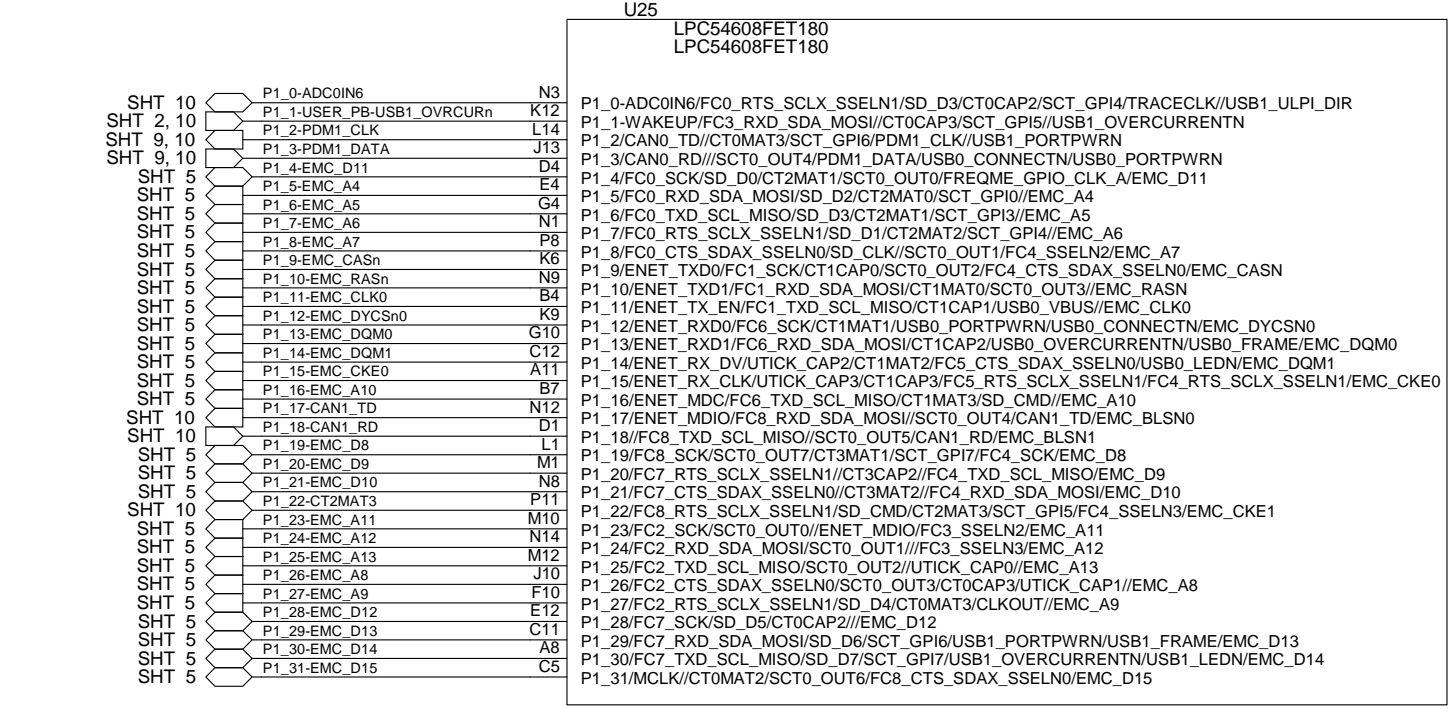
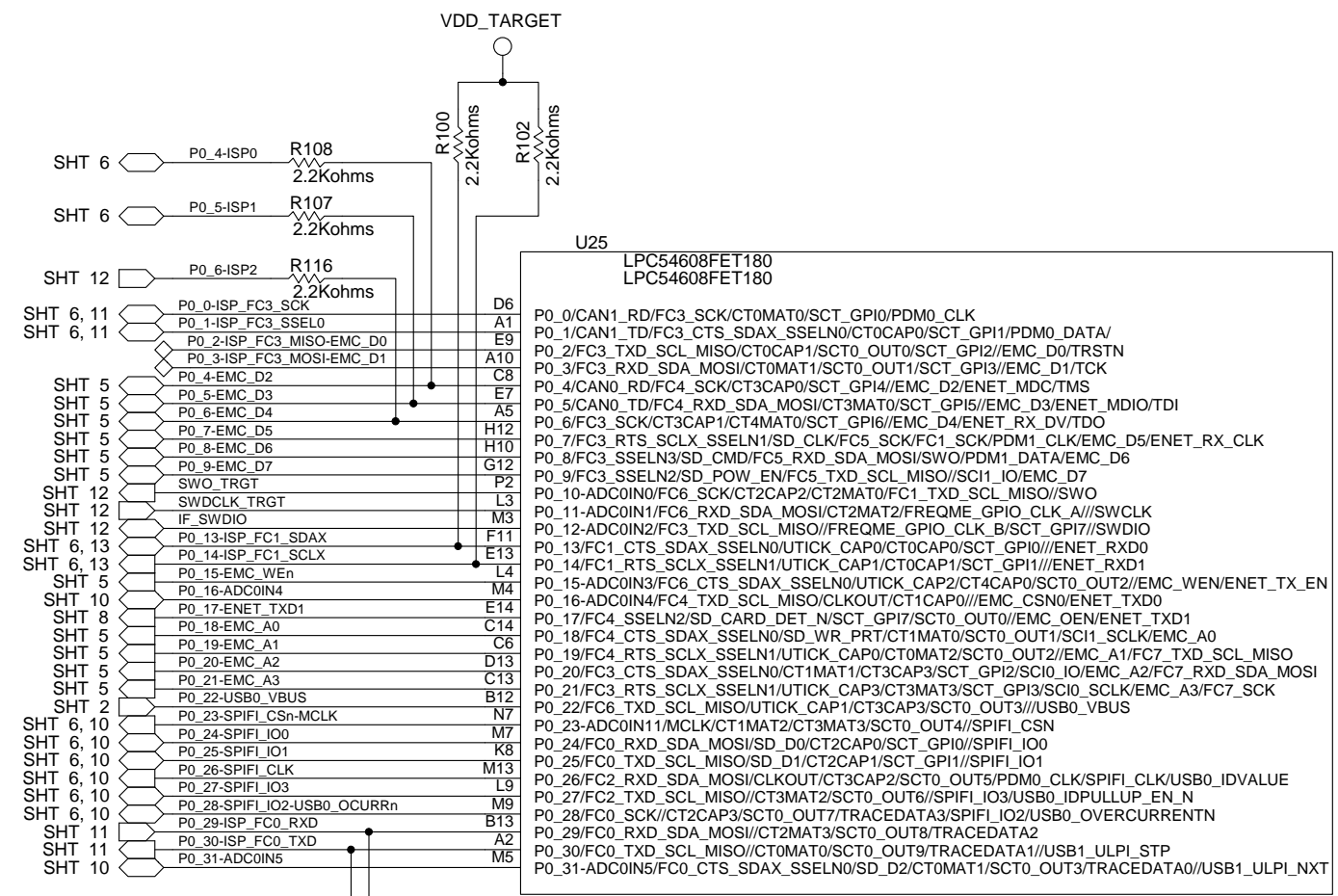
CONTRACT NO.		LPC546xx		
APPROVALS	DATE	NXP Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/		
DRAWN	d.consiglio			6/14/2017
CHECKED				
ISSUED	06/14/2017			
SCALE		SIZE / FSCM NO.	DWG. NO.	
		D	LPC546xx Eval brd	
			REV D	
		SHEET	1 OF 13	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

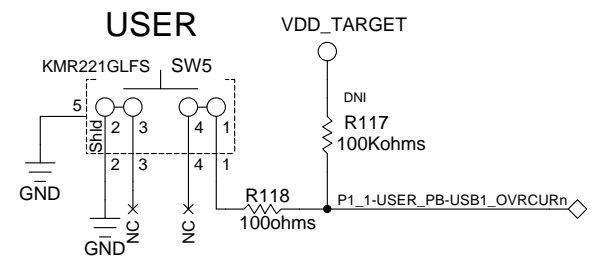
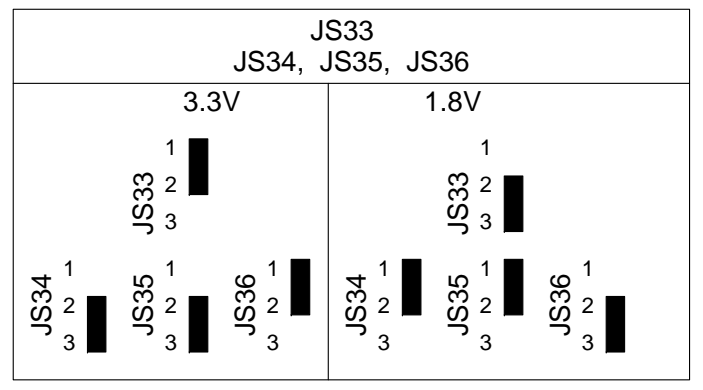
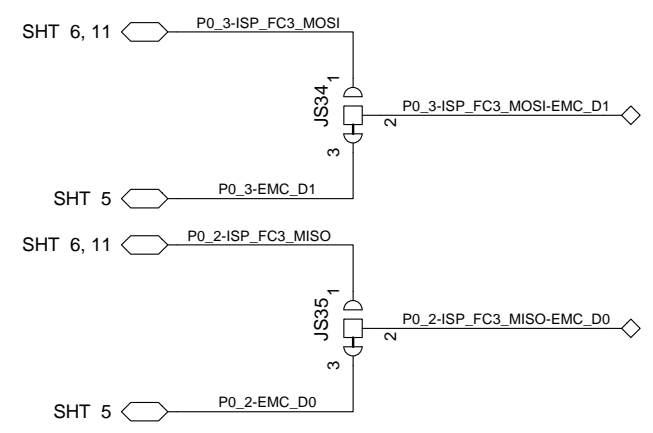


CONTRACT NO.		Target LPC54608 Power / USB	
APPROVALS	DATE	NXP Semiconductors	
DRAWN	d.consiglio	411 E. Plumeria Dr	
CHECKED	6/14/2017	San Jose, CA 95134	
ISSUED	06/14/2017	www.standardics.nxp.com/microcontrollers/	
		SIZE	D
		FSCM NO.	
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		REV	D
		SCALE	
		SHEET	2 OF 13

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

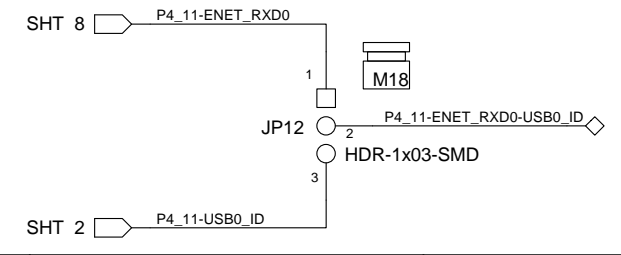
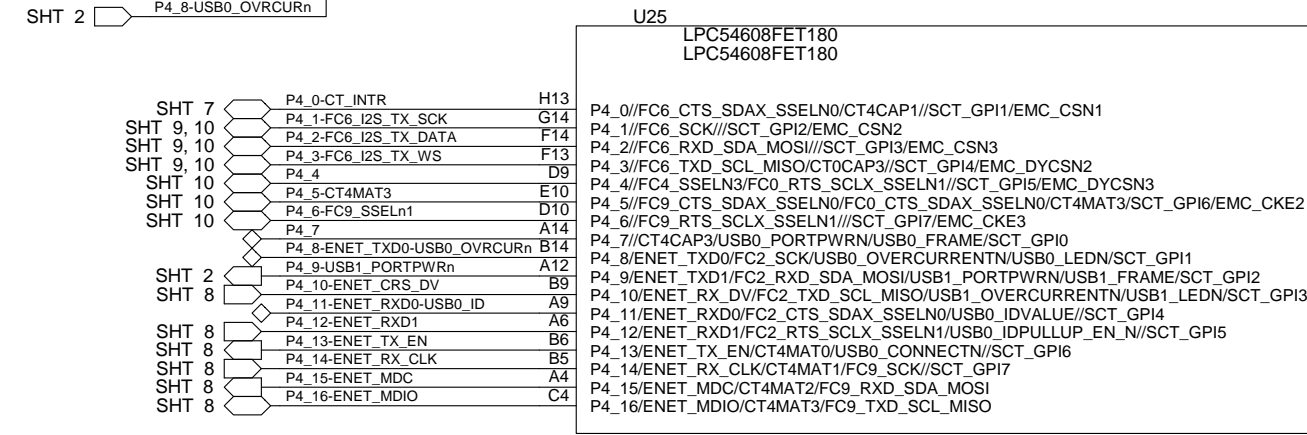
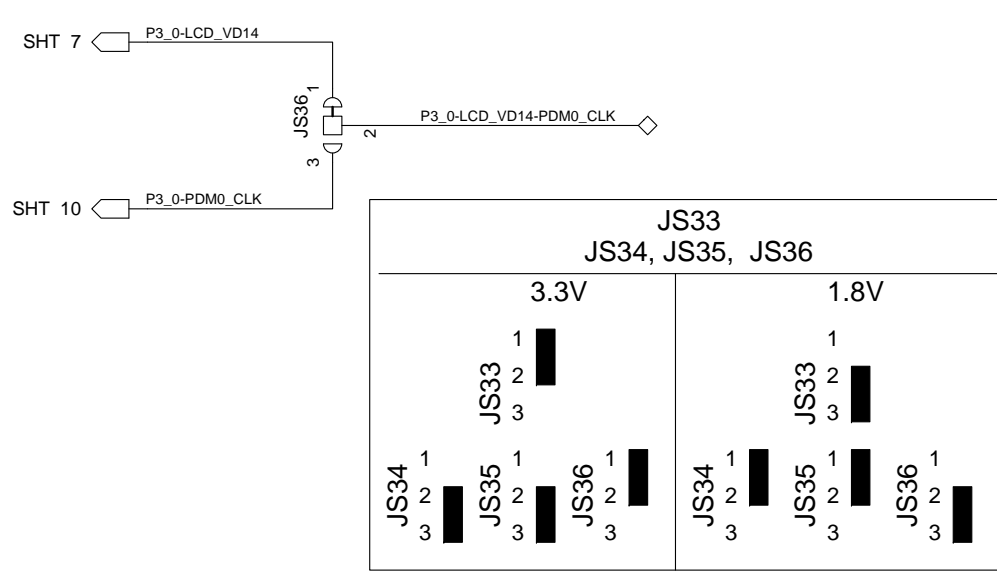
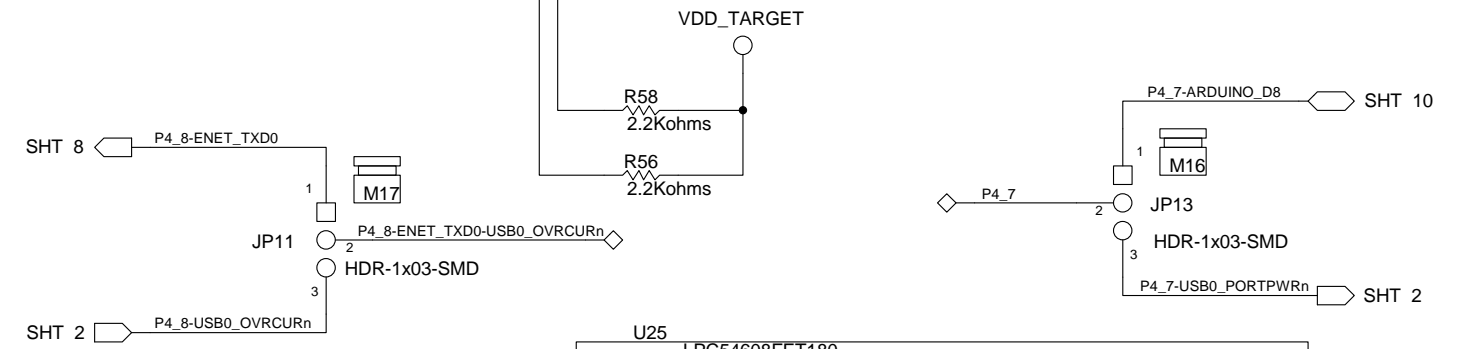
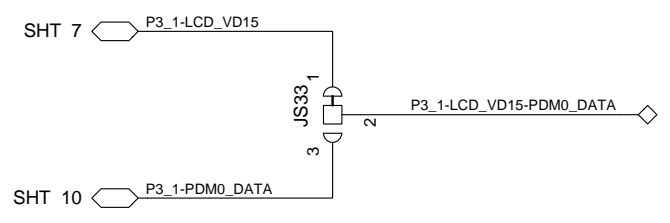
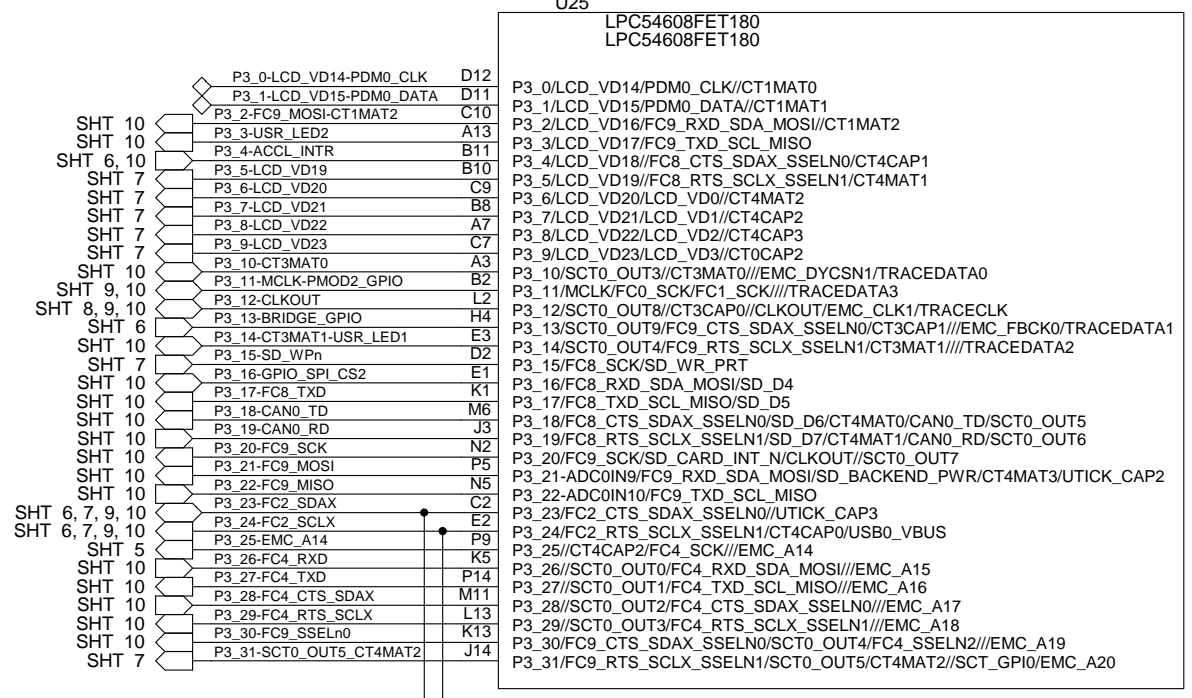
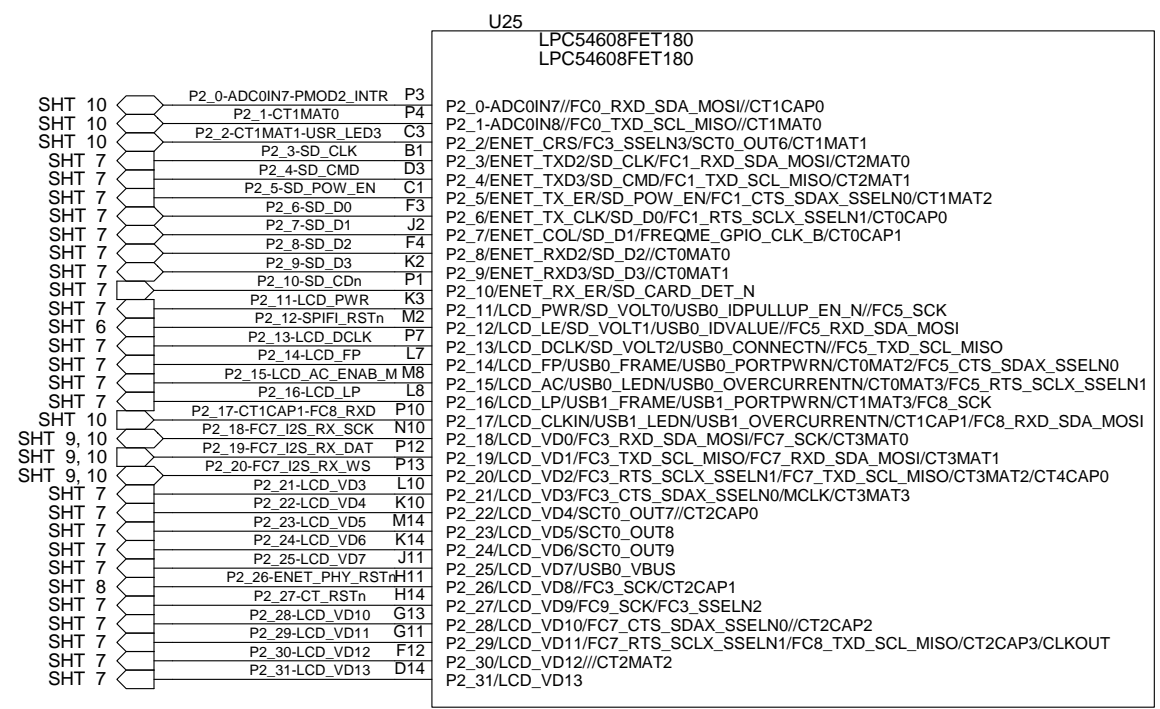


Target LPC54608 Boot			
Mode	ISP2 P0_6	ISP1 P0_5	ISP0 P0_4
Internal Flash boot	high	high	high
ISP USB1 HS	low	high	high
ISP CAN	high	low	low
ISP USB0 FS	high	low	high
ISP UART/I2C/SPI	high	high	low



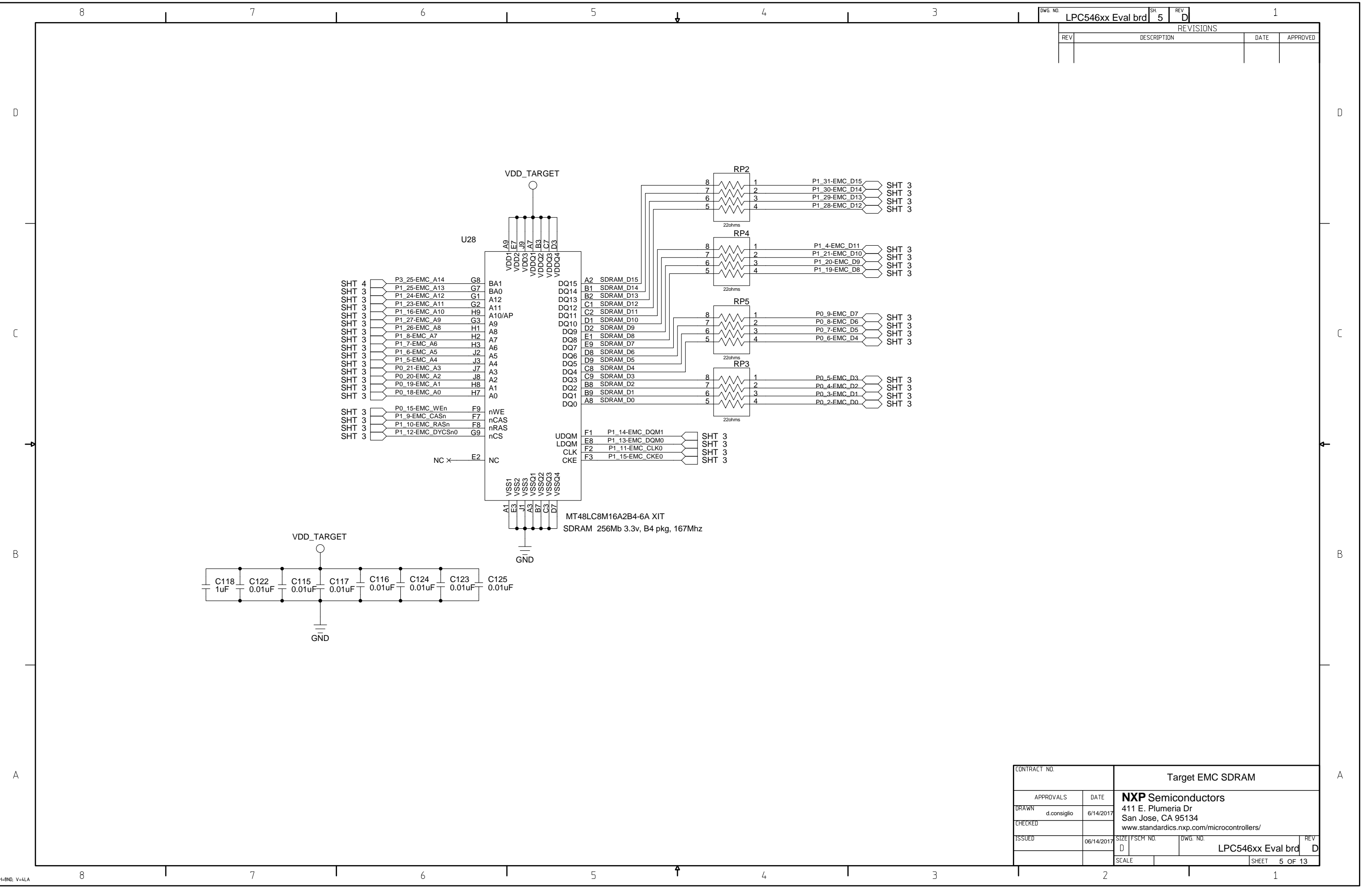
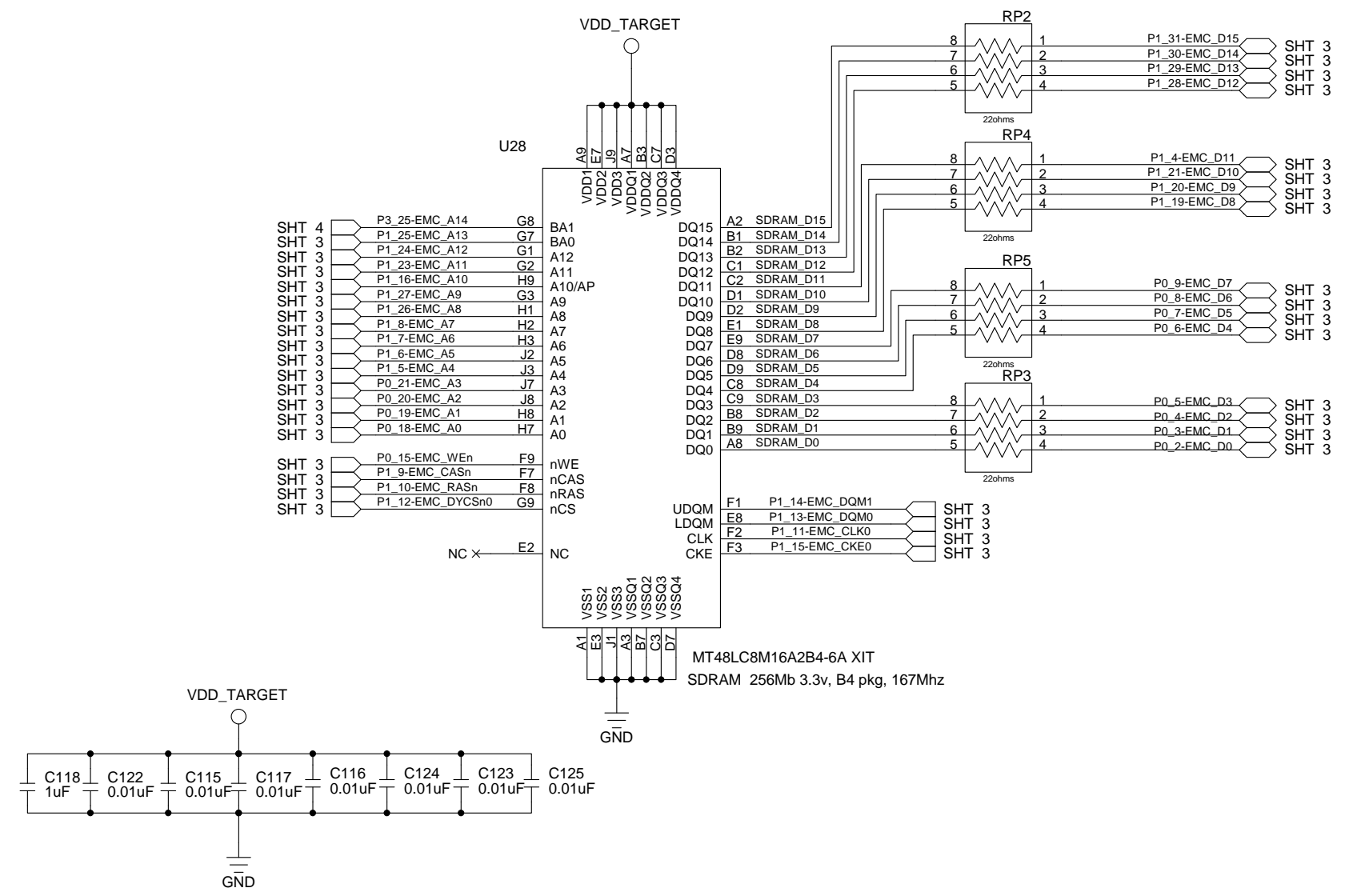
CONTRACT NO.		Target LPC54608 port0, 1 / Boot select	
APPROVALS	DATE	NXP Semiconductors	
DRAWN	d.consiglio	411 E. Plumeria Dr	
CHECKED	6/14/2017	San Jose, CA 95134	
ISSUED	06/14/2017	www.standardics.nxp.com/microcontrollers/	
SCALE		SIZE	D
		DWG. NO.	LPC546xx Eval brd
		REV	D
		SHEET	3 OF 13

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



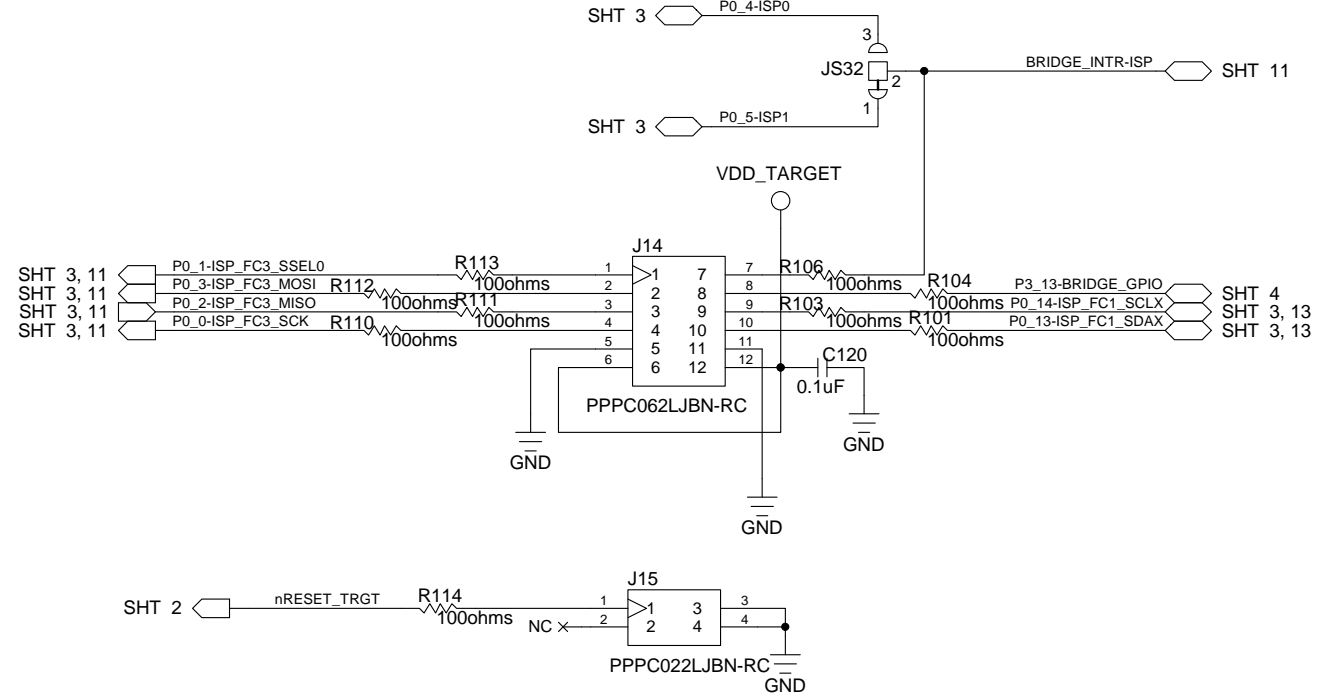
CONTRACT NO.		Target LPC54608 port 2, 3 & 4	
APPROVALS	DATE	NXP Semiconductors	
DRAWN d.consiglio	6/14/2017	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
CHECKED		SIZE	DWG. NO.
ISSUED	06/14/2017	D	LPC546xx Eval brd
		SCALE	SHEET 4 OF 13

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



CONTRACT NO.		Target EMC SDRAM		
APPROVALS	DATE	NXP Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/		
DRAWN	d.consiglio			6/14/2017
CHECKED				
ISSUED	06/14/2017	SIZE	D	
SCALE		DWG. NO.	LPC546xx Eval brd	
		REV	D	
		SHEET 5 OF 13		

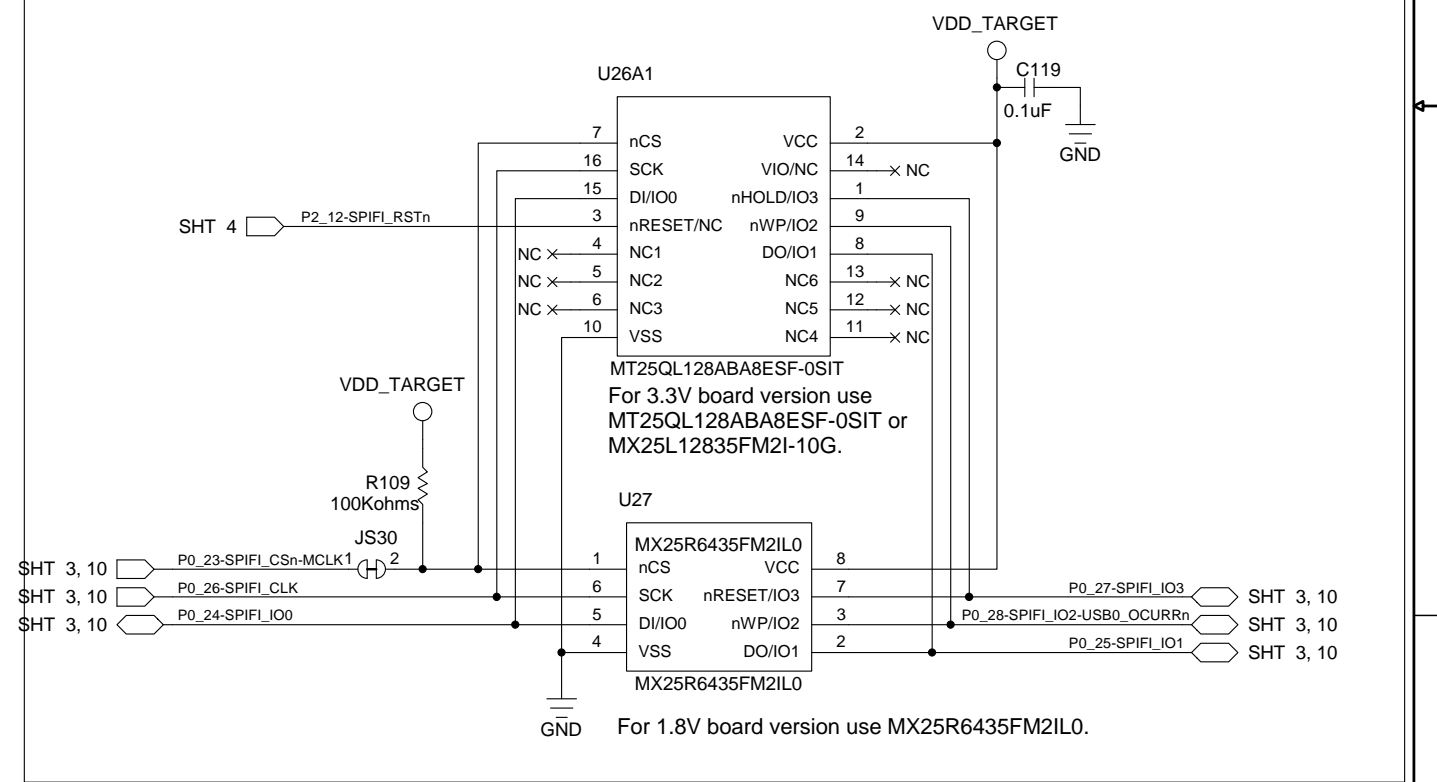
SPI / I2C header (PMOD compatible) Host interface



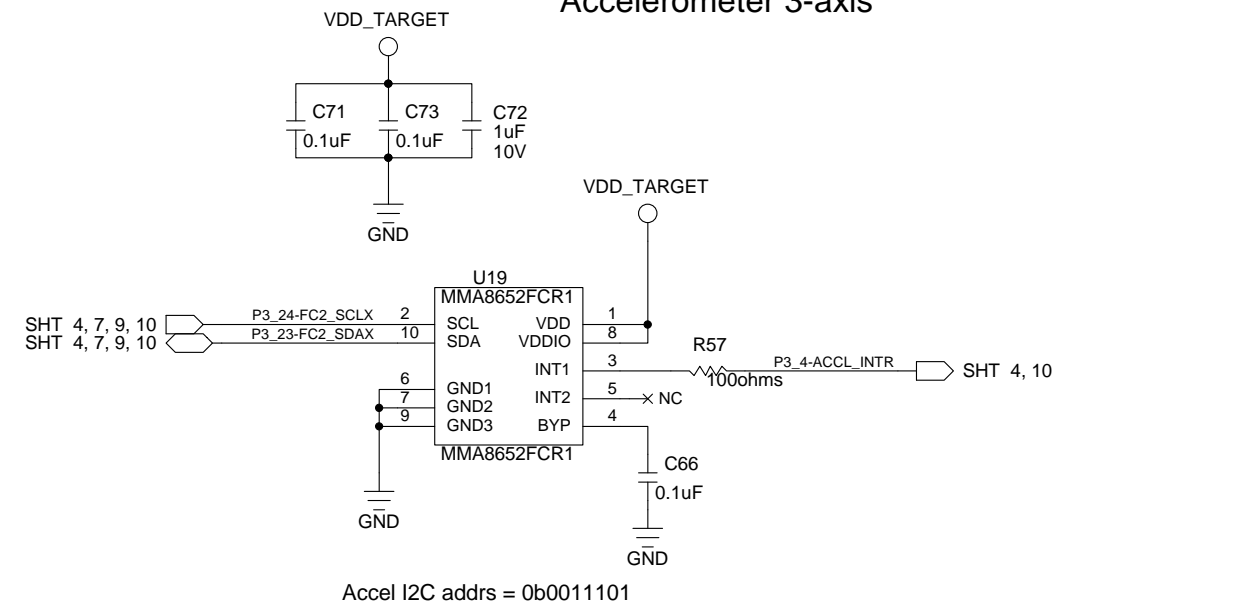
PMOD pin function	LPC54608 supported function
Pin 1: GPIO/SPI-SSEL(out)/UART-CTS(in)	GPIO/SPI-SSEL(in/out)
Pin 2: GPIO/SPI-MOSI(out)/UART-TXD(out)	GPIO/SPI-MOSI(in/out)
Pin 3: GPIO/SPI-MISO(in)/UART-RXD(in)	GPIO/SPI-MISO(out/in)
Pin 4: GPIO/SPI-SCK(out)/UART-RTS(out)	GPIO/SPI-SCK(in/out)
Pin 5: GND	GND
Pin 6: VCC(3.3V)	VCC(3.3V)
Pin 7: GPIO/INT(in)	GPIO/INT(out/in)
Pin 8: GPIO/RESET(out)	GPIO/RESET(out)
Pin 9: GPIO/SCL	SCL
Pin 10:GPIO/SDA	SDA
Pin 11:GND	GND
Pin 12:VCC(3.3V)	VCC(3.3V)

QSPI (SPIFI) NOR Flash

SO16 pkg / SO8 pkg mutually exclusive

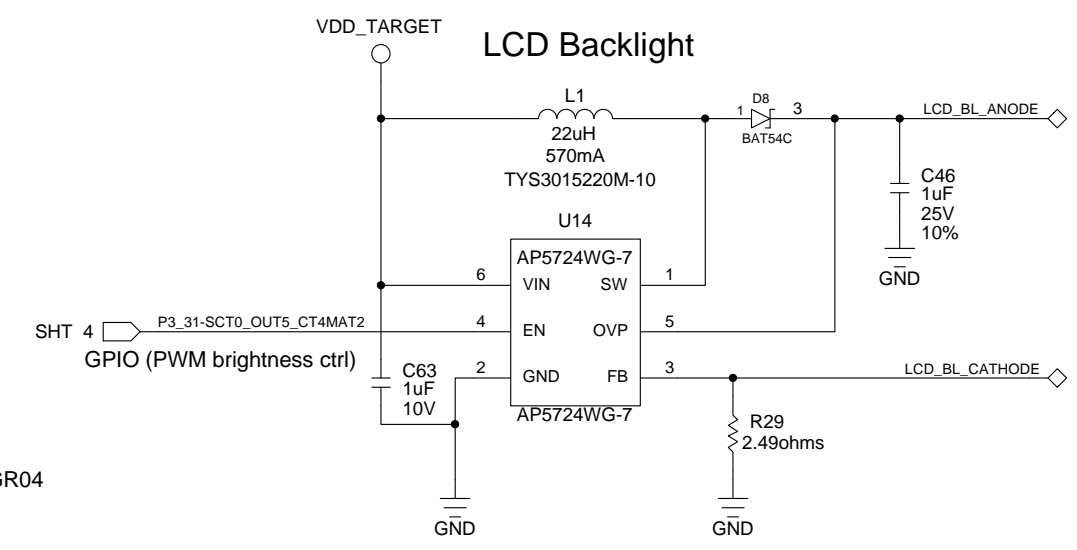
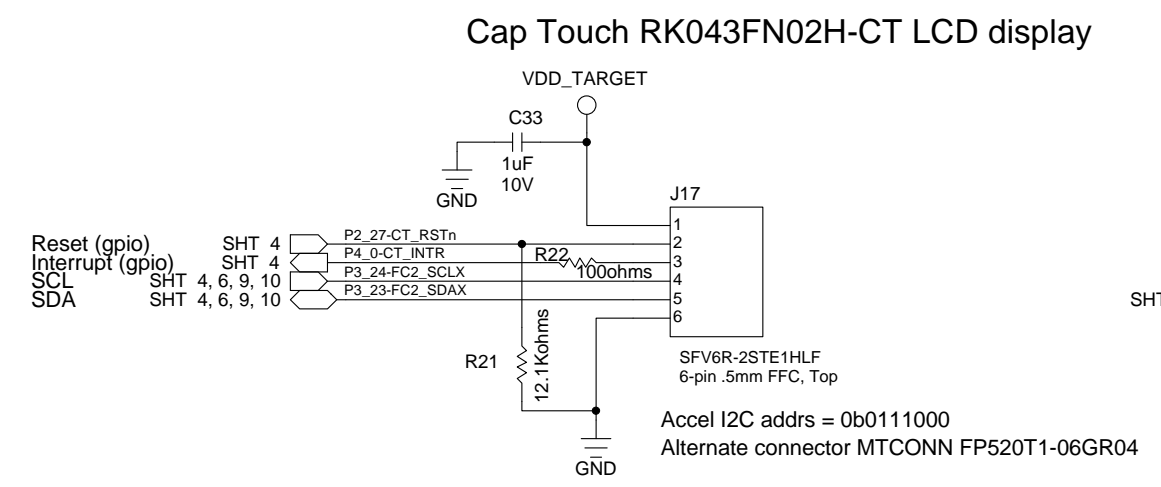
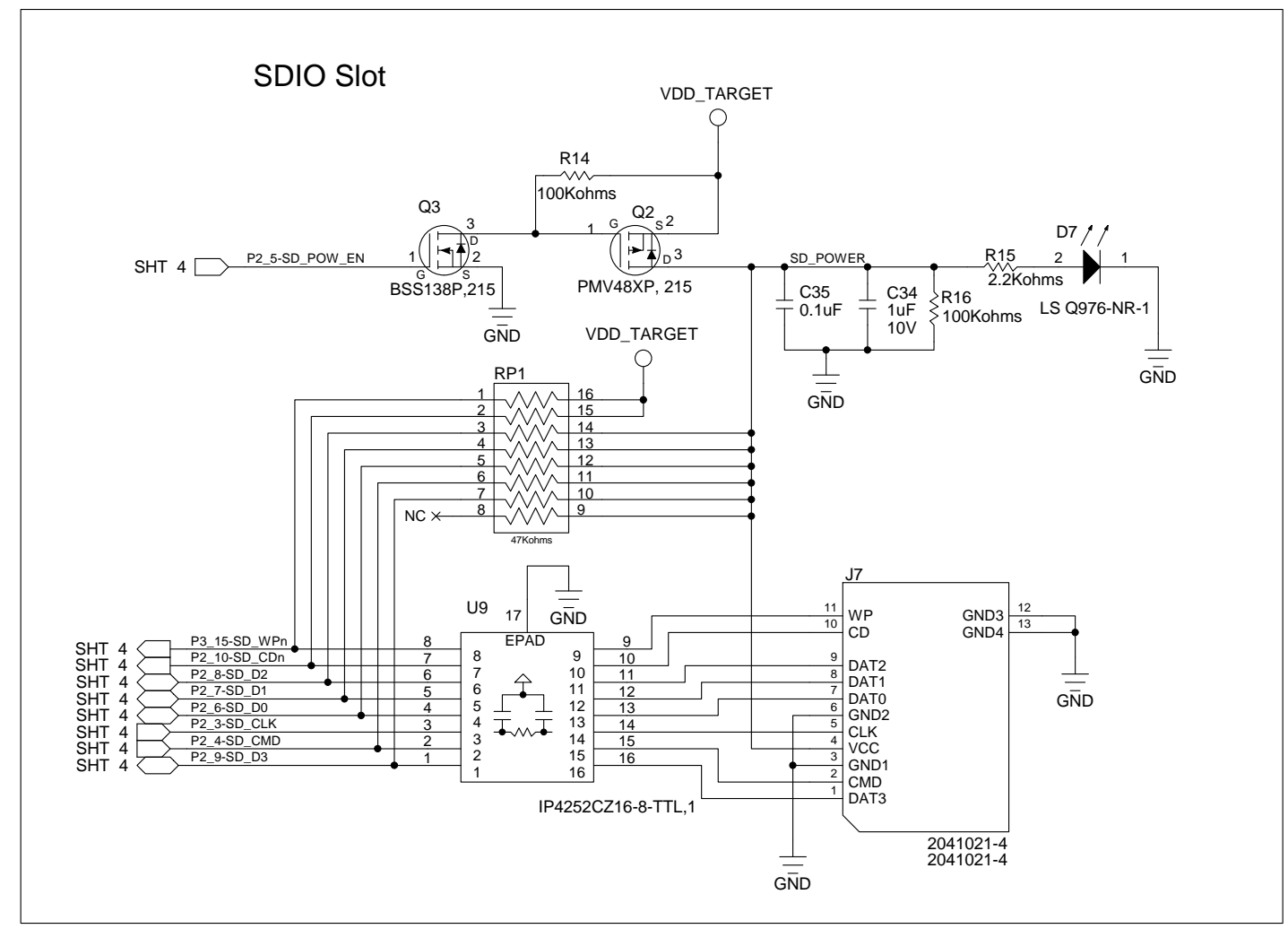
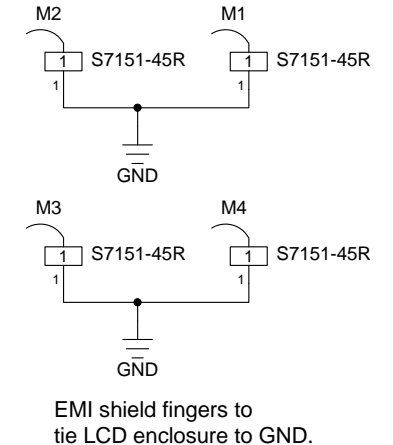
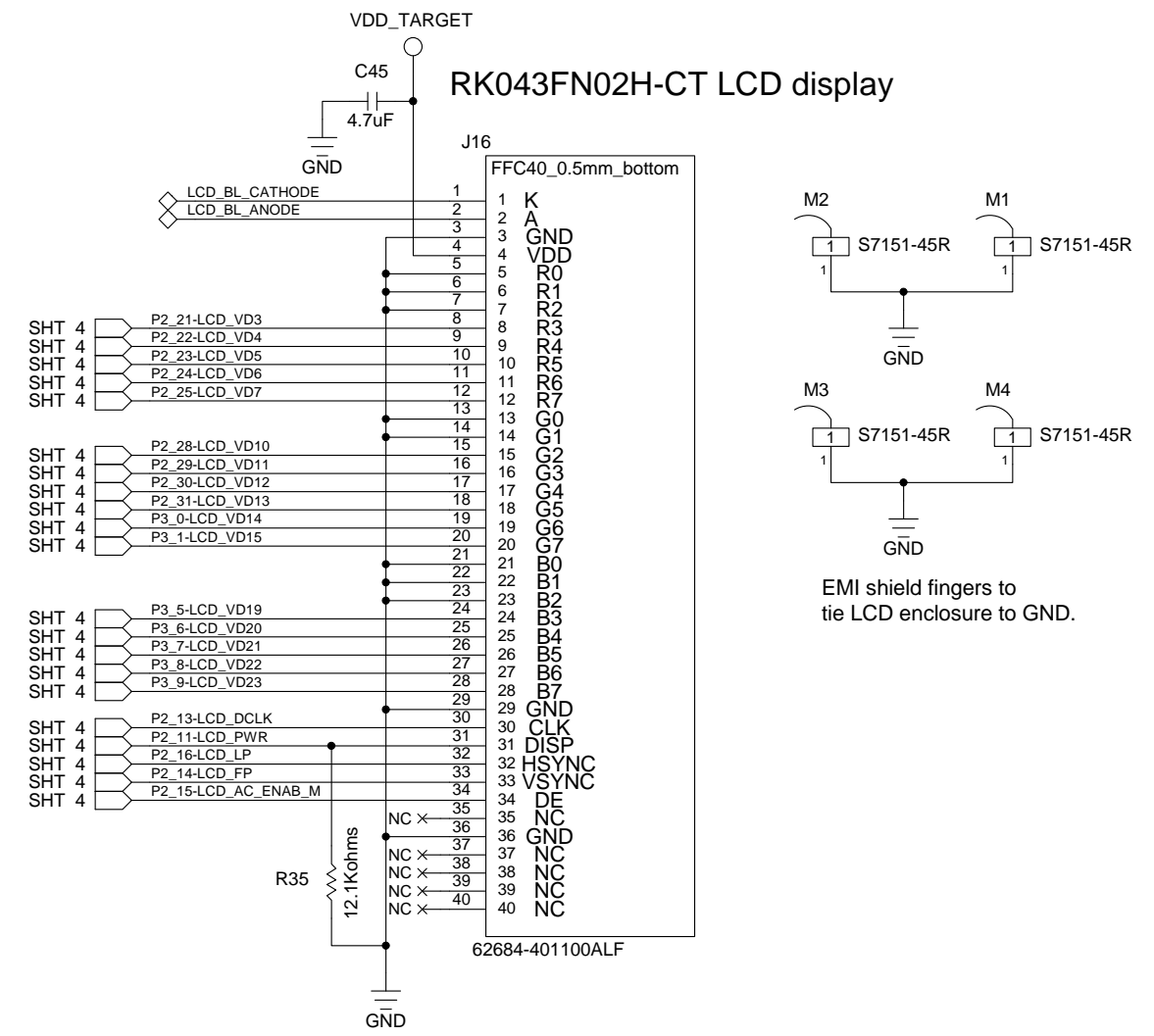


Accelerometer 3-axis

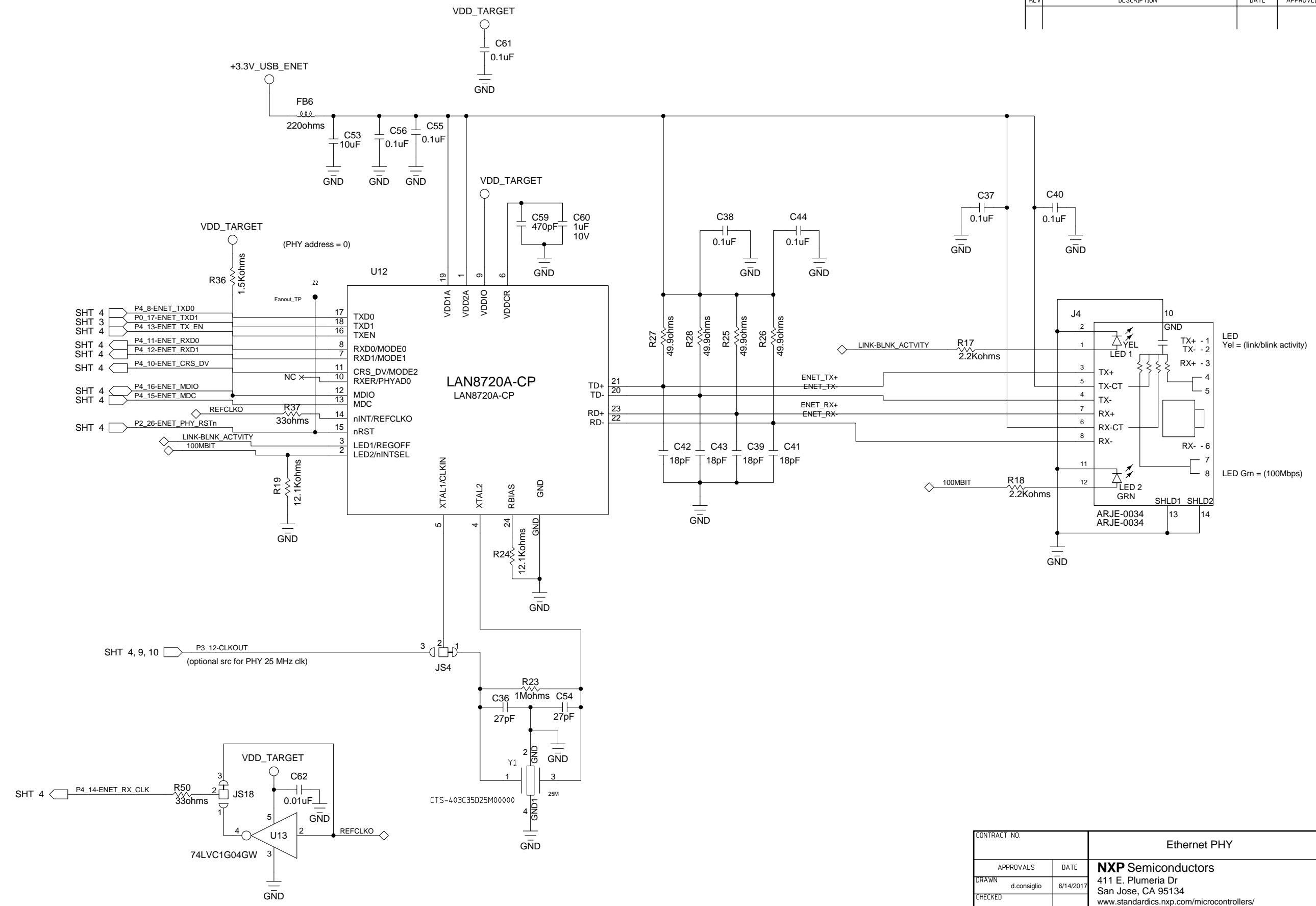


CONTRACT NO.		Pmod / SPIFI Flash / Accelerometer	
APPROVALS	DATE	NXP Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN	d.consiglio		
CHECKED			
ISSUED	06/14/2017	SIZE	D
		DWG. NO.	LPC546xx Eval brd
		SCALE	SHEET 6 OF 13

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

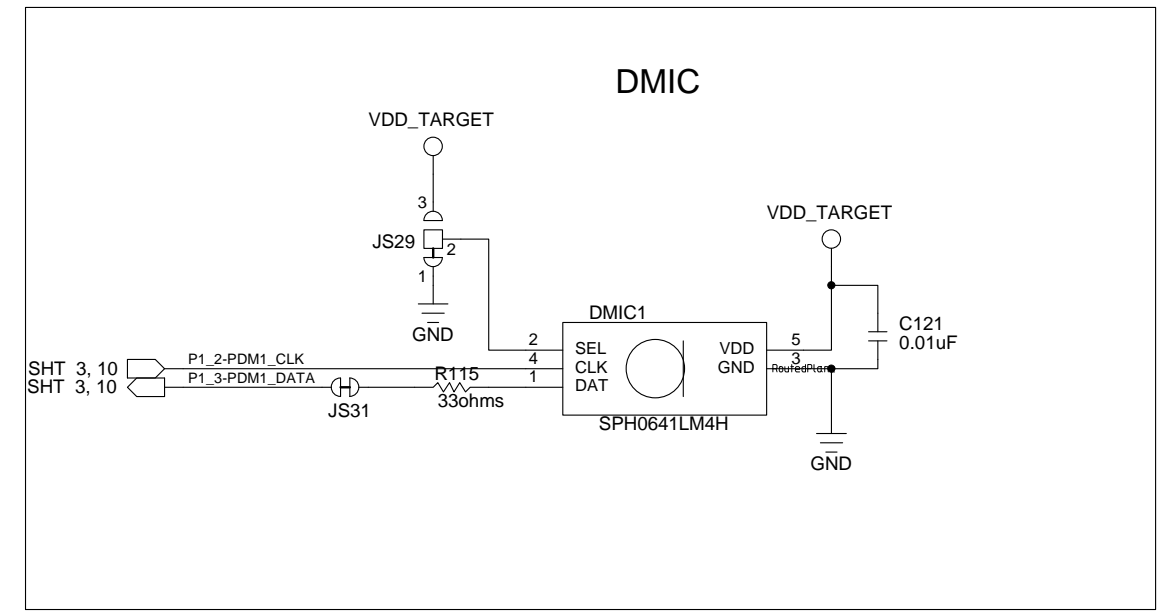
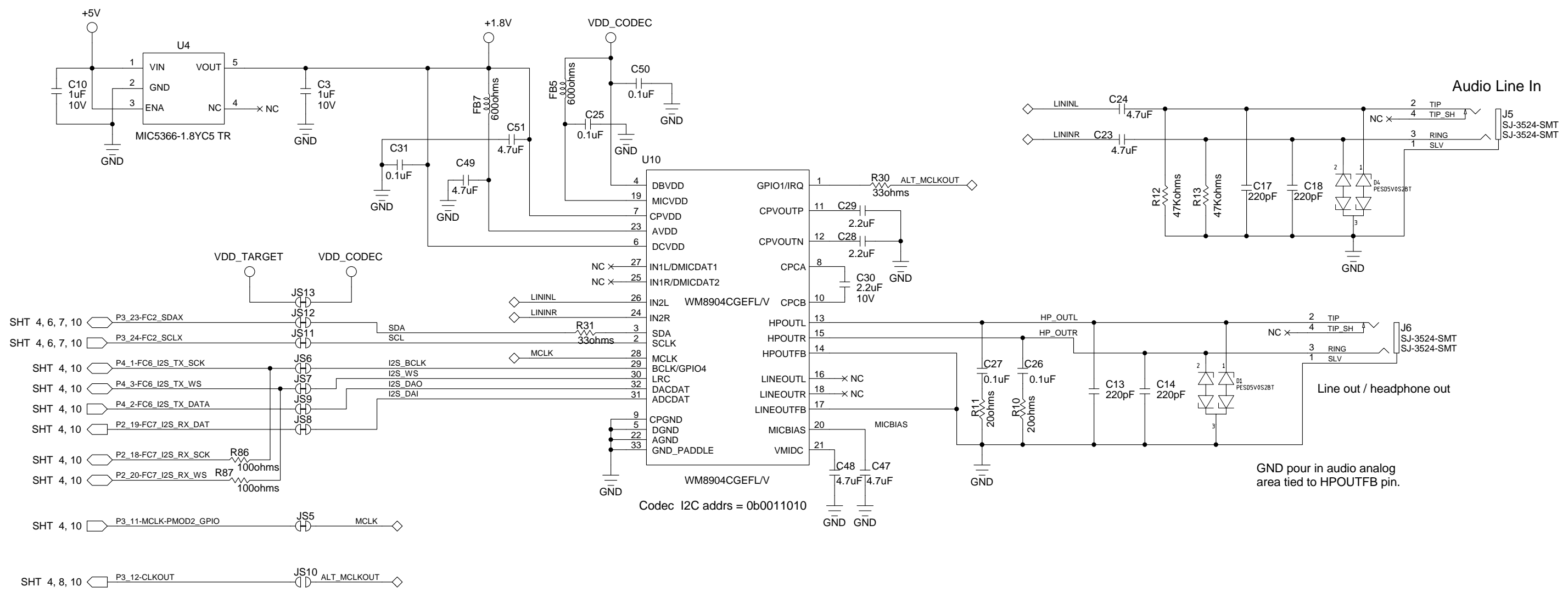


CONTRACT NO.		LCD display + Cap touch / SD Card slot		
APPROVALS	DATE	NXP Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/		
DRAWN	d.consiglio			6/14/2017
CHECKED				
ISSUED	06/14/2017			
SCALE		SIZE	D	
		DWG. NO.	LPC546xx Eval brd	
		REV	D	
		SHEET	7 OF 13	



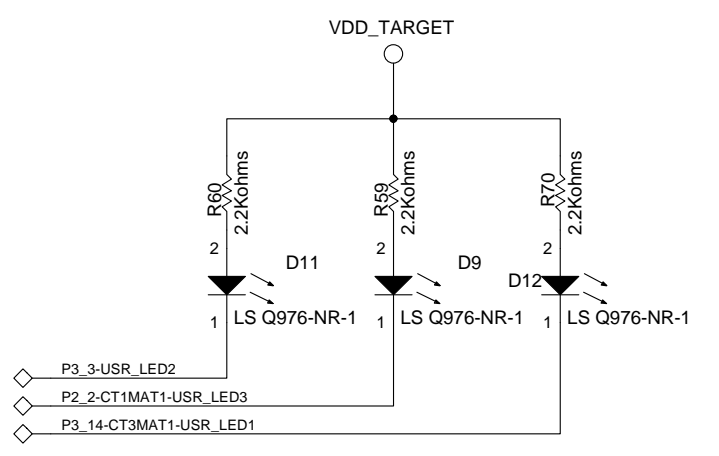
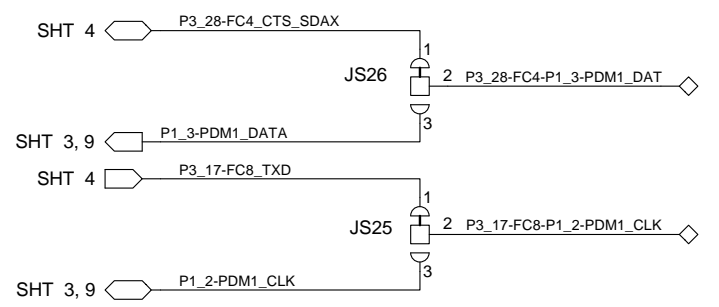
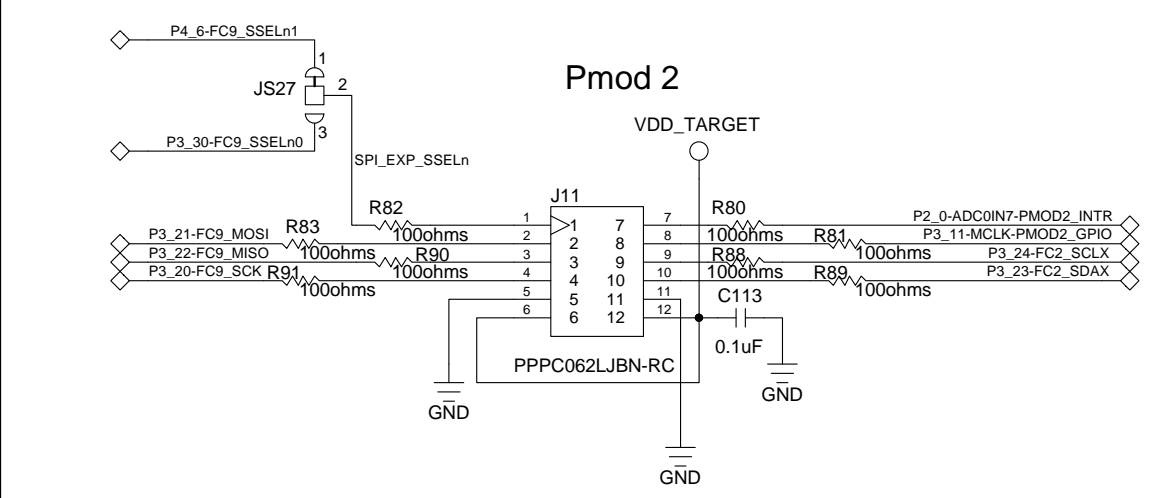
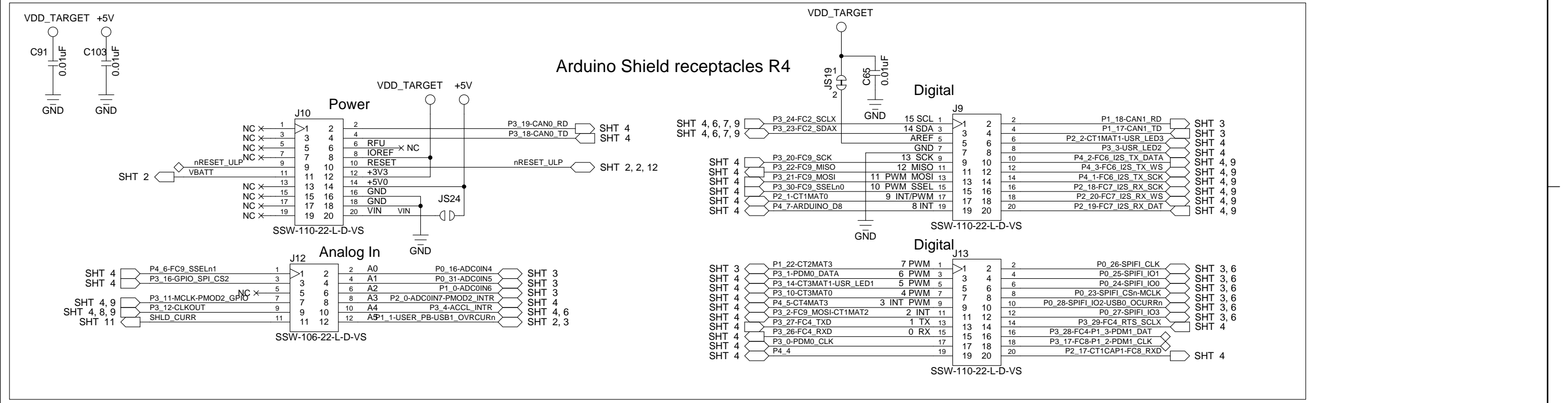
CONTRACT NO.		Ethernet PHY	
APPROVALS	DATE	NXP Semiconductors	
DRAWN	d.consiglio	411 E. Plumeria Dr	
CHECKED	6/14/2017	San Jose, CA 95134	
ISSUED	06/14/2017	www.standardics.nxp.com/microcontrollers/	
		SIZE / FSCM NO.	DWG. NO.
			LPC546xx Eval brd
		SCALE	SHEET 8 OF 13

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

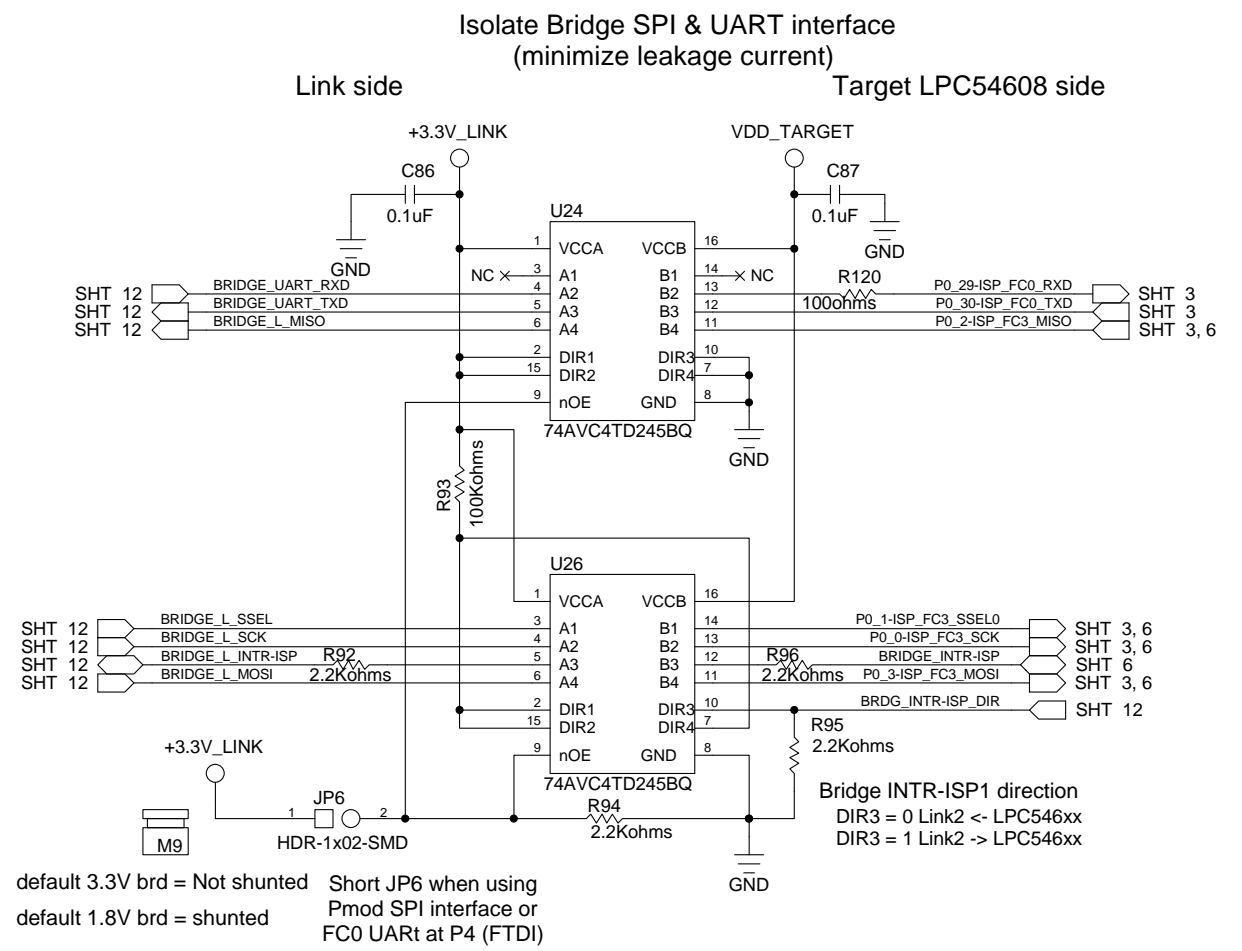


CONTRACT NO.		Audio Codec / DMIC		
APPROVALS	DATE	NXP Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/		
DRAWN	d.consiglio			6/14/2017
CHECKED				
ISSUED	06/14/2017	SIZE	FSCM NO.	
		D		
		SCALE		
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		SHEET	9 OF 13	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

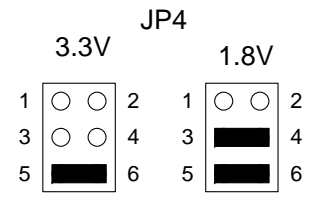


CONTRACT NO.		Shield Receptacles / Pmod2 / User LEDs	
APPROVALS	DATE	NXP Semiconductors	
DRAWN	d.consiglio	411 E. Plumeria Dr	
CHECKED		San Jose, CA 95134	
ISSUED	06/14/2017	www.standardics.nxp.com/microcontrollers/	
SCALE		SIZE	REV
		D	D
		LPC546xx Eval brd	
		SHEET 10 OF 13	



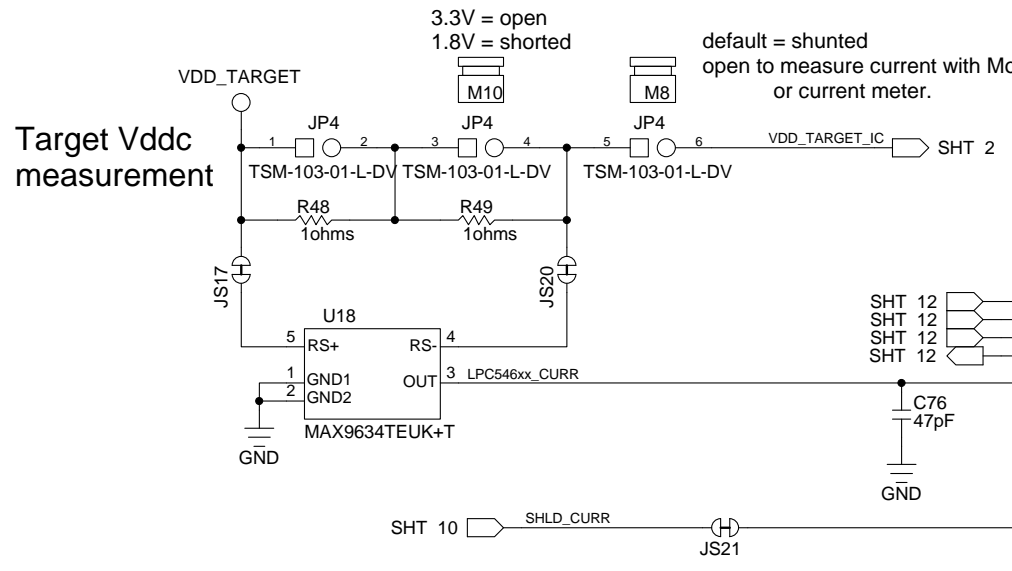
LPC54608				
LPC54608				ADC111S021 12bit ADC
Vsense (1) voltage 1-lsb	JP4.3/4 open LPC54608	JP4.3/4 shunted LPC54608	maximum current	ADC input 1- lsb 800uV
32uV	16uA	32uA	65mA	

(1) Vsense voltage is between U18 RS+ to RS-. Total Rvsense = R48 + (R49 || JP4.5/6).



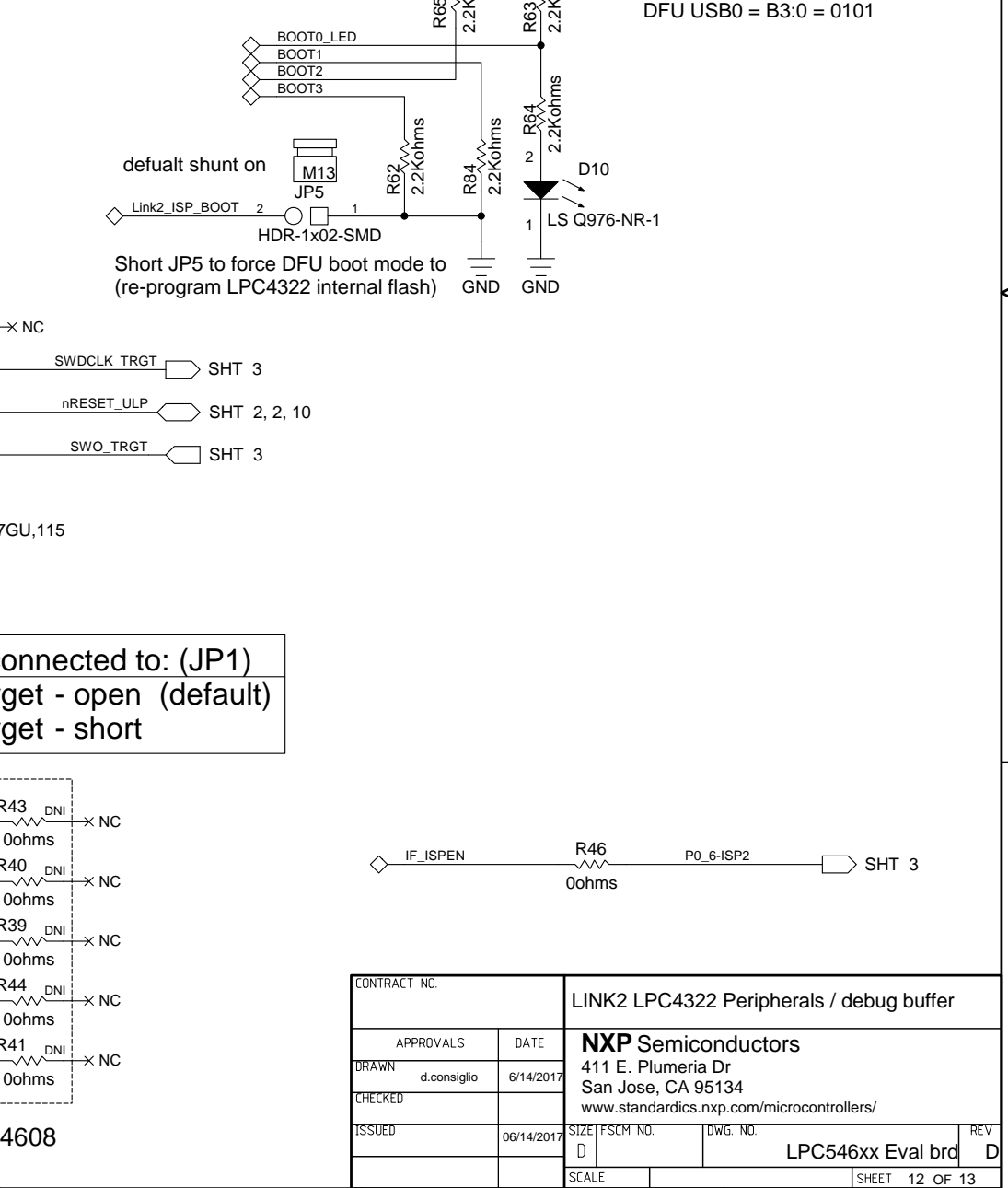
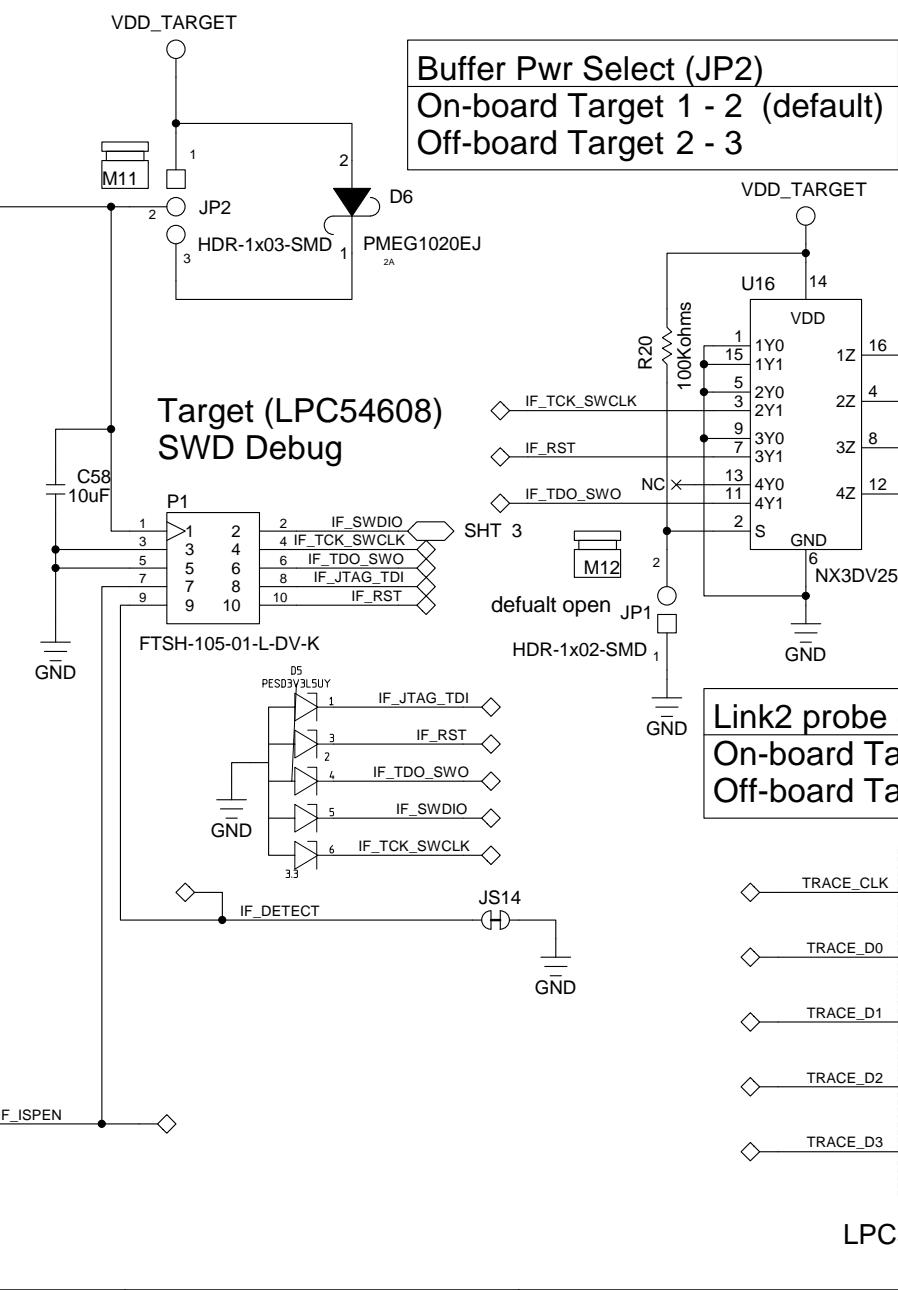
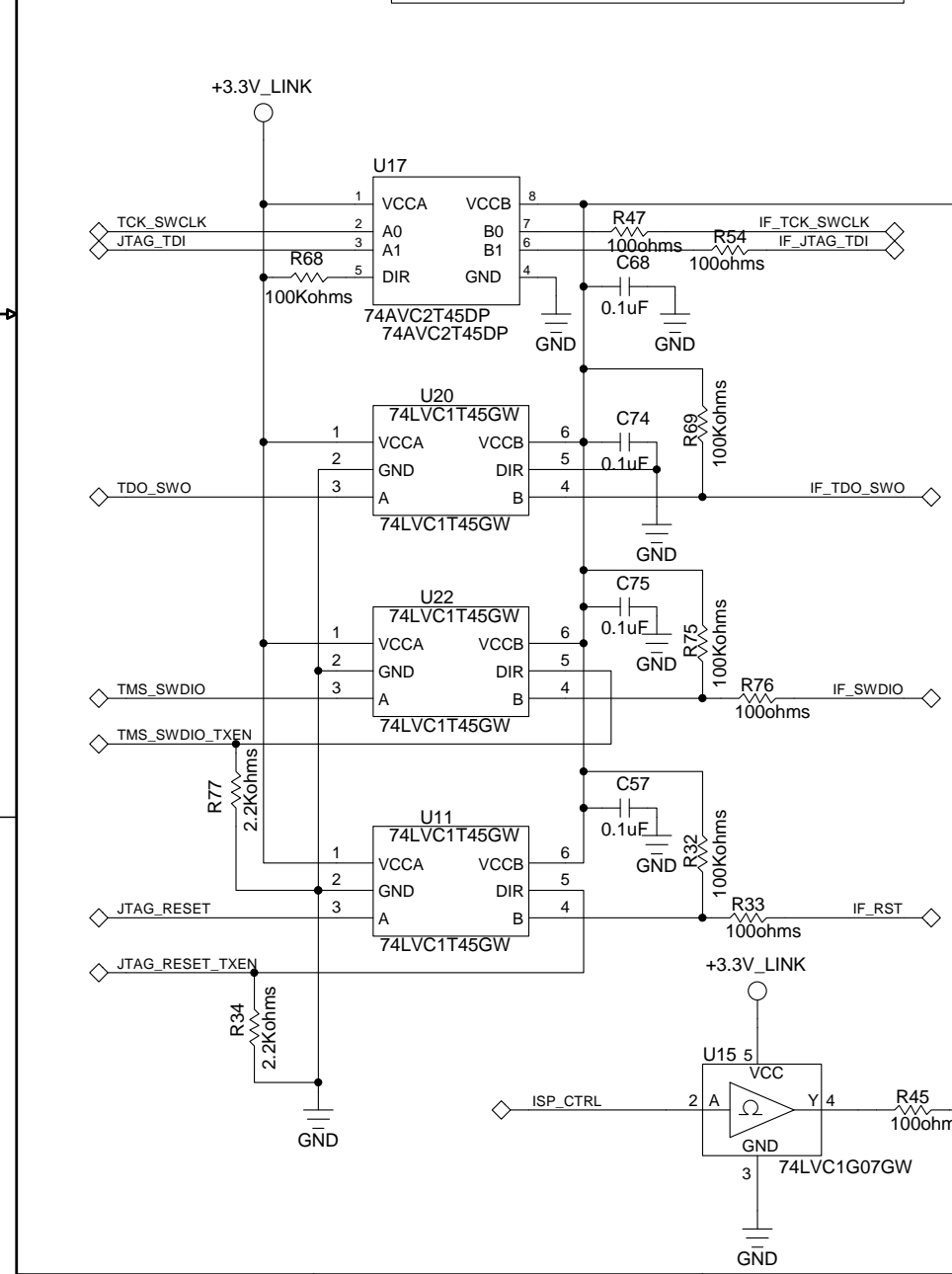
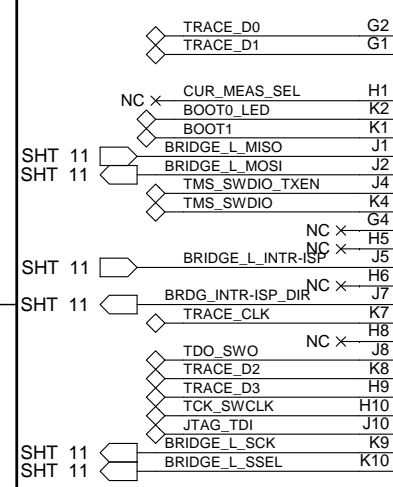
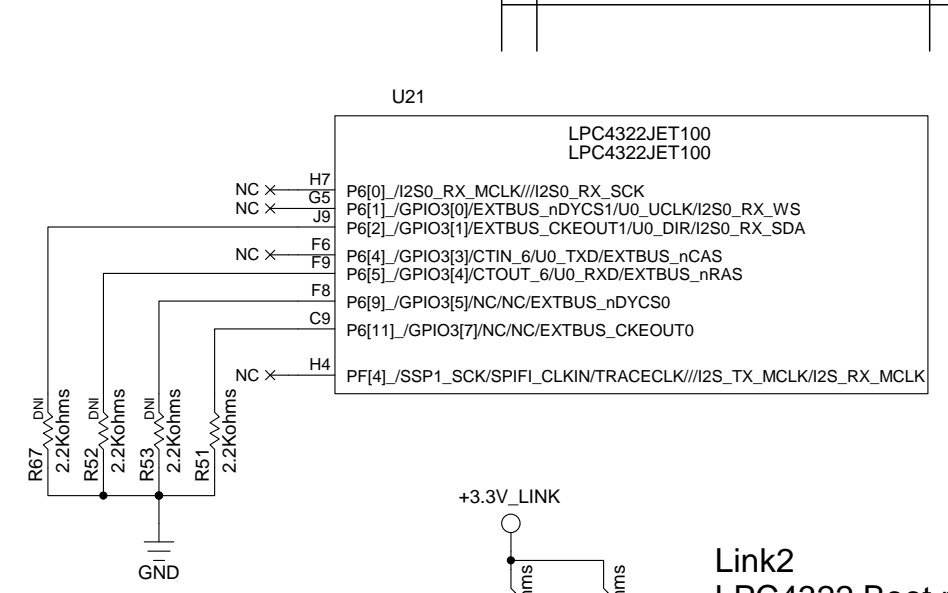
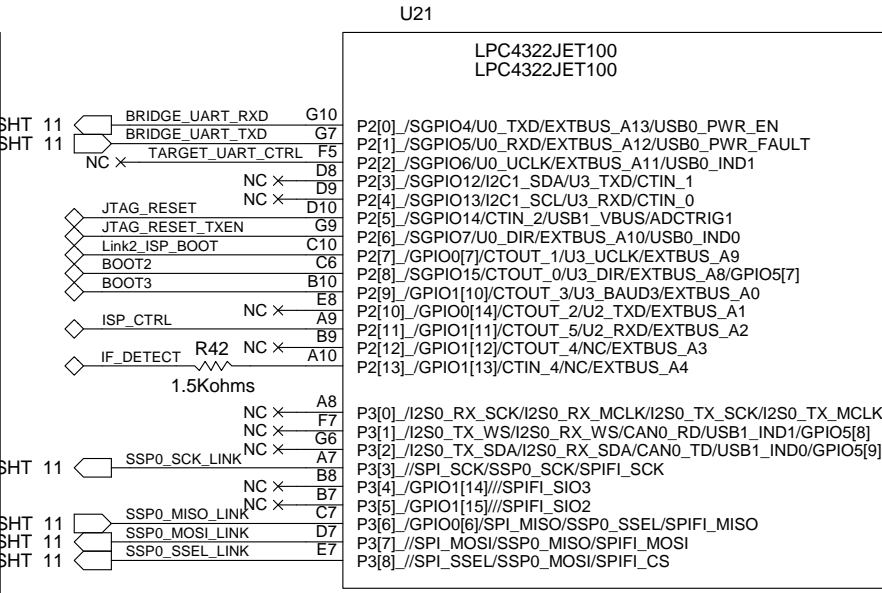
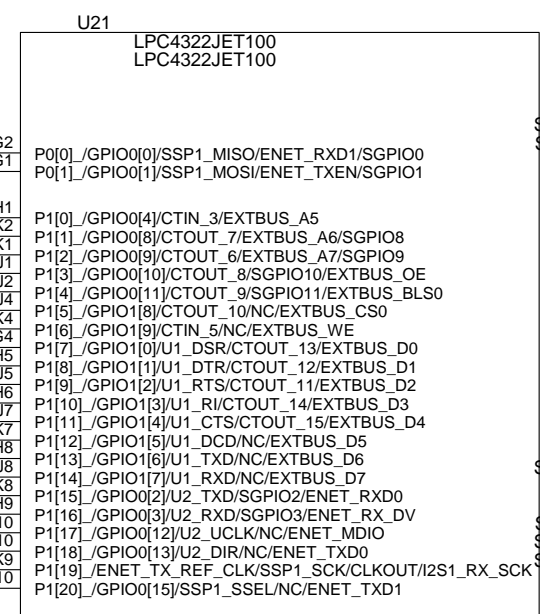
JP4 Setting

VDD LPC54608 (volts)	JP4	Total Rvsense (ohms)
3.3V	open	2
1.8V	shunted	1

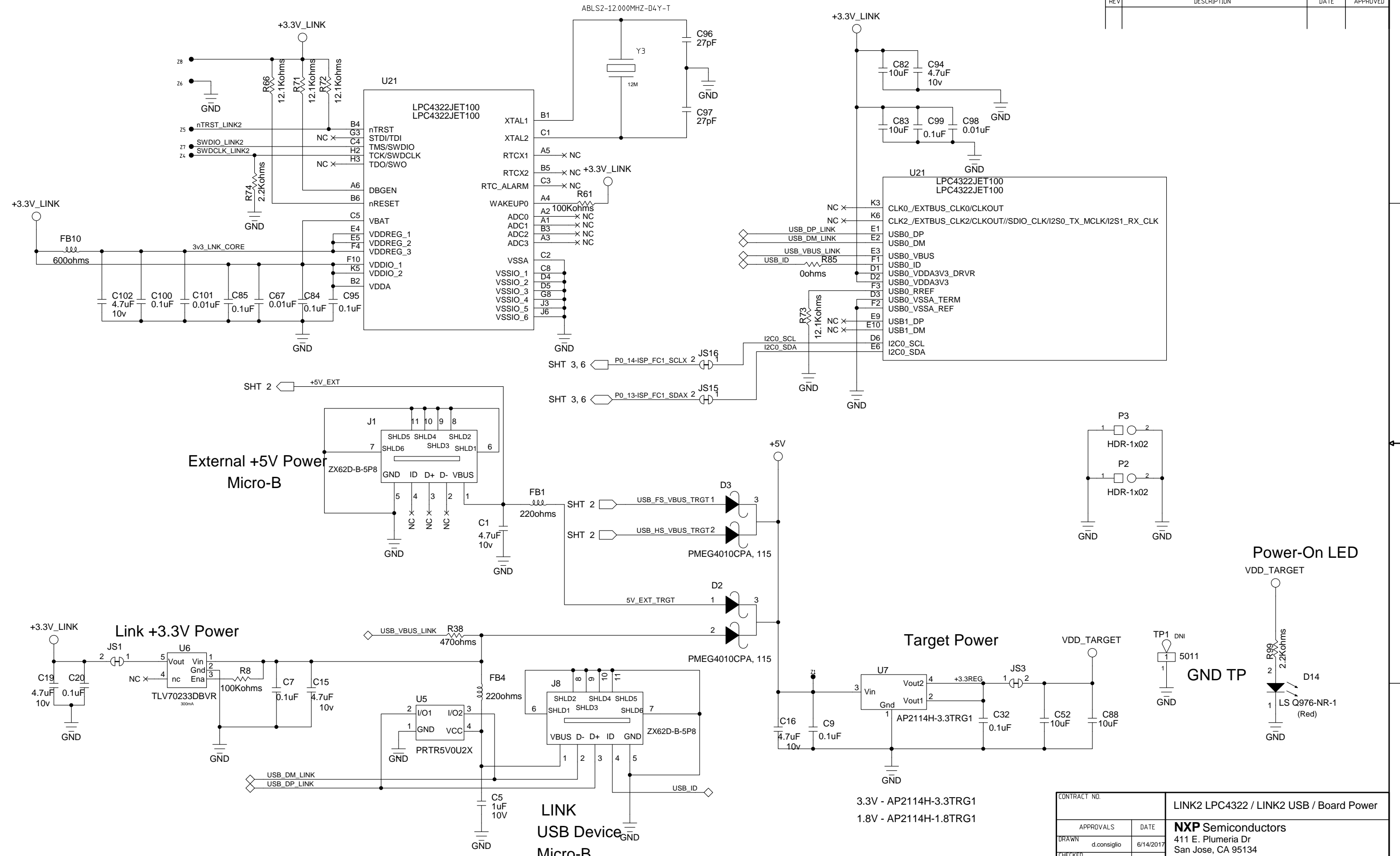


CONTRACT NO.		LPC54608 current monitor LINK2 Bridge buffer	
APPROVALS	DATE	NXP Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standards.nxp.com/microcontrollers/	
DRAWN	d.consiglio	6/14/2017	REV
CHECKED			
ISSUED	06/14/2017	SIZE FSCM NO.	DWG. NO.
		LPC546xx Eval brd D	
SCALE		SHEET 11 OF 13	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



CONTRACT NO.		LINK2 LPC4322 / LINK2 USB / Board Power			
APPROVALS	DATE	NXP Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/			
DRAWN	d.consiglio			6/14/2017	
CHECKED					
ISSUED	06/14/2017				
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		D		LPC546xx Eval brd	D
		SCALE			SHEET 13 OF 13