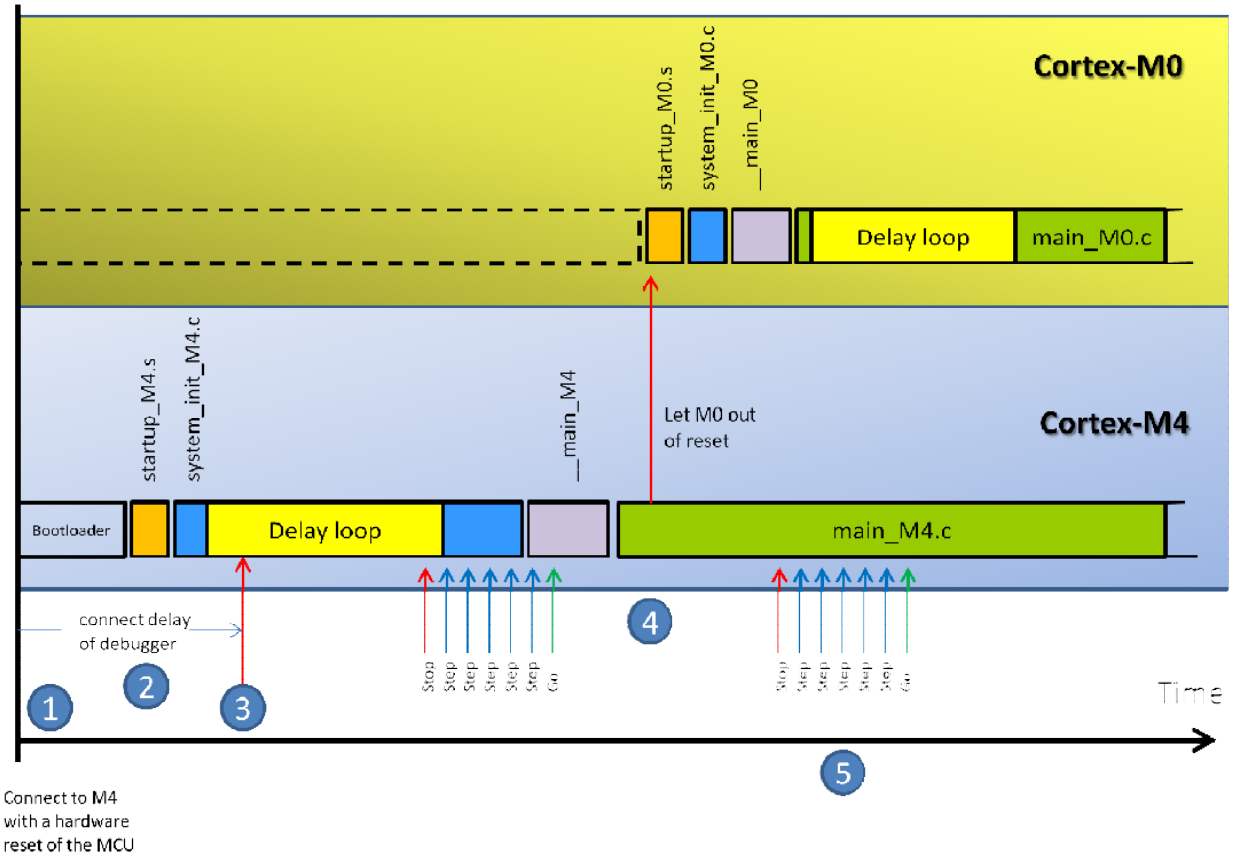
CONDITIONS FOR DEBUGGING LPC4357 DUAL CORE PROJECTS WITH IAR EWARM

- Tested with IAR EWARM 6.70
- I-jet Ver. A + NXP Link2 with J-Link firmware
- Project for Cortex-M4 in flash bank #A
- Project for Cortex-M0 in flash bank #B
- Delay loops at the beginning of the code for each core (see graphics)

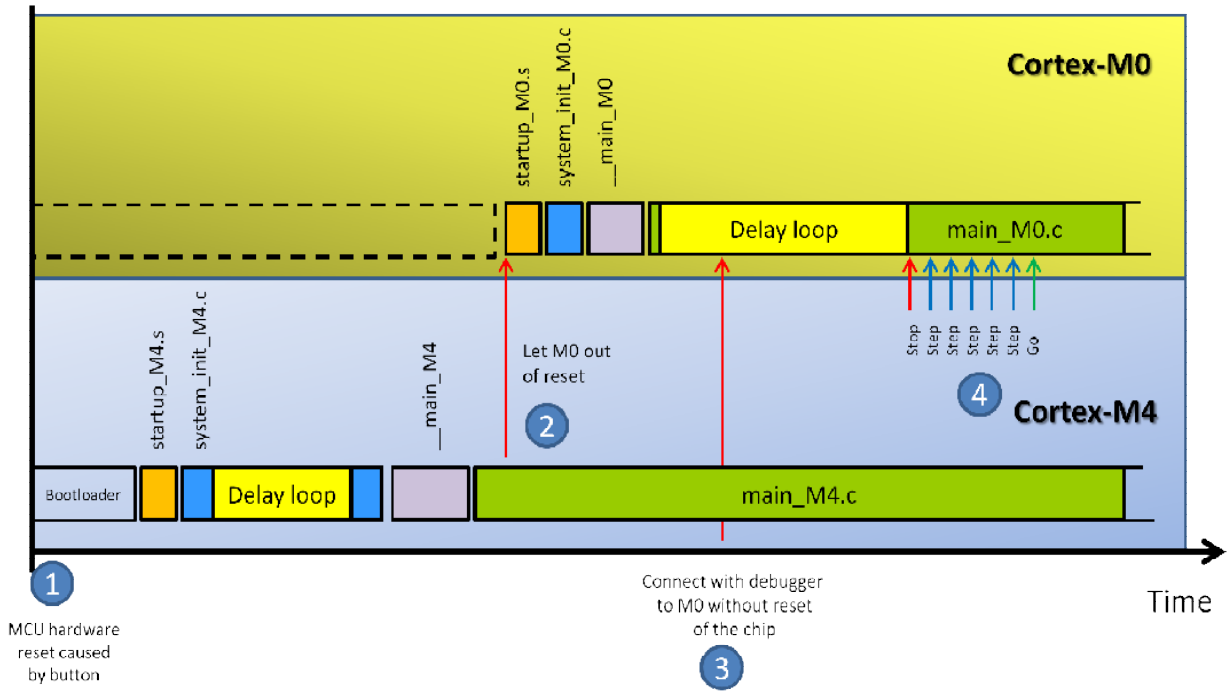
The timing principle (delay loops and order of debug connection) also applies to debugging with Keil µVision and other tools. The required settings for the debuggers are quite individual, but mostly more or less self explaining.

TIMING FLOW FOR DEBUGGING THE CORTEX-M4:



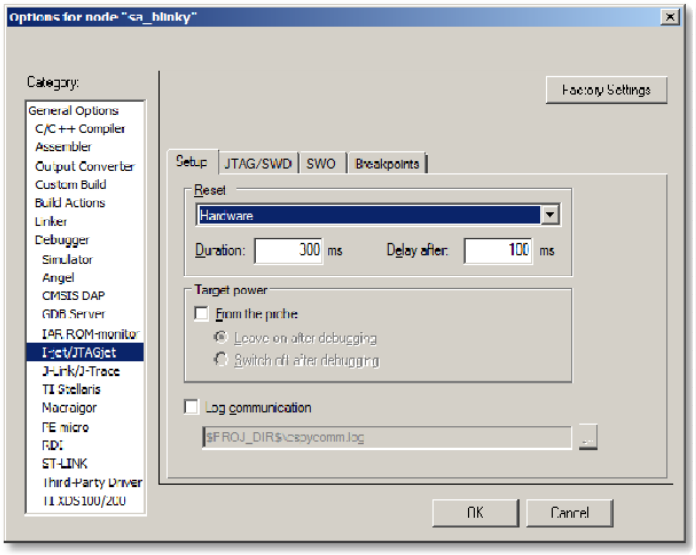
1) The debugger can (but mustn't) create a hardware reset to the MCU.
2) There is a (normally unspecified) period until the debugger tries to get access via SWD or JTAG. During this time the Cortex-M4 already runs through the bootloader and starts the application code. If this application code configures the chip by accident or by purpose in such a way that the JTAG access must fail, then at timing point 3 the access will fail. Therefore we have this delay loop at the beginning of the Cortex-M4 program code.
3) At this point in time the debugger gets access to the Cortex-M4. From here onwards the user can step through the M4 code. For the access to the Cortex-M4 you can use the JTAG port or the SWD port.
4) After the M4 code prepared the Cortex-M0 and took it out of reset, the Cortex-M0 runs independently from the Cortex-M4 core.
5) The debug control is limited to the Cortex-M4 core, any debugger activity here will not affect the run time behavior of the Cortex-M0.

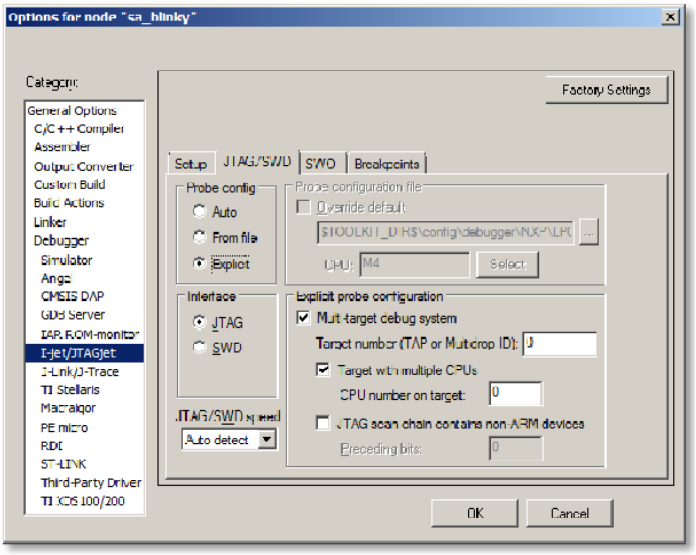
TIMING FLOW FOR DEBUGGING THE CORTEX-M0:



1) The user causes a hardware reset for the MCU. The debugger could do this job as well, but then you need to know the time period between the reset signal and the debugger access (see also the previous graphic) to ensure that the debugger access to the Cortex-M0 happens at the right time between 2 and 3.
2) After the M4 code prepared the Cortex-M0 and took it out of reset, the Cortex-M0 gets accessible in the scan chain and starts running independently from the Cortex-M4 core.
3) The debugger tries to get access to the Cortex-M0. This needs to be done without a reset signal to the rest of the chip. Otherwise the MCU starts over, the M0 goes back to reset state and is not longer accessible in the scan chain. Most of the debuggers do not accept this behavior and issue an error. Each debugger hardware/software follows individual strategies with regards to the reset control, possible settings for J-Link and I-jet are provided further below. If the JTAG access was successful, the user can start stepping through the M0 code.
   For the access to the Cortex-M0 you need to select the JTAG port, the SWD port works only for the Cortex-M4.
4) The debug control is limited to the Cortex-M0 core, any debugger activity here will not affect the run time behavior of the Cortex-M4.

M4 debug settings for I-jet:

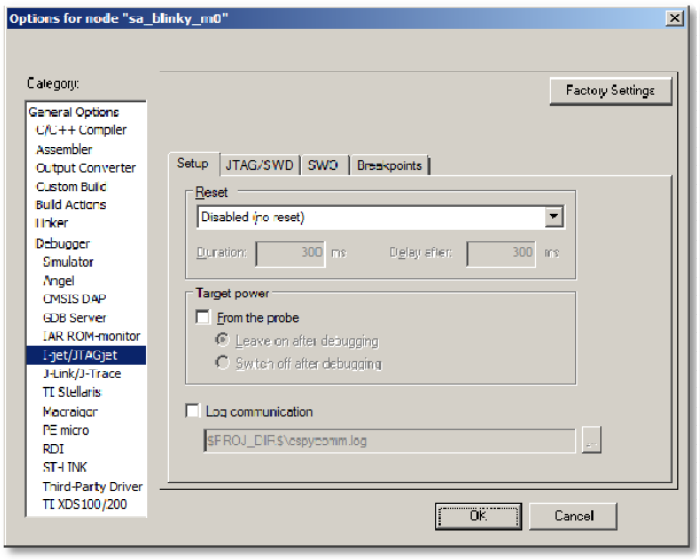


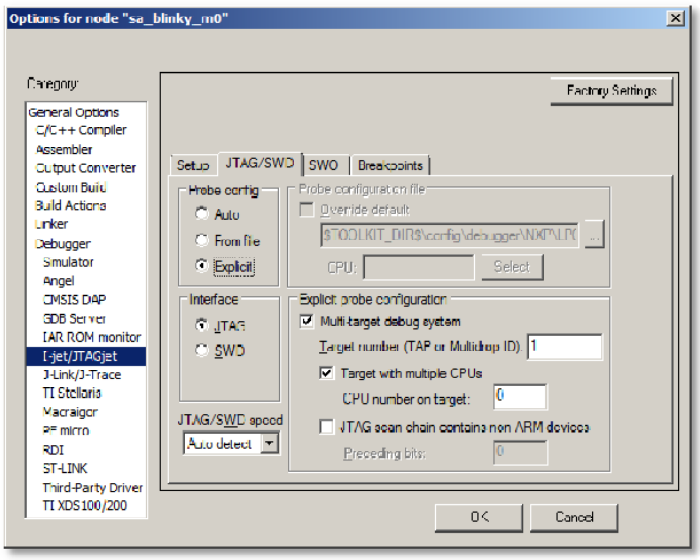


Log for a successful connection:

```
14:14:37: Loaded macro file:
C:\Users\nxp\Programs\IAR Systems\EWARM-6.7\arm\config\debugger\NXP\Trace_LPC18xx_LPC43xx.dmac
14:14:37: Loading the I-jet/JTAGjet driver
14:14:37: Probe: Probe SW module ver 1.23
14:14:37: Probe: Opened connection to I-jet:73159
14:14:37: Probe: USB connection verified (2585 packets/sec)
14:14:37: Probe: I-jet, FW ver 1, HW rev A
14:14:37: Probe: IJET-MIPI20 adapter detected
14:14:37: Probe: Versions: JTAG=1.54 SWO=1.21 A2D=1.41 Stream=1.26
14:14:37: EARM v.3.44
14:14:38: JTAG clock detected: 12MHz
14:14:38: JTAG chain configuration #0 converted to 4 CORTEX-M4:4 [IR bits].
14:14:38: Connecting Cortex-M core ID = 0x24770011 on DAP port 0
14:14:38: Recognized CPUID=0x410fc241 Cortex-M4 r0p1 arch ARMv7-M
14:14:38: Debug resources: 6 instruction comparators, 4 data watchpoints.
14:14:38: Emulation layer version 3.44
14:14:38: Emulation layer status 0x0
14:14:39: CPU status OK
14:14:39: LowLevelReset(hardware, delay 100)
14:14:39: CPU status - IN RESET
14:14:39: Connecting Cortex-M core ID = 0x24770011 on DAP port 0
14:14:39: Recognized CPUID=0x410fc241 Cortex-M4 r0p1 arch ARMv7-M
14:14:39: Debug resources: 6 instruction comparators, 4 data watchpoints.
14:14:39: CPU status OK
14:14:40: Loaded debugee:
C:\Temp\lpcopen_2_09_mcb_4357\applications\lpc18xx_43xx\iar_ewarm_projects\keil_mcb_4357\dualcor
e\sa_blinky\iar_output\keil_mcb_4357\Exe\sa_blinky.out
14:14:40: SWO: Manchester, CPU clock = 72000kHz, Auto divider = 4
14:14:40: Warning: TDO is used as JTAG pin. Select SWD mode or TraceD0 as SWO pin.
14:14:40: Measuring channel[s] ITrgPwr started. Sampling Frequency 23437Hz.
14:14:40: Measurements stopped
14:14:40: Download completed.
14:14:40: LowLevelReset(software, delay 100)
14:14:40: SWO: Manchester, CPU clock = 72000kHz, Auto divider = 4
14:14:40: Warning: TDO is used as JTAG pin. Select SWD mode or TraceD0 as SWO pin.
14:14:40: Target reset
14:14:40: There were 2 warnings during the initialization of the debugging session.
```

M0 debug settings for I-jet:

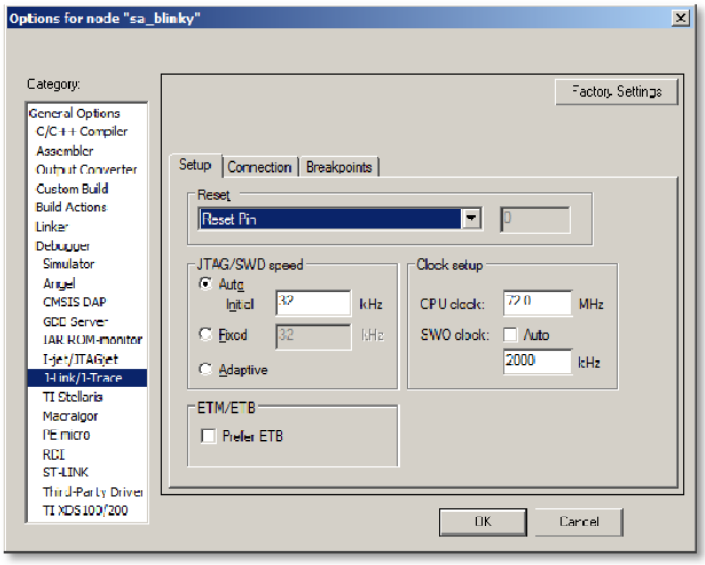


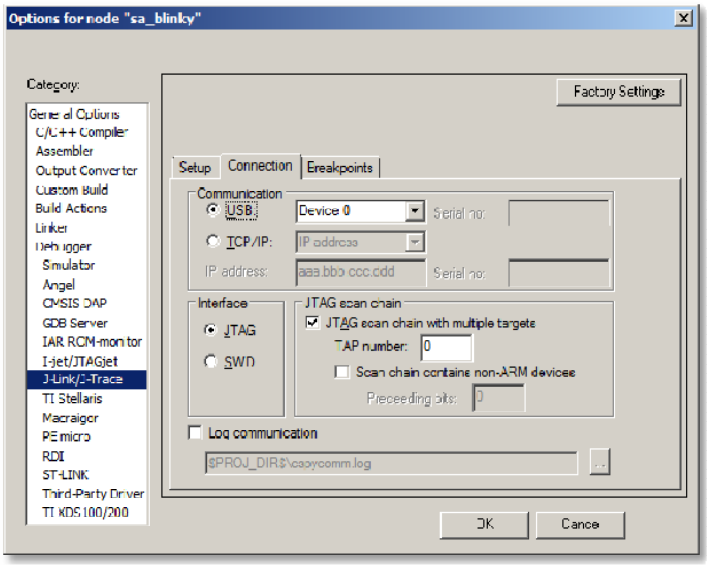


Log for a successful connection:

```
13:58:13: Loaded macro file:
C:\Users\nxp\Programs\IAR Systems\EWARM-6.7\arm\config\debugger\NXP\Trace_LPC18xx_LPC43xx.dmac
13:58:13: Loading the I-jet/JTAGjet driver
13:58:13: Probe: Probe SW module ver 1.23
13:58:13: Probe: Opened connection to I-jet:73159
13:58:13: Probe: USB connection verified (2605 packets/sec)
13:58:13: Probe: I-jet, FW ver 1, HW rev A
13:58:13: Probe: IJET-MIPI20 adapter detected
13:58:13: Probe: Versions: JTAG=1.54 SWO=1.21 A2D=1.41 Stream=1.26
13:58:13: EARM v.3.44
13:58:14: JTAG clock detected: 12MHz
13:58:14: JTAG chain configuration #1 converted to CORTEX-M0:4 4 [IR bits].
13:58:14: Connecting Cortex-M core ID = 0x4770021 on DAP port 0
13:58:14: Recognized CPUID=0x410cc200 Cortex-M0 r0p0 arch ARMv6-M
13:58:14: Debug resources: 2 instruction comparators, 1 data watchpoints.
13:58:14: Emulation layer version 3.44
13:58:14: Emulation layer status 0x0
13:58:14: Connecting Cortex-M core ID = 0x4770021 on DAP port 0
13:58:14: Recognized CPUID=0x410cc200 Cortex-M0 r0p0 arch ARMv6-M
13:58:14: Debug resources: 2 instruction comparators, 1 data watchpoints.
13:58:14: CPU status OK
13:58:14: LowLevelReset(disabled, delay 200)
13:58:15: Loaded debugee:
C:\Temp\lpcopen_2_09_mcb_4357\applications\lpc18xx_43xx\iar_ewarm_projects\keil_mcb_4357\dualcor
e\sa_blinky_m0\iar_output\keil_mcb_4357\Exe\sa_blinky_m0.out
13:58:15: Measuring channel[s] ITrgPwr started. Sampling Frequency 23437Hz.
13:58:15: Measurements stopped
13:58:15: Download completed.
13:58:15: LowLevelReset(software, delay 200)
13:58:15: Target reset
13:58:20: CPU status - SLEEPING
13:58:21: CPU status OK
```

M4 debug settings for J-Link:

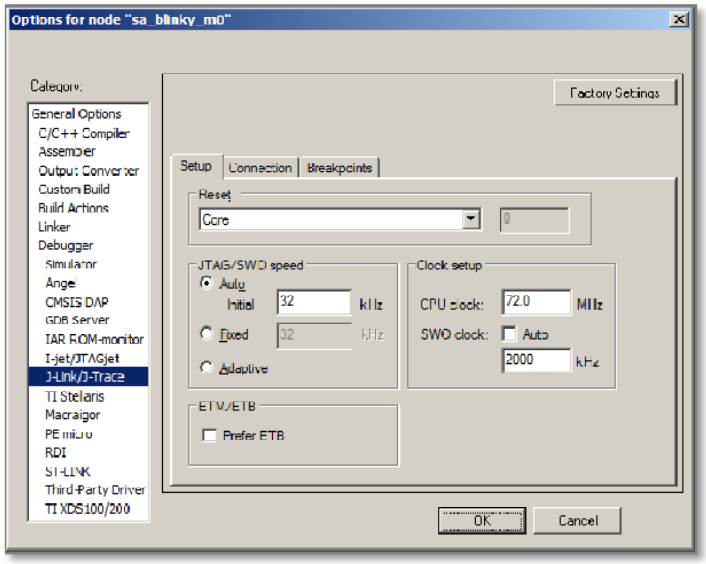


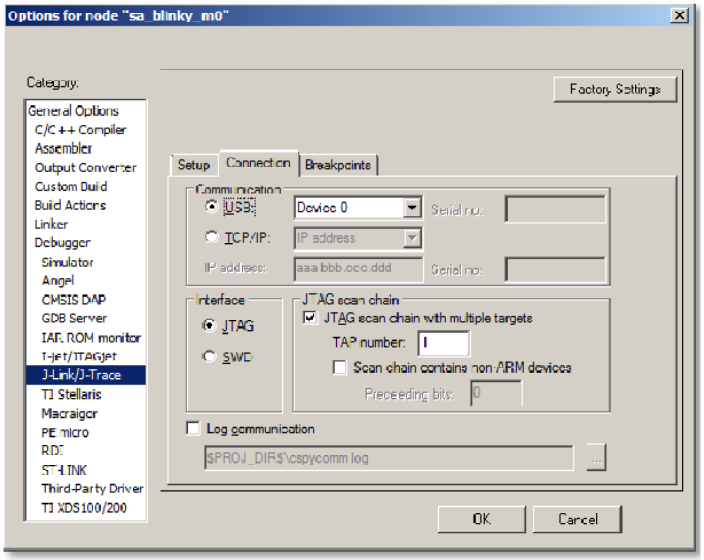


Log for a successful connection:

```
14:29:42: Loaded macro file:
C:\Users\nxp\Programs\IAR Systems\EWARM-6.7\arm\config\debugger\NXP\Trace_LPC18xx_LPC43xx.dmac
14:29:43: JLINK command: ProjectFile =
C:\Temp\lpcopen_2_09_mcb_4357\applications\lpc18xx_43xx\iar_ewarm_projects\keil_mcb_4357\dualcor
e\sa_blinky\settings\sa_blinky_iflash_keil_mcb_4357.jlink, return = 0
14:29:43: JLINK command: scriptfile = C:\Users\dep00717\Programs\IAR Systems\EWARM-
6.7\arm\config\debugger\NXP\LPC4350_DebugCortexM4.JLinkScript, return = 0
14:29:43: Device "LPC4357_M4" selected (1024 KB flash, 40 KB RAM).
14:29:43: DLL version: V4.80g, compiled Feb 13 20:50:02
14:29:43: Firmware: J-Link LPC-Link 2 compiled May 31 2013 17:31:46
14:29:43: JTAG speed is initially set to: 32 kHz
14:29:43: NXP LPC4350 (Cortex-M4+M0 core) J-Link script
14:29:43: TotalIRLen = 8, IRPrint = 0x0011
14:29:43: J-Link script: Cortex-M0 already enabled.
14:29:43: TotalIRLen = 8, IRPrint = 0x0011
14:29:43: Found Cortex-M4 r0p1, Little endian.
14:29:43: FPUnit: 6 code (BP) slots and 2 literal slots
14:29:43: TPIU fitted.
14:29:43: ETM fitted.
14:29:43: ETB present.
14:29:43: Configured reset type is not supported for this device. Changing reset type to type 0
14:29:51: Hardware reset with strategy 2 was performed
14:29:51: Initial reset was performed
14:29:51: Found 2 JTAG devices, Total IRLen = 8:
14:29:51:  #0 Id: 0x4BA00477, IRLen:  4, IRPrint: 0x1 CoreSight JTAG-DP
14:29:51:  #1 Id: 0x0BA01477, IRLen:  4, IRPrint: 0x1 CoreSight SW-DP
14:29:52: 9820 bytes with download suppressed
14:29:52: Loaded debugee:
C:\Temp\lpcopen_2_09_mcb_4357\applications\lpc18xx_43xx\iar_ewarm_projects\keil_mcb_4357\dualcor
e\sa_blinky\iar_output\keil_mcb_4357\Exe\sa_blinky.out
14:29:52: Software reset was performed
14:29:52: Target reset
```

M0 debug settings for J-Link:





Log for a successful connection:

```
14:27:44: Loaded macro file:
C:\Users\nxp\Programs\IAR Systems\EWARM-6.7\arm\config\debugger\NXP\Trace_LPC18xx_LPC43xx.dmac
14:27:45: JLINK command: ProjectFile =
C:\Temp\lpcopen_2_09_mcb_4357\applications\lpc18xx_43xx\iar_ewarm_projects\keil_mcb_4357\dualcor
e\sa_blinky_m0\settings\sa_blinky_m0_iflash_keil_mcb_4357.jlink, return = 0
14:27:45: JLINK command: scriptfile = C:\Users\dep00717\Programs\IAR Systems\EWARM-
6.7\arm\config\debugger\NXP\LPC4350_DebugCortexM0.JLinkScript, return = 0
14:27:45: Device "LPC4357_M0" selected (0 KB flash, 0 KB RAM).
14:27:45: DLL version: V4.80g, compiled Feb 13 20:50:02
14:27:45: Firmware: J-Link LPC-Link 2 compiled May 31 2013 17:31:46
14:27:45: JTAG speed is initially set to: 32 kHz
14:27:45: NXP LPC4350 (Cortex-M4+M0 core) J-Link script
14:27:45: TotalIRLen = 8, IRPrint = 0x0011
14:27:45: TotalIRLen = 8, IRPrint = 0x0011
14:27:45: Found Cortex-M0 r0p0, Little endian.
14:27:45: FPUnit: 2 code (BP) slots and 0 literal slots
14:27:45: J-Link script: Performing reset sequence
14:27:45: Hardware reset with strategy 1 was performed
14:27:45: Initial reset was performed
14:27:45: Found 2 JTAG devices, Total IRLen = 8:
14:27:45:  #0 Id: 0x4BA00477, IRLen:  4, IRPrint: 0x1 CoreSight JTAG-DP
14:27:45:  #1 Id: 0x0BA01477, IRLen:  4, IRPrint: 0x1 CoreSight SW-DP
14:27:46: 4004 bytes with download suppressed
14:27:46: Loaded debugee:
C:\Temp\lpcopen_2_09_mcb_4357\applications\lpc18xx_43xx\iar_ewarm_projects\keil_mcb_4357\dualcor
e\sa_blinky_m0\iar_output\keil_mcb_4357\Exe\sa_blinky_m0.out
14:27:46: J-Link script: Performing reset sequence
14:27:46: Software reset was performed
14:27:46: Target reset
14:27:46: Failed to read one or more register values (busy).
```