Understanding LPC55S6x Revisions and Tools

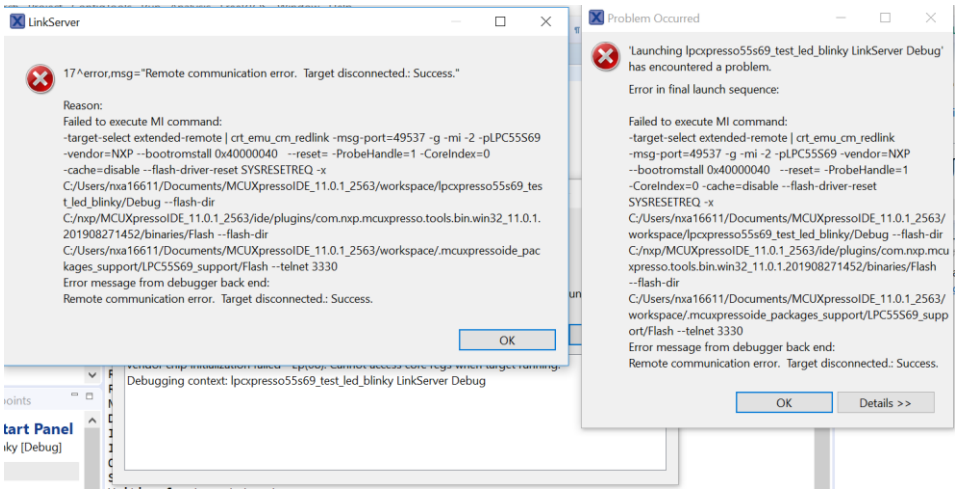
At the time of the LPC55S6x launch, the latest silicon revision of the LPC55S6x is revision 1B. Since Nov,2019, all the LPCXpresso55S69 EVK boards marked as Revision A2 are equipped with revision 1B silicon.

NXP introduced its new debug session request functionality on silicon revision 1B. For some IDE versions, the method of initiating a debug session is designed for current 1B silicon revisions and will result in an endless loop when used on older revision 0A parts. The protocol for this debug connection method is included in the latest LPC55S6x/S2x/2x User Manual, section ***Debug session protocol***.

IDE Consideration:

- MCUXpresso IDE:

  Due to above debug access protocol changes, the latest MCUXpresso IDE v11.0.1, who expects silicon to handle silicon revision 1B debug session requests correctly, can't connect silicon revision 0A production under some situations. When connecting LPCXpresso55S69 Revision A1 board, you may have connection error like this:



NXP has released MCUXpresso IDE v11.0.1 LPC55xx Debug Hotfix① for this issue. Please follow the steps to fix the issue if you use IDE v11.0.1 with silicon revision 0A:

https://community.nxp.com/community/mcuxpresso/mcuxpresso-ide/blog/2019/10/30/mcuxpresso-ide-v1101-lpc55xx-debug-hotfix

The newer version of MCUXpresso IDE has already fixed this issue.

- IAR:

  According to our test:

  IAR Embedded Workbench for ARM v8.42 and later can support both silicon revision 1B and 0A production without issue, which can be downloaded from

  https://www.iar.com/iar-embedded-workbench/tools-for-arm/arm-cortex-m-edition/

  Note: The IAR 8.50.5 changed the CMSIS-DAP debug support for trustzone feature. There is **known debug issue** with the combination of IAR 8.50.5+SDK2.8.0. Thus our recommendation is:

  - Use IAR 8.50.5 with SDK2.8.0
  - Use IAR 8.40.2 with SDK 2.7.1

- Keil MDK:

  Both Keil MDK v5.28 and v5.29+ latest LPC55S69 pack v12.01 can support silicon reversion 1B without problem but can't support silicon revision 0A.

LPC55S69 Revision 0A vs. 1B

Silicon Revision	**0A production**	**1B production**
Board Revision	A1	A2
Deliver Date	Before Nov,2019	After Nov,2019
Debug Access	None	Add New Debug Session Access Method
Secure Boot Revision	SB2.0	SB2.1

Maximum CPU Frequency	100MHz	150MHz
IDE revision required	1. MCUXpresso IDE v11.0.0 and older 2. MCUXpresso IDE v11.0.1 + hotfix① 3. MCUXpresso IDE next version	MCUXpresso IDE v11.0.0 and newer
SDK version	SDK2.5 and newer are supported; SDK2.6.3 and newer are recommended	SDK2.6.3 and newer

LPC55S69 Defect Fix: 0A vs. 1B

0A Production	1B Production
Defect: For PRINCE encrypted region, partial erase cannot be performed	Fixed
Defect: For PUF based key provisioning, a reset must be performed	Fixed
Defect: Unprotected sub regions in PRINCE defined regions cannot be used.	Fixed
Defect: Last page of image is erased when simultaneously programming the signed image and CFPA region	Fixed
Defect: the minimum operating range is 1.85 V.	Fixed: The LPC55S6x operating voltage range specification is from 1.80 V to 3.6 V.
Defect: PHY does not auto-power down in suspend mode	Fixed

For more detail, see Errata sheet LPC55S6x which can be downloaded from NXP web site.

Pre-production Silicon:

Note that NO BOARDS WERE EVER SOLD THROUGH DISTRIBUTION WITH PRE-PRODUCTION SILICON. In case you have board marked with Revision 1, 2 ,A, or A1 board with 1B silicon, contact NXP to ask for production replacement.

Get Silicon Revision:

The silicon revision info is marked on the chip and board revision is marked on the board silkscreen. For silicon revision marking information, please consult LPC55S6x Data Sheet *section 4. Marking* . Below is an example of silicon revision marking information where revision is highlighted in red:

The LPC55S6x VFBGA98 package has the following top-side marking:

- First line: LPC55S6x
- Second line: JEV98
- Third line: xxxxxxxx
- Fourth line: zzzyywwxR
  - yyww: Date code with yy = year and ww = week.
  - xR: Device revision 1B

The LPC55S6x HLQFP100 package has the following top-side marking:

- First line: LPC55S6x
- Second line: xxxxxxxx
- Third line: zzzyywwxR
  - yyww: Date code with yy = year and ww = week.
  - xR: Device revision 0A or Device revision 1B

The LPC55S6x HTQFP64 package has the following top-side marking:

- First line: LPC55S6x
- Second line: JBD64
- Third line: xxxx
- Fourth line: xxxx
- Third line: zzzyywwxR
  - yyww: Date code with yy = year and ww = week.
  - xR: Device revision 1B

The user application can also get the silicon revision through chip revision ID and number: SYSCON->DIEID:

Table 149. Chip revision ID and number (DIEID, offset = 0xFFC)

Bit	Symbol	Description	Reset value
3:0	REV_ID	Device Revision. Value read as 0x0 applies to device revision 0A and 0x1 to device revision 1B.	0x1
31:4	-	Reserved. Read value is undefined, only zero should be written.	undefined