Kinetis Lock issue analysis and unlock way

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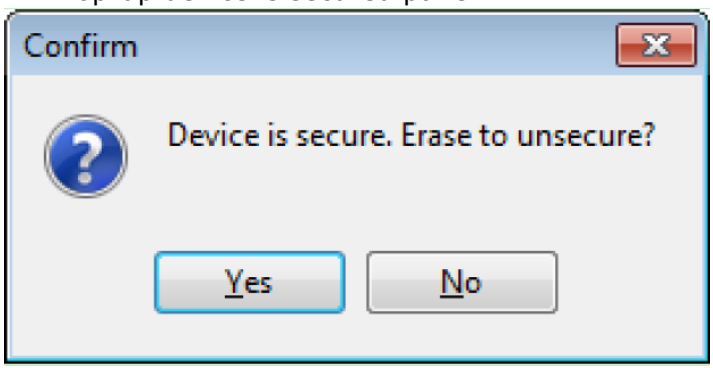
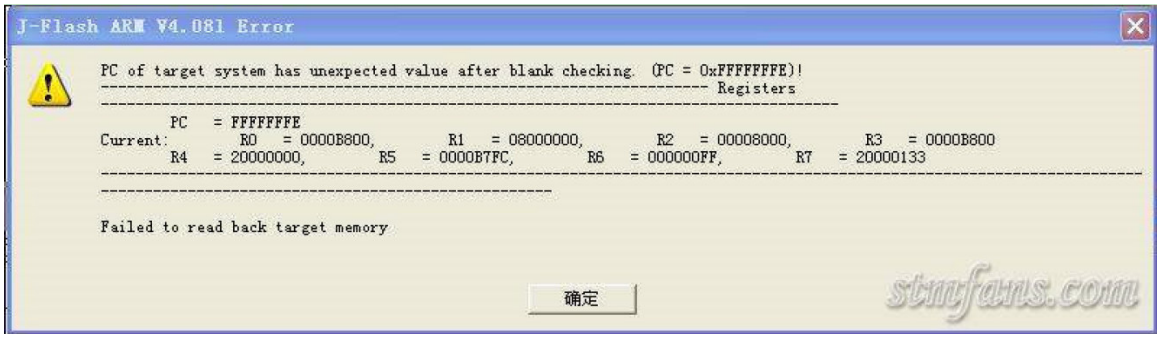
Customer may meet Kinetis chips lock issue during software debug, prototype production, mass-production phase. This document will try to list the potential root causes and how to figure out.

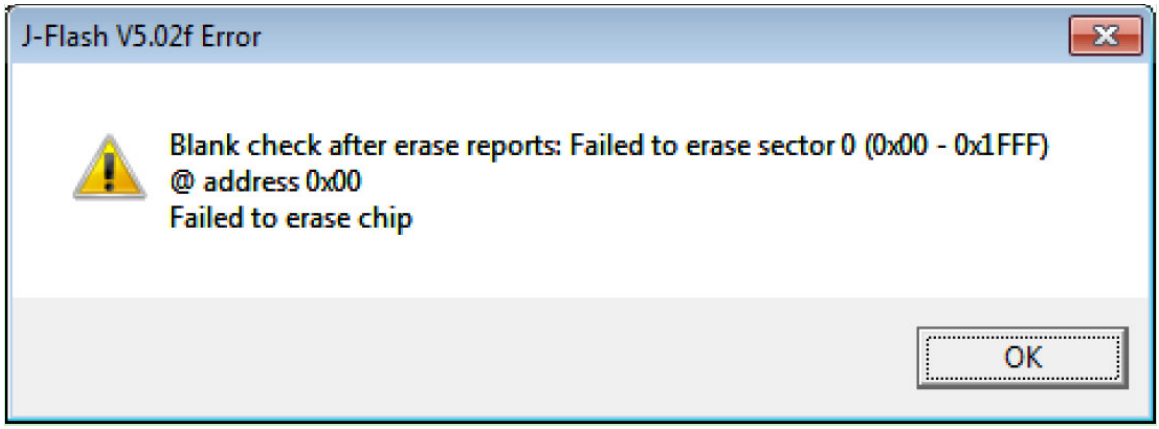
1. Kinetis locked behaviors
   1.1 During IDE debug phase, it couldn't find the device and debug processing halted.
   1.2 Pop-up device is secured panel:



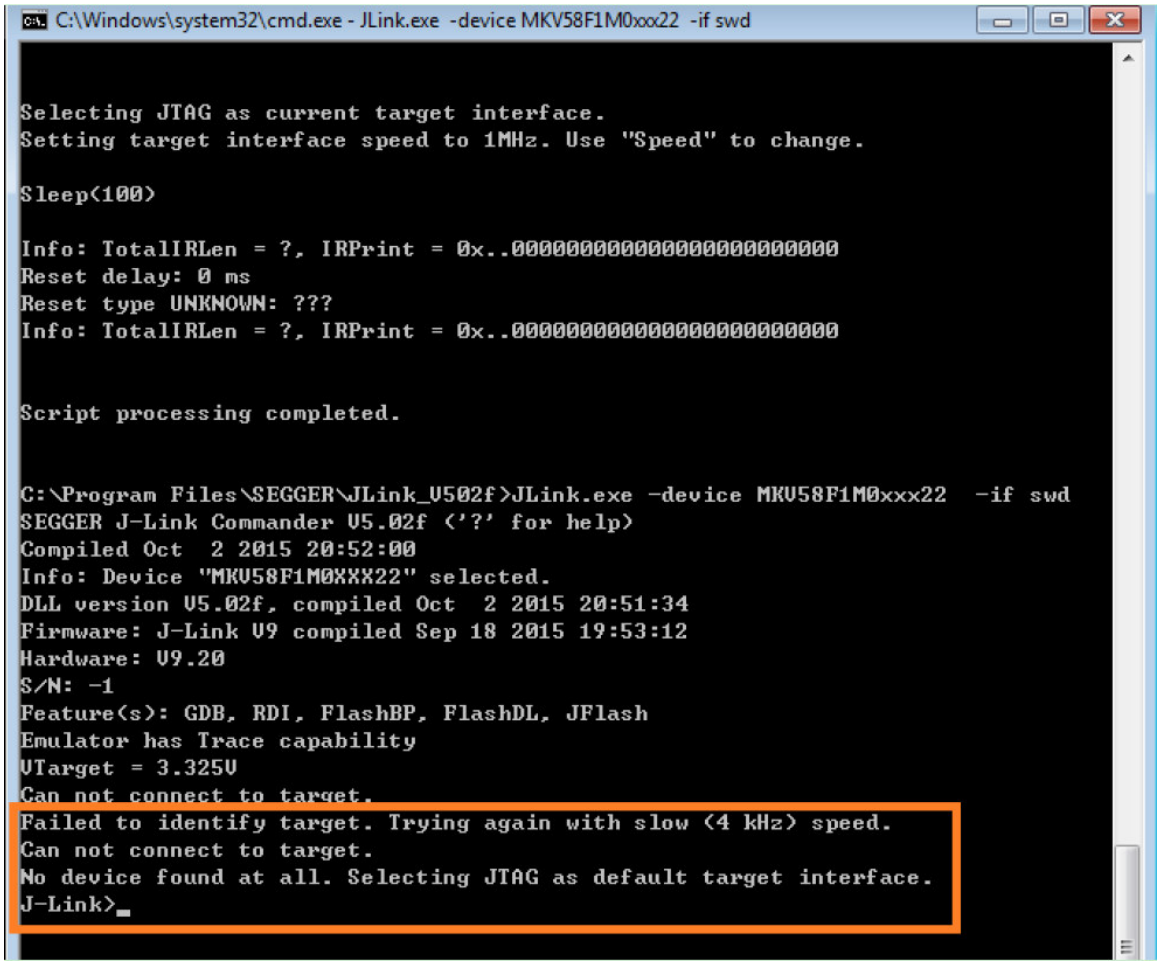
   1.3 No connection for J-Flash tool



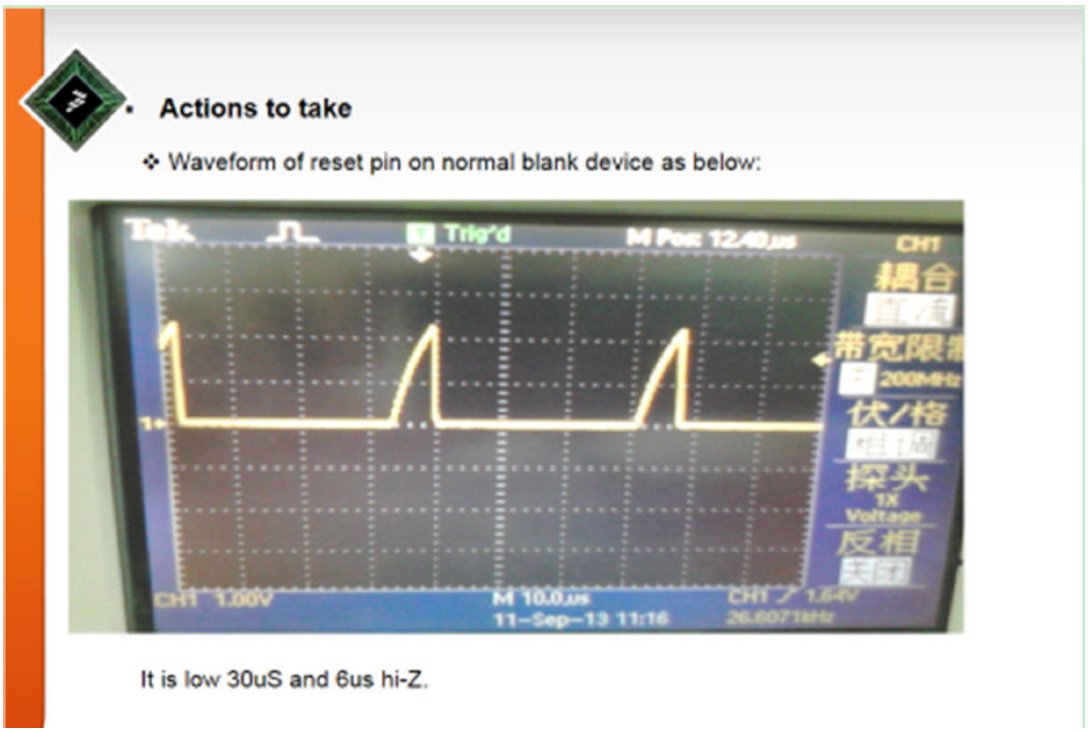
   1.4 Even connected, it will report "RAM check failed" error and no operation available



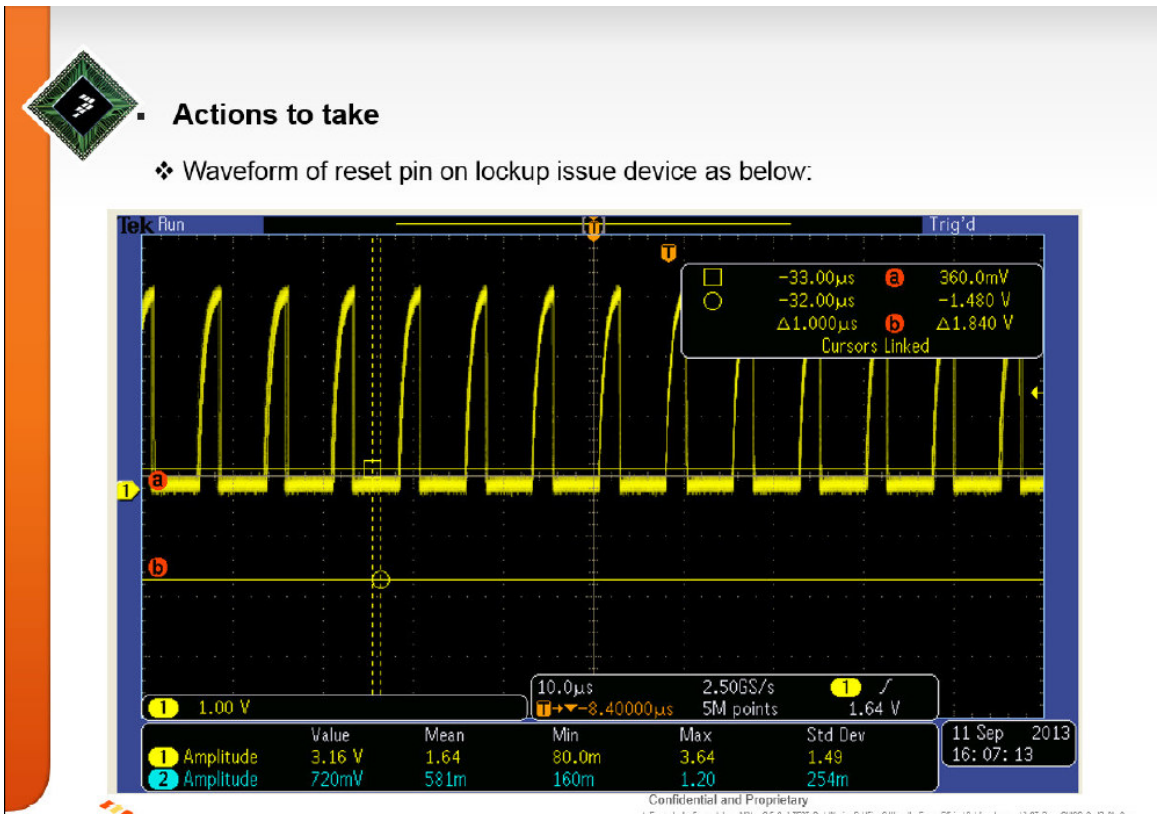
1.5 Using J-Link commander tool, could not find MCU core



1.6 With power up, Reset pin will always with low voltage, or output oscillated signals (different with blanked chip), for example, KL chip without programmed, the reset pin output normal signal period is 36us and low voltage about 30us:



Locked KL chip the reset pin output signal with higher frequency, the signal may be different. And if the external circuit exists capacitive reactance, the signal period maybe changed.



Above behaviors most meet during software debug and production phase.

2. What's could be the root cause? It belongs to inevitable reasons and possible causes.

2.1 Inevitable reasons

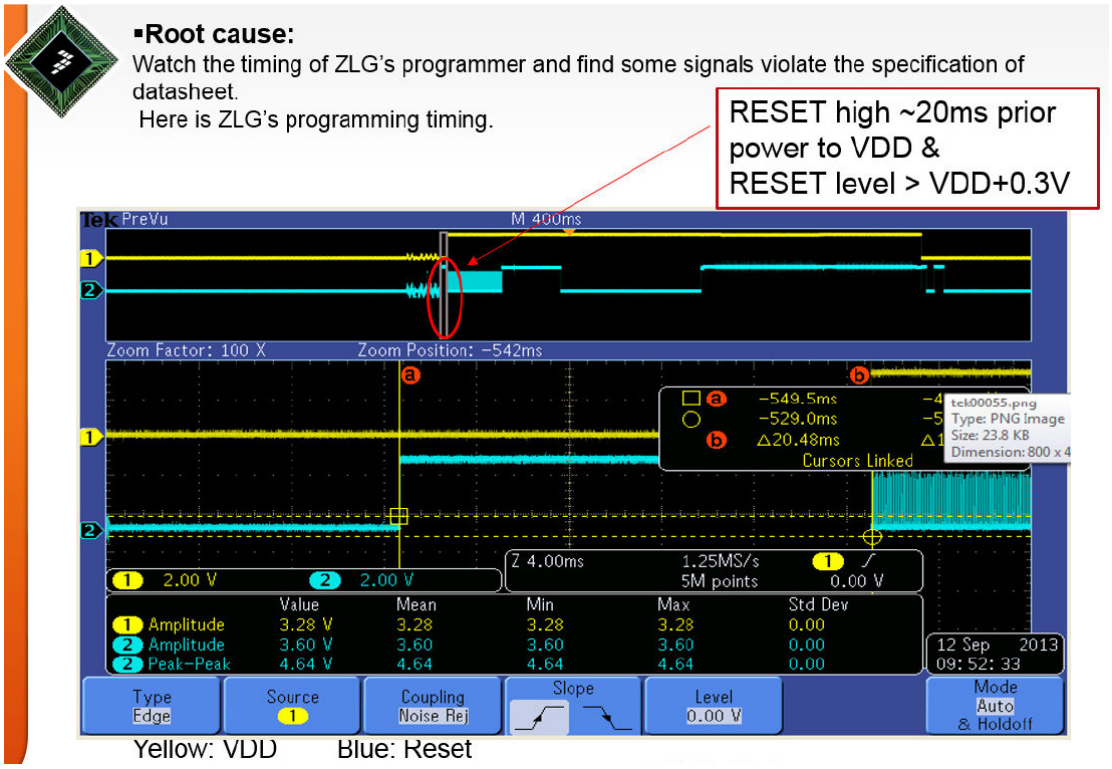
<1> Welding problem: This problem with the highest probability during production phase. There with requirement the solder package peak temperature is 260° C, while during prototype production phase, there with problem to control the soldering temperature and the chip locked. That issue is hard to recover and maybe the chip is damaged. Even if there with temperature controlled (within 260° C) soldering station, the soldering time also be a consideration factor. The long soldering time also could cause chip locked. It must control the package peak temperature below 260° C with using SMT machine.

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

<2> Power up sequence: if reset pin power up earlier than VDD, it will lock the chip and hard to recover. It must be careful to check the power up sequence with power circuit or programmer tool.



<3> Add high voltage to Reset pin to modify the chip internal NVM/IFR setting, which was confirmed a manufactory operation, in order to change the chip ID configuration.

The mode of operation is latched on the rising edge of the reset pin. The monitor mode is selected by connecting two port lines to V_{ss} and applying an over-voltage of approximately 2 x V_{DD} to the $\overline{IRQ1}$ pin concurrent with the rising edge of reset (see Table 3-1). Port allocation varies from part to part.

Table 3-1. Mode Selection

$\overline{IRQ1}$ Pin	Port x	Port y	Mode
≤ V_{DD}	X	X	User
2 x V_{DD}	1	0	Monitor

<4> Too long debugger cable (such as 40~50cm) can lock the chip and make the debugger working unstable.

<5> Set chip in secured state, could be unsecured with external mass erased.

<6> Using fake J-Link tool can damage the debug port and cause chip lock.

Testing on the ATE revealed that four of the devices failed for leakage on various pins including the RESET pin. Unpowered curve trace analysis showed the RESET pin was open on Device 1 and normal on the remaining four units. The TCLK pin had no positive diode on Device 1 and leakage on Devices 2, 3, and 4. Devices 2, 3, and 4 exhibited leakage between Vdd and ground. Device 2 was selected for further analysis and decapsulated. OBIRCH (Optical Beam Induced Resistance Change) revealed a unique site near the JTAG TCLK pin. A visual inspection found evidence of EOS. Deprocessing and visual inspections found damage indicative of EOS.

2.2 Possible causes

<1> Hot plug.

<2> Software code: for example: enable LVD detection, program Flash to record this case and cause Flash content was modified; Frequently Erase-Program-Read cycling test trigger Flash self-protection mechanism.

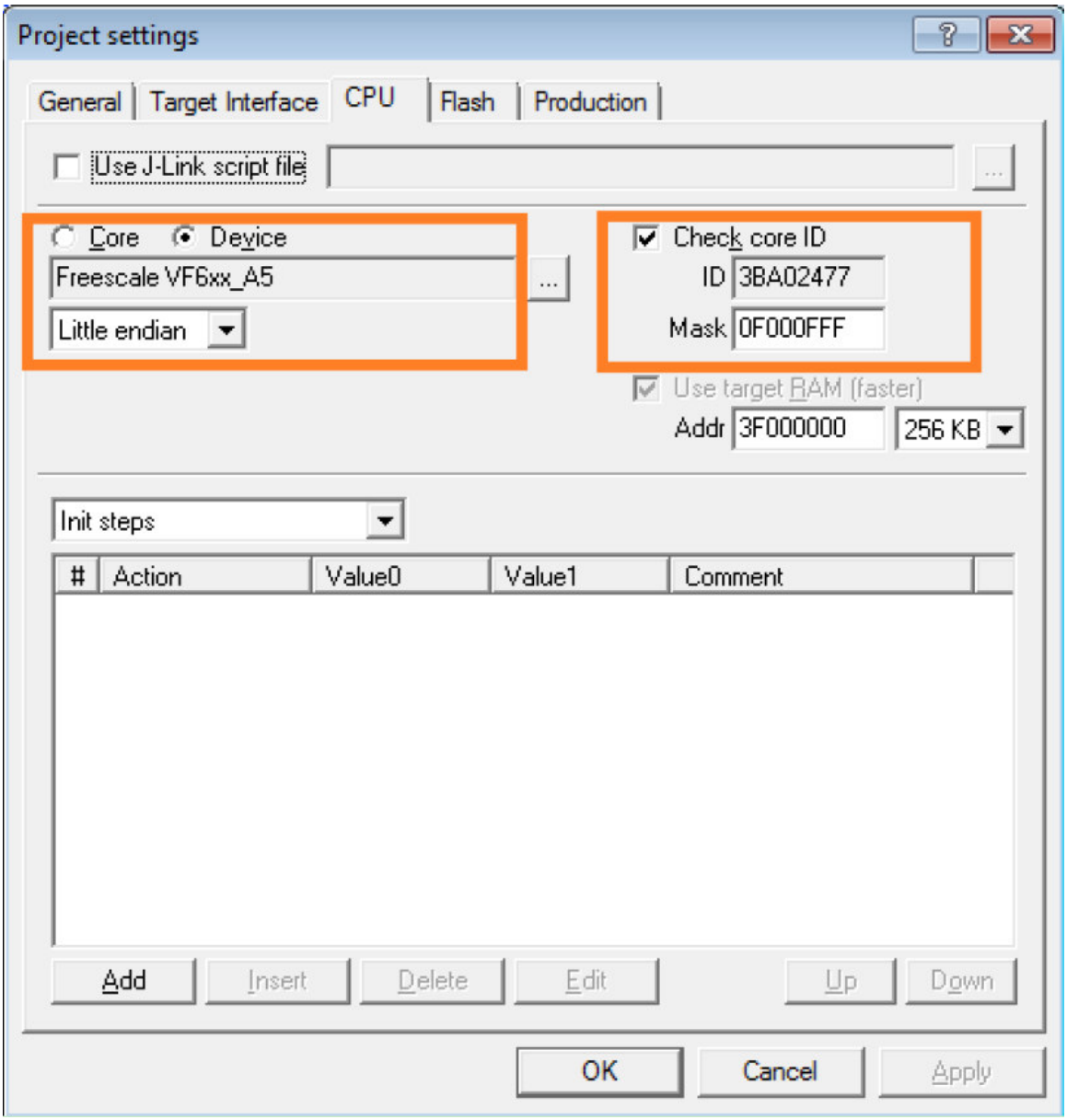
<3> Unstable power.

<4> Unstable debugger signals or glitch.

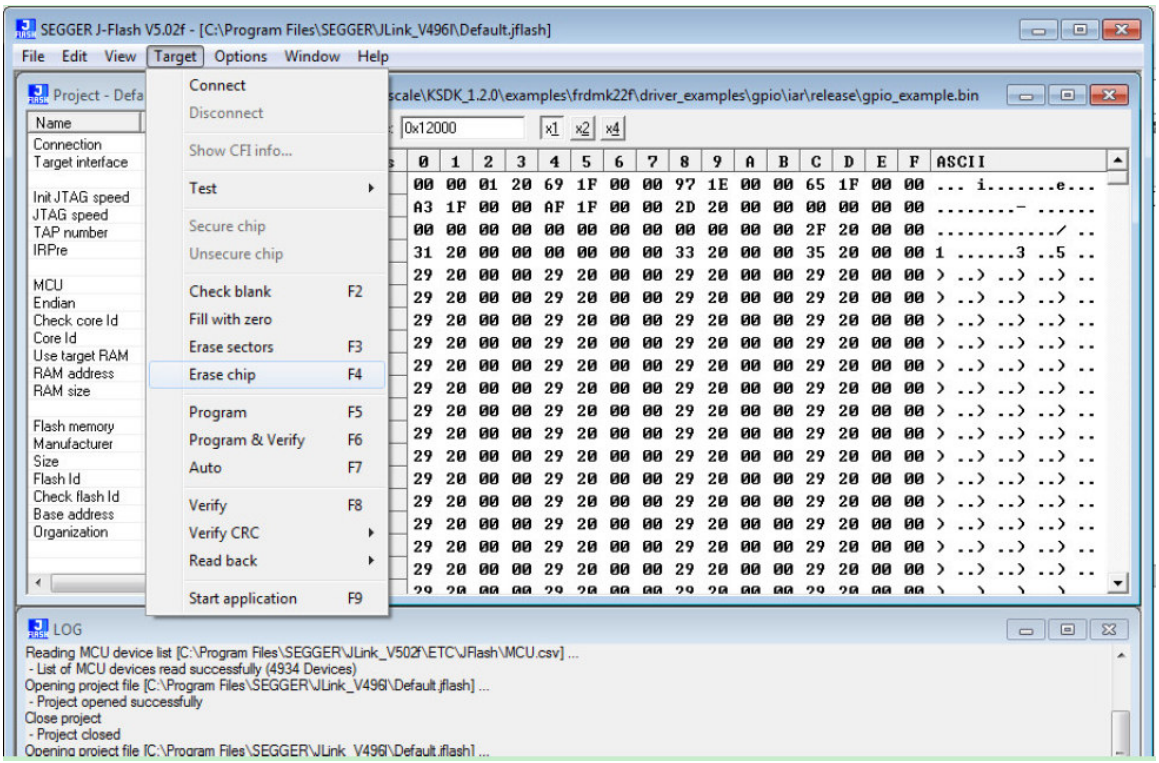
3. Unlock way (from easy to complex)

<1> It could check the reset pin signal, for the blanked chip will output the saw wave. Using the IDE software download the program will unlock the chip. If the chip was locked, it would pop up “chip secured” notification. Just using external mass erase will unlock the chip.

<2> Using J-Flash software and select chip part number and click [Check core ID], then connect the chip. The J-Flash tool try to find the device and compare with the core ID. If core ID isn’t match or could not find the device, the connection will be failed.



<3> If connection done, then using [Target] menu's [Erase chip] command to unlock the chip.



<4> If above steps don't work, keep the reset pin low and using [erase chip] command again.

<5> If still not work, please use J-Link software command window and using "unlock Kinetis" command to unlock the chip. Using this way, the chip's reset pin should connect with debugger's reset pin.

<6> Using Erase_all_pin.jlk script with J-Link tool. In J-Link software command window call "Jlink.exe erase_all_pin.jlk" and check the log, which will indicate if find the "Debug Access Port" and if using this port find MCU core. If it could find the AHB-AP, then it can use this interface to access MDM-AP and to check MCU status & ID.

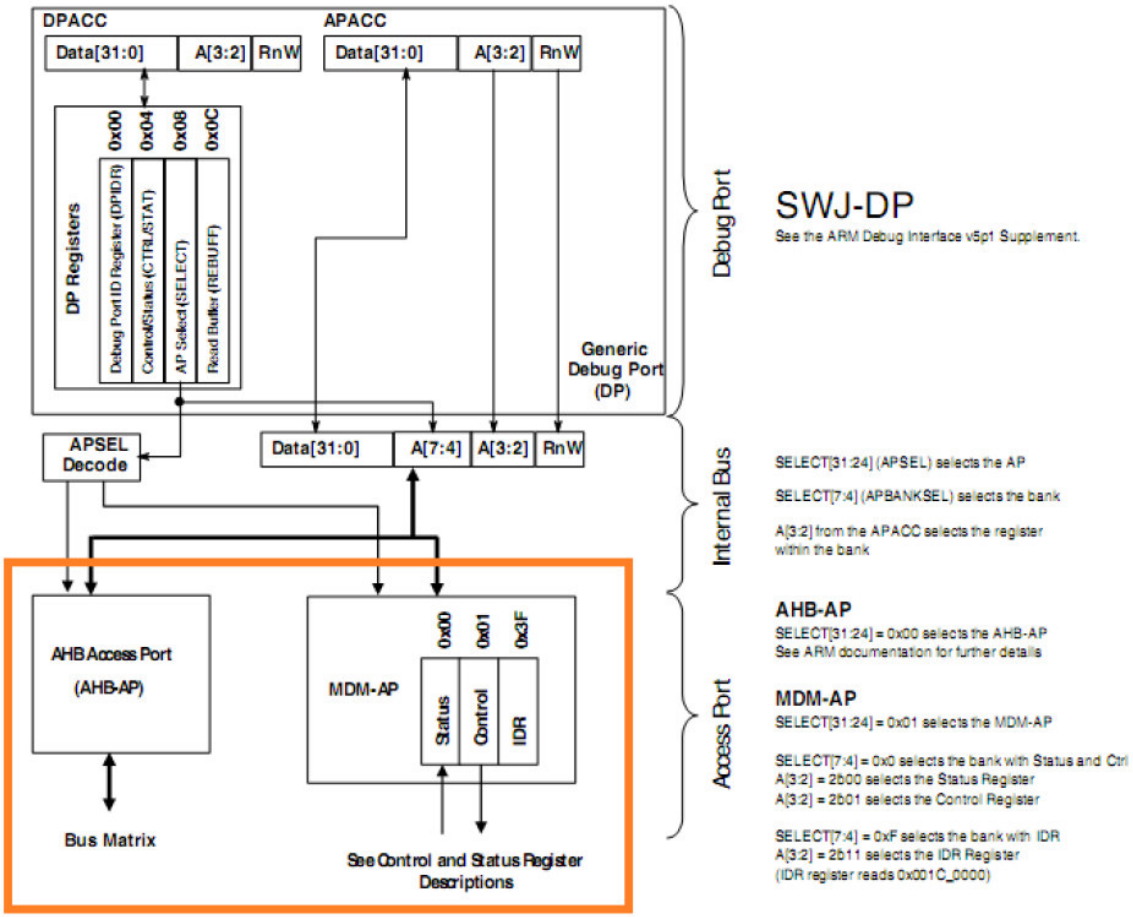
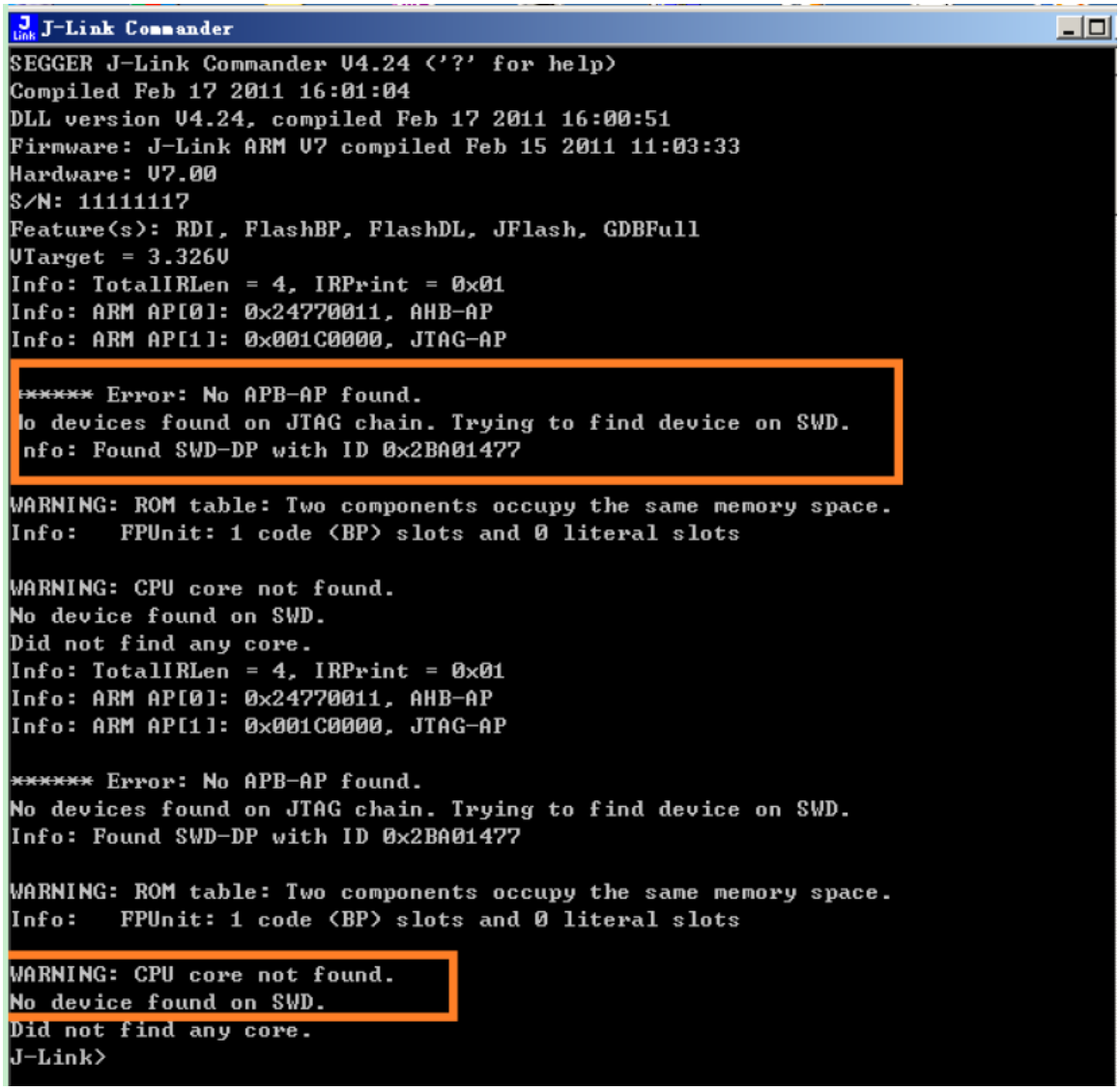


Figure 9-3. MDM AP Addressing

<7> If the SWD-DP interface could not be found, the debug port may be damaged or could not accept connecting or could not find the MCU core. Then the way left was to keep the reset pin in low voltage and run this script many times. There exist using this script more time could unlock the chip. After the chip unlocked, the chip will work normally.



<8> If above ways do not work, please update J-Link hardware firmware and related J-Link software, or using P&E USB Multilink tool. There with successfully unlock examples with that suggestion.