Kinetis FIT Summary

SUMMARY

The FIT data represented below is comprised of recent qualification HTOL device-level stress data for the Kinetis Family C86TFS (0, 1 and 2) N03G, 1N41K, 0/1N83J, 0N50M, 0N51M, 0N36M, N52N and 0N74K mask sets manufactured in the **Global Foundries Fab7** facility. Materials represented in these calculations are from the same technology and processes. These values are measures of observed accelerated life stress data and do not constitute guarantees of future performance levels. See below for actual results and FIT/MTTF assessments.

High Temperature Operational Life – Global Foundries

STRESS	READ POINT	Qty of DEVICES	Qty of REJECTS	% REJECTS
Q221591 1.558V core/125C	1008	80	0	0
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Q222166 1.558V core/125C	168	80	0	0
Q225516 1.558V core/125C	168	79	0	0
Q224185 1.558V core/125C	1008	80	0	0
Q224185 1.558V core/125C	168	77	0	0
Q224185 1.558V core/125C	168	80	0	0
Q225446 1.6V Core/125C	264	239	0	0
Q226519 1.63V Core/125C	264	80	0	0
Q225737 1.6V Core/125C	264	80	0	0
Q227084 1.6V Core/125C	264	79	0	0
Q226520 1.63V Core/125C	264	80	0	0
Q233909 1.63V Core/125C	264	231	0	0

***Note**: Stress data collected in the above table is from initial qualification studies and onwards.*

FIT Rates are calculated for each die size using the above data.

(0, 1 and 2) N03G and 1N41K**:** Current FIT data stands at 2.0 FIT at 60% Upper Confidence Limit at 55℃ Tj constant duty cycle. Respective MTTF calculations are 56820.87.

(0/1N83J**):** Current FIT data stands at 2.3 FIT at 60% Upper Confidence Limit at 55℃ Tj constant duty cycle. Respective MTTF calculations are 48697.52.

(0N50M): Current FIT data stands at 1.3 FIT at 60% Upper Confidence Limit at 55℃ Tj constant duty cycle. Respective MTTF calculations are 90612.67.

(0N51M): Current FIT data stands at 1.3 FIT at 60% Upper Confidence Limit at 55℃ Tj constant duty cycle. Respective MTTF calculations are 90612.67.

(0N74K): Current FIT data stands at 0.8 FIT at 60% Upper Confidence Limit at 55℃ Tj constant duty cycle. Respective MTTF calculations are 138,868.52.

(0N36M): Current FIT data stands at 0.8 FIT at 60% Upper Confidence Limit at 55°C Tj constant duty cycle. Respective MTTF calculations are 138,868.52.

(N52N): Current FIT data stands at 1.2 FIT at 60% Upper Confidence Limit at 55°C Tj constant duty cycle. Respective MTTF calculations are 94,189.72.

Please note; larger die size results in higher FIT rates and lower MTTF values; therefore each mask calculation is provided above. Lower junction temperatures and duty cycles will result in lower FIT rates and higher MTTF values.

DESCRIPTION OF STRESS TEST

High Temperature Operational Life test (HTOL)

150° or 125°C, 1.558, 1.6, 1.63 Volts

To determine the constant failure rate of the product at the specified operating temperature (usually 55-70°C), by accelerating temperature and voltage-activated failure mechanisms to produce device failures.

A dynamic electrical bias is applied to stimulate the device during the life test. Microcontrollers are cycled through software routines, developed to stress the devices to simulate actual use, at elevated temperature and voltage. Reject quantities at the test temperature are modified by the Chi-squared distribution function at 90% confidence levels. The failure rates are then calculated and derated to the required temperature using the Arrhenius equation with a 0.54 eV activation energy assumed as an average for the failure mechanisms. Further details are given in 'Calculation of Failure Rates'.

CALCULATION OF FAILURE RATES

Life test is a technique for determining constant failure rate. To derate from the temperature at which the life test is carried out to the maximum operating temperature an acceleration factor is applied. This calculation uses the Arrhenius equation, with **0.54eV** assumed for the activation energy.

Temperature Acceleration Factor, **$Aft = \exp(\theta/k\,(1/To - 1/Tt))$**

Where: θ is activation energy (eV)
k is Boltzmann's constant (8.617×10^{-5} eV/K) (K = -273.16°C)
$To = Ta\,(op) + (Pd \times \theta ja)$
$Tt = Ta\,(tst) + (Pd \times \theta ja)$

And: Ta (op) is the ambient user operating temperature (K)
Ta (tst) is the ambient temperature on stress test (K)
Pd is power dissipated by the device (W)
θja is thermal resistance of the package (°C/W)

Rejects obtained in the sample must be modified at a stated confidence level to obtain the rejects which would occur were the entire population tested. This is done using the Chi-square distribution function.

Failure Rate, **Fa = Z / (2 x N x h x Aft)** where: Z is Chi-square ($\chi 2$) reject quantity

N is number of devices on test
h is test duration (hours)

* Fa is multiplied by 10^9 to give the result in FITS (1 FIT = 1 failure in 10^9 device hours).
* Fa is multiplied by 10^5 for % per 1000 hours.

$\chi 2$ value Z, is derived from statistical tables using (2 x Qty. fails + 2) for the Degrees of Freedom:

Qty fails	60% confidence level $\chi 2$ qty	90% confidence level $\chi 2$ qty
0	1.833	4.605
1	4.045	7.779
2	6.211	10.645
3	8.351	13.362
4	10.473	15.987
5	12.584	18.549
6	14.685	21.064
7	16.780	23.542
8	18.868	25.989
9	20.951	28.412

Voltage Acceleration is also taken into account when determining the life of devices. This is calculated by taking the oxide thickness into consideration and derating from the stress test voltage to the life operating voltage.

Voltage Acceleration Factor, $\mathbf{Afv = \exp^{\beta[Vt - Vo]}}$

Where:
Vo = Gate voltage under typical operating conditions (in Volts) *
Vt = Gate voltage under accelerated test conditions (in Volts) *
β = Voltage acceleration factor (in 1/Volts)

** For devices with dual gate oxide, the thin gate oxide voltages are applicable.*
*** Specified by technology in the Reliability Model document 68MWS00084B.*

Family 60% FIT Curve Based on HTOL Stress data provided above