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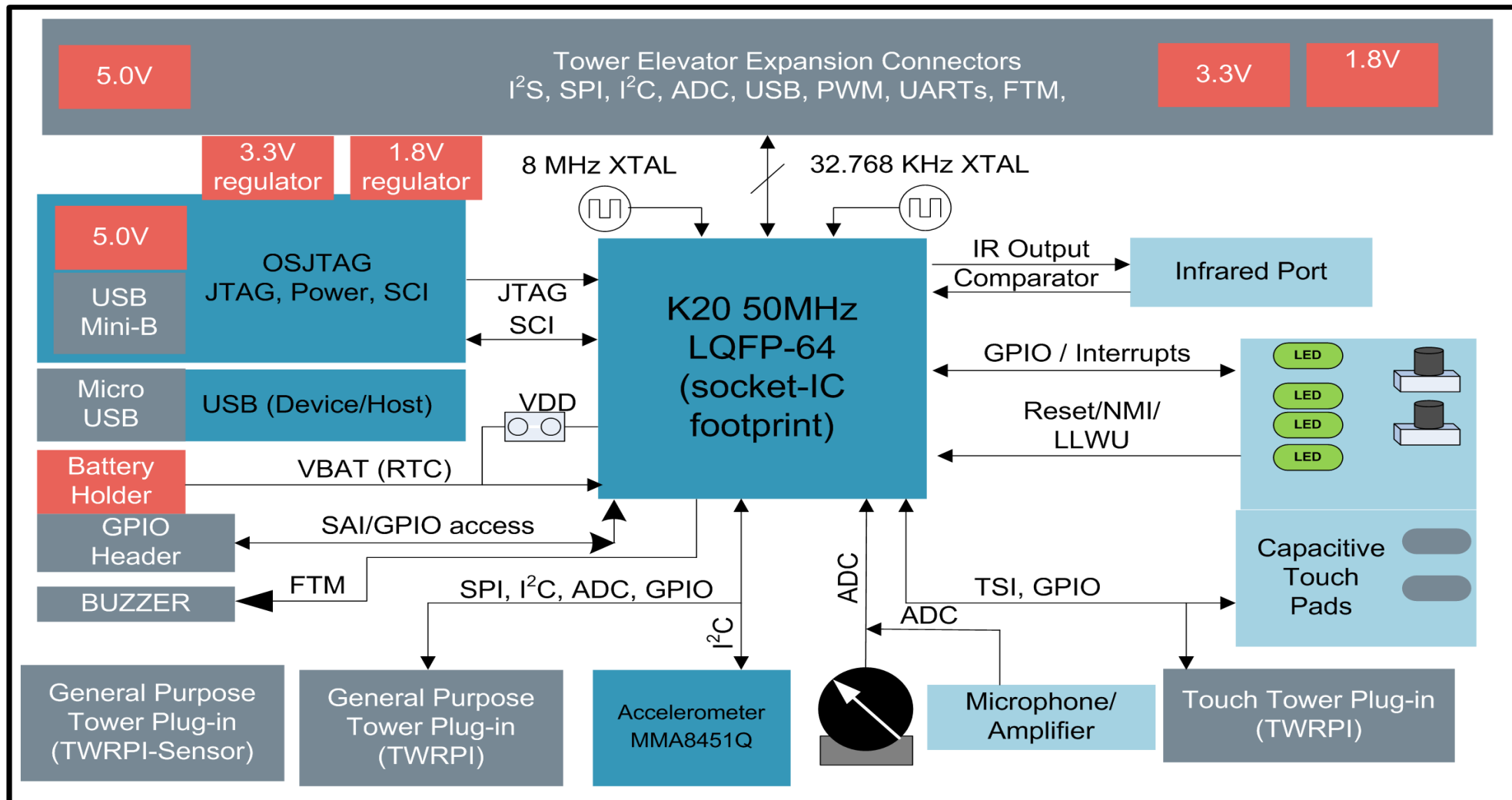
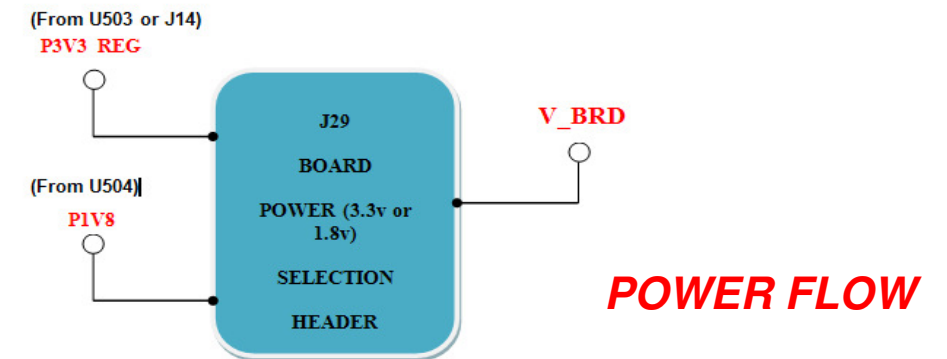
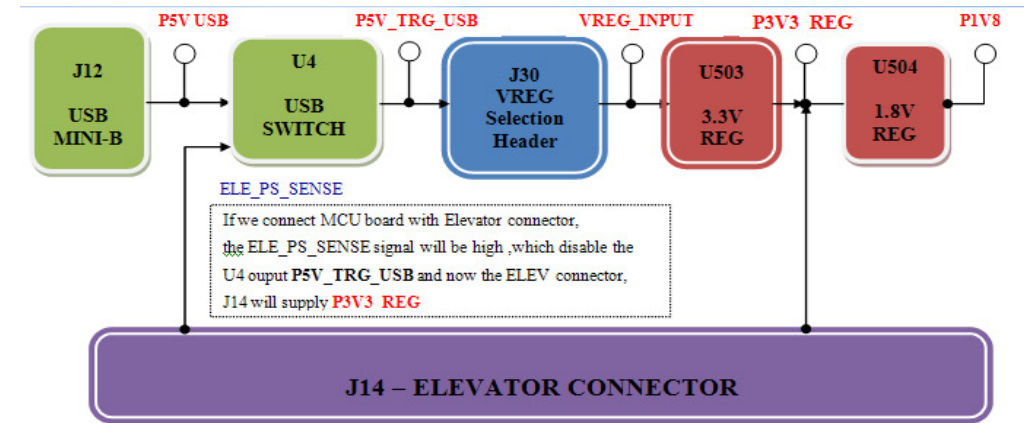
Revisions			
Rev	DESCRIPTION	DATE	APPROVED
X1	A070 Release	August-03-2011	Luis Puebla Palma / Alberto
X2	01 Buzzer will select MCU pins 49 through a 2 pin header 02 R70 & C501 Changed to DNP 03 R55 should be loaded 04 15Pf /DNP capacitor added to USB differential pairs 05 P3V3 sourced from Regulator output (Not from Elevator conn) 06 Address latch circuit should be DNP for this board 07 MCU part number changed to MK20DX128VLH5(R) 08 Updated block diagram placed in the schematic page 09 D2/D3 Led's changed to 0603 from 1206 devices 10 To improve space, connectors replaced for (211-77579 to 211-75113) & (211-30011 to 211-00003-00) 11 PTA5 connected to 1 pin header DNP Only as general GPIO through a 0 ohm resistor. 12 USB mini B connector 211-77581 replaced with 211-78997 13 SW1, SW2, SW3 part number changed to 510-77653 (12V, 50mA) 14 Four GND populated test points PN - 210-75685 added 15 Test points (like 1 pin header DNP) added to electrodes 16 Buzzer, PKLCS1212E4001-R1 added 17 Optional header added for PTA12 to select MCU_PWR or GND 18 Connections on Elevator connector & TWRPI J20 are changed UART1 connections introduced 19 Y500- Crystal part number changed to ECS-40-20-5PVX-TR	August-16-2011	Luis Puebla Palma / Alberto
A	BACK ANNOTATION done	August-17-2011	Luis Puebla Palma
	1. UART1 RX/TX Connection swapped at Elevator connector pins A43/A44 2. 1X1 DNP headers moved in between the Resistor & Electrode 3. Accelerometer, VDD pins are given option to P3V3 (default) or MCU_PWR	August-18-2011	Luis Puebla Palma
	1. Block Diagram Updated 2. UART1 Signals net naming alone changed 3. SAI Header renamed to GPIO Header 4. Option to power MCU_PWR from VBATD added through jumpers	August-22-2011	Luis Puebla Palma
B	01 Microphone connection changed from PTB0/ADC0_SE8/TSI0_CH0 to ADC0_DP3 02 J17/J18 Jumper options changed to default disconnected 03 TEXT- FTMO_CH3 assigned to Buzzer connection 04 J15 Jumper option comment changed to Enable potentiometer 05 Net label changed to CMP1_IN3/ADC0_SE23, DAC0_OUT is not on P0 (MCU Pin18) 06 Elevator connector symbol got updated. Pins A47 & A48 connections VREFH/VREFL deleted	October-10-2011	Luis Puebla Palma
C	1. Jumper , J33 deleted (option for P3V3) 2. P3V3_ELEV net name changed to P3V3_REG 3. P3V3 Net name changed to V_BRD for the following Interfaces Microphone,POT, Flex Bus, IRDA & OSBDM Buffers 4. Led part number changed for 1.7v forward voltage D2 (green) changed to LG L29K-G2J1-24-Z and D3(RED) changed to 597-5112-407F 5. Buffer (U501) SN74HCT125D replaced with Voltage translators (U12,U13,U14), SN74LVC1T45DCKR	November-18-2011	Alberto/Luis Puebla Palma

		Microcontroller Solutions Group 6501 William Cannon Drive West Austin, TX 78735-8598	
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ICAP Classification:		FCP:	FIUC: <input checked="" type="checkbox"/> PUBI:
Designer: Jones	Drawing Title: TWR-K20D50M		
Drawn by: Jones	Page Title: TABLE OF CONTENTS / REVISION		
Approved: Luis Puebla Palma	Size C	Document Number SCH-27272 PDF: SPF-27272	Rev C
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- Unless Otherwise Specified:
All resistors are in ohms
All capacitors are in uF
All voltages are DC
- Interrupted lines coded with the same letter or letter combinations are electrically connected.
- Device type number is for reference only. The number varies with the manufacturer.
- Special signal usage:
_B Denotes - Active-Low Signal
<> or [] Denotes - Vectored Signals
- Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Power & Ground Nets

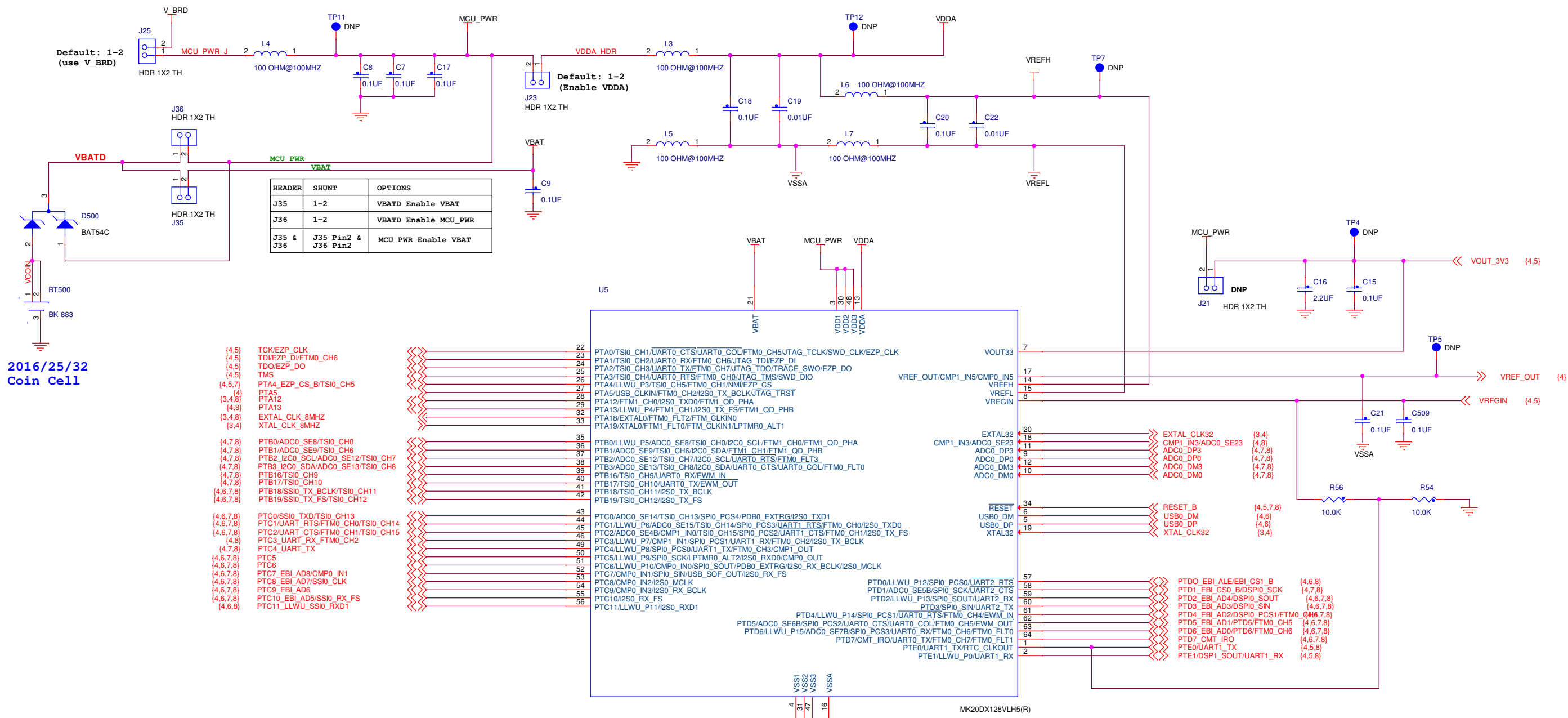
NET	VOLTAGE	DESCRIPTION
P5V_USB	5V	Primary input power. Filtered from USB connector. Input to USB power switch.
P5V_SW	5V	Output of USB power switch controlled by the 5V_EN signal from the JM60 MCU. Used by OSBDM voltage translation circuits.
P5V_TRG_USB	5V	Output of USB power switch controlled by the VTRG_EN signal from the JM60 MCU. Provides input to regulator.
P3V3_REG	3.3V	Output of regulator U503 or from the Elevator connector
P1V8	1.8V	Output of regulator U504
V_BRD	3.3v or 1.8v	MCU & Interface circuit input power
VDDA	3.3V	VDDA power for MCU and analog circuits. Filtered from MCU_PWR.
VREFH	3.3V	Upper reference voltage for ADC on the MCU. Filtered from VDDA.
VREFL	0V	Lower reference voltage for ADC on the MCU. Filtered from VSSA.
VSSA	0V	VSSA power for MCU and analog circuits. Filtered from GND.
GND	0V	Digital Ground.



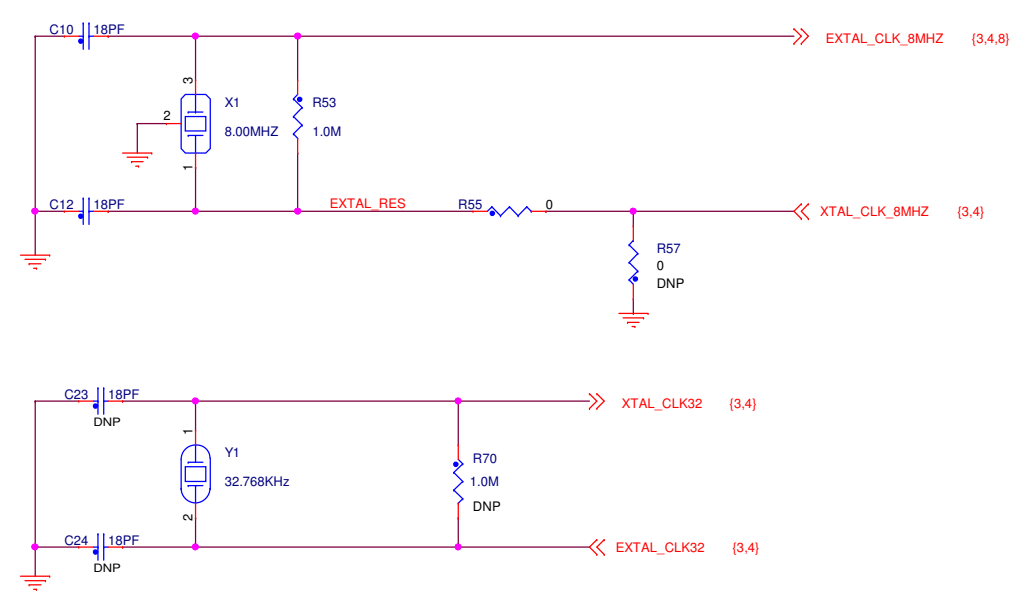
■ Freescale Device
 ■ External Connectors
 ■ Interface Circuits
 ■ Power

BLOCK DIAGRAM

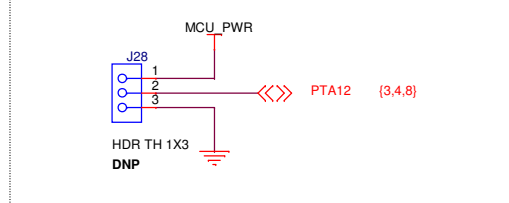
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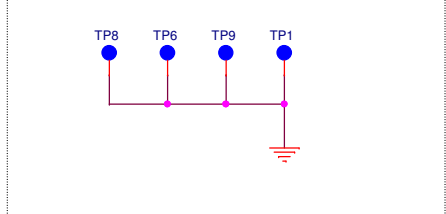
CRYSTAL - CLOCK SIGNALS



PTA12 - OPTION



GND LOOP TEST POINTS



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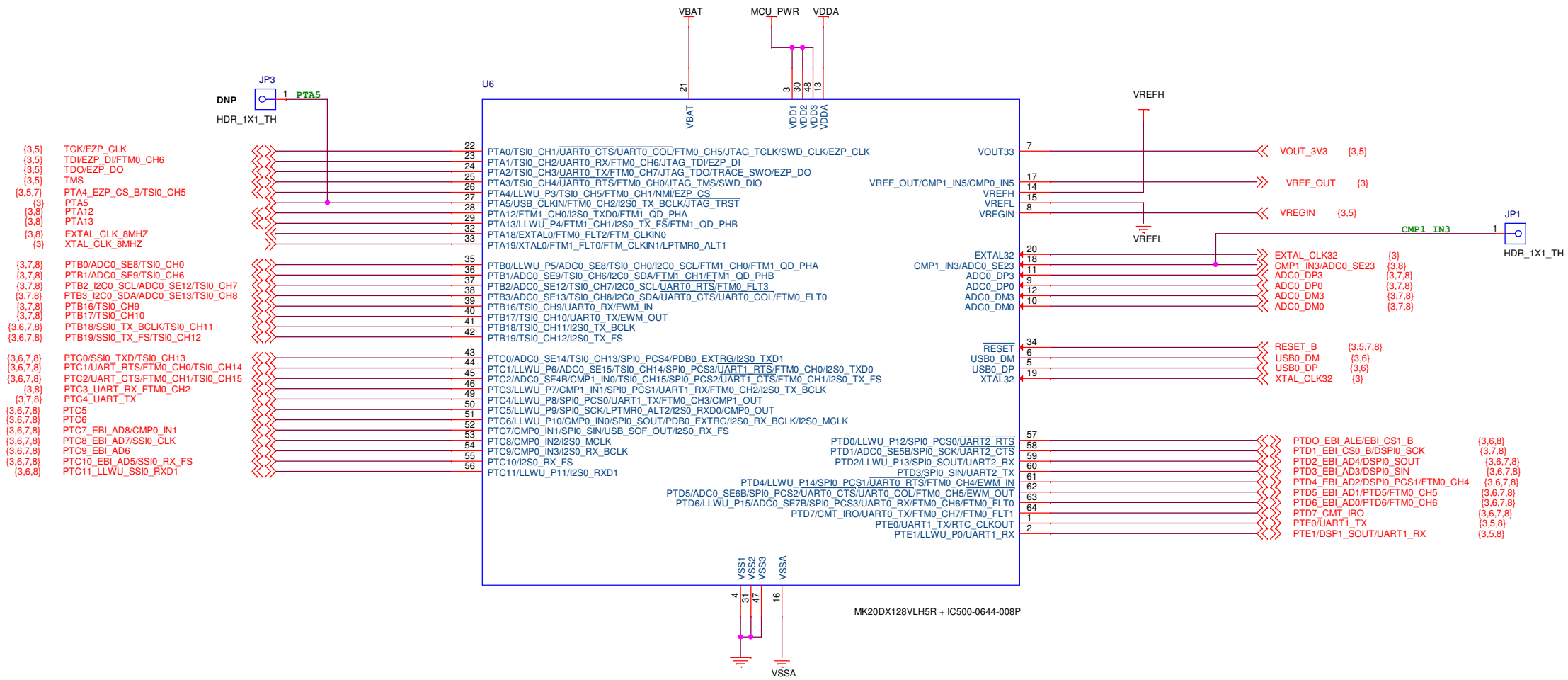
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Page Title: **MK20DX128VLH5(R) 64LQFP - CLOCK Connections**

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MK20DX64VLH5 (R) – SOCKET



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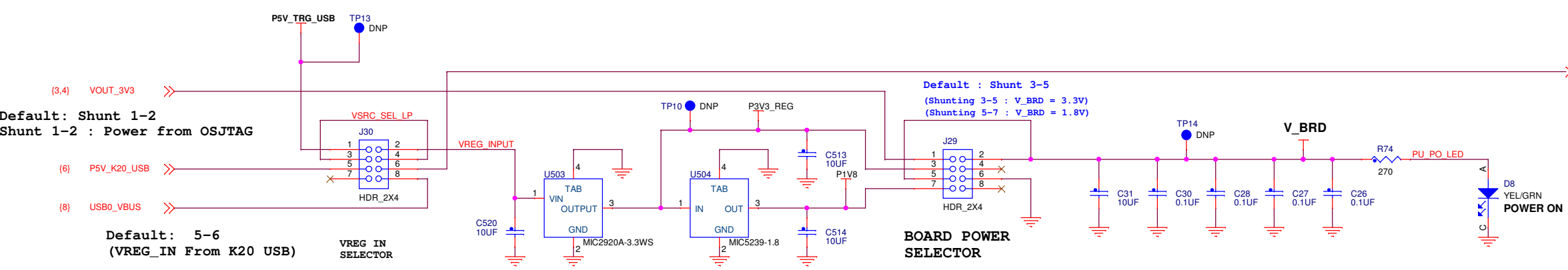
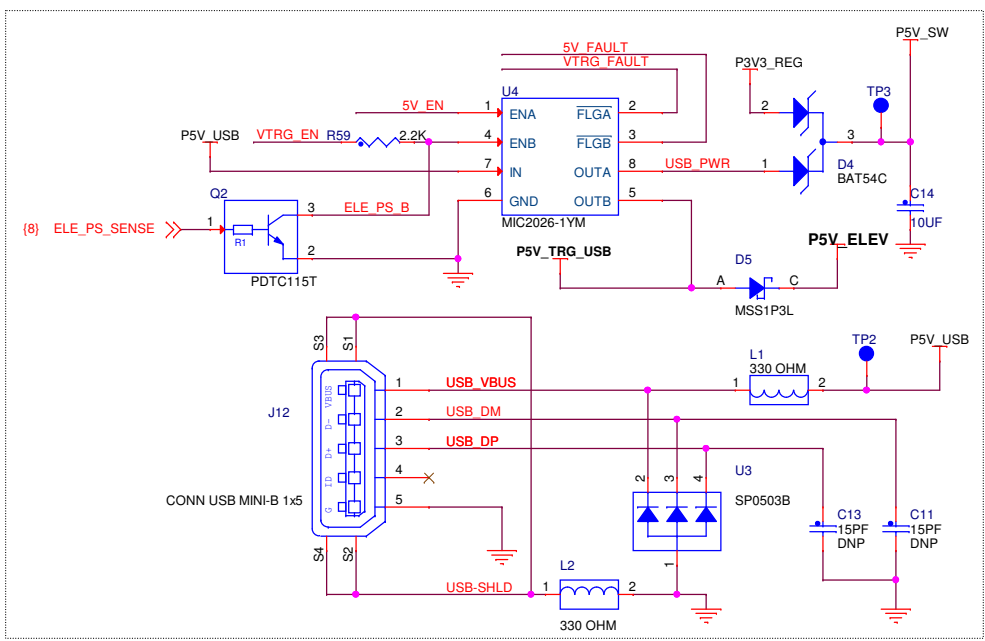
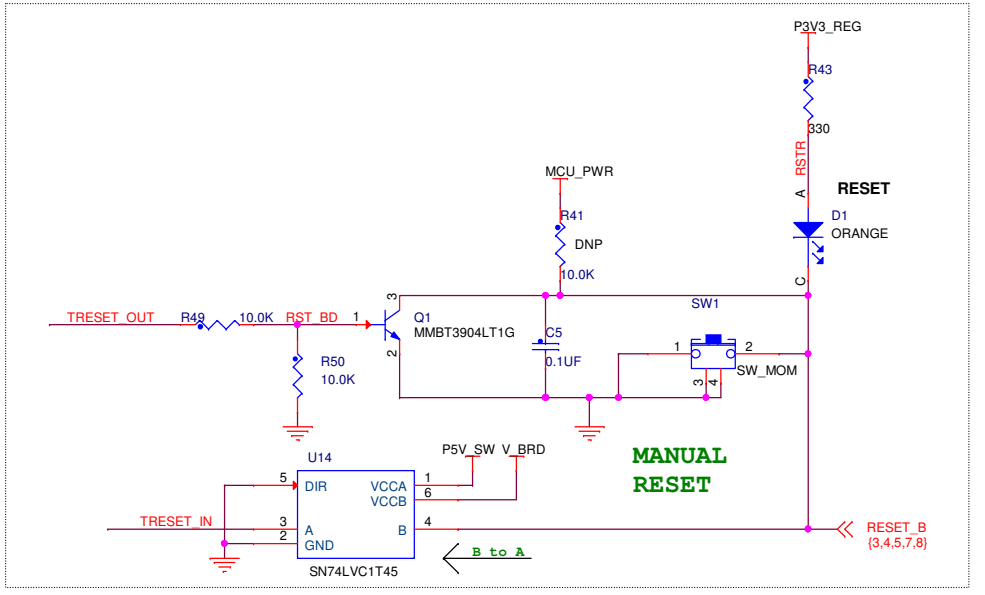
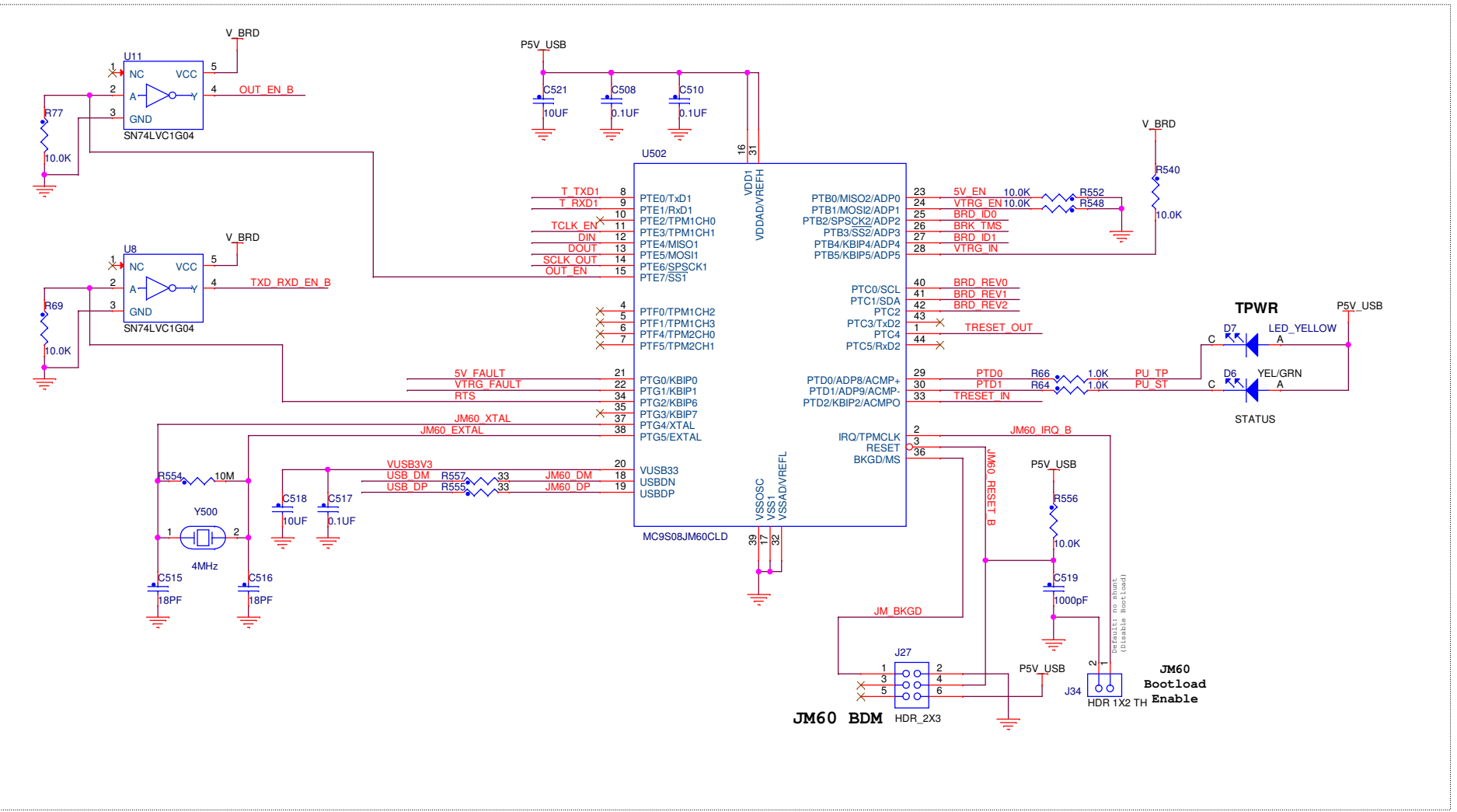
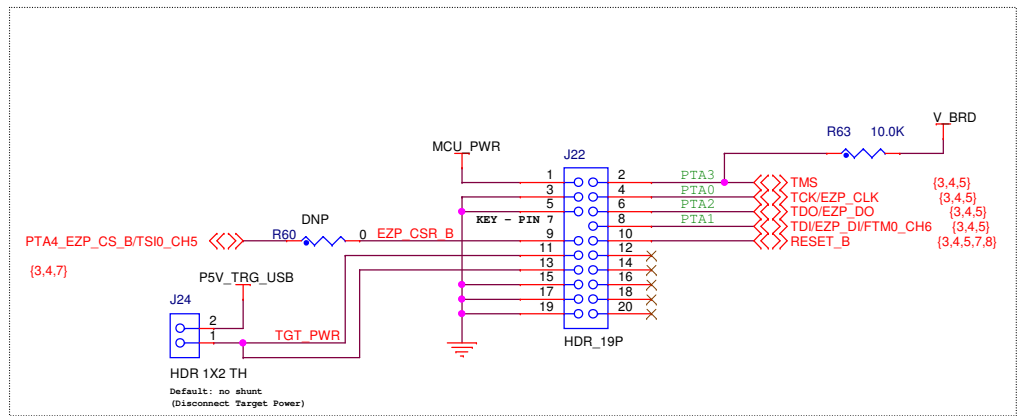
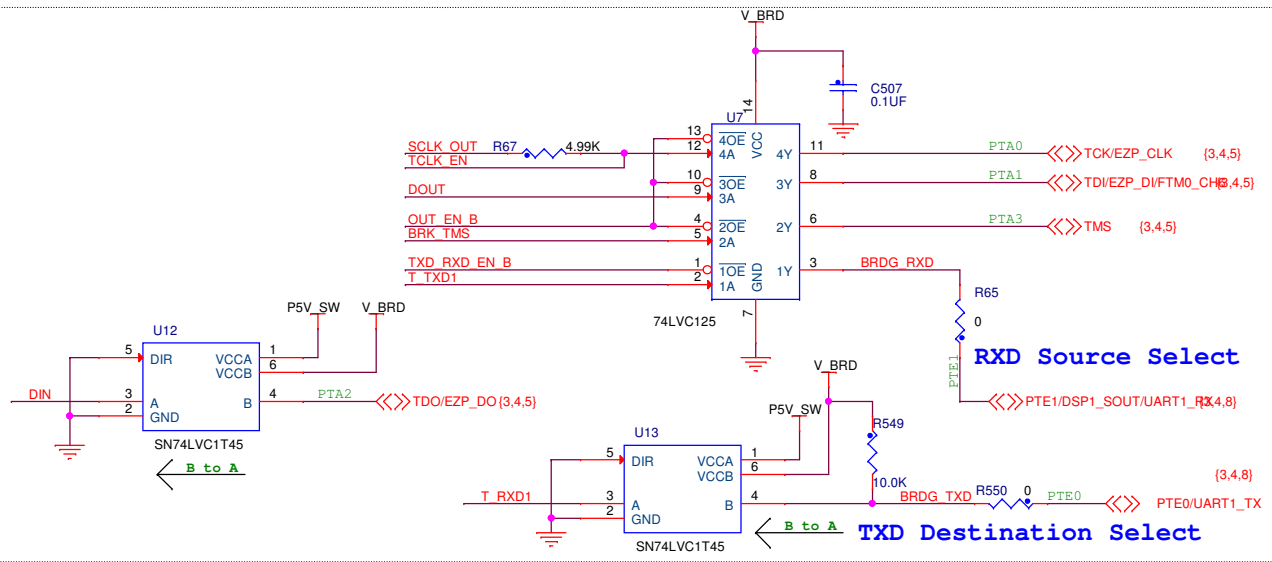
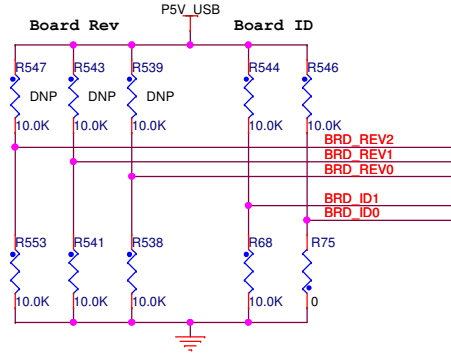
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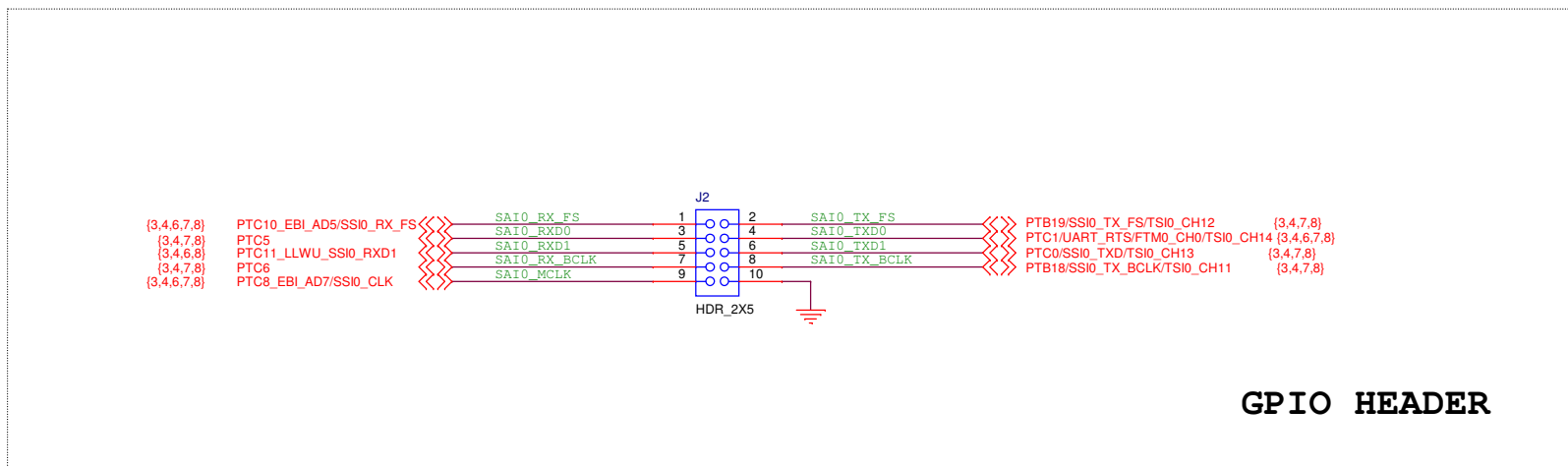
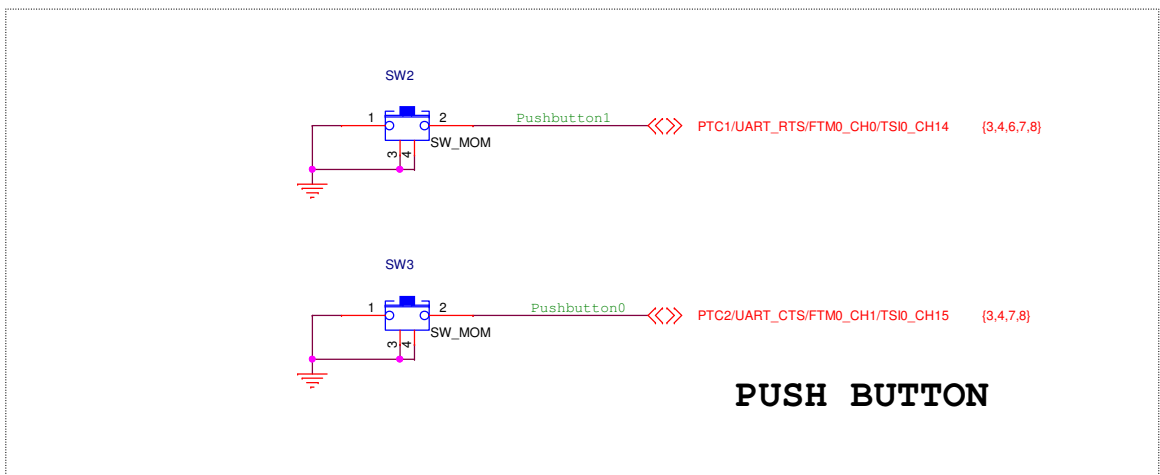
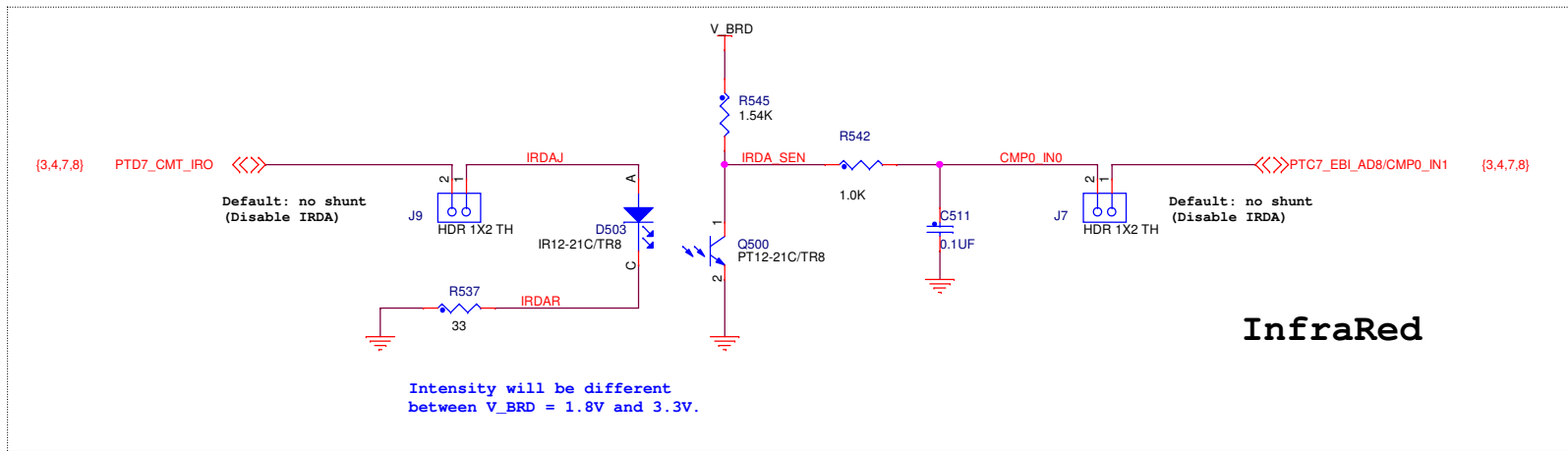
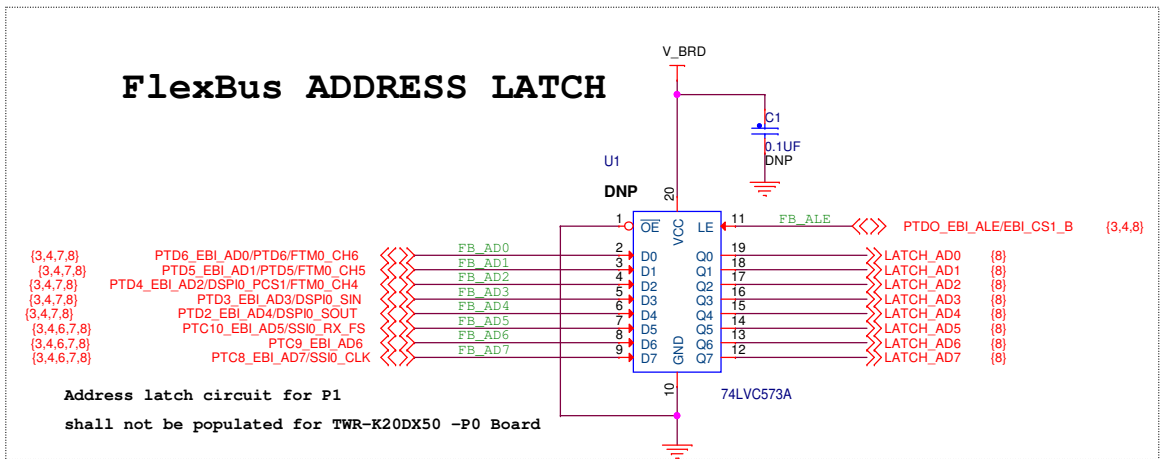
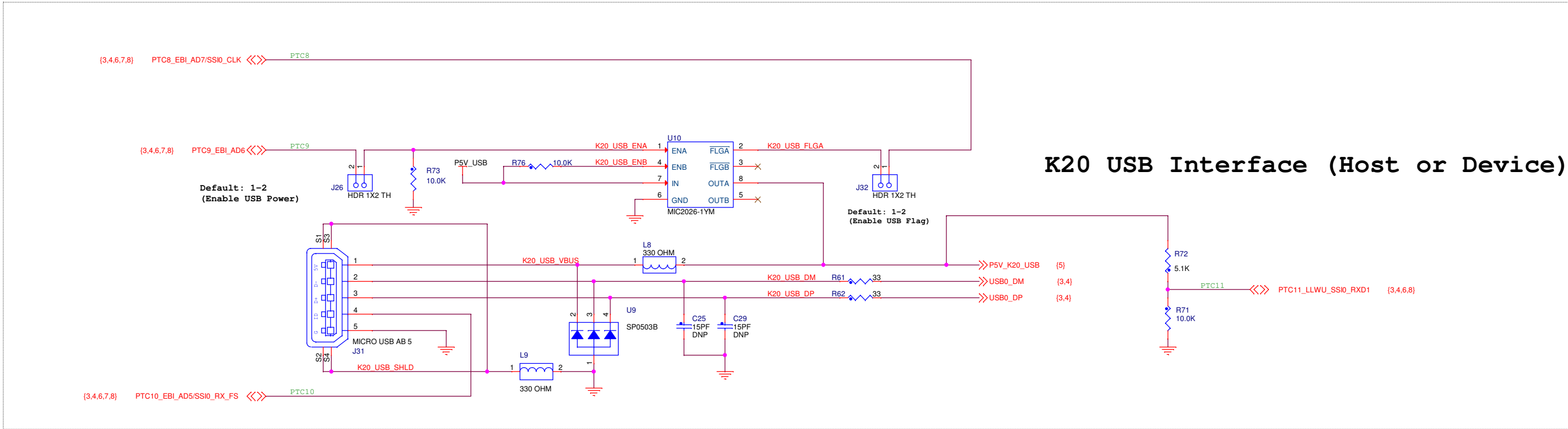
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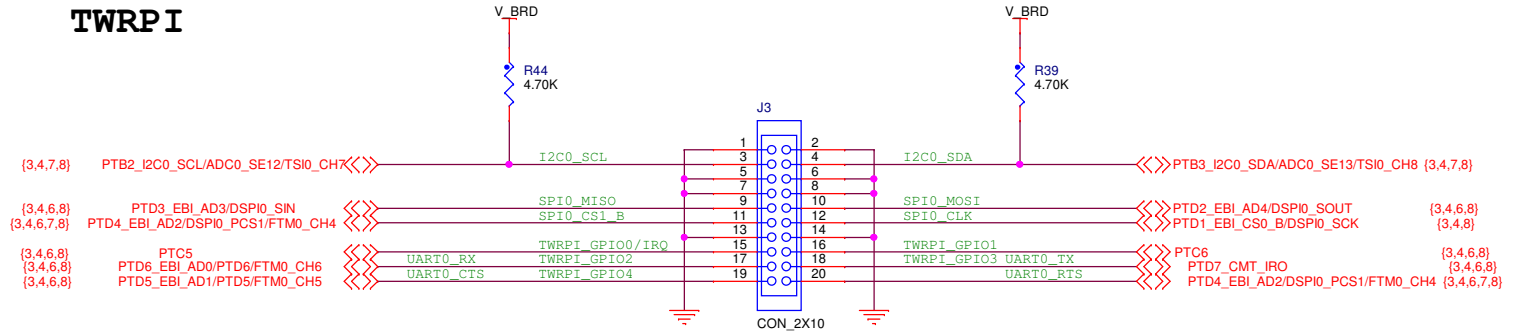
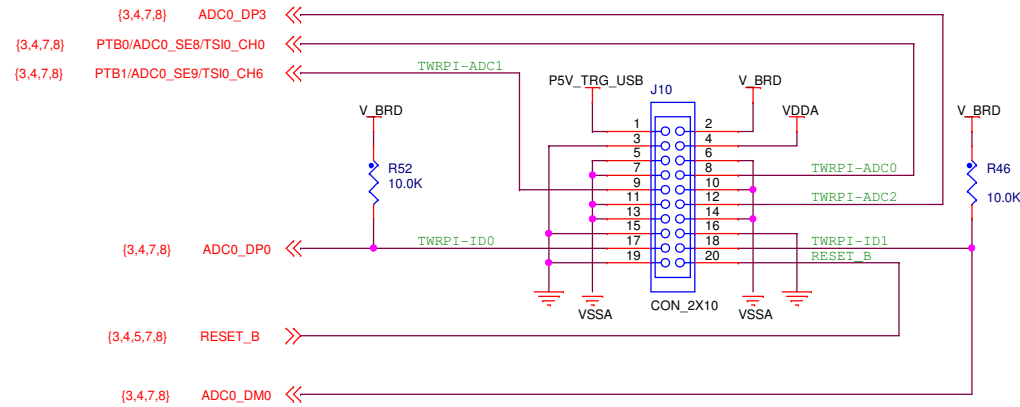
On Board OSBDM/Serial Bridge



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Drawing Title:	FIUC: X PUBLI: _____
TWR-K20D50M	
Page Title: USB/OSBDM/VTRAN/PWR	
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GENERAL PURPOSE TWRPI

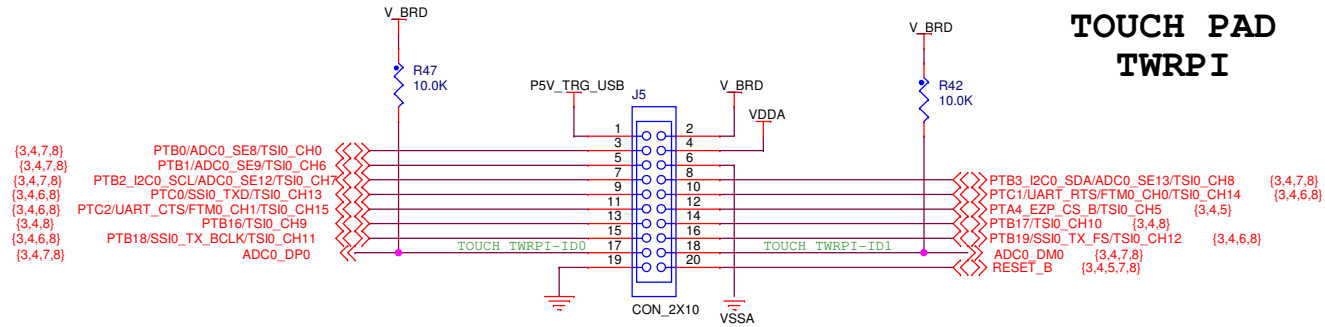


Note: The TWRPI connectors are powered by V_BRD which may be 1.8V or 3.3V.

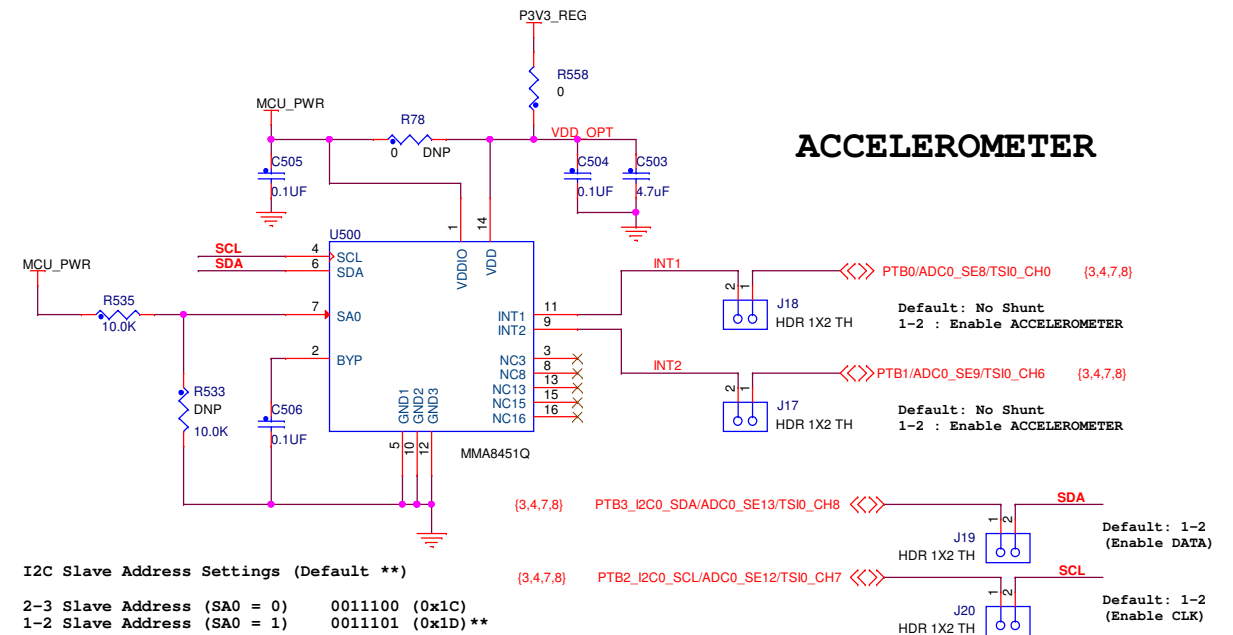
Not all TWRPI boards will work at 1.8V.

Check that the TWRPI board will work at 1.8V before using it when this board is set for 1.8V.

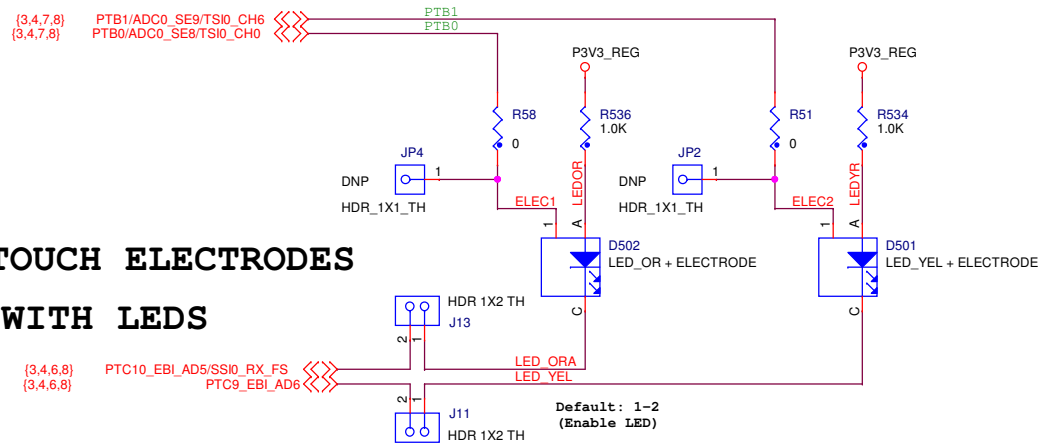
TOUCH PAD TWRPI



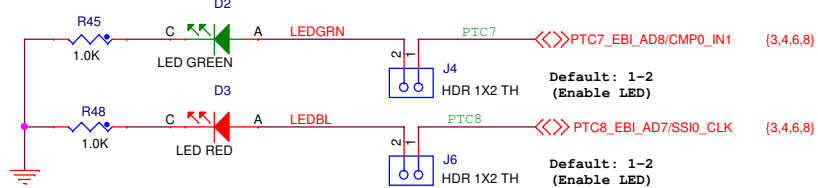
ACCELEROMETER



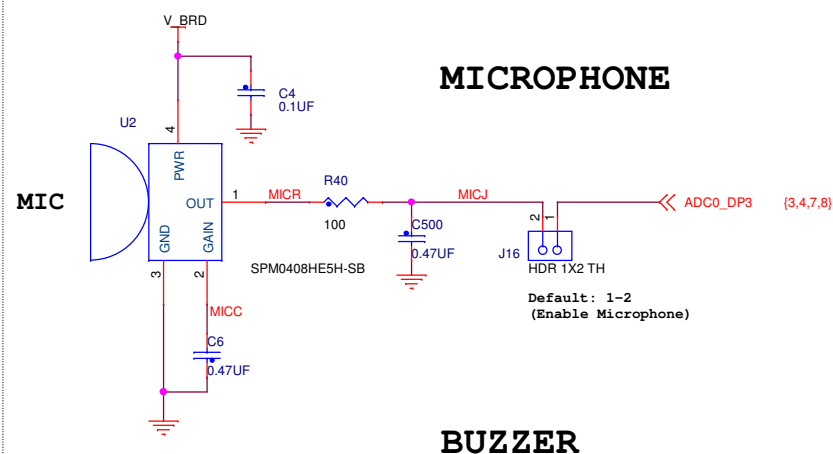
TOUCH ELECTRODES WITH LEDES



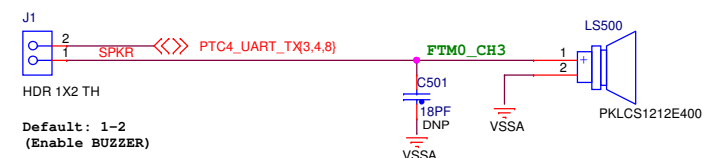
LEDES



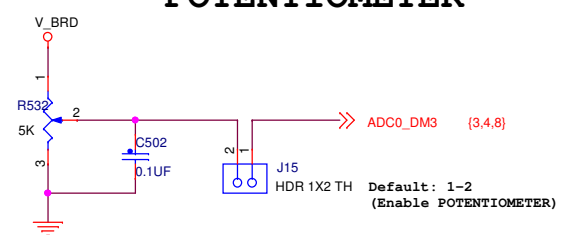
MICROPHONE

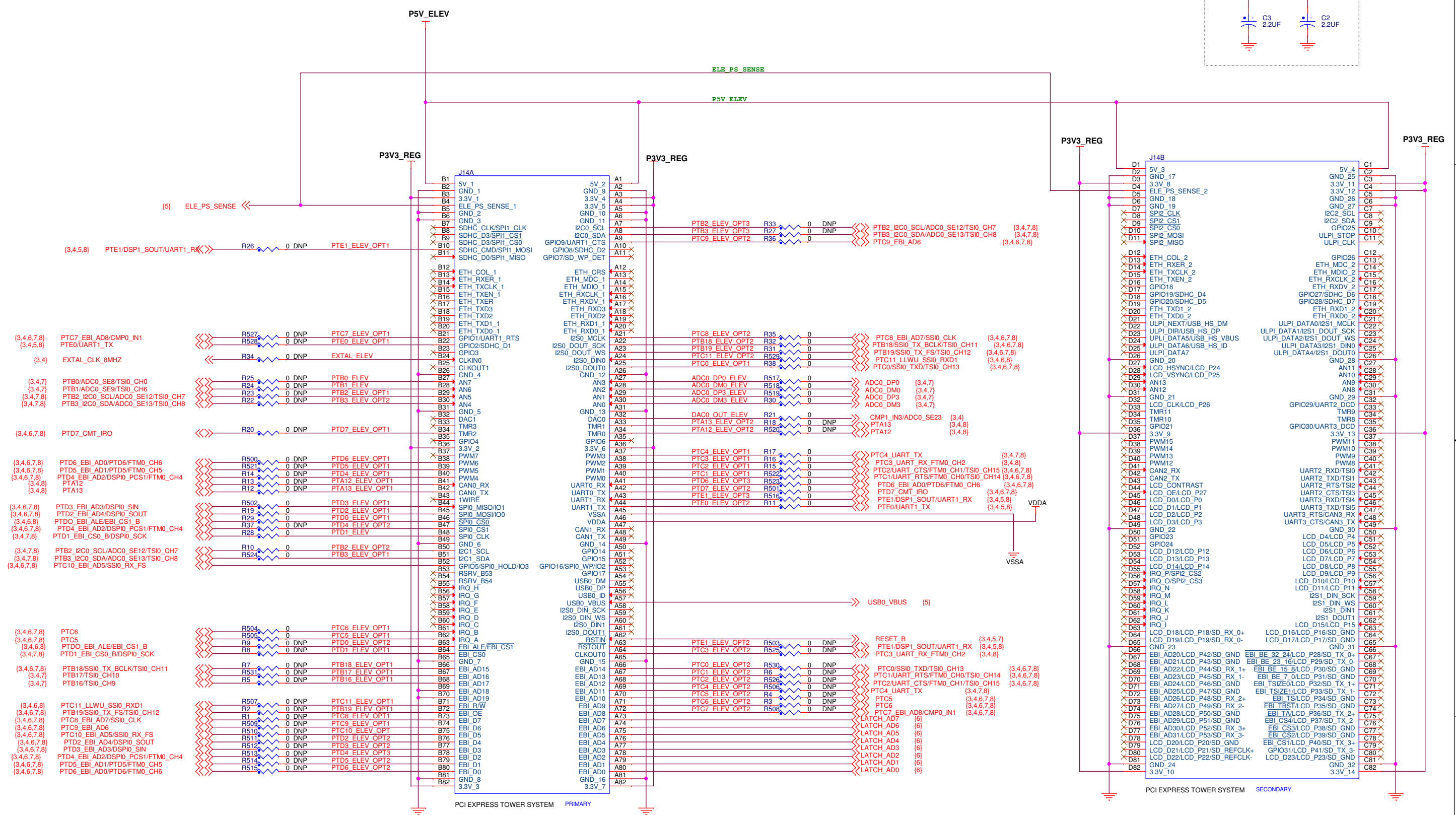
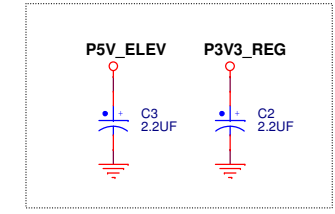


BUZZER



POTENTIOMETER





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ELEVATOR CONNECTOR

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