6.4.5.1   SWBST setup and control

Boost regulator control is done through a single register SWBSTCTL described in Table 88. SWBST is included in the power-up sequence if its OTP power-up timing bits, SWBST_SEQ[4:0], are not all zeros.

Table 88. Register SWBSTCTL - ADDR 0x66

Name	Bit #	R/W	Default	Description
SWBST1VOLT	1:0	R/W	0x00	Set the output voltage for SWBST • 00 = 5.000 V • 01 = 5.050 V • 10 = 5.100 V • 11 = 5.150 V
SWBST1MODE	3:2	R	0x02	Set the Switching mode on normal operation • 00 = OFF • 01 = PFM • 10 = Auto (Default)[61] • 11 = APS
UNUSED	4	–	0x00	unused
SWBST1STBYMODE	6:5	R/W	0x02	Set the switching mode on standby • 00 = OFF • 01 = PFM • 10 = Auto (Default)[61] • 11 = APS
UNUSED	7	–	0x00	unused

Notes
61. In auto mode, the controller automatically switches between PFM and APS modes depending on the load current. The SWBST regulator starts up by default in the auto mode if SWBST is part of the startup sequence.

6.4.5.2   SWBST external components

Table 89. SWBST external component requirements

Components	Description	Values
C_{INBST}[62]	SWBST input capacitor	10 µF
$C_{INBSTHF}$[62]	SWBST decoupling input capacitor	0.1 µF
C_{OBST}[62]	SWBST output capacitor	2 x 22 µF
L_{SBST}	SWBST inductor	2.2 µH
D_{BST}	SWBST boost diode	1.0 A, 20 V Schottky

Notes
62. Use X5R or X7R capacitors.

Table 93. VGEN3/ 4/ 5/ 6 output voltage configuration (continued)

Set point	VGENx[3:0]	VGENx output (V)
3	0011	2.10
4	0100	2.20
5	0101	2.30
6	0110	2.40
7	0111	2.50
8	1000	2.60
9	1001	2.70
10	1010	2.80
11	1011	2.90
12	1100	3.00
13	1101	3.10
14	1110	3.20
15	1111	3.30

Besides the output voltage configuration, the LDOs can be enabled or disabled at anytime during normal mode operation, as well as programmed to stay "ON" or be disabled when the PMIC enters Standby mode. Each regulator has associated I^{2}C bits for this. Table 94 presents a summary of all valid combinations of the control bits on VGENxCTL register and the expected behavior of the LDO output.

Table 94. LDO control

VGENxEN	VGENxLPWR	VGENxSTBY	STANDBY[64]	VGENxOUT
0	X	X	X	Off
1	0	0	X	On
1	1	0	X	Low power
1	X	1	0	On
1	0	1	1	Off
1	1	1	1	Low power

Notes
64. STANDBY refers to a standby event as described earlier.

For more detail information, Table 95 through Table 100 provide a description of all registers necessary to operate all six general purpose LDO regulators.

Table 95. Register VGEN1CTL - ADDR 0x6C

Name	Bit #	R/W	Default	Description
VGEN1	3:0	R/W	0x80	Sets VGEN1 output voltage. See Table 92 for all possible configurations.
VGEN1EN	4	–	0x00	Enables or disables VGEN1 output • 0 = OFF • 1 = ON
VGEN1STBY	5	R/W	0x00	Set VGEN1 output state when in standby. Refer to Table 94.
VGEN1LPWR	6	R/W	0x00	Enable low-power mode for VGEN1. Refer to Table 94.
UNUSED	7	–	0x00	unused