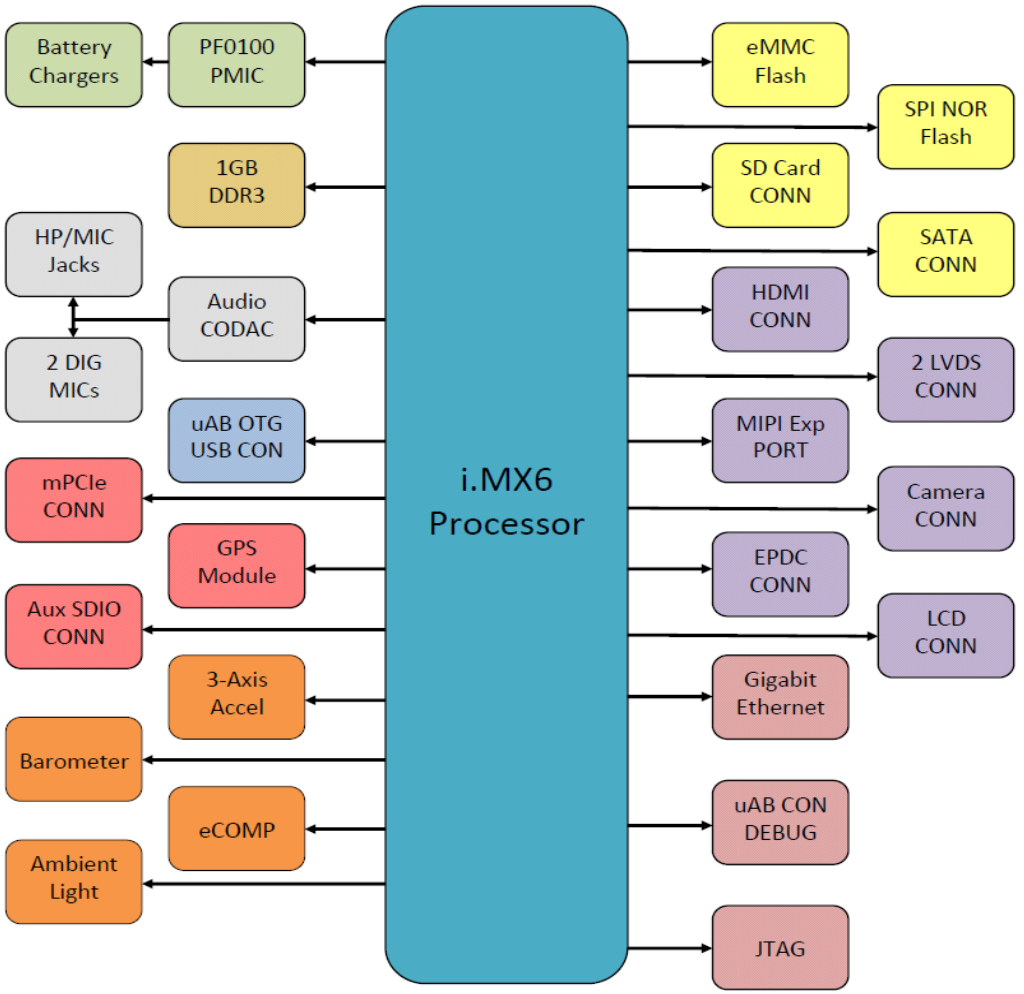
Table of Content

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass production design. For an added resource, refer to Hardware Development Guide document number IMX6DQ6SDLHDG.

i.MX6 SMART DEVICE SYSTEM

MCIMX6QP-SDB

Smart Device System Block Diagram



GENERAL DESIGN NOTES

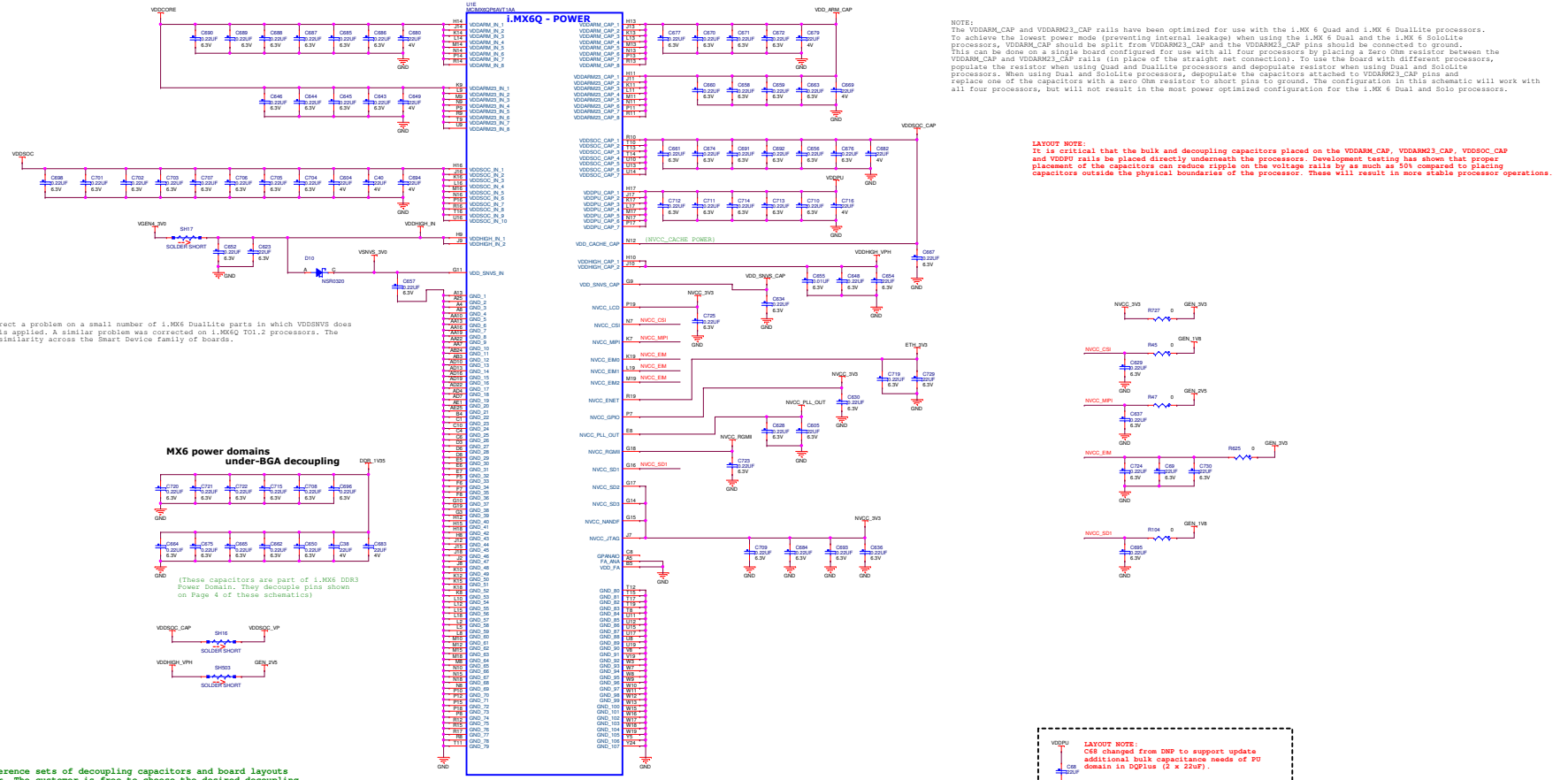
1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/16 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are Tantalum
2. Critical compenents that require tolerances tighter than listed in Note 1are labeled with required tolerance on schematic. Non-critical components may be filled with tighter tolerance parts for BOM consolidation purposes, but may be changed to meet the general tolerances of Note 1 if desired.
3. Interrupted lines coded with the same letter or letter combinations are electrically connected.
4. Device type number is for reference only. The number varies with the manufacturer.
5. Special signal usage:
   _B or 'n' Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals
6. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

AC ADAPTER SPECIFICATIONS

DC Voltage Output: 5VDC
Current Output: ~ 5A (depending on application)
Polarity:
Inner Diameter: 2.1mm
Outer Diameter: 5.5mm

NXP Classification:	CP: A/C: PUBL X
Designer: Ross M	Drawing Title: MCIMX6QP-SMART DEVICE BOARD
Drawn by: Ross M	Page Title: TITLE PAGE
Approved:	Size: D; Document Number: SCH-28857 PDF: SPF-28857; Rev: A2
	Date: Monday, February 29, 2016; Sheet 1 of 26

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598



NOTE:
Diode D10 is required to correct a problem on a small number of i.MX6 DualLite parts in which VDDSNVS does not come up when VDDHIGH_IN is applied. A similar problem was corrected on i.MX6Q T01.2 processors. The diode is left populated for similarity across the Smart Device family of boards.

NOTE:
The VDDARM_CAP and VDDARM23_CAP rails have been optimized for use with the i.MX 6 Quad and i.MX 6 DualLite processors. To achieve the lowest power mode (preventing internal leakage) when using the i.MX 6 Dual and the i.MX 6 SoloLite processors, VDDARM_CAP should be split from VDDARM23_CAP and the VDDARM23_CAP pins should be connected to ground. This can be done on a single board configured for use with all four processors by placing a Zero Ohm resistor between the VDDARM_CAP and VDDARM23_CAP rails (in place of the straight net connection). To use the board with different processors, populate the resistor when using Quad and DualLite processors and depopulate resistor when using Dual and SoloLite processors. When using Dual and SoloLite processors, depopulate the capacitors attached to VDDARM23_CAP pins and replace one of the capacitors with a zero Ohm resistor to short pins to ground. The configuration in this schematic will work with all four processors, but will not result in the most power optimized configuration for the i.MX 6 Dual and Solo processors.

LAYOUT NOTE:
It is critical that the bulk and decoupling capacitors placed on the VDDARM_CAP, VDDARM23_CAP, VDDSOC_CAP and VDDPU rails be placed directly underneath the processors. Development testing has shown that proper placement of the capacitors can reduce ripple on the voltage rails by as much as 50% compared to placing capacitors outside the physical boundaries of the processor. These will result in more stable processor operations.

NOTE:
Freescale has validated two difference sets of decoupling capacitors and board layouts for use with the i.MX 6 processor. The customer is free to choose the desired decoupling scheme. This scheme uses fewer components. The alternate scheme can be found on the AI (Automotive Infotainment) board. Refer to SCH-28615 and LAY-28615.

LAYOUT NOTE:
C68 changed from DNP to support update additional bulk capacitance needs of PU domain in DQPlus (2 x 22uF).

Extra Bulk Capacitors

NOTE:
In early designs of the Smart Device board, these bulk capacitors were used. After testing of the board, it was found that these capacitors could be removed with no effect. This reduces the capacitive loading on the internal processor LDOs. The coponents/footprints have been left in place in the event that future applications and/or software changes show that these capacitors are needed.

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Page Title:	CPU POWER		
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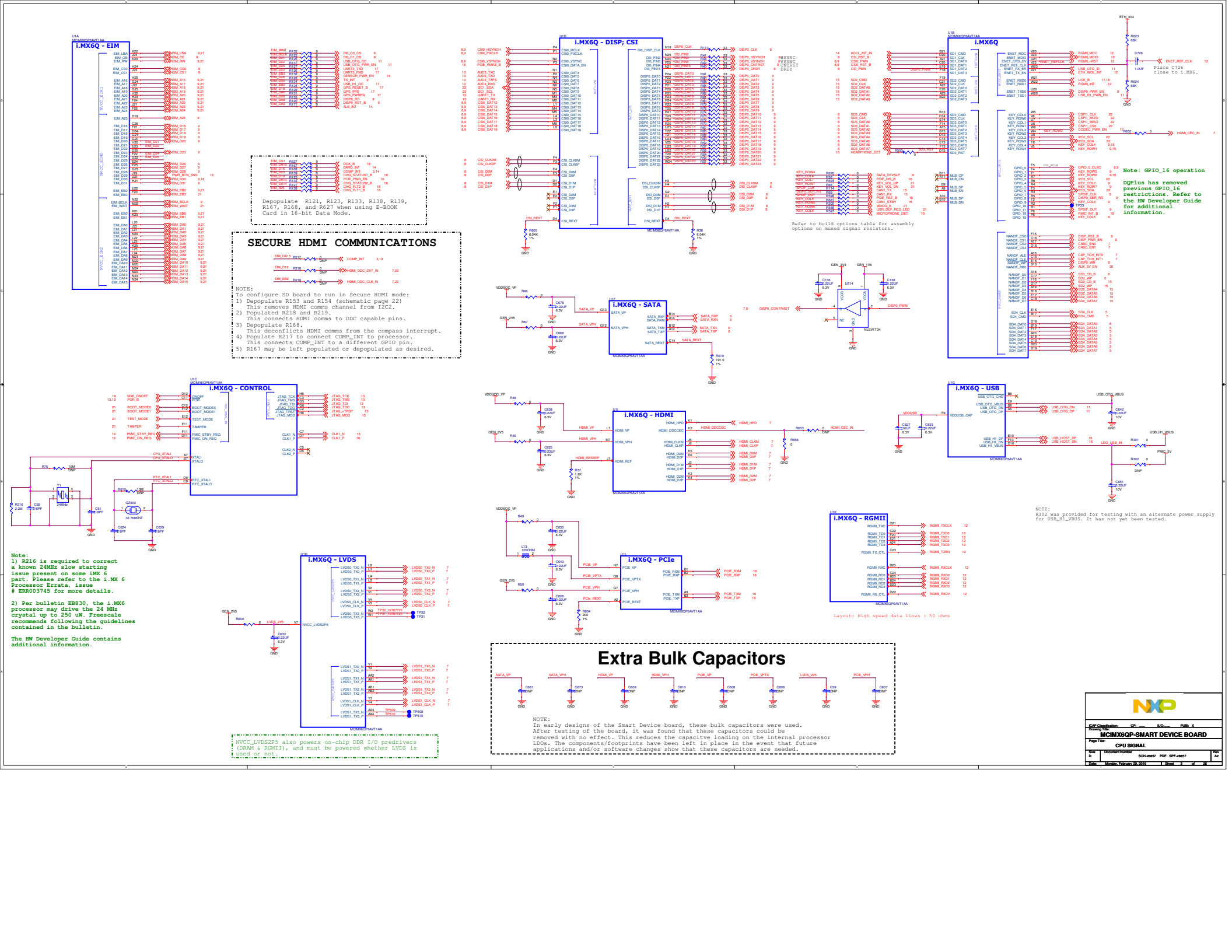
i.MX6Q - EIM
i.MX6Q - DISP; CSI
i.MX6Q - SATA
i.MX6Q - CONTROL
i.MX6Q - HDMI
i.MX6Q - USB
i.MX6Q - LVDS
i.MX6Q - PCIe
i.MX6Q - RGMII
Depopulate R121, R123, R133, R138, R139, R167, R168, and R627 when using E-BOOK Card in 16-bit Data Mode.
SECURE HDMI COMMUNICATIONS
NOTE:
To configure SD board to run in Secure HDMI mode:
1) Depopulate R153 and R154 (schematic page 22)
This removes HDMI comms channel from I2C2.
2) Populated R218 and R219.
This connects HDMI comms to DDC capable pins.
3) Depopulate R168.
This deconflicts HDMI comms from the compass interrupt.
4) Populate R217 to connect COMP_INT to processor.
This connects COMP_INT to a different GPIO pin.
5) R167 may be left populated or depopulated as desired.
Note:
1) R216 is required to correct a known 24MHz slow starting issue present on some iMX 6 part. Please refer to the i.MX 6 Processor Errata, issue # ERR003745 for more details.
2) Per bulletin EB830, the i.MX6 processor may drive the 24 MHz crystal up to 250 uW. Freescale recommends following the guidelines contained in the bulletin.
The HW Developer Guide contains additional information.
NVCC_LVDS2P5 also powers on-chip DDR I/O predrivers (DRAM & RGMII), and must be powered whether LVDS is used or not.
Extra Bulk Capacitors
NOTE:
In early designs of the Smart Device board, these bulk capacitors were used. After testing of the board, it was found that these capacitors could be removed with no effect. This reduces the capacitive loading on the internal processor LDOs. The components/footprints have been left in place in the event that future applications and/or software changes show that these capacitors are needed.
Note: GPIO_16 operation
DQPlus has removed previous GPIO_16 restrictions. Refer to the HW Developer Guide for additional information.
Refer to build options table for assembly options on muxed signal resistors.
Layout: High speed data lines : 50 ohms
NOTE:
R302 was provided for testing with an alternate power supply for USB_H1_VBUS. It has not yet been tested.
Place C726 close to i.MX6.
NXP
ICAP Classification: CP: IUO: PUBL_X
Drawing Title: MCIMX6QP-SMART DEVICE BOARD
Page Title: CPU SIGNAL
Size: D
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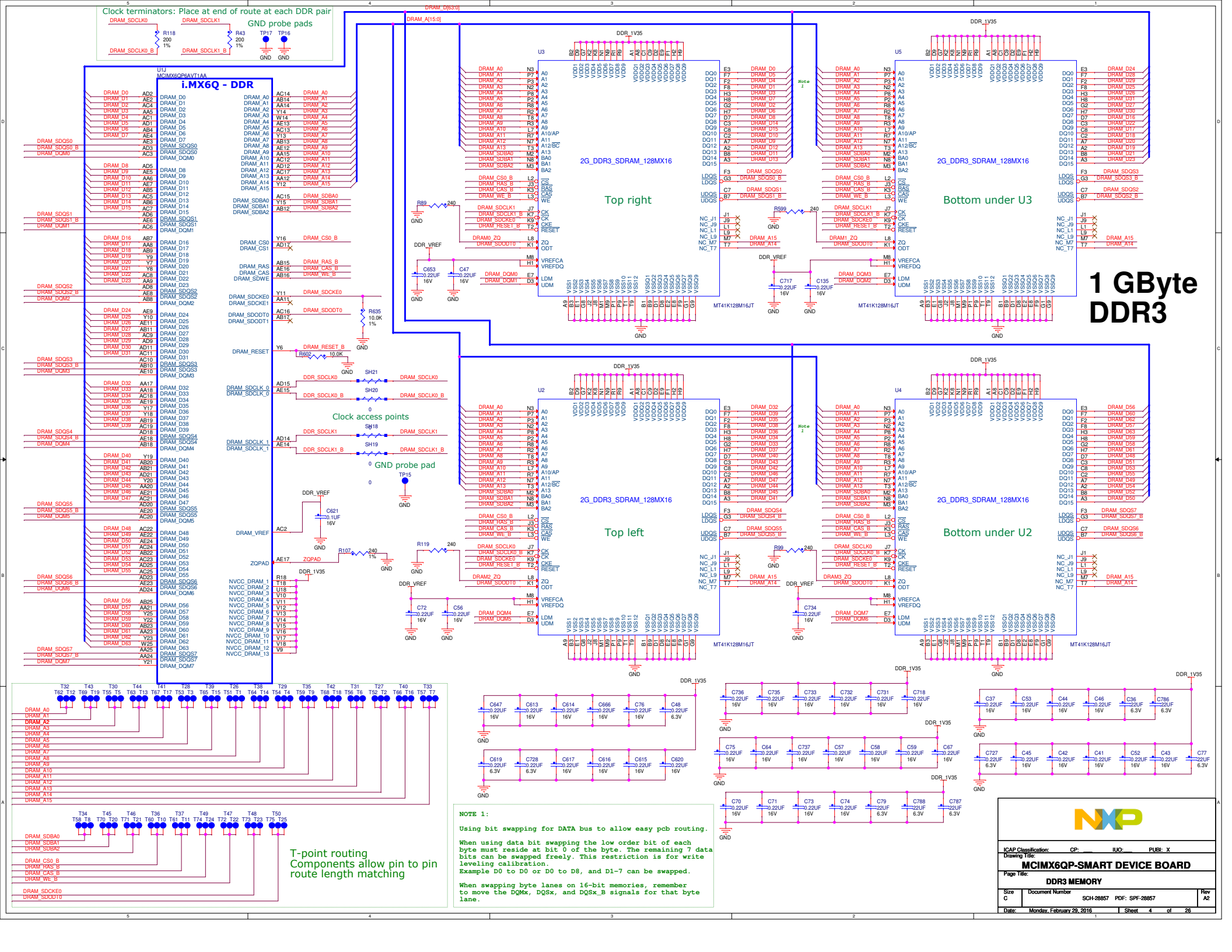
Clock terminators: Place at end of route at each DDR pair
GND probe pads
i.MX6Q - DDR
1 GByte DDR3
Top right
Bottom under U3
Top left
Bottom under U2
Clock access points
GND probe pad
T-point routing
Components allow pin to pin route length matching
NOTE 1:
Using bit swapping for DATA bus to allow easy pcb routing.
When using data bit swapping the low order bit of each byte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration.
Example D0 to D0 or D0 to D8, and D1-7 can be swapped.
When swapping byte lanes on 16-bit memories, remember to move the DQMx, DQSx, and DQSx_B signals for that byte lane.
ICAP Classification:
Drawing Title:
MCIMX6QP-SMART DEVICE BOARD
Page Title:
DDR3 MEMORY
Size C
Document Number SCH-28857 PDF: SPF-28857
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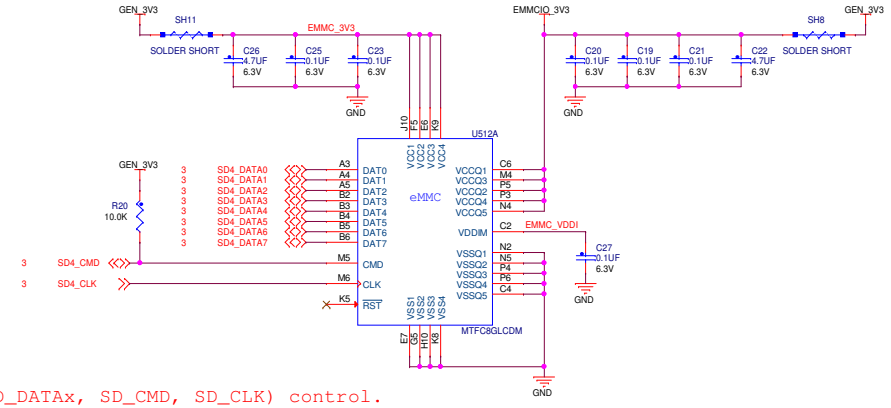
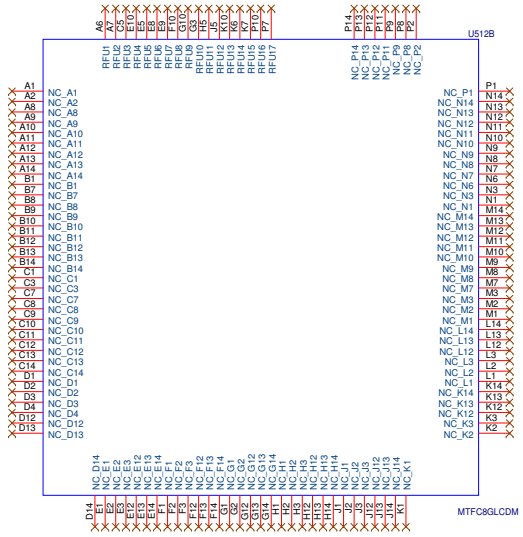
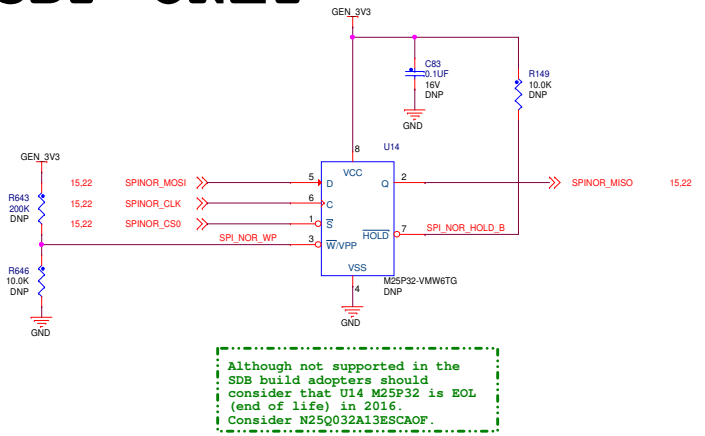
8GB eMMC MEMORY



Layout:
50ohm, SD signals (SD_DATAx, SD_CMD, SD_CLK) control.



4MB SPI NOR FLASH
SDP ONLY



Although not supported in the SDB build adopters should consider that U14 M25P32 is EOL (end of life) in 2016. Consider N25Q032A13ESCAOF.

ICAP Classification: CP: ___ IUO: ___ PUBI: X

Drawing Title: MCIMX6QP-SMART DEVICE BOARD

Page Title: eMMC, SPI NOR FLASH

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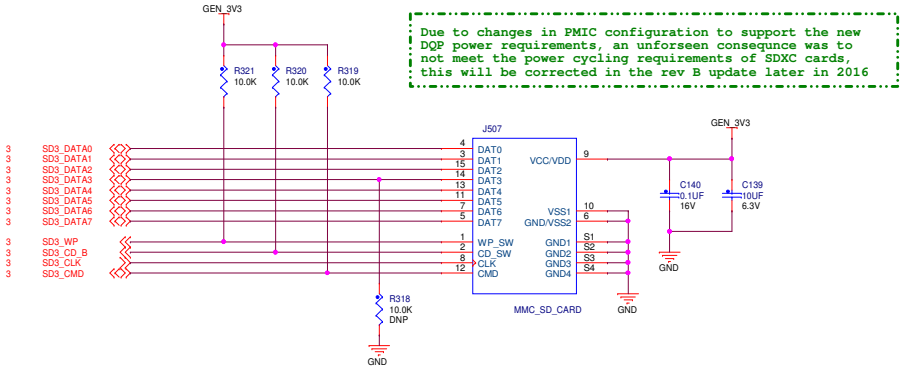
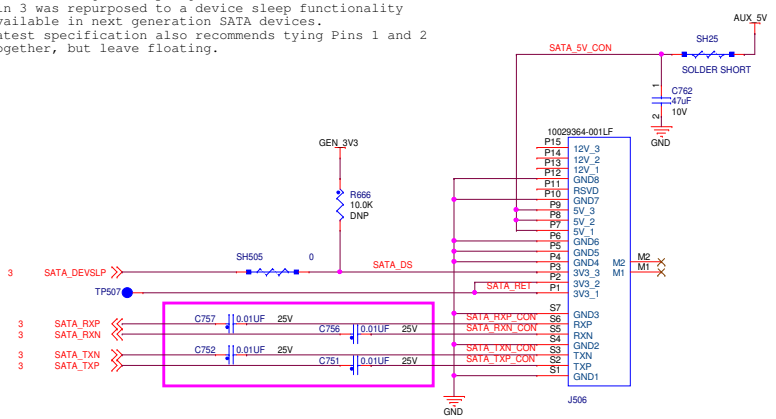
SD CARD SOCKET



Layout:
50ohm, SD signals(SD_DATAx, SD_CMD, SD_CLK) length equal

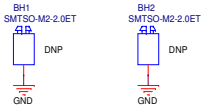
SATA CONNECTOR

NOTE:
The new SATA specification retires the 3V3 pins as they were not being used by regular sized SATA devices. Pin 3 was repurposed to a device sleep functionality available in next generation SATA devices. Latest specification also recommends tying Pins 1 and 2 together, but leave floating.



Layout:
1. 100ohm diff pairs, length equal
2. Mount these capacitors very close to the connector J506.

hard drive standoff



ICAP Classification:	CP: ___ IUO: ___ PUBI: X	
Drawing Title:	MCIMX6QP-SMART DEVICE BOARD	
Page Title:	SD CARD, SATA	
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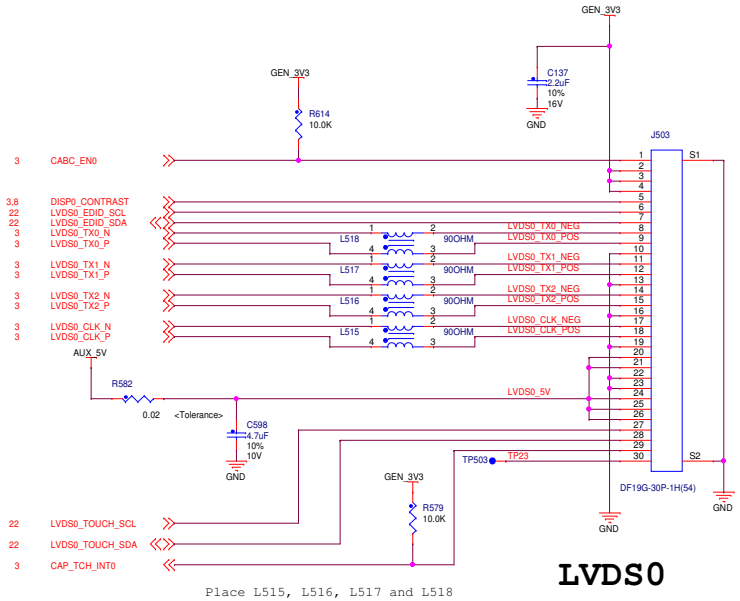
LVDS

Compatible Display:
Freescale part number
MCIMX-LVDS1

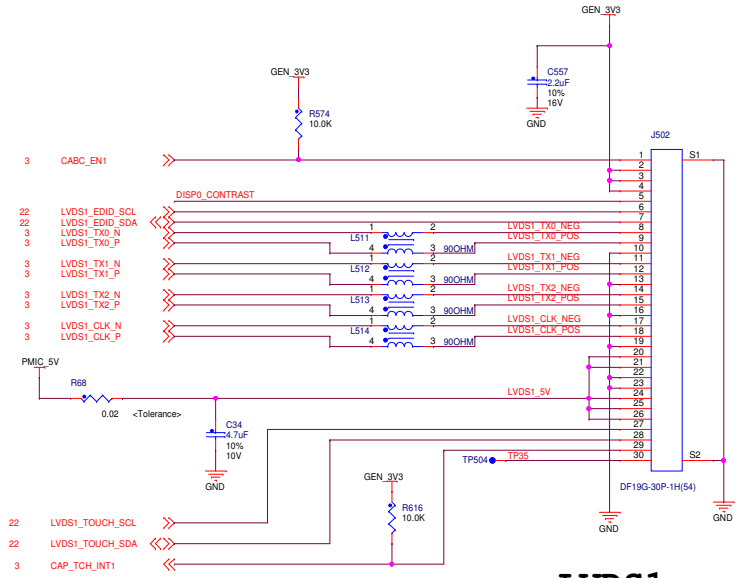
Freescale has purchased enough MCIMX-LVDS1 panels to meet its own development platform needs.

Adopters should consider their preferred display's requirements and check on lifetime availability.



LVDS0

Place L515, L516, L517 and L518
CMCs close to J403 connector.

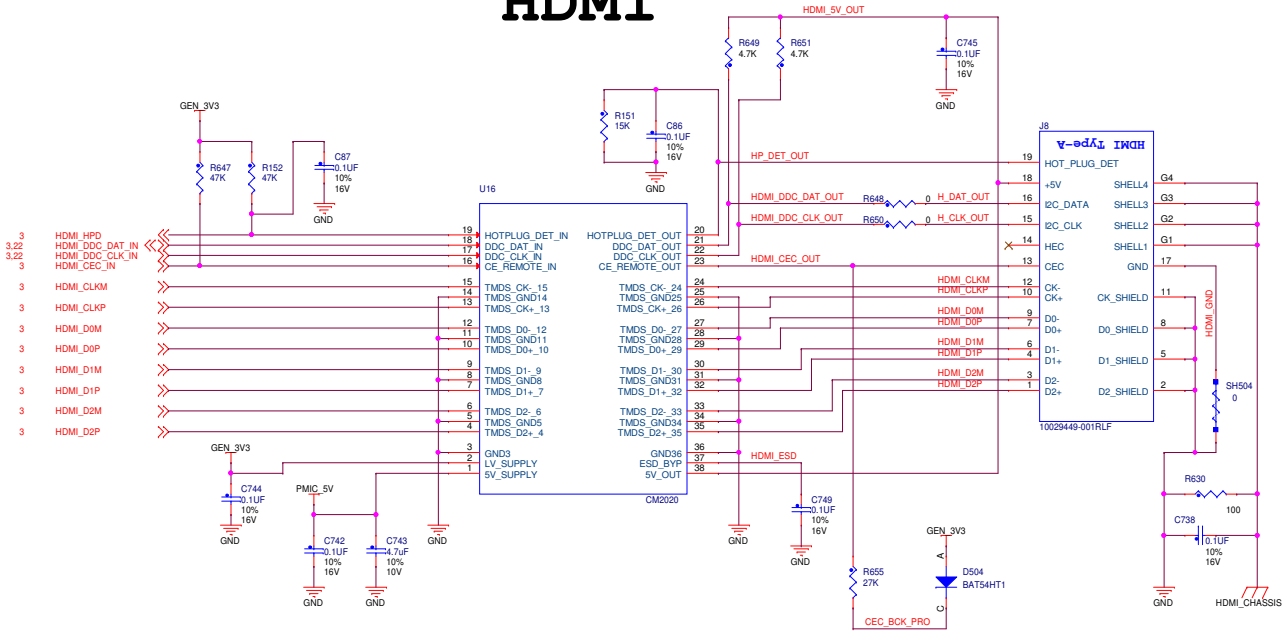


LVDS1

Place L511, L512, L513 and L514
CMCs close to J402 connector.

Layout: LVDS 100 ohm differential pairs

HDMI



Layout: HDMI 100 ohm differential pairs

NOTE:
When using HDMI, I2C2 bus is limited to 100 kHz to read EDID values due to HDMI standards. I2C2 bus speed should be limited to 100 kHz whenever Hot Plug Detect is high.

LVDS Connector notes:
Pin 1: This pin is the Display Enable pin. It is used to Enable/Disable the HannStar display.
Pin 5: This pin is the Display Brightness control. It provides a PWM signal to the display to increase/decrease display brightness depending on PWM duty cycle. This signal is shared by all displays, so all displays will change brightness together.

ICAP Classification: CP: ___ IUO: ___ PUBI: X

Drawing Title: MCIMX6QP-SMART DEVICE BOARD

Page Title: LVDS, HDMI

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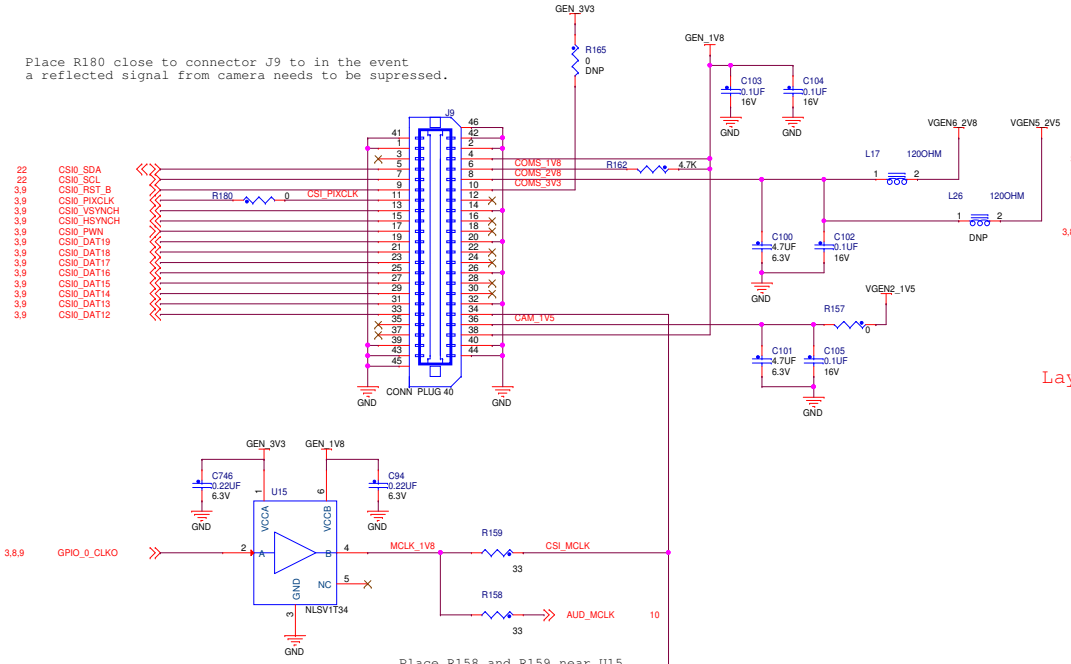
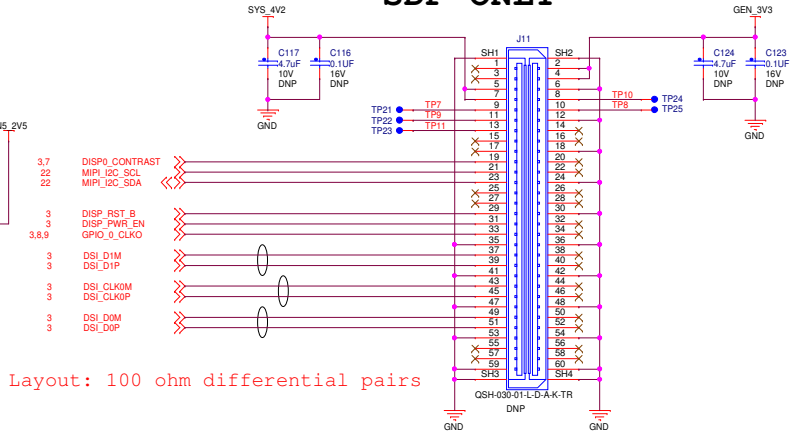
CSI CMOS Sensor
OV5642 5M Pixel



Place R158 and R159 near U15.
Acts as source termination.

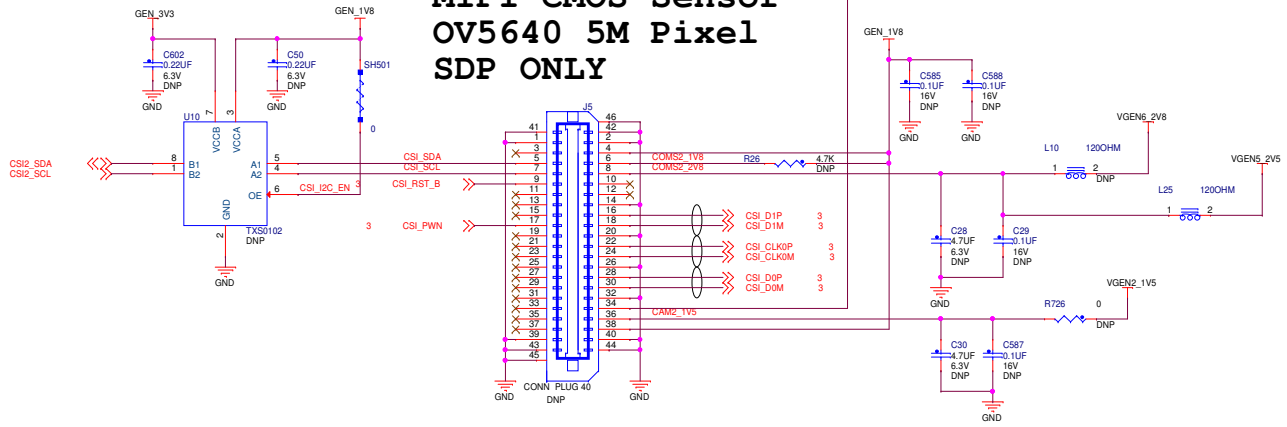
MIPI DISPLAY
EXP PORT
SDP ONLY



Layout: 100 ohm differential pairs

MIPI Connector

MIPI CMOS Sensor
OV5640 5M Pixel
SDP ONLY



Layout: 100 ohm differential pairs

ICAP Classification:	CP: ___	IUO: ___	PUBI: X
Drawing Title:	MCIMX6QP-SMART DEVICE BOARD		
Page Title:	CAMERA, EXP PORT		
Size: C	Document Number: SCH-28857 PDF: SPF-28857		Rev: A2
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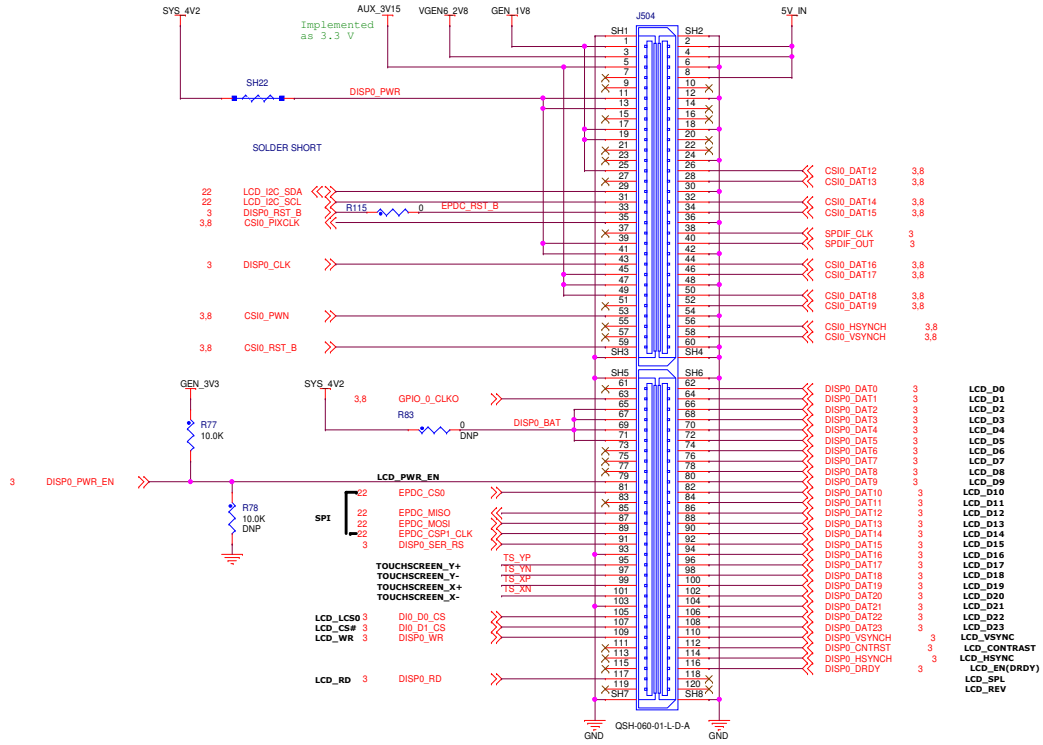
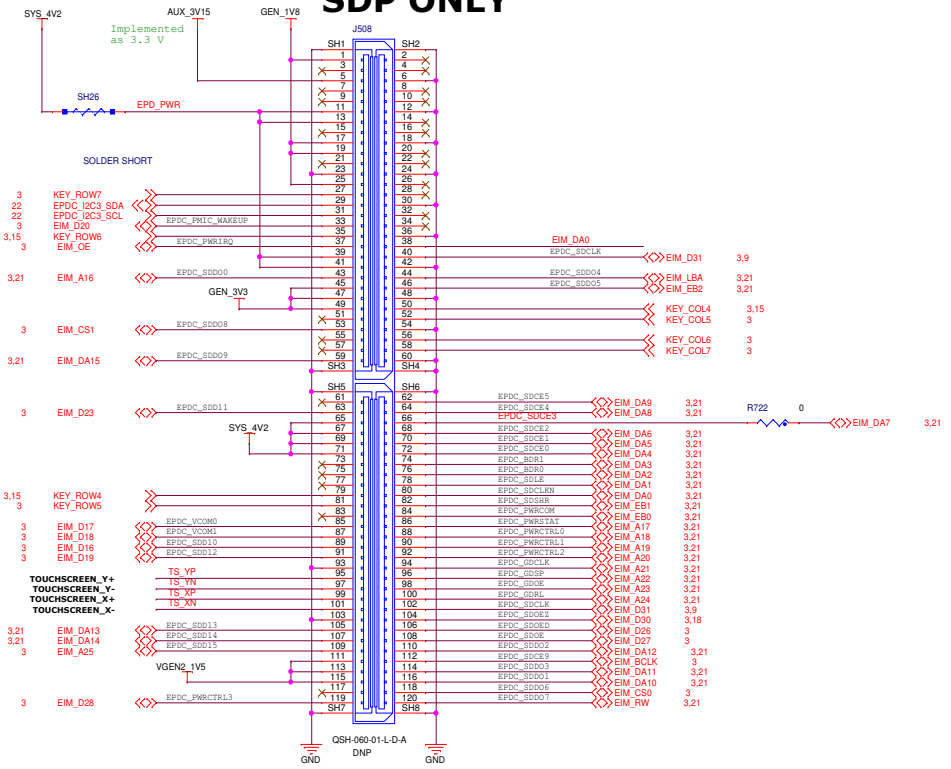
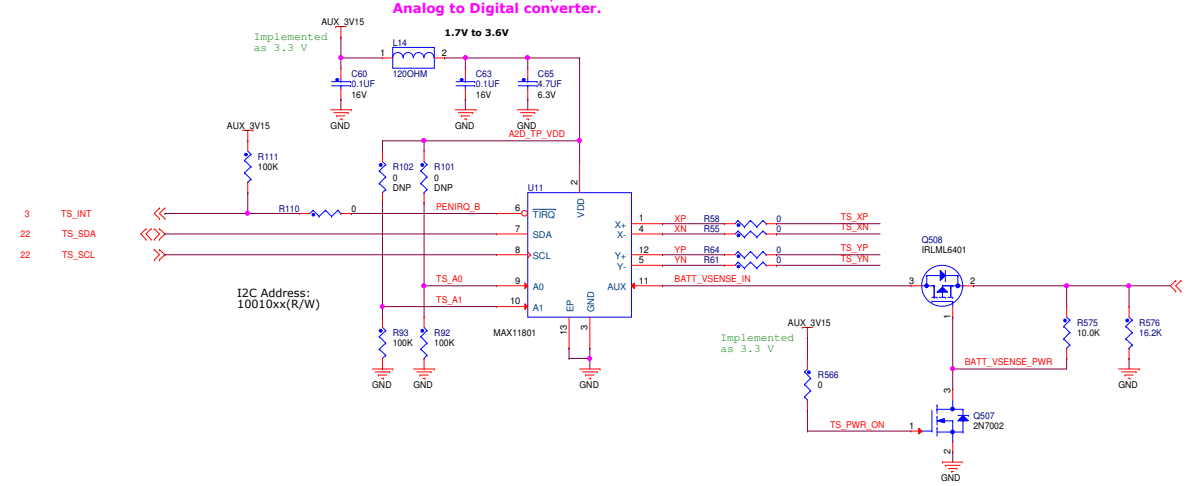
DISP0 Expansion Connector



For EPD SDP ONLY



Touch Panel decoder, Analog to Digital converter.



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Size: C	Document Number: SCH-28857 PDF: SPF-28857		Rev: A2
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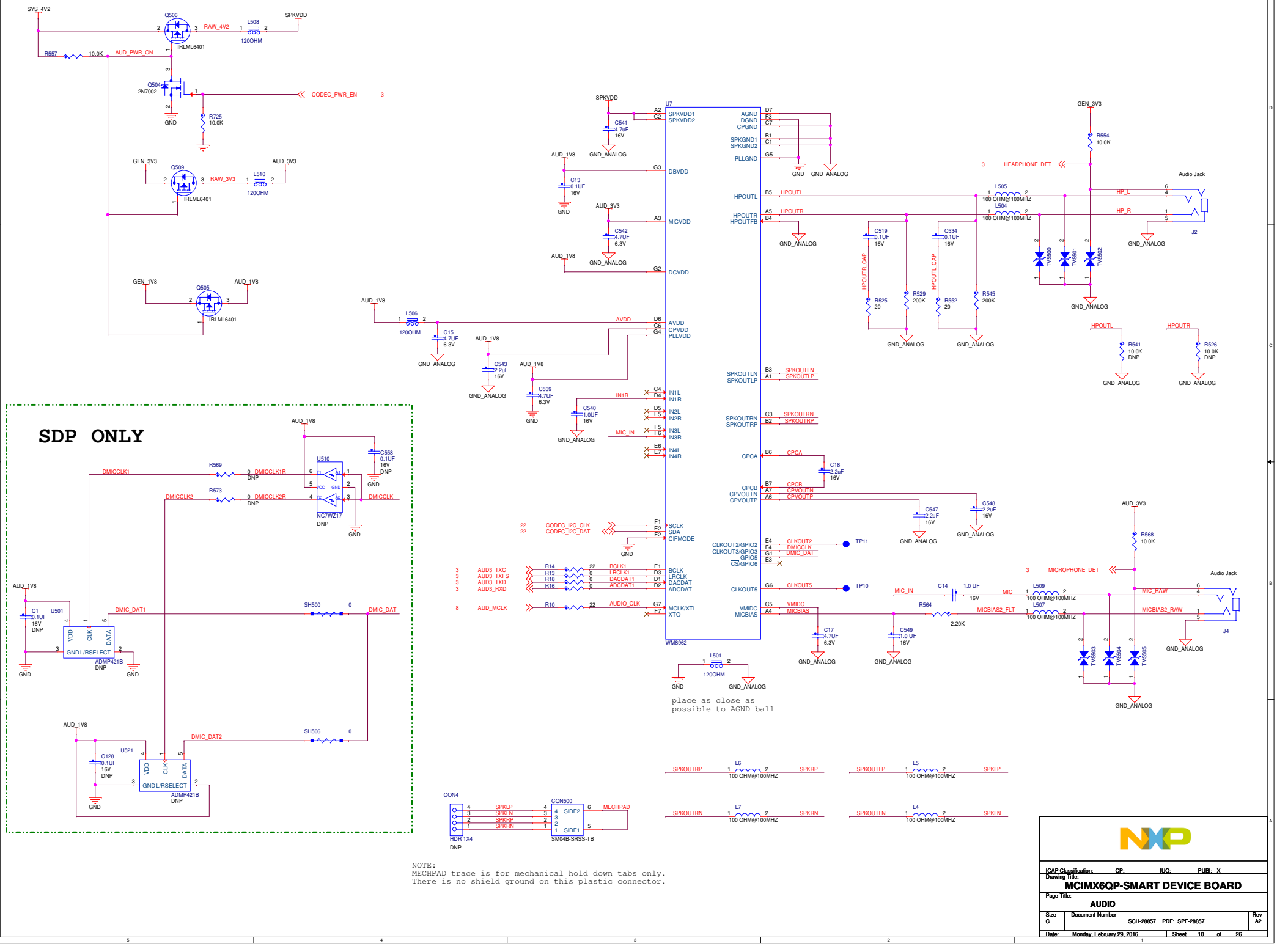
SDP ONLY
U7
WM8962
Q506
Q504
Q509
Q505
IRLML6401
2N7002
L508
L510
L506
120OHM
SYS_4V2
SPKVDD
GEN_3V3
AUD_3V3
GEN_1V8
AUD_1V8
RAW_4V2
RAW_3V3
AUD_PWR_ON
CODEC_PWR_EN
R557
10.0K
R725
GND
GND_ANALOG
C541
4.7uF
16V
C13
0.1UF
C542
6.3V
C15
C543
2.2uF
C539
C540
1.0UF
SPKVDD1
SPKVDD2
DBVDD
MICVDD
DCVDD
AVDD
CPVDD
PLLVDD
AGND
DGND
CPGND
SPKGND1
SPKGND2
PLLGND
IN1L
IN1R
IN2L
IN2R
IN3L
IN3R
IN4L
IN4R
SCLK
SDA
CIFMODE
BCLK
LRCLK
DACDAT
ADCDAT
MCLK/XTI
XTO
HPOUTL
HPOUTR
HPOUTFB
SPKOUTLN
SPKOUTLP
SPKOUTRN
SPKOUTRP
CPCA
CPCB
CPVOUTN
CPVOUTP
CLKOUT2/GPIO2
CLKOUT3/GPIO3
GPIO5
CS/GPIO6
CLKOUT5
VMIDC
MICBIAS
HPOUTL
HPOUTR
HPOUTR_CAP
HPOUTL_CAP
R519
R525
R529
R534
R552
R545
R554
R541
R526
L505
L504
100 OHM@100MHZ
HP_L
HP_R
HEADPHONE_DET
Audio Jack
J2
TVS500
TVS501
TVS502
C18
2.2uF
C547
C548
C17
4.7UF
6.3V
C549
1.0 UF
TP11
TP10
CLKOUT2
DMICCLK
DMIC_DAT
CLKOUT5
VMIDC
MICBIAS
MIC_IN
MIC
C14
1.0 UF
L509
L507
MICBIAS_FLT
MICBIAS2_FLT
MICBIAS2_RAW
MIC_RAW
MICROPHONE_DET
R564
2.20K
R568
10.0K
J4
TVS503
TVS504
TVS505
L501
120OHM
place as close as
possible to AGND ball
CODEC_I2C_CLK
CODEC_I2C_DAT
AUD3_TXC
AUD3_TXFS
AUD3_TXD
AUD3_RXD
AUD_MCLK
AUDIO_CLK
R14
R13
R18
R16
R10
BCLK1
LRCLK1
DACDAT1
ADCDAT1
IN1R
MIC_IN
R569
R573
DMICCLK1
DMICCLK2
DMICCLK1R
DMICCLK2R
U510
NC7WZ17
C558
0.1UF
U501
U521
ADMP421B
DMIC_DAT1
DMIC_DAT2
SH500
SH506
C1
C128
VDD
CLK
DATA
GND L/RSELECT
CON4
HDR 1X4
CON500
SM04B-SRSS-TB
MECHPAD
SPKLP
SPKLN
SPKRP
SPKRN
L6
L5
L7
L4
SPKRP
SPKLP
SPKRN
SPKLN
NOTE:
MECHPAD trace is for mechanical hold down tabs only.
There is no shield ground on this plastic connector.
ICAP Classification:
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Page Title:
AUDIO
Size
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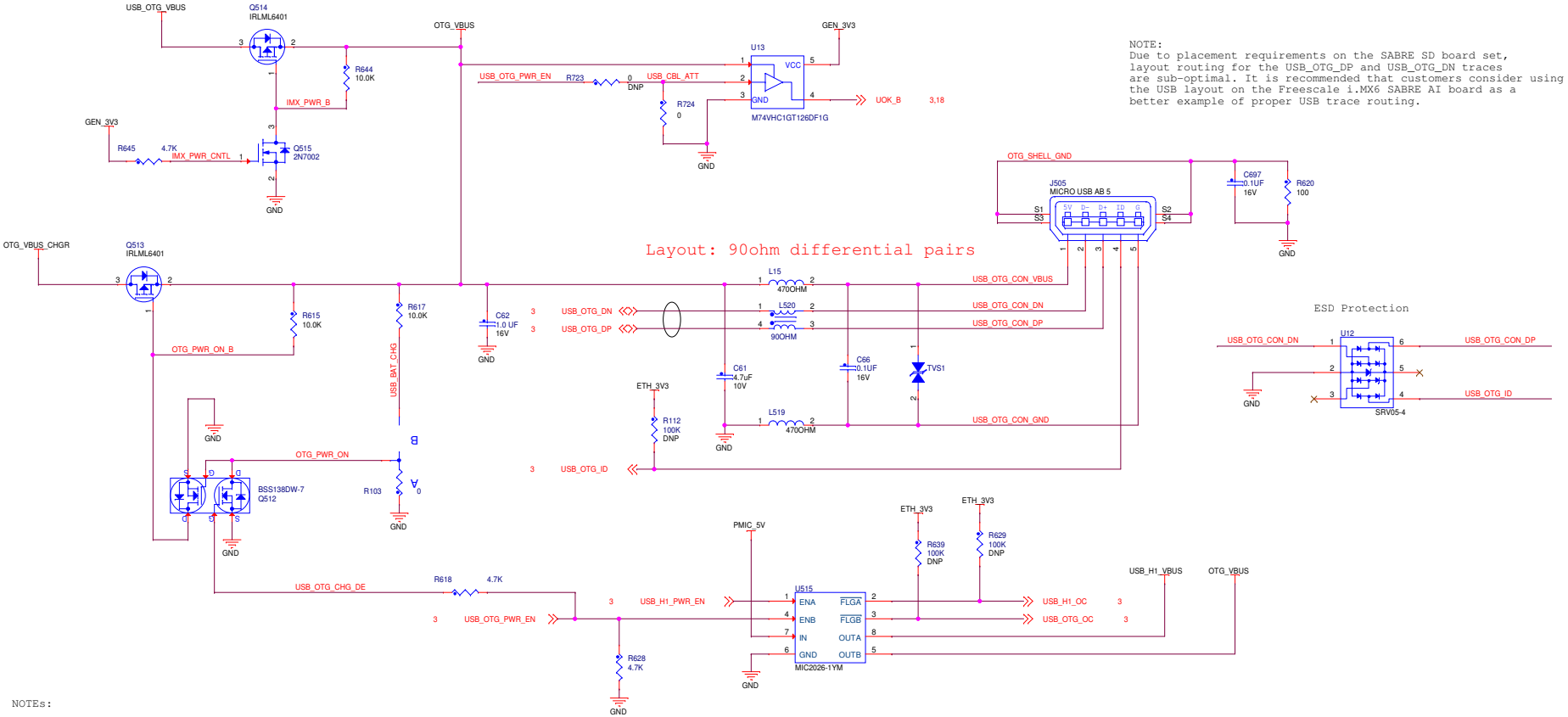

NOTEs:

1. R103 populated in A position to prevent USB_5V path to battery charge ICs when no batteries are attached. To enable charging batteries from USB, move resistor from Position A to Position B.

TRUTH TABLE

OTG_VBUS INPUT TO BATTERY CHARGERS

USB_OTG _PWR_EN	OTG_PWR _ON	OTG_PWR _ON_B	OTG_VBUS _CHGR
LOW	HIGH	LOW	POWERED
HIGH	LOW	HIGH	NOT POWERED

NOTE:
On all three pad resistor options, resistors are to be initially populated on pads 1 - 2 (Option A). Users may move resistors from their default locations as needed.

ICAP Classification: CP: ___ IUO: ___ PUBI: X

Drawing Title: MCIMX6QP-SMART DEVICE BOARD

Page Title: USB

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To Processor I/O supply

Alternate power source for processor I/O

NOTE:
Solder short normally connects NVCC_RGMII to ETH_VDDIO.
To connect NVCC_RGMII to VGEN2_1V5, cut the trace between pads 1 - 2 and solder a 0 Ohm resistor between pads 2 - 3.

Layout: High speed data lines : 50 ohms
Place R634 near the AR8031 PHY.

Layout: 100 ohm differential pairs

EMI Filter Reserved
470pF are for LED

NOTE:
Place R626 close to Ethernet PHY.

Note: ENET_REF_CLK

On the DQP processors this connection is now optional, the internal Ethernet PLL can be used to provide the ENET clock reference

Place LED D11 near LED for pins 11 - 12 of RJ-45 connector. Orange LED indicates 1000 speed.

Power-on Strapping Pins

MODE2[3:0]

(Default assemble: 0000)
1100 BaseT, RMII1;
1101 BaseT, RMII2;
1110 100X, RGMII, 75OHMS;
1111 100X, TRANS, 75OHMS;
0000 BaseT, RGMII;
0001 BaseT, SGMII;
0010 1000X, RGMII, 50OHMS;
0011 1000X, RGMII, 75OHMS;
0100 1000X, TRANS, 50OHMS;
0101 1000X, TRANS, 75OHMS;
0110 100X, RGMII, 50OHMS;
0111 100X, TRANS, 50OHMS;
Others Reserved

PHYADDRESS0
PHYADDRESS1
MODE2[1]
MODE2[3]
MODE2[2]
MODE2[0]
SEL_GPIO_INT
ANA_MOD

ICAP Classification: CP: ___ IUO: ___ PUBI: X

Drawing Title: **MCIMX6QP-SMART DEVICE BOARD**

Page Title: **ETHERNET**

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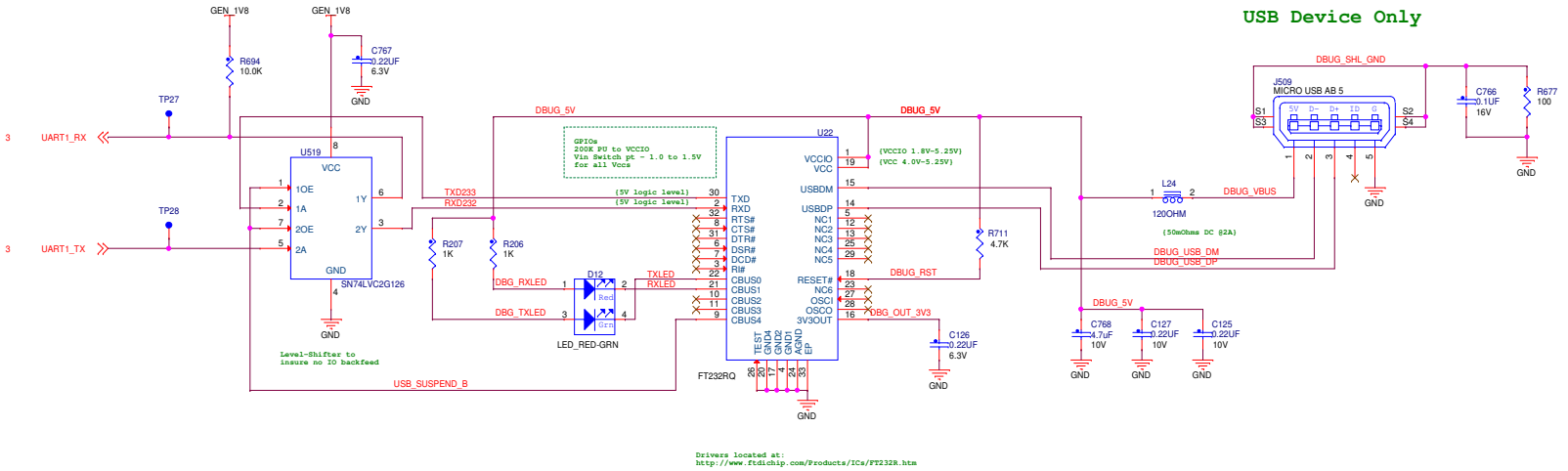
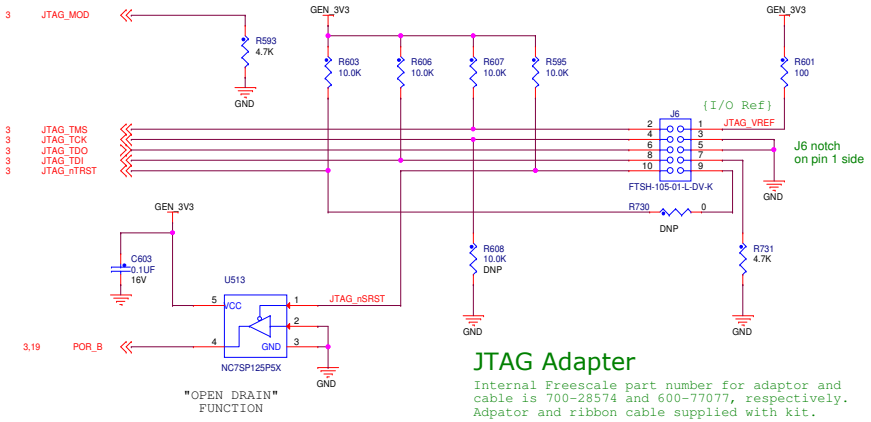
DEBUG UART TO USB CONVERSION

Library Revision - A



JTAG



JTAG Adapter

Internal Freescale part number for adaptor and cable is 700-28574 and 600-77077, respectively. Adpator and ribbon cable supplied with kit.

ICAP Classification:	CP: ___	IUO: ___	PUBI: X
Drawing Title:	MCIMX6QP-SMART DEVICE BOARD		
Page Title:	JTAG, DEBUG		
Size: C	Document Number: SCH-28857 PDF: SPF-28857		Rev: A2
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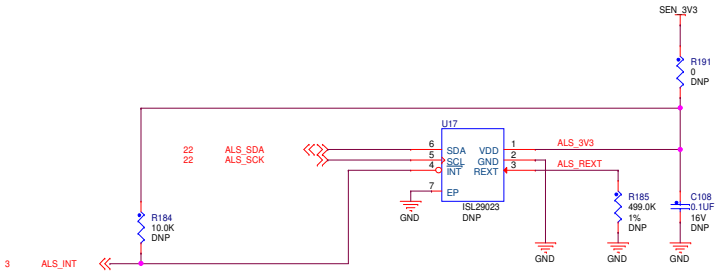
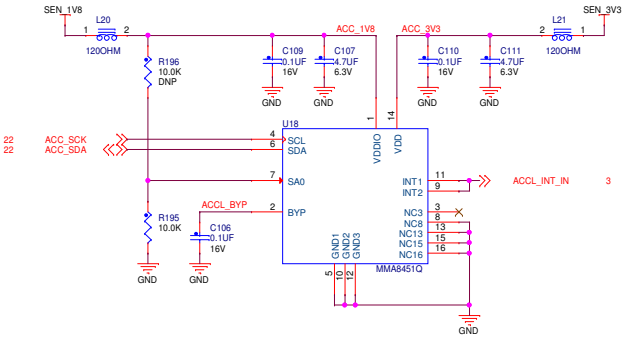
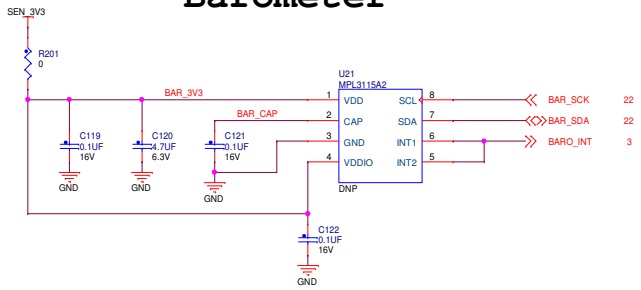
Ambient Light Sensor
SDP ONLY



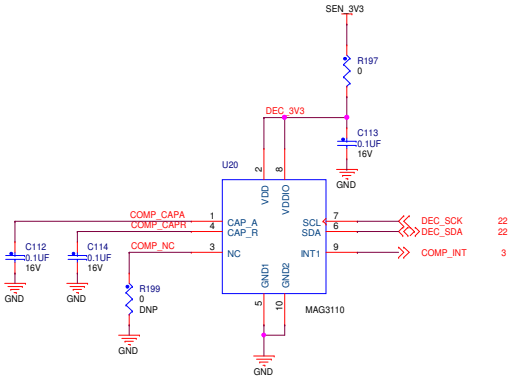
3-AXIS ACC

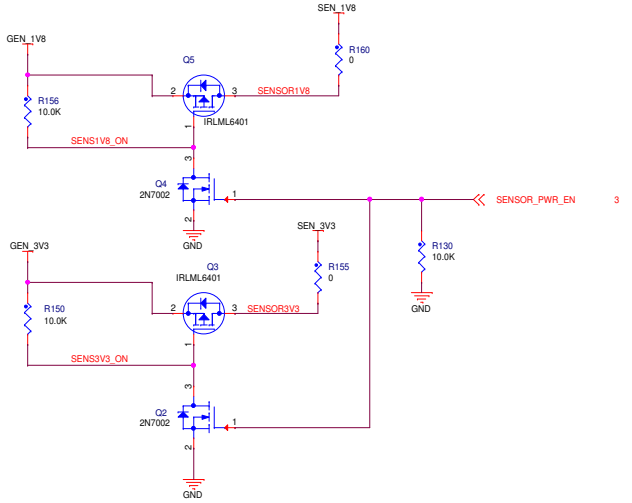


Barometer



Digital eCompass





ICAP Classification:	CP: ___	IUO: ___	PUBI: X
Drawing Title: MCIMX6QP-SMART DEVICE BOARD			
Page Title: SENSORS			
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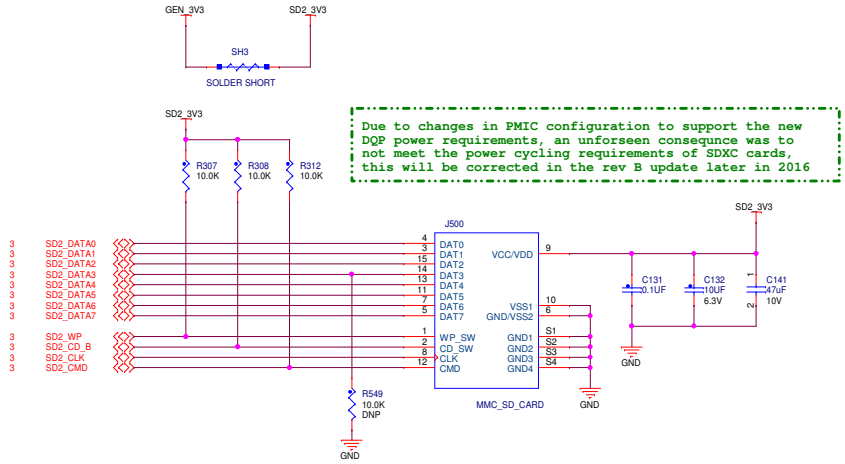
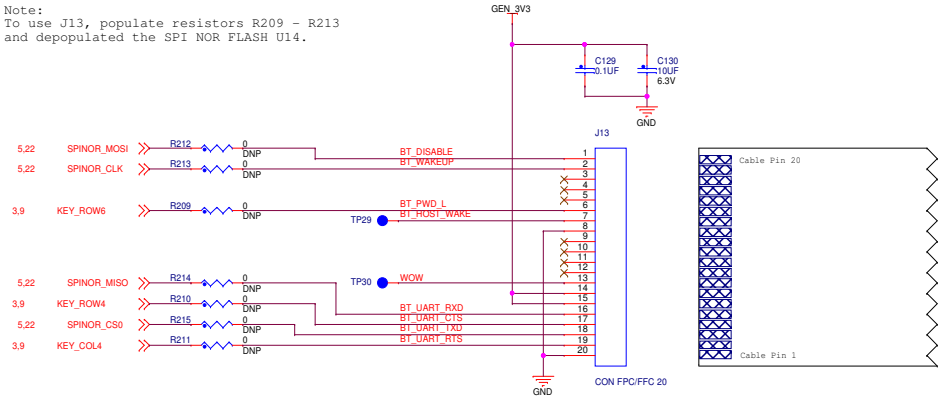
AUX SDIO CARD SOCKET



Layout:
50ohm, SD signals(SD_DATAx, SD_CMD, SD_CLK) length equal

BLUETOOTH CABLE CONNECTOR

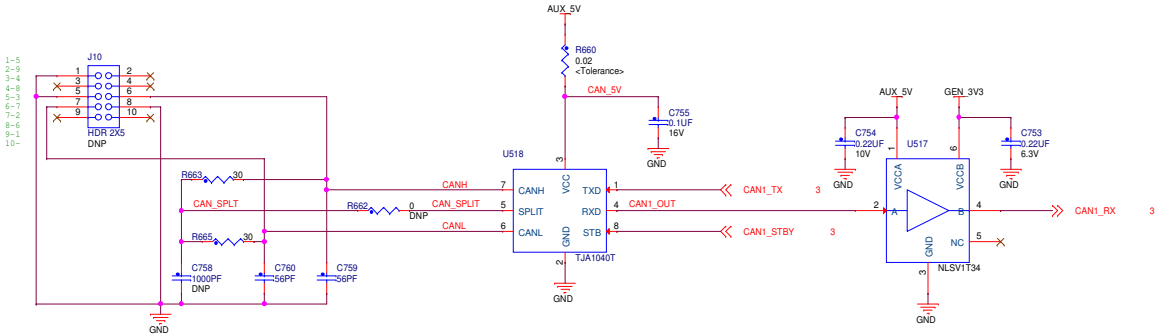
Note:
To use J13, populate resistors R209 - R213
and depopulated the SPI NOR FLASH U14.



NOTE:
The AUX SDIO CARD SOCKET and the BLUETOOTH CABLE CONNECTOR have been designed and tested specifically for use with the WIFI/BT combo card SX-SDCAN-2830BT Developed and sold by Silex Technolgy. The developer may need to consult the datasheet of other WIFI solutions for compatibility with this card socket.

NOTE:
Pin 1 of the cable connector on the Smart Device board is opposite Pin 20 of the WIFI/BT module. For the FFC to lie flat, the pin order number needs to be reversed on the schematics.

OPTIONAL CAN PINOUT SDP ONLY



ICAP Classification:	CP: ___	IUO: ___	PUBI: X
Drawing Title:	MCIMX6QP-SMART DEVICE BOARD		
Page Title:	AUX SDIO CONN, CAN		
Size: C	Document Number: SCH-28857 PDF: SPF-28857		Rev: A2
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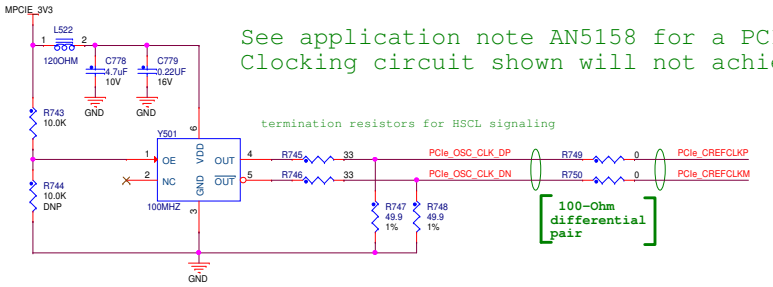
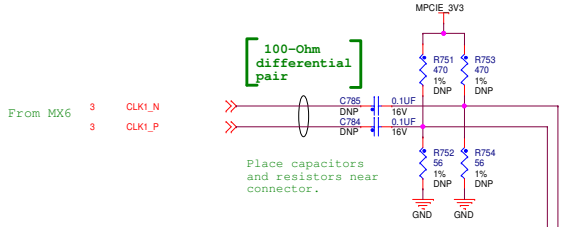
PCIe Oscillator

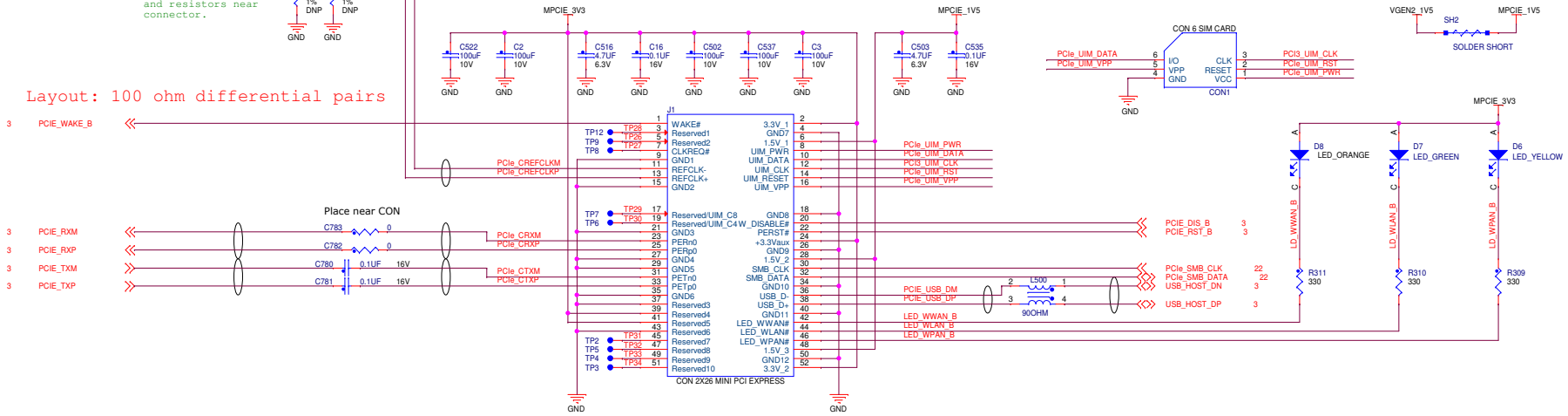


See application note AN5158 for a PCIe certification guide.
Clocking circuit shown will not achieve certification.

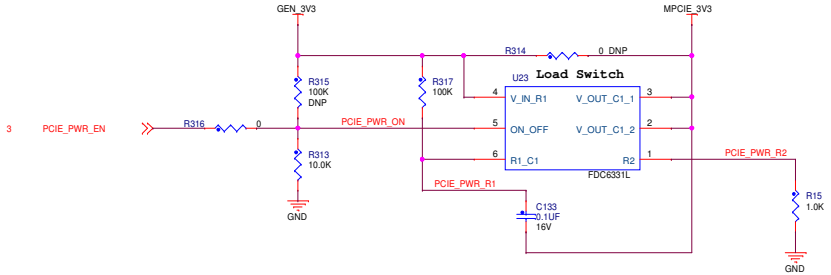
Mini-PCIE



Layout: 100 ohm differential pairs



NOTE:
This design assumes a normal loading on the MPCIE_3V3 rail of up to 1A.
If more than 1A loading is desired, the designer must consider other load on the GEN_3V3 rail and depopulate other loads to allow additional loading on the MPCIE_3V3 rail. The MPCIE_1V5 rail is allowed a maximum of 100 mA.



ICAP Classification:	CP: ___	IUO: ___	PUBI: X
Drawing Title:	MCIMX6QP-SMART DEVICE BOARD		
Page Title:	mPCIe CONN		
Size: C	Document Number: SCH-28857 PDF: SPF-28857		Rev: A2
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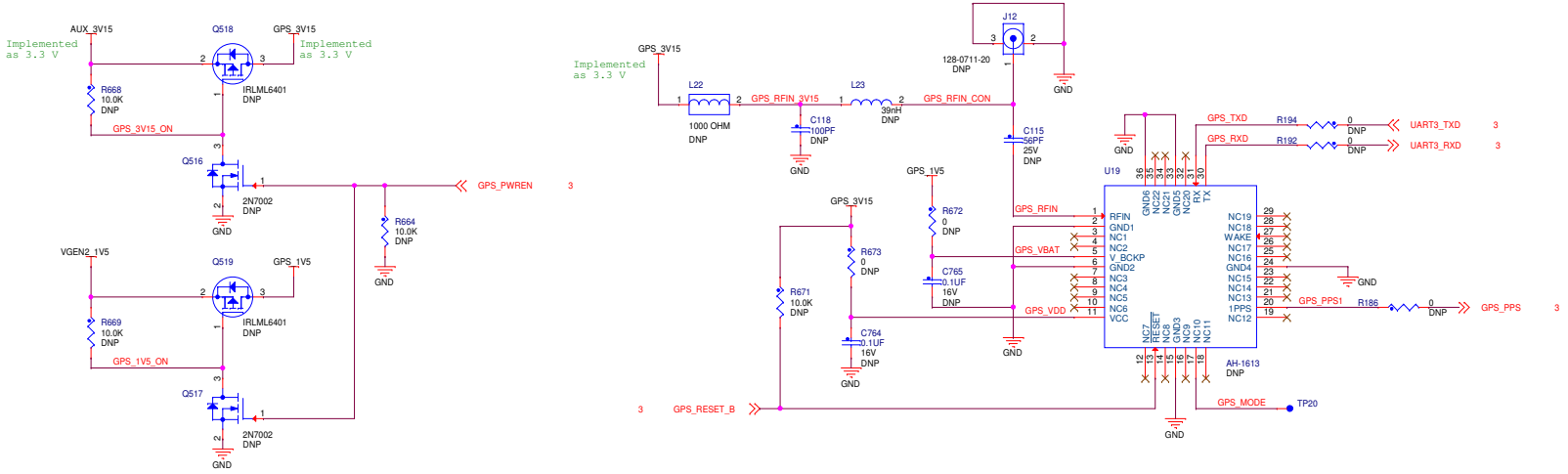
GPS Receiver
SDP ONLY



ICAP Classification:	CP: ___	IUO: ___	PUBI: X
Drawing Title:	MCIMX6QP-SMART DEVICE BOARD		
Page Title:	GPS MODULE		
Size: C	Document Number: SCH-28857 PDF: SPF-28857		Rev: A2
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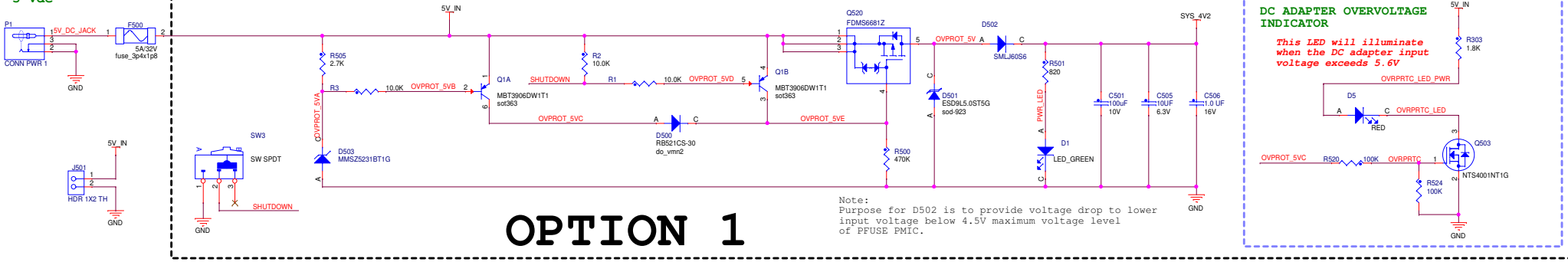
OVER VOLTAGE PROTECTION

External Power 5 Vdc



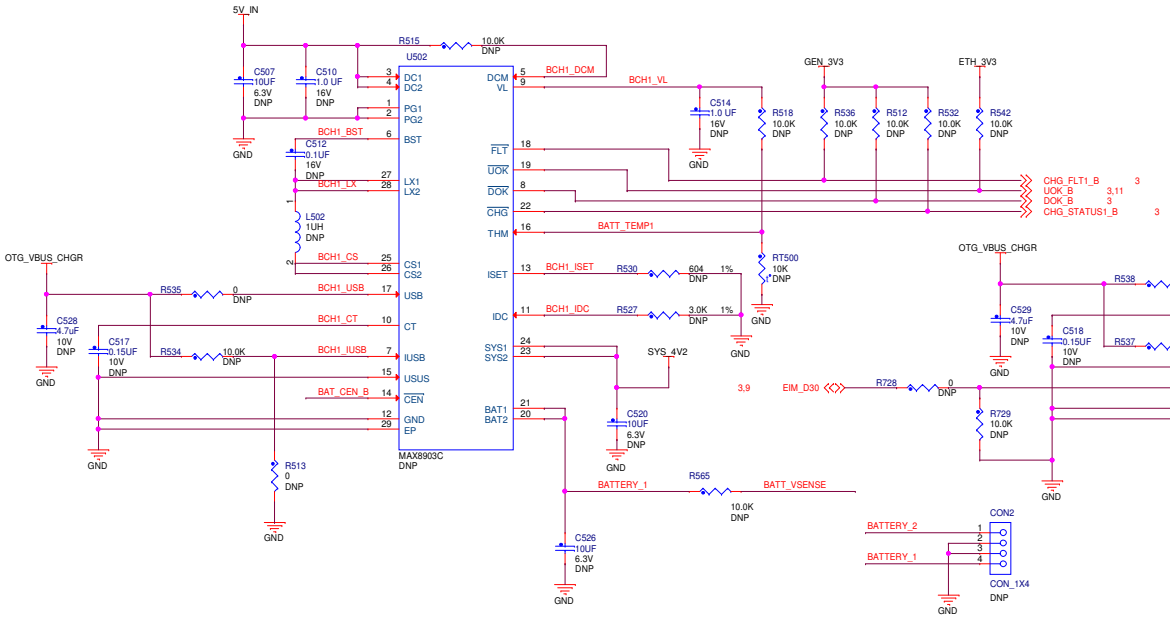
Note:
Purpose for D502 is to provide voltage drop to lower input voltage below 4.5V maximum voltage level of PFUSE PMIC.

DC ADAPTER OVERVOLTAGE INDICATOR

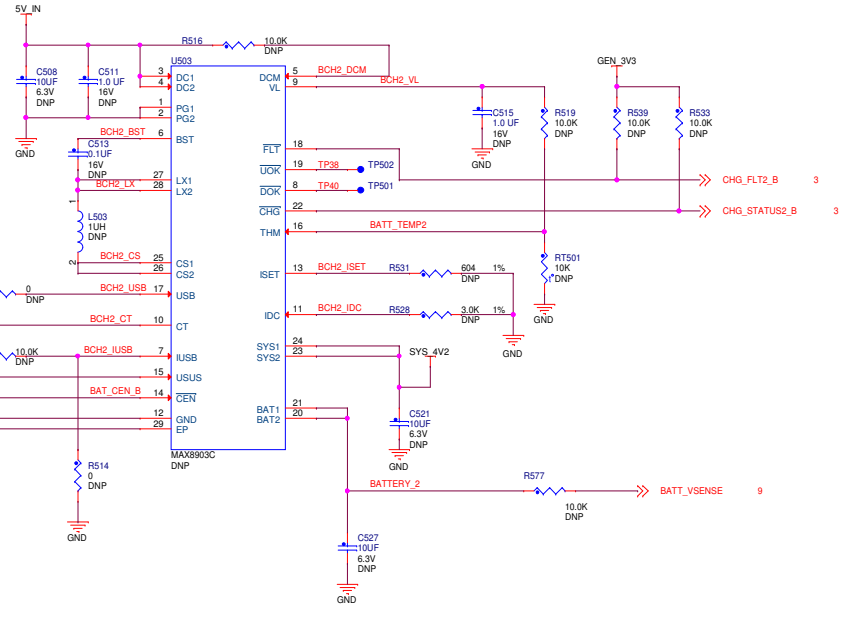
This LED will illuminate when the DC adapter input voltage exceeds 5.6V

OPTION 1

BATTERY 1 CHARGE CIRCUIT



BATTERY 2 CHARGE CIRCUIT



OPTION 2

NOTE:
Battery posts are meant for two, single cell 3.7 Li-ION batteries to be added in parallel.

Note: Populate either
Option #1 for the Smart Device Board (SDB), or
Option #2 for the Smart Device Platform (SDP) - NOT SUPPORTED on 6QP-SDB

ICAP Classification:	CP: ___	IUO: ___	PUBI: X
Drawing Title:	MCIMX6QP-SMART DEVICE BOARD		
Page Title:	BATTERY CHARGER		
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1.825 V setpoint ensures compliance with VIN1 min voltage spec

PMIC Powered-ON LED indicator

Note:
Bulk capacitors on VGEN1-6 are all 4.7uF for BOM consolidation purposes. Freescale recommended guidance for minimum capacitance on VGEN1, VGEN3, VGEN5, VGEN6 is 2.2uF.

NOTE:
R632 is provided for testing an alternate gating source for PMIC_5V power. The circuit has not been tested.

VDDOTP -

Connect TP14 to 8 volts to program PMIC OTP fuses

Freescale uses the automotive grade PMIC for single part usage across multiple board designs. Adopters should consider industrial grade version for cost reduction.

OPTIONAL:
PMIC Power On Circuit

Note:
To turn off board "AUTO ON" feature, depopulate R30 and R31, and populate U509. This feature has not been tested.

SYSTEM POWER RAILS

Voltge	Rail Name	Block	Generated By	Current Capability (mA)	NOTES
5.0	PMIC_5V	USB LVDS1 HDMI	PF0100 SWBST	600	
	AUX_5V	SATA LVDS0 CAN	MAX8815	1000	
3.3	GEN_3V3	EMMC SD3 NOR SATA LVDS HDMI MIPI mPCIe SENSORS ETH	LT3680	2400	NVCC_LCD NVCC_EIM0/1/2 NVCC_GPIO NVCC_SD2/3 NVCC_NANDF NAND_JTAG NVCC_ENET
	AUX_3V15	EXP HDR TOUCH GPS			
3	VDDHIGH_IN	IMX6	PF0100 VGEN4	350	
2.8	VGEN6_2V8	CAMERA	PF0100 VGEN6	200	PGOOD LED
2.5	VGEN5_2V5	CAMERA	PF0100 VGEN5	100	GEN_3V3 ENABLE
	GEN_2V5	SATA HDMI MIPI mPCIe	IMX6 VDDHIGH_CAP	TBD	NVCC_MIPI
1.825	GEN_1V8	AUDIO CAMERA ACC	PF0100 SW4	1000	NVCC_SD1 NVCC_CSI VGEN1 & 2
1.5	VGEN2_1V5	CAMERA GPS mPCIe	PF0100VGEN2	250	
1.375	VDDCORE	ARMCORE	PF0100 SW2	2500	
	VDDSOC	VDDSOC	PF0100 SW1ABC	4500	
1.35	DDR_1V35	DDR	PF0100 SW3AB	2500	
0.675	VREFDDR	DDR	PF0100 VREFDDR	10	

ICAP Classification: CP: ___ IUO: ___ PUBI: X

Drawing Title: MCIMX6QP-SMART DEVICE BOARD

Page Title: PF0100 PMIC

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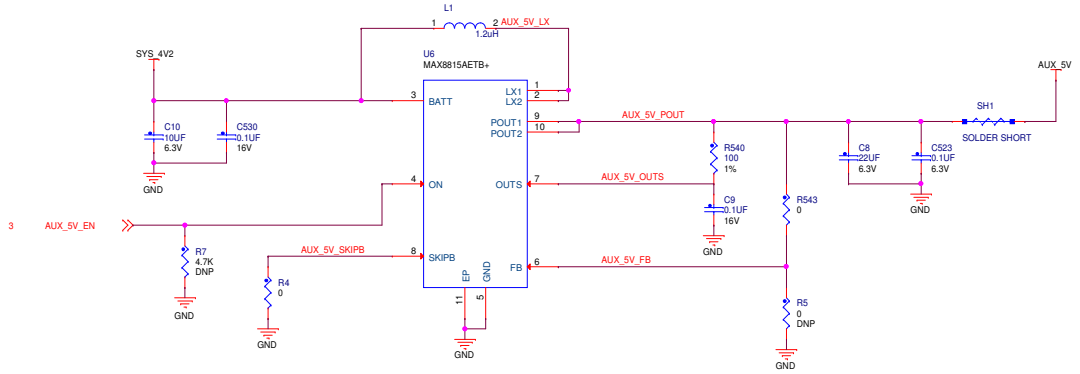
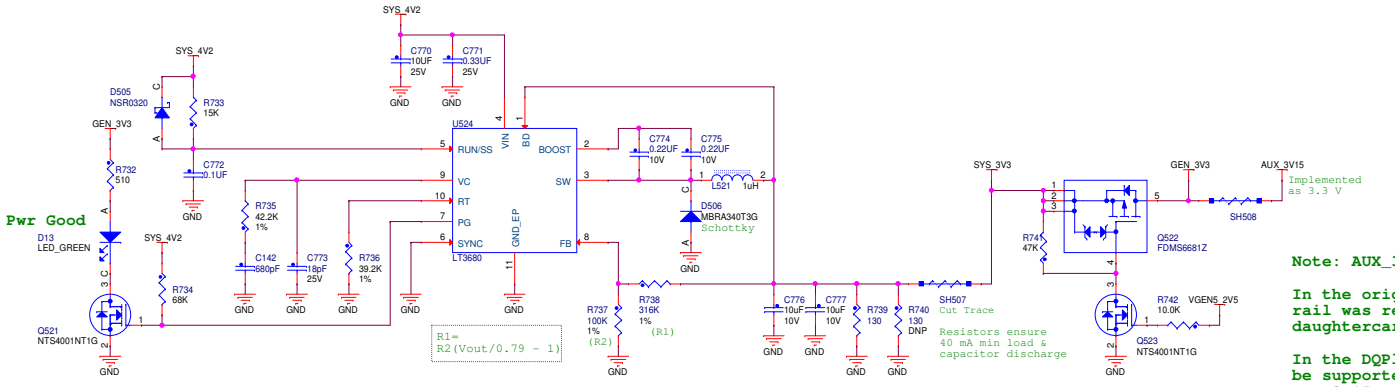
5.0V@1A DC-to-DC Converter



Peripheral Power Supply 2.4 A Max Load



Note: AUX_3V15 Supply

In the original DQ/DLS SDP design a 3.15V rail was required to support the EBook daughtercard (EPDC connector - J508).

In the DQPlus design only the SDB build will be supported making it possible to add the AUX_3V15 rail to the standard GEN_3V3 rail.

ICAP Classification: CP: ___ IUO: ___ PUBI: X		
Drawing Title: MCIMX6QP-SMART DEVICE BOARD		
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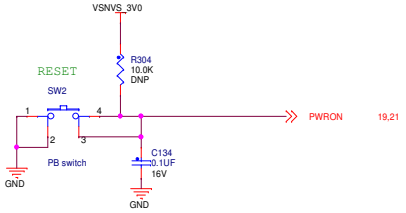
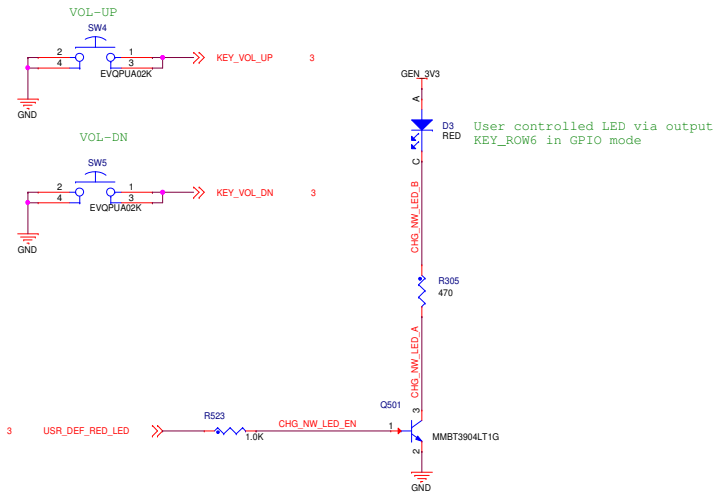
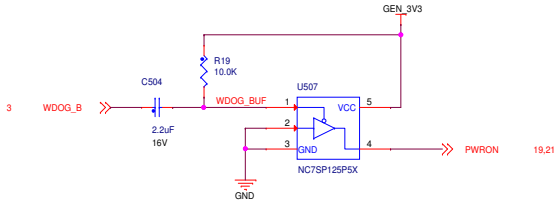


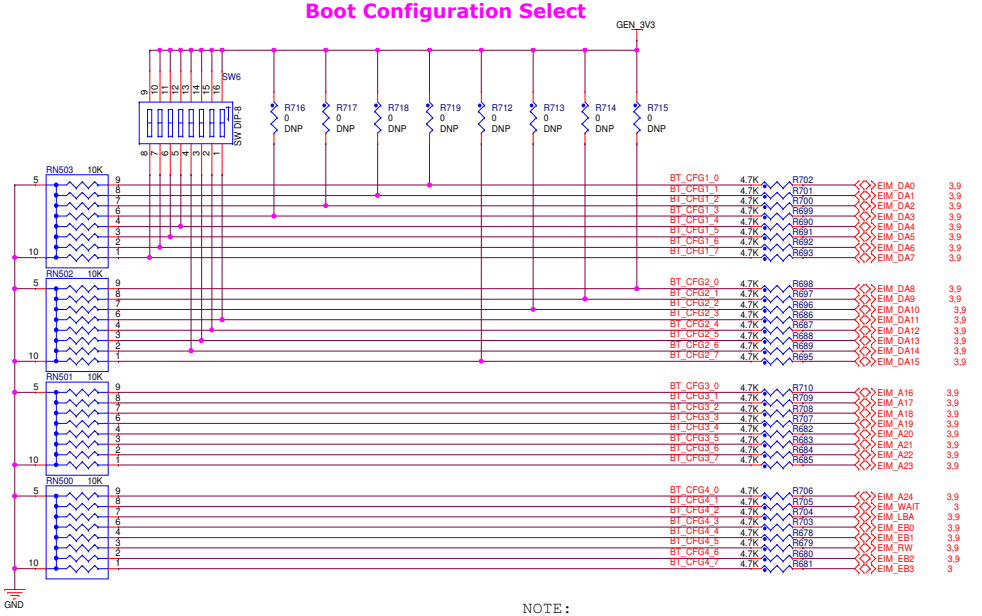
NOTE:
The RESET button is connected directly to the PWRON input
of the PMIC. This will cause a complete board reset
(Processor & PMIC) when the RESET button is pressed.

U/I KEY





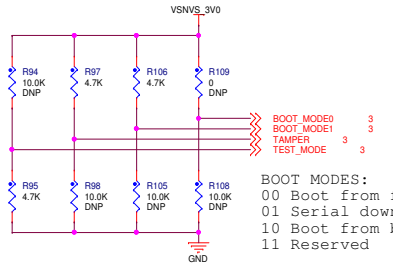
Boot Configuration Select



NOTE:
Place series resistors so as to minimize EIM portion of
trace length. Two layout possibilites include:
1) As close to processor as possbile.
2) Close to other componets using EIM signals.

Boot Select Table

8	7	6	5	4	3	2	1
BT_CFG1_7	BT_CFG1_6	BT_CFG1_5	BT_CFG1_4	BT_CFG2_6	BT_CFG2_5	BT_CFG2_4	BT_CFG2_3
011X = MMC/eMMC Boot				X0 = 1-bit X1 = 4-bit 10 = 8-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
010X = SD/eSD Boot				X0 = 1-bit X1 = 4-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
0010 = SATA Boot				X	X	X	0



BOOT MODES:
00 Boot from fuses
01 Serial downloader
10 Boot from board settings (DEFAULT)
11 Reserved

ICAP Classification: CP: ___ IUO: ___ PUBI: X

Drawing Title: **MCIMX6QP-SMART DEVICE BOARD**

Page Title: **BOOT SELECT**

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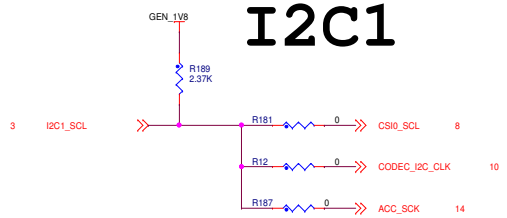
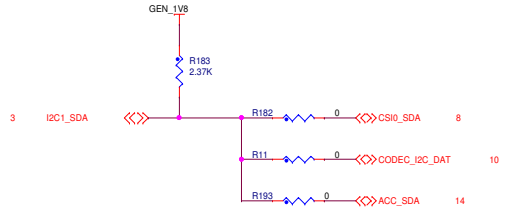
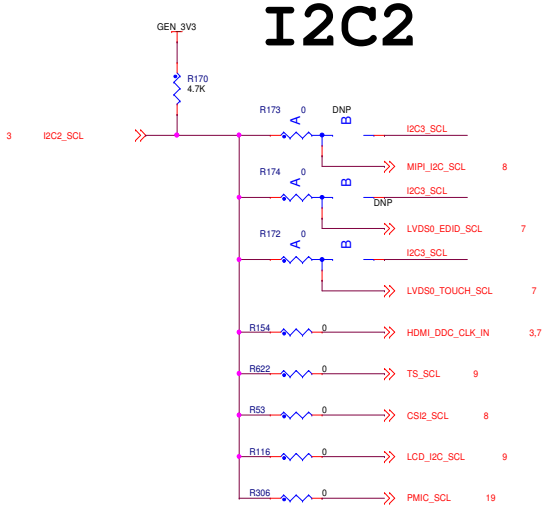
I2C1

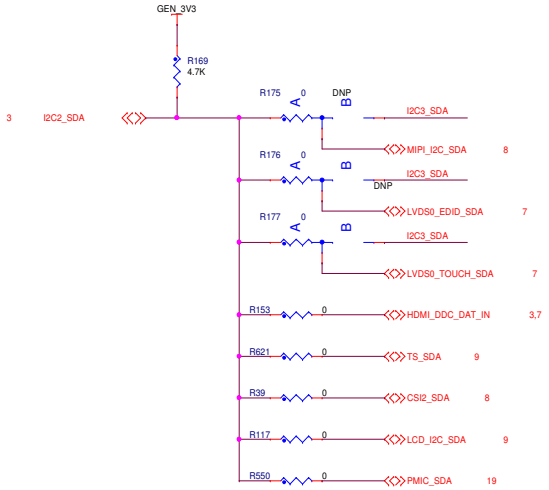




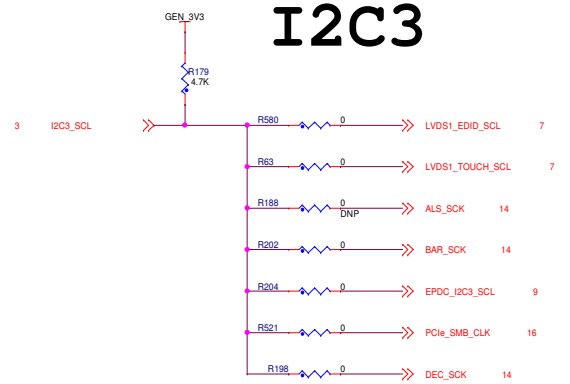
NOTE:
R183 and R189 were changed to bring I2C rise time from LOW >> HIGH within electric specification. If using a CODEC other than the one used in this design, it may be possbile to switch pull up resistors back to 4.7K.

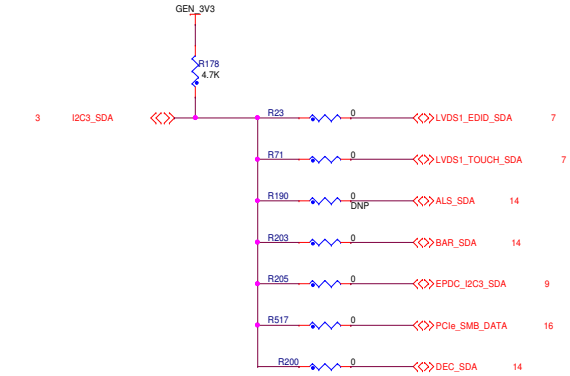
I2C2





I2C3





CSPI1

NOTE:
On all three pad resistor options, resistors are to be initially populated on pads 1 - 2 (Option A). Users may move resistors from their default locations as needed.

ICAP Classification:	CP: ___	IUO: ___	PUBI: X
Drawing Title:	MCIMX6QP-SMART DEVICE BOARD		
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Build Option: MCIMX6QP-SDB

1.	CAN Output not populated: J10
2.	Battery Charging circuit not populated: C507, C508, C510, C511, C512, C513, C514, C515, C517, C518, C520, C521, C526, C527, C528, C529, CON2, CON3, L502, L503, R512, R513, R514, R515, R516, R518, R519, R527, R528, R530, R531, R532, R533, R534, R535, R536, R537, R538, R539, R542, R565, R577, R729, RT500, RT501, U502, U503
3.	SPI NOR Flash not populated: C83, R149, R643, R646, U14
4.	MIPI Display/Camera Expansion Ports not populated: C28, C29, C30, C50, C116, C117, C123, C124, C585, C587, C588, C602, J11, J5, L25, R26, R165, R173, R175, R726, U10
5.	Audio Block Components not populated: C1, C128, C558, R569, R573, U501, U510, U521
6.	EPDC Port Connector not populated: J508
7.	Ambient Light Sensor not populated: C108, R184, R185, R188, R190, R191, U17
8.	GPS Module not populated: C115, C118, C764, C765, J12, L22, L23, Q516, Q517, Q518, Q519, R186, R192, R194, R664, R668, R669, R671, R672, R673, U19
9.	Extra Bulk Capacitors not populated: C39, C54, C606, C607, C608, C609, C610, C611, C612, C673, C681
10.	BlueTooth Connector Isolation Resistors: R209, R210, R211, R212, R213, R214, R215

Build Option: MCIMX6QP-SDP IS NOT SUPPORTED

1.	CAN Output not populated: J10
2.	OverVoltage Protection circuit not populated: (OverVoltage Protection provided by battery charge ICs) D5, D500, D501, D502, D503, J501, Q1, Q6, Q503, R1, R2, R3, R303, R500, R505, R520, R524, SW3
3.	Extra Bulk Capacitors not populated: C39, C54, C68, C606, C607, C608, C609, C610, C611, C612, C673, C681
4.	BlueTooth Connector Isolation Resistors: R209, R210, R211, R212, R213, R214, R215

NXP

ICAP Classification: CP: ___ IUO: ___ PUBI: X

Drawing Title: MCIMX6QP-SMART DEVICE BOARD

Page Title: BUILD OPTON TABLES

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PIN MUX TABLES

Ball Name	Ball Number	IO MUX	Use
CSI0_DAT10	M1	ALT3	UART1_TXD_MUX
CSI0_DAT11	M3	ALT3	UART1_RXD_MUX
CSI0_DAT12	M2	ALT0	CSI0_D[12]
CSI0_DAT13	L1	ALT0	CSI0_D[13]
CSI0_DAT14	M4	ALT0	CSI0_D[14]
CSI0_DAT15	M5	ALT0	CSI0_D[15]
CSI0_DAT16	L4	ALT0	CSI0_D[16]
CSI0_DAT17	L3	ALT0	CSI0_D[17]
CSI0_DAT18	M6	ALT0	CSI0_D[18]
CSI0_DAT19	L6	ALT0	CSI0_D[19]
CSI0_DAT4	N1	ALT4	AUD3_TXC
CSI0_DAT5	P2	ALT4	AUD3_TXD
CSI0_DAT6	N4	ALT4	AUD3_TXFS
CSI0_DAT7	N3	ALT4	AUD3_RXD
CSI0_DAT8	N6	ALT4	I2C1_SDA
CSI0_DAT9	N5	ALT4	I2C2_SCL
CSI0_MCLK	P4	ALT0	CSI0_HSYNC
CSI0_PIXCLK	P1	ALT0	CSI0_PIXCLK
CSI0_VSYNC	N2	ALT0	CSI0_VSYNC
DI0_DISP_CLK	N19	ALT1	DI0_DISP_CLK
DI0_PIN15	N21	ALT1	DISP0_DRDT
DI0_PIN2	N25	ALT1	DISP0_HSYNCH
DI0_PIN3	N20	ALT1	DISP0_VSYNCH
DI0_PIN4	P25	ALT1	DISP0_CONTRST
DISP0_DAT0	P24	ALT1	DISP0_DAT[0]
DISP0_DAT1	P22	ALT1	DISP0_DAT[1]
DISP0_DAT10	R21	ALT1	DISP0_DAT[10]
DISP0_DAT11	T23	ALT1	DISP0_DAT[11]
DISP0_DAT12	T24	ALT1	DISP0_DAT[12]
DISP0_DAT13	R20	ALT1	DISP0_DAT[13]
DISP0_DAT14	U25	ALT1	DISP0_DAT[14]
DISP0_DAT15	T22	ALT1	DISP0_DAT[15]
DISP0_DAT16	T21	ALT1	DISP0_DAT[16]
DISP0_DAT17	U24	ALT1	DISP0_DAT[17]
DISP0_DAT18	V25	ALT1	DISP0_DAT[18]
DISP0_DAT19	U23	ALT1	DISP0_DAT[19]
DISP0_DAT2	P23	ALT1	DISP0_DAT[2]
DISP0_DAT20	U22	ALT1	DISP0_DAT[20]
DISP0_DAT21	T20	ALT1	DISP0_DAT[21]
DISP0_DAT22	V24	ALT1	DISP0_DAT[22]
DISP0_DAT23	W24	ALT1	DISP0_DAT[23]
DISP0_DAT3	P21	ALT1	DISP0_DAT[3]
DISP0_DAT4	P20	ALT1	DISP0_DAT[4]
DISP0_DAT5	R25	ALT1	DISP0_DAT[5]
DISP0_DAT6	R23	ALT1	DISP0_DAT[6]
DISP0_DAT7	R24	ALT1	DISP0_DAT[7]
DISP0_DAT8	R22	ALT1	DISP0_DAT[8]
DISP0_DAT9	T25	ALT1	DISP0_DAT[9]
EIM_D21	H20	ALT4	USB_OTG_OC
EIM_D22	E23	ALT4	USB_OTG_PWR_EN
EIM_D24	F22	ALT2	UART3_TXD_MUX
EIM_D25	G22	ALT2	UART3_RXD_MUX
EIM_D30	J20	ALT6	USB_H1_OC
ENET_MDC	V20	ALT1	MDC
ENET_MDIO	V23	ALT1	MDIO
ENET_REF_CLK	V22	ALT1	ENET_TX_CLK
ENET_RX_ER	W23	ALT0	USB_OTG_ID
GPIO_0	T5	ALT0	CLKO
GPIO_1	T4	ALT1	WDOG_B
GPIO_3	R7	ALT2	I2C3_SCL
GPIO_6	T3	ALT3	I2C3_SDA
GPIO_7	R3	ALT3	TXCAN
GPIO_8	R5	ALT3	RXCAN
GPIO_16	R2	ALT1	No-Connect
KEY_COL0	W5	ALT0	SCLK
KEY_COL1	U7	ALT0	MISO
KEY_COL3	U5	ALT4	I2C2_SCL
KEY_ROW0	V6	ALT0	CSPI1_MOSI
KEY_ROW1	U6	ALT0	CSPI1_SS0
KEY_ROW3	T7	ALT4	I2C2_SDA
KEY_ROW2	W4	ALT6	HDMI_CEC_IN

Ball Name	Ball Number	IO MUX	Use
NANDF_D4	A19	ALT1	SD2_DAT4
NANDF_D5	B18	ALT1	SD2_DAT5
NANDF_D6	E17	ALT1	SD2_DAT6
NANDF_D7	C18	ALT1	SD2_DAT7
RGMII_RD0	C24	ALT1	RGMII_RD0
RGMII_RD1	B23	ALT1	RGMII_RD1
RGMII_RD2	B24	ALT1	RGMII_RD2
RGMII_RD3	D23	ALT1	RGMII_RD3
RGMII_RX_CTL	D22	ALT1	RGMII_RX_CTL
RGMII_RXC	B25	ALT1	RGMII_RXC
RGMII_TD0	C22	ALT1	RGMII_TD0
RGMII_TD1	F20	ALT1	RGMII_TD1
RGMII_TD2	E21	ALT1	RGMII_TD2
RGMII_TD3	A24	ALT1	RGMII_TD3
RGMII_TX_CTL	C23	ALT1	RGMII_TX_CTL
RGMII_TXC	D21	ALT1	RGMII_TXC
SD1_DAT3	F18	ALT3	PWM0
SD2_CLK	C21	ALT0	SD2_CLK
SD2_CMD	F19	ALT0	SD2_CMD
SD2_DAT0	A22	ALT0	SD2_DAT0
SD2_DAT1	E20	ALT0	SD2_DAT1
SD2_DAT2	A23	ALT0	SD2_DAT2
SD2_DAT3	B22	ALT0	SD2_DAT3
SD3_CLK	D14	ALT0	SD3_CLK
SD3_CMD	B13	ALT0	SD3_CMD
SD3_DAT0	E14	ALT0	SD3_DAT0
SD3_DAT1	F14	ALT0	SD3_DAT1
SD3_DAT2	A15	ALT0	SD3_DAT2
SD3_DAT3	B15	ALT0	SD3_DAT3
SD3_DAT4	D13	ALT0	SD3_DAT4
SD3_DAT5	C13	ALT0	SD3_DAT5
SD3_DAT6	E13	ALT0	SD3_DAT6
SD3_DAT7	F13	ALT0	SD3_DAT7
SD4_CLK	E16	ALT0	SD4_CLK
SD4_CMD	B17	ALT0	SD4_CMD
SD4_DAT0	D18	ALT1	SD4_DAT0
SD4_DAT1	B19	ALT1	SD4_DAT1
SD4_DAT2	F17	ALT1	SD4_DAT2
SD4_DAT3	A20	ALT1	SD4_DAT3
SD4_DAT4	E18	ALT1	SD4_DAT4
SD4_DAT5	C19	ALT1	SD4_DAT5
SD4_DAT6	B20	ALT1	SD4_DAT6
SD4_DAT7	D19	ALT1	SD4_DAT7

Reserved For i.MX6DLS

NANDF_WP_B	E15	ALT5	DISP0_WR
EIM_RW	K20	ALT8	EPDC_SDDO7
EIM_LBA	K22	ALT8	EPDC_SDDO4
EIM_CS0	H24	ALT8	EPDC_SDDO6
EIM_EB1	K23	ALT8	EPDC_SDSHR
EIM_EB2	E22	ALT8	EPDC_SDDO5
EIM_A16	H25	ALT8	EPDC_SDDO0
EIM_A18	J22	ALT8	EPDC_PWRCTRL0
EIM_A21	H23	ALT8	EPDC_GDCLK
EIM_A22	F24	ALT8	EPDC_GDSP
EIM_A23	J21	ALT8	EPCD_GDOE
EIM_A24	F25	ALT8	EPDC_GDRL
EIM_D17	F21	ALT8	EPDC_VCOM0
EIM_D27	E25	ALT8	EPDC_SDOE
EIM_D31	H21	ALT8	EPDC_SDCLK
EIM_DA1	J25	ALT8	EPDC_SDLE
EIM_DA2	L21	ALT8	EPDC_BDR0
EIM_DA3	K24	ALT8	EPDC_BDR1
EIM_DA4	L22	ALT8	EPDC_SDCE0
EIM_DA5	L23	ALT8	EPDC_SDCE1
EIM_DA6	K25	ALT9	EPDC_SDCE2
EIM_DA10	M22	ALT8	EPDC_SDDO1
EIM_DA11	M20	ALT8	EPDC_SDDO3
EIM_DA12	M24	ALT8	EPDC_SDDO2

Ball Name	Ball Number	IO MUX	Use	GPIO Function	Direction	Active
SD1_CMD	B21	ALT5	GPIO1[18]	ACCL_INT_IN	Input	High
EIM_DA9	M21	ALT5	GPIO3[9]	ALS_INT	Input	High
NANDF_WP_B	E15	ALT5	GPIO6[9]	DISP0_WR	Output	High
NANDF_RB0	B16	ALT5	GPIO6[10]	AUX_5V_EN	Output	High
EIM_DA15	N24	ALT5	GPIO3[15]	BARO_INT	Input	High
NANDF_CS2	A17	ALT5	GPIO6[15]	CABC_EN0	Output	High
NANDF_CS3	D16	ALT5	GPIO6[16]	CABC_EN1	Output	High
GPIO_19	P5	ALT5	GPIO4[5]	CAN1_STBY	Output	High
NANDF_ALE	A16	ALT5	GPIO6[8]	CAP_TCH_INT0	Input	High
NANDF_CLE	C15	ALT5	GPIO6[7]	CAP_TCH_INT1	Input	High
EIM_A25	H19	ALT5	GPIO5[2]	CHG_FLT1_B	Input	Low
EIM_DA14	N23	ALT5	GPIO3[14]	CHG_FLT2_B	Input	Low
EIM_D23	D25	ALT5	GPIO3[23]	CHG_STATUS1_B	Input	Low
EIM_DA13	M23	ALT5	GPIO3[13]	CHG_STATUS2_B	Input	Low
KEY_COL2	W6	ALT5	GPIO4[10]	CODEC_PWR_EN	Output	High
EIM_D16	C25	ALT5	GPIO3[16]	COMP_INT	Input	High
SD1_DAT2	E19	ALT5	GPIO1[19]	CSI_PWN	Output	High
SD1_CLK	D20	ALT5	GPIO1[20]	CSI_RST_B	Output	High
SD1_DAT0	A21	ALT5	GPIO1[16]	CSI0_PWN	Output	High
SD1_DAT1	C20	ALT5	GPIO1[17]	CSI0_RST_B	Output	High
EIM_WAIT	M25	ALT5	GPIO5[0]	DI0_D0_CS	Output	High
EIM_BCLK	N22	ALT5	GPIO6[31]	DI0_D1_CS	Output	High
NANDF_CS1	C16	ALT5	GPIO6[14]	DISP0_PWR_EN	Output	High
EIM_D28	G23	ALT5	GPIO3[28]	DISP0_RD	Output	High
EIM_DA8	L24	ALT5	GPIO3[8]	DISP0_RST_B	Output	Low
NANDF_CS0	F15	ALT5	GPIO6[11]	DISP0_RST_B	Output	Low
EIM_CS1	J23	ALT5	GPIO2[24]	DOK_B	Input	Low
EIM_A17	G24	ALT5	GPIO2[21]	E_PMIC_GOOD_B	Input	Low
EIM_D20	G20	ALT5	GPIO3[20]	EPDC_PMIC_WAKEUP	Output	High
EIM_A19	G25	ALT5	GPIO2[19]	EPDC_PWRCTRL1	Output	High
EIM_A20	H22	ALT5	GPIO2[18]	EPDC_PWRCTRL2	Output	High
EIM_OE	J24	ALT5	GPIO2[25]	EPDC_PWRIRQ	Input	High
ENET_TX_EN	V21	ALT5	GPIO1[28]	ETH_WOL_INT	Input	High
EIM_D18	D24	ALT5	GPIO3[18]	GPS_PPS	Input	High
EIM_DA0	L20	ALT5	GPIO3[0]	GPS_PWREN	Output	High
EIM_EB0	K21	ALT5	GPIO2[28]	GPS_RESET_B	Output	Low
SD3_RST	D15	ALT5	GPIO7[8]	HEADPHONE_DET	Input	Low
GPIO_5	R4	ALT5	GPIO1[5]	KEY_VOL_DN	Input	Low
GPIO_4	R6	ALT5	GPIO1[4]	KEY_VOL_UP	Input	Low
KEY_COL4	T6	ALT5	GPIO4[14]	PCIE_DIS_B	Output	Low
GPIO_17	R1	ALT5	GPIO7[12]	PCIE_RST_B	Output	Low
EIM_D19	G21	ALT5	GPIO3[19]	PCIE_PWR_EN	Output	High
GPIO_18	P6	ALT5	GPIO7[13]	PMIC_INT_B	Input	Low
EIM_D29	J19	ALT5	GPIO3[29]	PWR_BTN_SNS	Input	High
ENET_CRS_DV	U21	ALT5	GPIO1[25]	RGMII_NRST	Output	High
NANDF_D2	F16	ALT5	GPIO2[2]	SD2_CD_B	Input	Low
NANDF_D3	D17	ALT5	GPIO2[3]	SD2_WP	Input	High
NANDF_D0	A18	ALT5	GPIO2[0]	SD3_CD_B	Input	Low
NANDF_D1	C17	ALT5	GPIO2[1]	SD3_WP	Input	High
EIM_EB3	F23	ALT5	GPIO2[31]	SENSOR_PWR_EN	Output	High
EIM_DA7	L25	ALT5	GPIO3[7]	KP_LOCK	Input	High
EIM_D26	E24	ALT5	GPIO3[26]	TS_INT	Input	High
ENET_RXD0	W21	ALT5	GPIO1[27]	UOK_B	Input	Low
ENET_RXD1	W22	ALT5	GPIO1[26]	RGMII_INT	Input	High
ENET_TXD0	U20	ALT5	GPIO1[30]	DISP0_WR	Output	High
ENET_TXD1	W20	ALT5	GPIO1[29]	USB_H1_PWR_EN	Output	High
GPIO_2	T1	ALT5	GPIO1[2]	USR_DEF_RED_LED	Output	High
GPIO_9	T2	ALT6	GPIO1[9]	MICROPHONE_DET	Input	Low
KEY_ROW4	V5	ALT5	GPIO4[15]	SATA_DEVSLP	Output	High
CSI0_DATA_EN	P3	ALT5	GPIO5[20]	PCIE_WAKE_B	Input	Low

I2C1 Bus (1.8V)

Peripheral	Bus Activity Level	Speed (kbps)	Addresses (hex)	Default Address (hex)
CSI Bus Camera	Low	400	Write: 0x78	Write: 0x78
Auido CODEC	Low	400	0x34, 0x36	0x34
MMA 8451Q Accelerometer	Low	400	0x3A, 0x39	0x39

I2C1_SDA = CSI0_DAT8
I2C1_SCL = CSI0_DAT9

I2C2 Bus (3.3V)

Peripheral	Bus Activity Level	Speed (kbps)	Addresses (hex)	Default Address (hex)
PF0100 PMIC	Low	400	0x08 - 0x0F	0x08
MIPI Bus Camera	Low	400	0x3C	0x3C
MIPI Bus Display	TBD	TBD	TBD	TBD
HDMI EDID	Low	100	0x50	0x50
LVDS0 EDID	Low	100	0x50	0x50
LVDS0 TOUCH SCREEN	High	400	0x82	0x82
RGB TFT LCD DISPLAY	TBD	TBD	TBD	TBD
LCD TOUCH SCREEN	Low	400	0x68, 0x69, 0x6A, 0x6B	0x68

I2C2_SDA = KEY_ROW3
I2C2_SCL = KEY_COL3

I2C3 Bus (3.3V)

Peripheral	Bus Activity Level	Speed (kbps)	Addresses (hex)	Default Address (hex)
LVDS1 EDID	Low	100	0x50	0x50
LVDS1 TOUCH SCREEN	High	400	0x82	0x82
PCIe EXP PORT	TBD	TBD	TBD	TBD
EPDC DISPLAY CARD	Low	400	0x68, 0x69, 0x6A, 0x6B	0x68
AMBIENT LIGHT SENSOR	Low	400	0x44	0x44
DIGITAL eCOMPASS	Low	400	0x0E	0x0E
BAROMETER	Low	400	0x60	0x60

I2C3_SDA = GPIO_16
I2C3_SCL = GPIO_3

NXP

ICAP Classification: CP: ___ IUO: ___ PUBI: X

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CHANGE REVISION DEFECT TRACKING

REV:	Change:	Reference Defect Number:

HISTORY OF TEMPORARY DEVIATIONS

TDA 5508

1. Change the following DNP to populate - R664, R668, Q516, Q518
2. Change following to DNP - R131
3. Change R15 from 1K to 10K

Revision History

Rev. Code	Date	Description
X1	04/03/2015 RM	Rev X1 Draft - Based on Agile 27516 revision C4, updated to support iMX6DQP power requirements, based on the F9 version of PF0100
X2	04/17/2015 RM	Sheet 2 - Removed VGEN_2V5 as alternate GEN_2V5 source Sheet 3 - Added test point to GPIO_16 Sheet 8 - Changed L17 to populate and L26 to DNP Sheet 9 - Changed DISP0 supply from VGEN5_2V5 to VGEN6_2V8 Sheet 13 - Changed from 20-pin to 10-pin JTAG connector, removed R611 on JTAG_TDO Sheet 15 - Swapped over BT UART RxD/TxD connections Sheet 20 - Removed optional SNVS LDO and associated components, changed R1 to 316K for 3.3V setting
X3	05/07/2015 RM	Mainly cosmetic changes and annotation of new parts Sheet 19 - VGEN1 and VGEN3 changed to test points from globals
X4	05/22/2015 RM	Synchronised design to current FCL status Sheet 5 - Updated U512 (eMMC) replacing EOL SanDisk part Sheet 15 - Changed J9 from 9-way D-type to 2x5 HDR to make room for larger SD connectors, removed alternate AUX SD card supply voltage (AUX_3V15) Sheet 16 - Changed PCIe clock source to external oscillator Sheet 18 - Removed CON3 to make room for larger SD connectors Sheet 20 - Fixed schematic error Q901 pin 5
X5	07/02/2015 DB	Sheet 1 - Update title block with new core number. Near top of sheet, corrected part number. Sheet 5 - eMMC was EOL; changed U512 to active device. Sheet 10 - Changed mics (U501, U521) and associated devices to DNP. Mics are EOL. Sheet 18 - Fixed broken connection on Q520 drain - DRC flag. Sheet 19 - Changed R31 from 10k to 47k for improved VIL (due to voltage divider action with R30. Sheet 19 - Corrected SNVS backup power net name on U8.43 -- changed from PMIC_SNVS to VSNVS_3V0.
A	07/10/2015 DB	Sheet 5 - Revised SPI NOR note. Sheet 13 - Revised JTAG adapter note. Sheet 26 - Revised PMIC note (brown text). Sheets 9, 17, 19, and 20 - Added note that AUX_3V15 is 3.3 V. Schematic sync'd with revised layout by CAD engineer. Released first-pass schematic.
A1	10/20/2015 GK	Updated U1 to correct part number and naming - QP MCIMX6QP6AVT1AA
A2	01/26/2016 RM	Cosmetic changes and corrections throughout to guidance notes, updated title blocks to NXP, changed classification to "Public Information" to support product launch, no electrical changes

Customized Programming Information

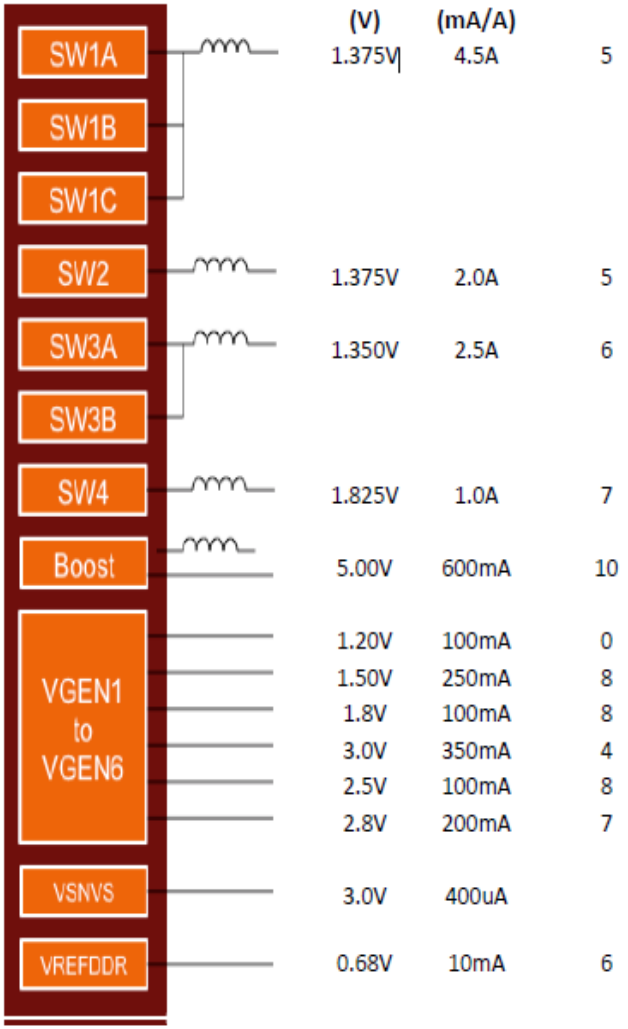
Orderable part number

SMPF0100F9AZES	Bulk
SMPF0100F9AZESR2	Tape and reel
Automotive AEC100-Grade 3	

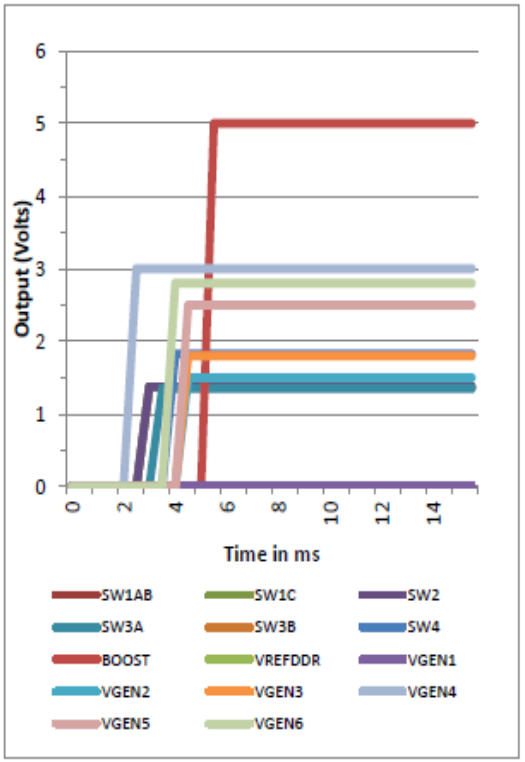
SMPF0100

MPU - ONLY

ES SUFFIX (WF-TYPE)
56 QFN 8x8
0.5MM PITCH



	VOUT (V)	IMAX (mA/A)	Sequence*
SW1A, SW1B, SW1C	1.375V	4.5A	5
SW2	1.375V	2.0A	5
SW3A, SW3B	1.350V	2.5A	6
SW4	1.825V	1.0A	7
Boost	5.00V	600mA	10
VGEN1 to VGEN6	1.20V	100mA	0
	1.50V	250mA	8
	1.8V	100mA	8
	3.0V	350mA	4
	2.5V	100mA	8
	2.8V	200mA	7
VSNVS	3.0V	400uA	
VREFDDR	0.68V	10mA	6



I2C address: 0x08
SWDVS_CLK: 25mV step each 4us
PWRON_CNF: Standard (High-ON, Low-Off)
PWRGD_EN: Standard RESETBMCU
SEQ_CLK_SPEED: 0.5ms
SWx_FREQ: 2MHz

PMIC Regulator	Voltage	Load
VSNVS	3.0	i.MX SNVS
SW1	1.375	i.MX SoC
SW2	1.375	i.MX ARM
SW3	1.35	DRAM
SW4	1.825	AUDIO, CAMERA, SENSORS, VGEN1/2
SWBST	5.0	USB VBUS
VGEN1	0	-
VGEN2	1.5	CAMERA, GPS, PCIe
VGEN3	1.8	-
VGEN4	3.0	i.MX VDDHIGH
VGEN5	2.5	GEN_3V3 ENABLE
VGEN6	2.8	CAMERA, PGOOD LED
VREFDDR	0.675	DRAM Vref

* Sequence 0 indicates regulator is off

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