DATA SHEET

旭曜科技
ORISE TECH

OTM3201A

QVGA 120-channel 8-bit Source Driver with System-on-chip for Color LTPS-TFT LCDs

Preliminary

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Version 0.3

Table of Contents

120-CHANNEL DRIVER WITH SYSTEM-ON-CHIP (SOC) FOR COLOR LTPS-TFT LCD

1. GENERAL DESCRIPTION

The OTM3201A, a 16.7M-color System-on-Chip (SoC) driver LSI designed for small and medium sizes of LTPS TFT LCD display, is capable of supporting up to 240xRGBx320, 240xRGBx400, 240xRGBx432, 320xRGBx320 ,and 320xRGBx240 in resolution. The 120-channel source driver for QVGA Portrait and 107-channel source driver for QVGA Landscpae have true 8-bit resolution, which generates 256 Gamma-corrected values by an internal D/A converter. The source driver of OTM3201A adopts OP-AMP structure to enhance display quality and it cooperates with advanced circuitry techniques to reduce power consumption.

The OTM3201A is able to operate with low IO interface power supply up to 1.6V and incorporate with DC/DC converter or PUMP to generate various voltage levels that form an on-chip power management system for gate driver and common driver.

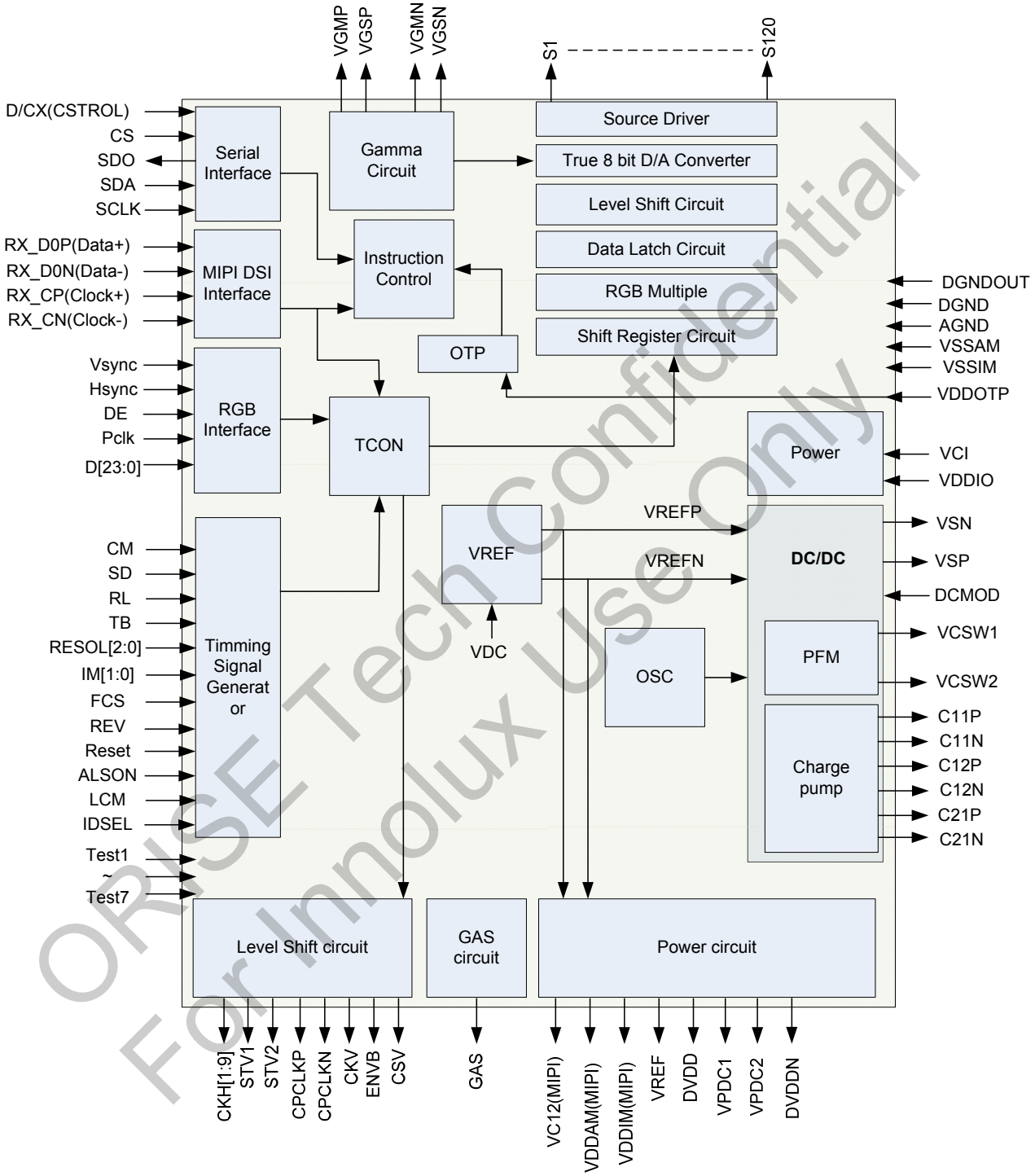
The built-in timing controller in OTM3201A can support several interfaces for the diverse request of medium or small size portable display. OTM3201A provides system interfaces, which include MIPI and 3&4 wire serial interface (SPI), to configure system. In addition, the OTM3201A incorporates 16, 18, and 24-bit RGB interfaces for picture movement display. The OTM3201A also supports standby mode and deep standby mdoe for power control consideration.

2. FEATURE

- **Single chip LTPS LCD driver.**
- **Reduced number of external components**
  - PFM: 16pcs for MIPI I/F, 13pcs for RGBI/F
  - Charge pump: 13pcs for MIPI I/F, 10pcs for RGBI/F
  - Cap free regulators
- **Resolution**
  - QVGA Portrait (240x320)
  - WQVGA Portrait(240x400 and 240x432)
  - QVGA Landscape(320x240, 320x320)
- **Graphics**
  - 1:6 mux for Portrait
    Full color mode 16M colors 24 bit 8R:8G:8B
  - 1:9 mux for Landscape
    Full color mode 16M colors 24 bit 8R:8G:8B
  - Reduced color mode:
    262k colors (18bit 6(R):6(G):6(B))
    65k colors (16bit 5(R):6(G):5(B))
    Saturated 8 color mode
  - Sleep mode
- **Outputs**
  - 120 source outputs portrait
  - 107 source outputs landscape
  - Control signals for on glass DC/DC converter to generate Gate voltages and supply for the on glass level shifters
- **Driving algorithm**
  - DC common drive
  - Dot inversion、1+2 Dot inversion、Column inversion
  - Dancing multiplex drive, same color
  - 24 bit color depth
- **Display features**
  - 3 kind of gamma curve and independent of RGB curve
  - Support normally white and normally black display type
  - Non-Volatile White Point Adjustment
- **Interface**
  - MIPI DSI (1 Data Lane): MIPI DSI (DSI v1.01.00, D-PHY v1.00.00 and DCS v1.01).
  - RGB/SPI System Interface.
    18bits, 24 bits RGB, serial RGB.
- **On chip**
  - Dual DC/DC mode: PFM and Charge pump.
  - Controlling signals and supply for the on-glass DC/DC to generate gate signals
  - Temp Sensor: A/D (6-bits, +/- 2°C)
    (-40~85°C)
  - OTP memory
- **Input power supply**
  - Logic supply voltage range VDDIO to VSS: 1.6V to 3.6V
  - Booster supply voltage range VCI to VSS: 2.3 V to 3.6 V
- **Output voltage levels**
  - Source Booster output +/- 6.5V max (0,175mV step)
  - Source output +/- 6.2V
  - For on-glass DC/DC VPDC1: 2.2~5V VPDC2: 1V~VCI-0.2 step 0.2V
  - Power clock for on-glass DC/DC and level shifters 0V to VSP
  - All control signals to the glass: 0V to VSP
- **Separate selectable registers in OTP for Normal and Idle mode**
  - Positive/Negative source booster output
  - Positive/Negative source voltage
  - DC/DC clock(CP fix 1~4frame)
  - Normally black and white selection(by hardware pin)

3. BLOCK DIAGRAM

3.1. Block Function



3.1.1. Grayscale Voltage Generating Circuit

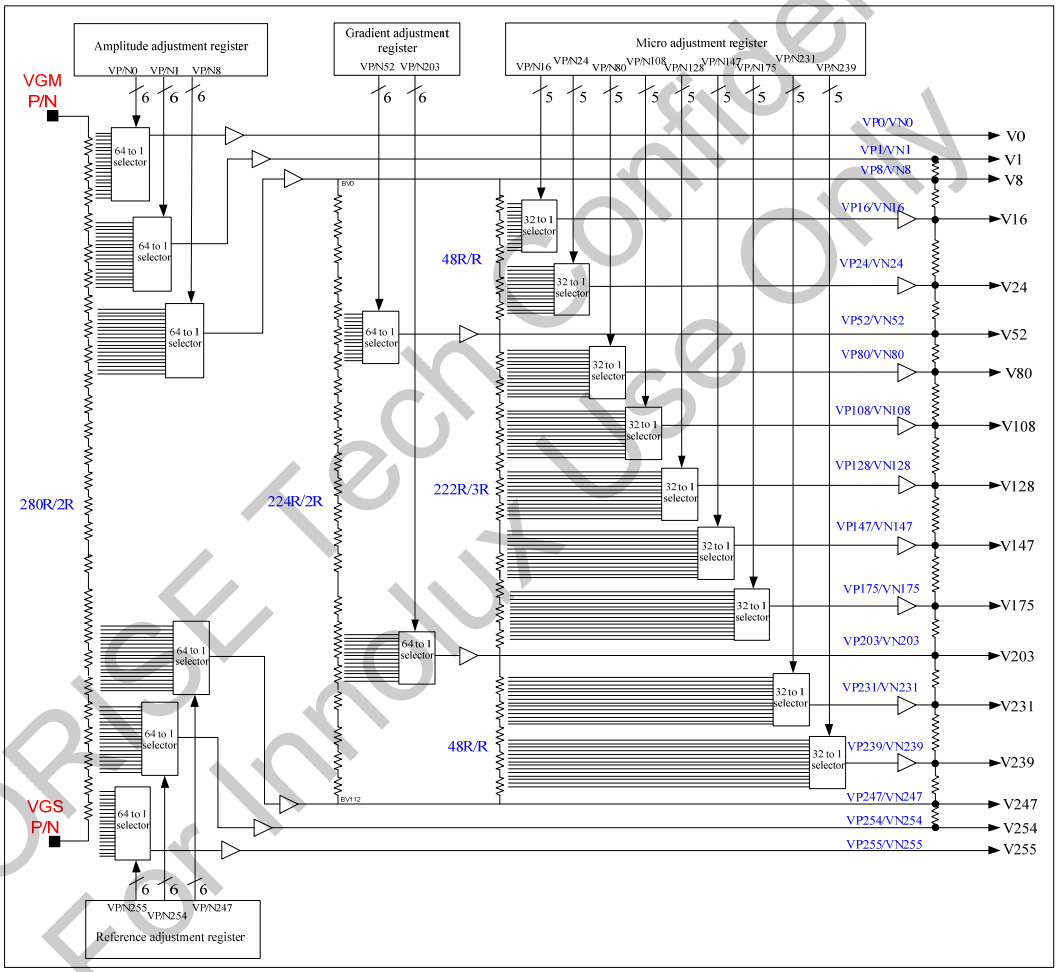
OTM3201A has true 8-bit resolution D/A converter, which generates 256 Gamma-corrected values and cooperates with OP-AMP structure to enhance display quality. The grayscale voltage can be adjusted by grayscale data set in the γ-correction register. For details, see the "γ-Correction Function" section.

3.1.2. Timing Controller

OTM3201A has a timing controller which can generate a timing signal for internal circuit operation such as source output timing.

3.1.3. Gamma

The structure of grayscale amplifier is shown as below. The 17 voltage levels (VIN0-VIN16) between VGMP/N and VGSP/N are determined by the gradient adjustment register. the reference adjustment register, the amplitude adjustment resister and the micro-adjustment register.



Gamma adjusting voltage formula

Table 3.1.3.1. Amplitude(V0,1,8) & Reference(V247,254,255) Adjustment

Formula: Voltage = **(RES/280R)*(VGMP(N)-VGSP(N))+VGSP(N)**

VP(N)0			VP(N)1			VP(N)8			VP(N)247			VP(N)254			VP(N)255		
VP(N)0 [5:0]	Selected voltage VP(N)0	Resistor (RES)	VP(N)1 [5:0]	Selected voltage VP(N)1	Resistor (RES)	VP(N)8 [5:0]	Selected voltage VP(N)8	Resistor (RES)	VP(N)247 [5:0]	Selected voltage VP(N)247	Resistor (RES)	VP(N)254 [5:0]	Selected voltage VP(N)254	Resistor (RES)	VP(N)255 [5:0]	Selected voltage VP(N)255	Resistor (RES)
0	AVP(N)0	280	0	AVP(N)2	276	0	AVP(N)5	270	0	AVP(N)72	136	0	AVP(N)75	130	0	AVP(N)77	126
1	AVP(N)1	278	1	AVP(N)3	274	1	AVP(N)6	268	1	AVP(N)73	134	1	AVP(N)76	128	1	AVP(N)78	124
2	AVP(N)2	276	2	AVP(N)4	272	2	AVP(N)7	266	2	AVP(N)74	132	2	AVP(N)77	126	2	AVP(N)79	122
3	AVP(N)3	274	3	AVP(N)5	270	3	AVP(N)8	264	3	AVP(N)75	130	3	AVP(N)78	124	3	AVP(N)80	120
4	AVP(N)4	272	4	AVP(N)6	268	4	AVP(N)9	262	4	AVP(N)76	128	4	AVP(N)79	122	4	AVP(N)81	118
5	AVP(N)5	270	5	AVP(N)7	266	5	AVP(N)10	260	5	AVP(N)77	126	5	AVP(N)80	120	5	AVP(N)82	116
6	AVP(N)6	268	6	AVP(N)8	264	6	AVP(N)11	258	6	AVP(N)78	124	6	AVP(N)81	118	6	AVP(N)83	114
7	AVP(N)7	266	7	AVP(N)9	262	7	AVP(N)12	256	7	AVP(N)79	122	7	AVP(N)82	116	7	AVP(N)84	112
8	AVP(N)8	264	8	AVP(N)10	260	8	AVP(N)13	254	8	AVP(N)80	120	8	AVP(N)83	114	8	AVP(N)85	110
9	AVP(N)9	262	9	AVP(N)11	258	9	AVP(N)14	252	9	AVP(N)81	118	9	AVP(N)84	112	9	AVP(N)86	108
10	AVP(N)10	260	10	AVP(N)12	256	10	AVP(N)15	250	10	AVP(N)82	116	10	AVP(N)85	110	10	AVP(N)87	106
11	AVP(N)11	258	11	AVP(N)13	254	11	AVP(N)16	248	11	AVP(N)83	114	11	AVP(N)86	108	11	AVP(N)88	104
12	AVP(N)12	256	12	AVP(N)14	252	12	AVP(N)17	246	12	AVP(N)84	112	12	AVP(N)87	106	12	AVP(N)89	102
13	AVP(N)13	254	13	AVP(N)15	250	13	AVP(N)18	244	13	AVP(N)85	110	13	AVP(N)88	104	13	AVP(N)90	100
14	AVP(N)14	252	14	AVP(N)16	248	14	AVP(N)19	242	14	AVP(N)86	108	14	AVP(N)89	102	14	AVP(N)91	98
15	AVP(N)15	250	15	AVP(N)17	246	15	AVP(N)20	240	15	AVP(N)87	106	15	AVP(N)90	100	15	AVP(N)92	96
16	AVP(N)16	248	16	AVP(N)18	244	16	AVP(N)21	238	16	AVP(N)88	104	16	AVP(N)91	98	16	AVP(N)93	94
17	AVP(N)17	246	17	AVP(N)19	242	17	AVP(N)22	236	17	AVP(N)89	102	17	AVP(N)92	96	17	AVP(N)94	92
18	AVP(N)18	244	18	AVP(N)20	240	18	AVP(N)23	234	18	AVP(N)90	100	18	AVP(N)93	94	18	AVP(N)95	90
19	AVP(N)19	242	19	AVP(N)21	238	19	AVP(N)24	232	19	AVP(N)91	98	19	AVP(N)94	92	19	AVP(N)96	88
20	AVP(N)20	240	20	AVP(N)22	236	20	AVP(N)25	230	20	AVP(N)92	96	20	AVP(N)95	90	20	AVP(N)97	86
21	AVP(N)21	238	21	AVP(N)23	234	21	AVP(N)26	228	21	AVP(N)93	94	21	AVP(N)96	88	21	AVP(N)98	84
22	AVP(N)22	236	22	AVP(N)24	232	22	AVP(N)27	226	22	AVP(N)94	92	22	AVP(N)97	86	22	AVP(N)99	82
23	AVP(N)23	234	23	AVP(N)25	230	23	AVP(N)28	224	23	AVP(N)95	90	23	AVP(N)98	84	23	AVP(N)100	80
24	AVP(N)24	232	24	AVP(N)26	228	24	AVP(N)29	222	24	AVP(N)96	88	24	AVP(N)99	82	24	AVP(N)101	78
25	AVP(N)25	230	25	AVP(N)27	226	25	AVP(N)30	220	25	AVP(N)97	86	25	AVP(N)100	80	25	AVP(N)102	76
26	AVP(N)26	228	26	AVP(N)28	224	26	AVP(N)31	218	26	AVP(N)98	84	26	AVP(N)101	78	26	AVP(N)103	74
27	AVP(N)27	226	27	AVP(N)29	222	27	AVP(N)32	216	27	AVP(N)99	82	27	AVP(N)102	76	27	AVP(N)104	72
28	AVP(N)28	224	28	AVP(N)30	220	28	AVP(N)33	214	28	AVP(N)100	80	28	AVP(N)103	74	28	AVP(N)105	70
29	AVP(N)29	222	29	AVP(N)31	218	29	AVP(N)34	212	29	AVP(N)101	78	29	AVP(N)104	72	29	AVP(N)106	68
30	AVP(N)30	220	30	AVP(N)32	216	30	AVP(N)35	210	30	AVP(N)102	76	30	AVP(N)105	70	30	AVP(N)107	66
31	AVP(N)31	218	31	AVP(N)33	214	31	AVP(N)36	208	31	AVP(N)103	74	31	AVP(N)106	68	31	AVP(N)108	64
32	AVP(N)32	216	32	AVP(N)34	212	32	AVP(N)37	206	32	AVP(N)104	72	32	AVP(N)107	66	32	AVP(N)109	62
33	AVP(N)33	214	33	AVP(N)35	210	33	AVP(N)38	204	33	AVP(N)105	70	33	AVP(N)108	64	33	AVP(N)110	60
34	AVP(N)34	212	34	AVP(N)36	208	34	AVP(N)39	202	34	AVP(N)106	68	34	AVP(N)109	62	34	AVP(N)111	58
35	AVP(N)35	210	35	AVP(N)37	206	35	AVP(N)40	200	35	AVP(N)107	66	35	AVP(N)110	60	35	AVP(N)112	56
36	AVP(N)36	208	36	AVP(N)38	204	36	AVP(N)41	198	36	AVP(N)108	64	36	AVP(N)111	58	36	AVP(N)113	54
37	AVP(N)37	206	37	AVP(N)39	202	37	AVP(N)42	196	37	AVP(N)109	62	37	AVP(N)112	56	37	AVP(N)114	52
38	AVP(N)38	204	38	AVP(N)40	200	38	AVP(N)43	194	38	AVP(N)110	60	38	AVP(N)113	54	38	AVP(N)115	50

VP(N)0			VP(N)1			VP(N)8			VP(N)247			VP(N)254			VP(N)255		
VP(N)0 [5:0]	Selected voltage VP(N)0	Resistor (RES)	VP(N)1 [5:0]	Selected voltage VP(N)1	Resistor (RES)	VP(N)8 [5:0]	Selected voltage VP(N)8	Resistor (RES)	VP(N)247 [5:0]	Selected voltage VP(N)247	Resistor (RES)	VP(N)254 [5:0]	Selected voltage VP(N)254	Resistor (RES)	VP(N)255 [5:0]	Selected voltage VP(N)255	Resistor (RES)
39	AVP(N)39	202	39	AVP(N)41	198	39	AVP(N)44	192	39	AVP(N)111	58	39	AVP(N)114	52	39	AVP(N)116	48
40	AVP(N)40	200	40	AVP(N)42	196	40	AVP(N)45	190	40	AVP(N)112	56	40	AVP(N)115	50	40	AVP(N)117	46
41	AVP(N)41	198	41	AVP(N)43	194	41	AVP(N)46	188	41	AVP(N)113	54	41	AVP(N)116	48	41	AVP(N)118	44
42	AVP(N)42	196	42	AVP(N)44	192	42	AVP(N)47	186	42	AVP(N)114	52	42	AVP(N)117	46	42	AVP(N)119	42
43	AVP(N)43	194	43	AVP(N)45	190	43	AVP(N)48	184	43	AVP(N)115	50	43	AVP(N)118	44	43	AVP(N)120	40
44	AVP(N)44	192	44	AVP(N)46	188	44	AVP(N)49	182	44	AVP(N)116	48	44	AVP(N)119	42	44	AVP(N)121	38
45	AVP(N)45	190	45	AVP(N)47	186	45	AVP(N)50	180	45	AVP(N)117	46	45	AVP(N)120	40	45	AVP(N)122	36
46	AVP(N)46	188	46	AVP(N)48	184	46	AVP(N)51	178	46	AVP(N)118	44	46	AVP(N)121	38	46	AVP(N)123	34
47	AVP(N)47	186	47	AVP(N)49	182	47	AVP(N)52	176	47	AVP(N)119	42	47	AVP(N)122	36	47	AVP(N)124	32
48	AVP(N)48	184	48	AVP(N)50	180	48	AVP(N)53	174	48	AVP(N)120	40	48	AVP(N)123	34	48	AVP(N)125	30
49	AVP(N)49	182	49	AVP(N)51	178	49	AVP(N)54	172	49	AVP(N)121	38	49	AVP(N)124	32	49	AVP(N)126	28
50	AVP(N)50	180	50	AVP(N)52	176	50	AVP(N)55	170	50	AVP(N)122	36	50	AVP(N)125	30	50	AVP(N)127	26
51	AVP(N)51	178	51	AVP(N)53	174	51	AVP(N)56	168	51	AVP(N)123	34	51	AVP(N)126	28	51	AVP(N)128	24
52	AVP(N)52	176	52	AVP(N)54	172	52	AVP(N)57	166	52	AVP(N)124	32	52	AVP(N)127	26	52	AVP(N)129	22
53	AVP(N)53	174	53	AVP(N)55	170	53	AVP(N)58	164	53	AVP(N)125	30	53	AVP(N)128	24	53	AVP(N)130	20
54	AVP(N)54	172	54	AVP(N)56	168	54	AVP(N)59	162	54	AVP(N)126	28	54	AVP(N)129	22	54	AVP(N)131	18
55	AVP(N)55	170	55	AVP(N)57	166	55	AVP(N)60	160	55	AVP(N)127	26	55	AVP(N)130	20	55	AVP(N)132	16
56	AVP(N)56	168	56	AVP(N)58	164	56	AVP(N)61	158	56	AVP(N)128	24	56	AVP(N)131	18	56	AVP(N)133	14
57	AVP(N)57	166	57	AVP(N)59	162	57	AVP(N)62	156	57	AVP(N)129	22	57	AVP(N)132	16	57	AVP(N)134	12
58	AVP(N)58	164	58	AVP(N)60	160	58	AVP(N)63	154	58	AVP(N)130	20	58	AVP(N)133	14	58	AVP(N)135	10
59	AVP(N)59	162	59	AVP(N)61	158	59	AVP(N)64	152	59	AVP(N)131	18	59	AVP(N)134	12	59	AVP(N)136	8
60	AVP(N)60	160	60	AVP(N)62	156	60	AVP(N)65	150	60	AVP(N)132	16	60	AVP(N)135	10	60	AVP(N)137	6
61	AVP(N)61	158	61	AVP(N)63	154	61	AVP(N)66	148	61	AVP(N)133	14	61	AVP(N)136	8	61	AVP(N)138	4
62	AVP(N)62	156	62	AVP(N)64	152	62	AVP(N)67	146	62	AVP(N)134	12	62	AVP(N)137	6	62	AVP(N)139	2
63	AVP(N)63	154	63	AVP(N)65	150	63	AVP(N)68	144	63	AVP(N)135	10	63	AVP(N)138	4	63	AVP(N)140	0

Table 3.1.3.2. Gradient Adjustment

Formula: Voltage = **(RES/224R)*(VP(N)8-VP(N)247)+VP(N)247**

VP(N)52		
VP(N)52 [5:0]	Selected voltage VP(N)52	Resistor (RES)
0	GVP(N)0	224
1	GVP(N)1	222
2	GVP(N)2	220
3	GVP(N)3	218
4	GVP(N)4	216
5	GVP(N)5	214
6	GVP(N)6	212
7	GVP(N)7	210
8	GVP(N)8	208
9	GVP(N)9	206
10	GVP(N)10	204
11	GVP(N)11	202
12	GVP(N)12	200
13	GVP(N)13	198
14	GVP(N)14	196
15	GVP(N)15	194
16	GVP(N)16	192
17	GVP(N)17	190
18	GVP(N)18	188
19	GVP(N)19	186
20	GVP(N)20	184
21	GVP(N)21	182
22	GVP(N)22	180
23	GVP(N)23	178
24	GVP(N)24	176
25	GVP(N)25	174
26	GVP(N)26	172
27	GVP(N)27	170
28	GVP(N)28	168
29	GVP(N)29	166
30	GVP(N)30	164
31	GVP(N)31	162
32	GVP(N)32	160
33	GVP(N)33	158
34	GVP(N)34	156
35	GVP(N)35	154
36	GVP(N)36	152
37	GVP(N)37	150
38	GVP(N)38	148
39	GVP(N)39	146
40	GVP(N)40	144
41	GVP(N)41	142
42	GVP(N)42	140

VP(N)203		
VP(N)203 [5:0]	Selected voltage VP(N)203	Resistor (RES)
0	GVP(N)64	148
1	GVP(N)65	146
2	GVP(N)66	144
3	GVP(N)67	142
4	GVP(N)68	140
5	GVP(N)69	138
6	GVP(N)70	136
7	GVP(N)71	134
8	GVP(N)72	132
9	GVP(N)73	130
10	GVP(N)74	128
11	GVP(N)75	126
12	GVP(N)76	124
13	GVP(N)77	122
14	GVP(N)78	120
15	GVP(N)79	118
16	GVP(N)80	116
17	GVP(N)81	114
18	GVP(N)82	112
19	GVP(N)83	110
20	GVP(N)84	108
21	GVP(N)85	106
22	GVP(N)86	104
23	GVP(N)87	102
24	GVP(N)88	100
25	GVP(N)89	98
26	GVP(N)90	96
27	GVP(N)91	94
28	GVP(N)92	92
29	GVP(N)93	90
30	GVP(N)94	88
31	GVP(N)95	86
32	GVP(N)96	84
33	GVP(N)97	82
34	GVP(N)98	80
35	GVP(N)99	78
36	GVP(N)100	76
37	GVP(N)101	74
38	GVP(N)102	72
39	GVP(N)103	70
40	GVP(N)104	68
41	GVP(N)105	66
42	GVP(N)106	64

VP(N)52		
VP(N)52 [5:0]	Selected voltage VP(N)52	Resistor (RES)
43	GVP(N)43	138
44	GVP(N)44	136
45	GVP(N)45	134
46	GVP(N)46	132
47	GVP(N)47	130
48	GVP(N)48	128
49	GVP(N)49	126
50	GVP(N)50	124
51	GVP(N)51	122
52	GVP(N)52	120
53	GVP(N)53	118
54	GVP(N)54	116
55	GVP(N)55	114
56	GVP(N)56	112
57	GVP(N)57	110
58	GVP(N)58	108
59	GVP(N)59	106
60	GVP(N)60	104
61	GVP(N)61	102
62	GVP(N)62	100
63	GVP(N)63	98

VP(N)203		
VP(N)203 [5:0]	Selected voltage VP(N)203	Resistor (RES)
43	GVP(N)107	62
44	GVP(N)108	60
45	GVP(N)109	58
46	GVP(N)110	56
47	GVP(N)111	54
48	GVP(N)112	52
49	GVP(N)113	50
50	GVP(N)114	48
51	GVP(N)115	46
52	GVP(N)116	44
53	GVP(N)117	42
54	GVP(N)118	40
55	GVP(N)119	38
56	GVP(N)120	36
57	GVP(N)121	34
58	GVP(N)122	32
59	GVP(N)123	30
60	GVP(N)124	28
61	GVP(N)125	26
62	GVP(N)126	24
63	GVP(N)127	22

Table 3.1.3.3. Micro Adjustment

V=(RES/48R)*(VP(N)8-VP(N)52)+VP(N)52						V=(RES/222R)*(VP(N)52-VP(N)203)+VP(N)203								
VP(N)16			**VP(N)24**			**VP(N)80**			**VP(N)108**			**VP(N)128**		
VP(N)16 [5:0]	Selected voltage VP(N)16	Resistor (RES)	VP(N)24 [5:0]	Selected voltage VP(N)24	Resistor (RES)	VP(N)80 [5:0]	Selected voltage VP(N)80	Resistor (RES)	VP(N)108 [5:0]	Selected voltage VP(N)108	Resistor (RES)	VP(N)128 [5:0]	Selected voltage VP(N)128	Resistor (RES)
0	MVP(N)0	**16**	0	MVP(N)32	**1**	0	MVP(N)64	**126**	0	MVP(N)96	**87**	0	MVP(N)128	**66**
1	MVP(N)1	**17**	1	MVP(N)33	**2**	1	MVP(N)65	**129**	1	MVP(N)97	**90**	1	MVP(N)129	**69**
2	MVP(N)2	**18**	2	MVP(N)34	**3**	2	MVP(N)66	**132**	2	MVP(N)98	**93**	2	MVP(N)130	**72**
3	MVP(N)3	**19**	3	MVP(N)35	**4**	3	MVP(N)67	**135**	3	MVP(N)99	**96**	3	MVP(N)131	**75**
4	MVP(N)4	**20**	4	MVP(N)36	**5**	4	MVP(N)68	**138**	4	MVP(N)100	**99**	4	MVP(N)132	**78**
5	MVP(N)5	**21**	5	MVP(N)37	**6**	5	MVP(N)69	**141**	5	MVP(N)101	**102**	5	MVP(N)133	**81**
6	MVP(N)6	**22**	6	MVP(N)38	**7**	6	MVP(N)70	**144**	6	MVP(N)102	**105**	6	MVP(N)134	**84**
7	MVP(N)7	**23**	7	MVP(N)39	**8**	7	MVP(N)71	**147**	7	MVP(N)103	**108**	7	MVP(N)135	**87**
8	MVP(N)8	**24**	8	MVP(N)40	**9**	8	MVP(N)72	**150**	8	MVP(N)104	**111**	8	MVP(N)136	**90**
9	MVP(N)9	**25**	9	MVP(N)41	**10**	9	MVP(N)73	**153**	9	MVP(N)105	**114**	9	MVP(N)137	**93**
10	MVP(N)10	**26**	10	MVP(N)42	**11**	10	MVP(N)74	**156**	10	MVP(N)106	**117**	10	MVP(N)138	**96**
11	MVP(N)11	**27**	11	MVP(N)43	**12**	11	MVP(N)75	**159**	11	MVP(N)107	**120**	11	MVP(N)139	**99**
12	MVP(N)12	**28**	12	MVP(N)44	**13**	12	MVP(N)76	**162**	12	MVP(N)108	**123**	12	MVP(N)140	**102**
13	MVP(N)13	**29**	13	MVP(N)45	**14**	13	MVP(N)77	**165**	13	MVP(N)109	**126**	13	MVP(N)141	**105**
14	MVP(N)14	**30**	14	MVP(N)46	**15**	14	MVP(N)78	**168**	14	MVP(N)110	**129**	14	MVP(N)142	**108**
15	MVP(N)15	**31**	15	MVP(N)47	**16**	15	MVP(N)79	**171**	15	MVP(N)111	**132**	15	MVP(N)143	**111**
16	MVP(N)16	**32**	16	MVP(N)48	**17**	16	MVP(N)80	**174**	16	MVP(N)112	**135**	16	MVP(N)144	**114**
17	MVP(N)17	**33**	17	MVP(N)49	**18**	17	MVP(N)81	**177**	17	MVP(N)113	**138**	17	MVP(N)145	**117**
18	MVP(N)18	**34**	18	MVP(N)50	**19**	18	MVP(N)82	**180**	18	MVP(N)114	**141**	18	MVP(N)146	**120**
19	MVP(N)19	**35**	19	MVP(N)51	**20**	19	MVP(N)83	**183**	19	MVP(N)115	**144**	19	MVP(N)147	**123**
20	MVP(N)20	**36**	20	MVP(N)52	**21**	20	MVP(N)84	**186**	20	MVP(N)116	**147**	20	MVP(N)148	**126**
21	MVP(N)21	**37**	21	MVP(N)53	**22**	21	MVP(N)85	**189**	21	MVP(N)117	**150**	21	MVP(N)149	**129**
22	MVP(N)22	**38**	22	MVP(N)54	**23**	22	MVP(N)86	**192**	22	MVP(N)118	**153**	22	MVP(N)150	**132**
23	MVP(N)23	**39**	23	MVP(N)55	**24**	23	MVP(N)87	**195**	23	MVP(N)119	**156**	23	MVP(N)151	**135**
24	MVP(N)24	**40**	24	MVP(N)56	**25**	24	MVP(N)88	**198**	24	MVP(N)120	**159**	24	MVP(N)152	**138**
25	MVP(N)25	**41**	25	MVP(N)57	**26**	25	MVP(N)89	**201**	25	MVP(N)121	**162**	25	MVP(N)153	**141**
26	MVP(N)26	**42**	26	MVP(N)58	**27**	26	MVP(N)90	**204**	26	MVP(N)122	**165**	26	MVP(N)154	**144**
27	MVP(N)27	**43**	27	MVP(N)59	**28**	27	MVP(N)91	**207**	27	MVP(N)123	**168**	27	MVP(N)155	**147**
28	MVP(N)28	**44**	28	MVP(N)60	**29**	28	MVP(N)92	**210**	28	MVP(N)124	**171**	28	MVP(N)156	**150**
29	MVP(N)29	**45**	29	MVP(N)61	**30**	29	MVP(N)93	**213**	29	MVP(N)125	**174**	29	MVP(N)157	**153**
30	MVP(N)30	**46**	30	MVP(N)62	**31**	30	MVP(N)94	**216**	30	MVP(N)126	**177**	30	MVP(N)158	**156**
31	MVP(N)31	**47**	31	MVP(N)63	**32**	31	MVP(N)95	**219**	31	MVP(N)127	**180**	31	MVP(N)159	**159**

V=(RES/222R)*(VP(N)52-VP(N)203)+VP(N)203

VP(N)147			VP(N)175		
VP(N)147 [5:0]	Selected voltage VP(N)147	Resistor (RES)	VP(N)175 [5:0]	Selected voltage VP(N)175	Resistor (RES)
0	MVP(N)160	30	0	MVP(N)192	3
1	MVP(N)161	33	1	MVP(N)193	6
2	MVP(N)162	36	2	MVP(N)194	9
3	MVP(N)163	39	3	MVP(N)195	12
4	MVP(N)164	42	4	MVP(N)196	15
5	MVP(N)165	45	5	MVP(N)197	18
6	MVP(N)166	48	6	MVP(N)198	21
7	MVP(N)167	51	7	MVP(N)199	24
8	MVP(N)168	54	8	MVP(N)200	27
9	MVP(N)169	57	9	MVP(N)201	30
10	MVP(N)170	60	10	MVP(N)202	33
11	MVP(N)171	63	11	MVP(N)203	36
12	MVP(N)172	66	12	MVP(N)204	39
13	MVP(N)173	69	13	MVP(N)205	42
14	MVP(N)174	72	14	MVP(N)206	45
15	MVP(N)175	75	15	MVP(N)207	48
16	MVP(N)176	78	16	MVP(N)208	51
17	MVP(N)177	81	17	MVP(N)209	54
18	MVP(N)178	84	18	MVP(N)210	57
19	MVP(N)179	87	19	MVP(N)211	60
20	MVP(N)180	90	20	MVP(N)212	63
21	MVP(N)181	93	21	MVP(N)213	66
22	MVP(N)182	96	22	MVP(N)214	69
23	MVP(N)183	99	23	MVP(N)215	72
24	MVP(N)184	102	24	MVP(N)216	75
25	MVP(N)185	105	25	MVP(N)217	78
26	MVP(N)186	108	26	MVP(N)218	81
27	MVP(N)187	111	27	MVP(N)219	84
28	MVP(N)188	114	28	MVP(N)220	87
29	MVP(N)189	117	29	MVP(N)221	90
30	MVP(N)190	120	30	MVP(N)222	93
31	MVP(N)191	123	31	MVP(N)223	96

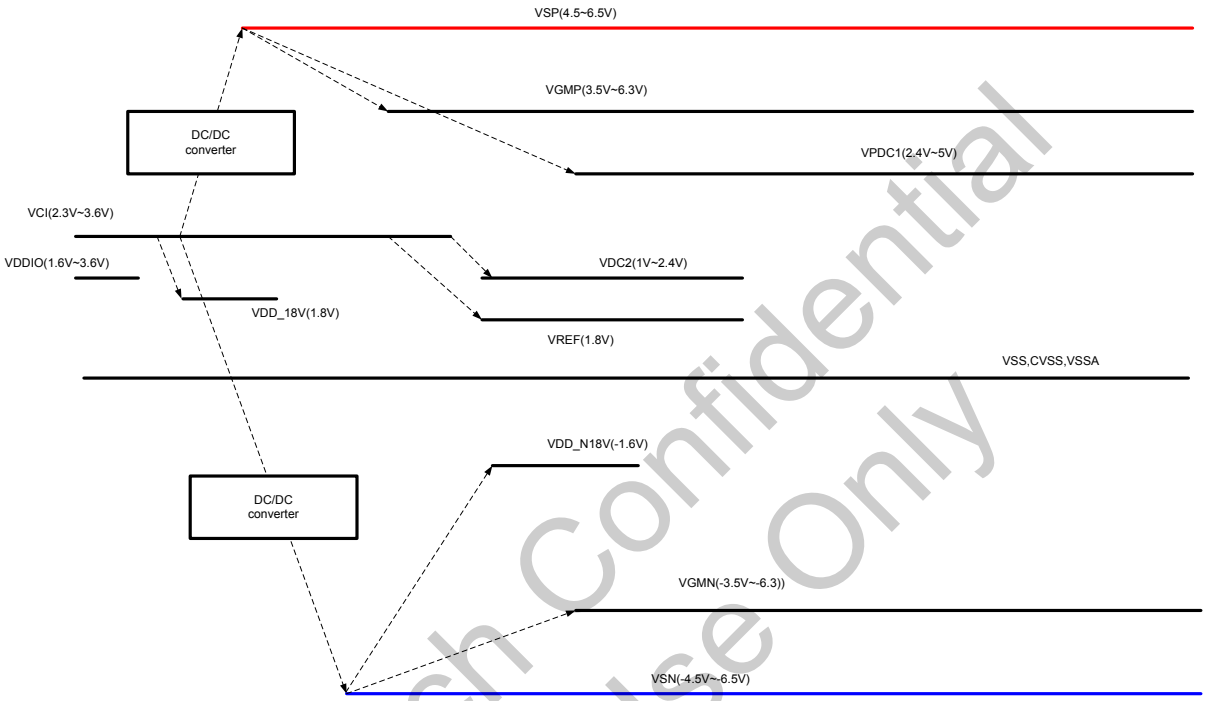
V=(RES/48R)*(VP(N)203-VP(N)247)+VP(N)247

VP(N)231			VP(N)239		
VP(N)231 [5:0]	Selected voltage VP(N)231	Resistor (RES)	VP(N)239 [5:0]	Selected voltage VP(N)239	Resistor (RES)
0	MVP(N)224	16	0	MVP(N)256	1
1	MVP(N)225	17	1	MVP(N)257	2
2	MVP(N)226	18	2	MVP(N)258	3
3	MVP(N)227	19	3	MVP(N)259	4
4	MVP(N)228	20	4	MVP(N)260	5
5	MVP(N)229	21	5	MVP(N)261	6
6	MVP(N)230	22	6	MVP(N)262	7
7	MVP(N)231	23	7	MVP(N)263	8
8	MVP(N)232	24	8	MVP(N)264	9
9	MVP(N)233	25	9	MVP(N)265	10
10	MVP(N)234	26	10	MVP(N)266	11
11	MVP(N)235	27	11	MVP(N)267	12
12	MVP(N)236	28	12	MVP(N)268	13
13	MVP(N)237	29	13	MVP(N)269	14
14	MVP(N)238	30	14	MVP(N)270	15
15	MVP(N)239	31	15	MVP(N)271	16
16	MVP(N)240	32	16	MVP(N)272	17
17	MVP(N)241	33	17	MVP(N)273	18
18	MVP(N)242	34	18	MVP(N)274	19
19	MVP(N)243	35	19	MVP(N)275	20
20	MVP(N)244	36	20	MVP(N)276	21
21	MVP(N)245	37	21	MVP(N)277	22
22	MVP(N)246	38	22	MVP(N)278	23
23	MVP(N)247	39	23	MVP(N)279	24
24	MVP(N)248	40	24	MVP(N)280	25
25	MVP(N)249	41	25	MVP(N)281	26
26	MVP(N)250	42	26	MVP(N)282	27
27	MVP(N)251	43	27	MVP(N)283	28
28	MVP(N)252	44	28	MVP(N)284	29
29	MVP(N)253	45	29	MVP(N)285	30
30	MVP(N)254	46	30	MVP(N)286	31
31	MVP(N)255	47	31	MVP(N)287	32

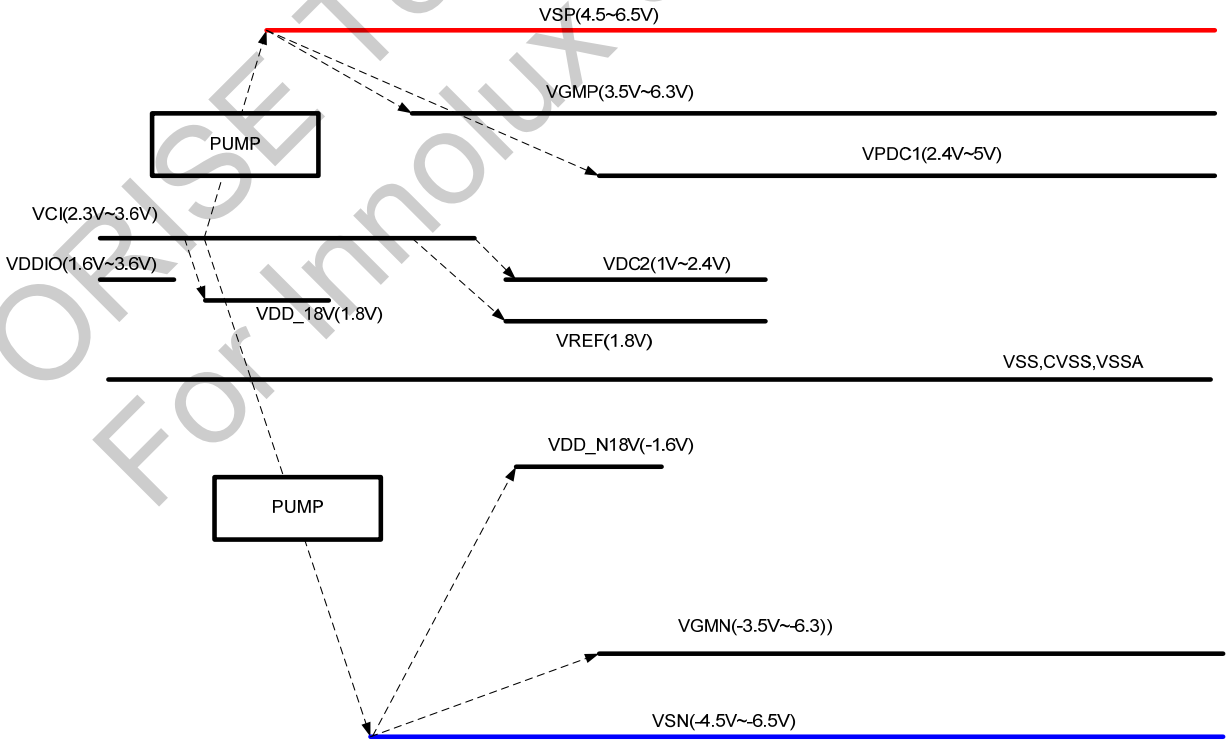
3.2. LCD Driving Power Supply Circuit

The LCD driving power supply circuit generates the voltage levels for driving an LCD. All this voltages can be adjusted by register setting.

DCMOD=0

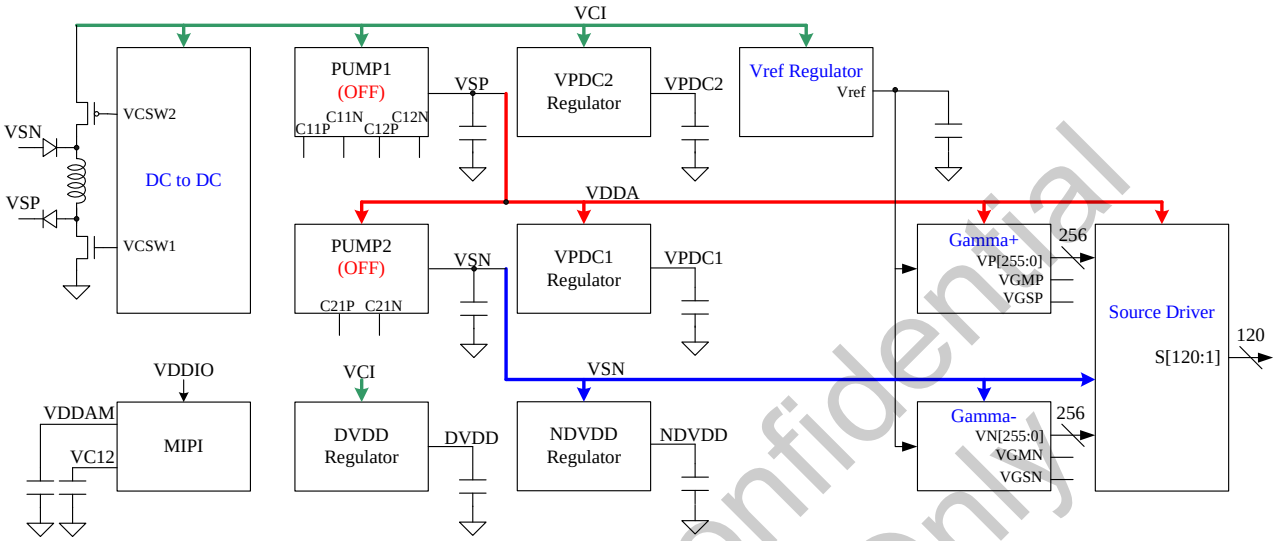


DCMOD=1

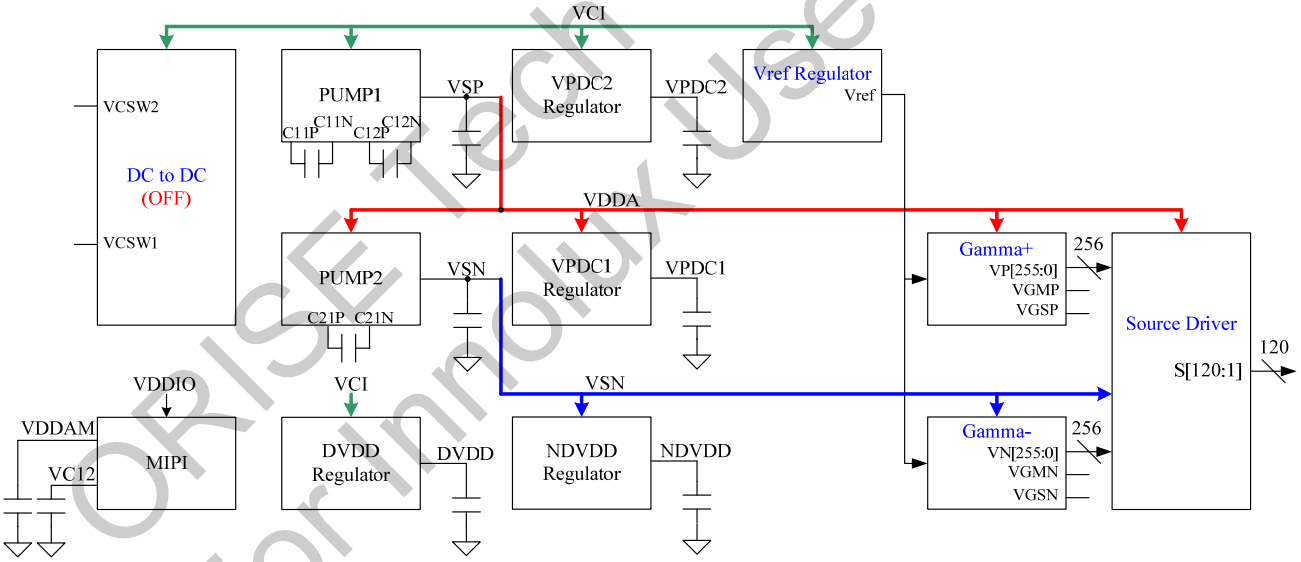


3.3. Power Block Diagram

3.3.1. DCMOD=0 (Two Coil Booster)



3.3.2. DCMOD=1 (Charge Pump)



3.4. BOM List

3.4.1. DCMOD=0 (Two Coil Booster)

No.	Signal name	Values	Max ability	Note
1	VDDIO	1.0uF	4.0V	
2	VCI	1.0uF	6.3V	
3	VSP	1.0uF	10.0V	
4	VSN	1.0uF	10.0V	
5	VDDAM	1.0uF	4.0V	
6	VC12	1.0uF	4.0V	
7	DVDD	1.0uF	4.0V	
8	NDVDD	1.0uF	4.0V	
9	VPDC1	1.0uF	10.0V	
10	VPDC2	1.0uF	10.0V	
11	VREF	1.0uF	4.0V	
12	VSS/VSN	Schottky Diode	-	
13	-	Diode	-	
14	-	Diode	-	
15	-	Inductor	-	
16	-	Power MOS	-	
17	-	Power MOS	-	

3.4.2. DCMOD=1 (Charge Pump)

No.	Signal name	Values	Max ability	Note
1	VDDIO	1.0uF	4.0V	
2	VCI	1.0uF	6.3V	
3	C11P/C11N	1.0uF	6.3V	
4	C12P/C12N	1.0uF	6.3V	
5	VSP	1.0uF	10.0V	
6	C21P/C21N	1.0uF	6.3V	
7	VSN	1.0uF	10.0V	
8	VDDAM	1.0uF	4.0V	
9	VC12	1.0uF	4.0V	
10	DVDD	1.0uF	4.0V	
11	NDVDD	1.0uF	4.0V	
12	VPDC1	1.0uF	10.0V	
13	VPDC2	1.0uF	10.0V	
14	VREF	1.0uF	4.0V	
15	VSS/VSN	Schottky Diode	-	

4. SIGNAL DESCRIPTIONS

4.1. Power Supply System Pins

Symbol	I/O	Type	Functions
Power Supply Pins			
VCI	I	P	Power supply voltage input pins (typical 2.75V). The input range is 2.3 to 3.6V, and the 1uF bypass capacitor is connected to this pin.
VDDIO	I	P	Power supply voltage input pins for the I/O interface pins. The input range is 1.6 to 3.3V, and the 1uF bypass capacitor is connected to this pin.
VDD_OTP	I	P	For OTP programming power supply(7.5v) -If DrIC is not at programming state, please floating this pin.
DGND	---	P	Ground for the internal logic. DGND = 0V.
AGND	---	P	Analog ground. AGND = 0V.
Charge Pump/ Booster / Regulator Related Pins			
DVDD	O	P	Regulated power output for core circuit. A 0.1uF~1uF bypass capacitor shall be connected to this pin.
DVDDN	O	P	Regulated power output for core circuit. A 0.1uF~1uF bypass capacitor shall be connected to this pin.
C11P	---	P	Voltage Generation Capacitor for AVDD, 2X VCI charge pump.
C11N	---	P	Voltage Generation Capacitor for AVDD, 2X VCI charge pump.
C12P	---	P	Voltage Generation Capacitor for AVDD, 2X VCI charge pump.
C12N	---	P	Voltage Generation Capacitor for AVDD, 2X VCI charge pump.
C21P	---	P	Voltage Generation Capacitor, -1X AVDD charge pump.
C21N	---	P	Voltage Generation Capacitor, -1X AVDD charge pump.
VSP	O	P	Power supply for the charge-pump of panel and positive source output from PFM structure.
VSN	O	P	Power supply for the charge-pump of panel and negative source output from PFM structure.
VCSW1	O	P	Control pin of PFM function -If not used, please floating this pin.
VCSW2	O	P	Control pin of PFM function -If not used, please floating this pin.
VGMP	O	P	VGMP serve as the highest voltage of positive gamma source.
VGSP	O	P	VGSP serve as the lowest voltage of positive gamma source.
VGMN	O	P	VGMN serve as the highest minus voltage of negative gamma source.
VGSN	O	P	VGMP serve as the lowest minus voltage of negative gamma source.
VPDC1	O	P	DC voltage for LCD (for gate).A 1uF bypass capacitor shall be connected to this pin.
VPDC2	O	P	DC voltage for LCD (for gate).A 1uF bypass capacitor shall be connected to this pin.
VREF	O	P	Reference voltage
DGNDOUT	O	P	DGNDOUT same DGND voltage level, Driver internal connection
VC12	O	P	Power supply voltage for MIPI DSI I/F.A 1uF bypass capacitor shall be connected to this pin. -If not used, please floating this pin.
VDDAM	O	P	Power supply voltage for MIPI DSI I/F.A 1uF bypass capacitor shall be connected to this pin. -If not used, please floating this pin.
VDDIM	O	P	Power supply voltage for MIPI DSI I/F.A 1uF bypass capacitor shall be connected to this pin. -If not used, please floating this pin.
CPCLKP	O	VSP	Charge Pump CLK1
CPCLKN	O	VSP	Charge Pump CLK2

4.2. Interface Logic pins

Symbol	I/O	Type	Functions
Global Control Signal			
IM1, IM0	I	VDDIO	-MIPI DSI, DPI interface and RGB/SPI interface select IM[1:0] 00: MIPI DSI 01: RGB I/F mode2 10: RGB I/F mode1_3 wire 11: MIPI DSI + SPI_3wire
RESOL0, RESOL1, RESOL2	I	VDDIO	Resolution select pin RESOL[2:0] 000:240x320 001:240x400 010:240x432 100:320x240 101:320x320
RESET	I	VDDIO	-This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
SPI Interface, RGB Interface pins			
D/CX(CSTROL)	I	VDDIO	When IM[1:0]=11 Data / Command selection pin -D/CX='1': Data -D/CX='0': Command When IM[1:0]=01 CSTROL is CS activity type control pin CSTROL=0: CS low activity type. CSTROL=1: CS high activity type. If not used, please fix this pin at VDDIO or DGND level.
CS	I	VDDIO	When IM[1:0] ='01','1x'(RGB I/F), - Chip select input pin (low enable)
SCLK	I	VDDIO	- SCLK function for RGB SPI I/F mode 1 or 2 -If not used, please fix this pin at VDDI or DGND level.
SDI	I	VDDIO	When IM[1:0] ='01','1x'(RGB I/F), Serial input signal. The data is input on the rising edge latch data of the SCL signal. -When IM[1:0] ='00'(DSI), -If not used, please fix this pin at DGND level.
SDO	O	VDDIO	When IM[1:0] ='01,'1x', Serial output signal. The data is output on the rising edge latch data of the SCL signal. -When IM[1:0] ='00'(DSI), please leave it open
D[23:16]	I	VDDIO	D[23:16] are used to DPI and RGB interface Red data bus. If use to 18bits, D16 connector to D22 D17 connector to D23 in foil design. If use to 16bits, D16 connector to D21 D17 connector to D22 D18 connector to D23 in foil design. -If not used, please fix this pin at DGND level.
D[15:8]	I	VDDIO	D[15:8] are used to DPI and RGB interface Green data bus. If use to 18 or 16bits, D8 connector to D14 D9 connector to D15 in foil design.

Symbol	I/O	Type	Functions
			-If not used, please fix this pin at DGND level.
D[7:0]	I	VDDIO	D[7:0] are used to DPI and RGB interface Blue data bus. If use to 18bits, D0 connector to D6 D1 connector to D7 in foil design. If use to 16bits, D0 connector to D5 D1 connector to D6 D2 connector to D7 in foil design. -If not used, please fix this pin at DGND level.
VSync	I	VDDIO	Vertical sync. Signal in DPI I/F and Moto RGB I/F mode If not used, please fix this pin at VDDIO or DGND level.
HSync	I	VDDIO	Horizontal sync. Signal in DPI I/F and Moto RGB I/F mode If not used, please fix this pin at VDDI or DGND level.
PCLK	I	VDDIO	Pixel clock signal in DPI I/F and Moto RGB I/F mode If not used, please fix this pin at VDDIO or DGND level.
DE	I	VDDIO	-Data enable signal in DPI I/F and Moto RGB I/F mode -If not used, please connect to ground or VDDIO this pin
DSI Interface pins			
RX_D0P(Data +)	I		When IM[1:0] ='00'(DSI I/F), Data transfer pin If not used, please fix this pin at DGND level or floating.
RX_D0PN(Data -)	I		When IM[1:0] ='00'(DSI I/F), Data transfer pin If not used, please fix this pin at DGND level or floating.
RX_CP(Clock +)	I		When IM[1:0] ='00'(DSI I/F), Clock transfer pin If not used, please fix this pin at DGND level or floating.
RX_CN(Clock -)	I		When IM[1:0] ='00'(DSI I/F), Clock transfer pin If not used, please fix this pin at DGND level or floating.

Note1: Input signal need use Schmitt trigger: HS, VS, PCLK, SDO, SDI, SCS,SCLK and D[23:0].

Note2: Model select pins need add De-bounce circuit.

4.3. Model Selection Pins

Symbol	I/O	Type	Functions
Mode Select pin			
EXTC	I	VDDIO	Engineering command enable pin 0: disable 1: enable
ALSON	I	VDDIO	ALS function on/off select 0: ALS off, and STV1 on, STV2 off 1: Disable
LCM	I	VDDIO	Liquid Crystal selection pin - LCM='0', NW - LCM='1', NB
DCMOD	I	VDDIO	DC voltage supply structure select pin: 0: PFM 1: Charge pump
CM	I	VDDIO	-Normal mode and Idle mode control pin For RGB I/F mode2 -Please refer RGB I/F for detail using -CM = '1', Idle partial mode -CM = '0', Normal display mode -If not used, please fix this pin at VDDIO or DGND level.
SD	I	VDDIO	-Display on/off H/W control pin in RGB I/F For RGB I/F mode2 -Please refer RGB I/F for detail using - SD='1' sleep mode - SD='0' normal operating mode -If not used, please fix this pin at VDDIO or DGND level.
RL	I	VDDIO	Input pin to select the Source driver data shift direction. For RGB I/F mode2 - RL ='1' , source scan from Left to Right - RL ='0' , source scan from Right to Left -If not used, please fix this pin at VDDIO or DGND level.
TB	I	VDDIO	Input pin to select the Gate driver scan direction. For RGB I/F mode2 - TB='1' , Gate scan from Top to Bottom - TB='0' , Gate scan from Bottom to Top -If not used, please fix this pin at VDDIO or DGND level.
REV	I	VDDIO	Source output polarity select H/W pin For RGB I/F mode2(Moto SPI+RGB) - REV=0, Data not reverse - REV=1, Data reverse - Please refer RGB I/F for detail using - If not used, please fix this pin at VDDIO or DGND level
FCS	I	VDDIO	This pin can selection control signal For RGB I/F mode2 FCS = 0: (default) IC accepts the values of internal register, and the external input pads are disable FCS = 1: IC accepts the value of external input pads.
IDSEL	I	VDDIO	When IM[1:0]=01, IDSEL is control SPI ID select pin IDSEL='0' ID select 0 IDSEL='1' ID select 1 If not used, please fix this pin at VDDIO or DGND level.

4.4. Driving System Pins

Symbol	I/O	Type	Functions
Source/LTPS Pins			
S1~S120	O	VSP	Output voltages applied to the liquid crystal. If pin useless, please floating.
GAS	O	VSP	Gate all select
CKH1	O	VSP	Horizontal clock 1 output
CKH2	O	VSP	Horizontal clock 2 output
CKH3	O	VSP	Horizontal clock 3 output
CKH4	O	VSP	Horizontal clock 4 output
CKH5	O	VSP	Horizontal clock 5 output
CKH6	O	VSP	Horizontal clock 6 output
CKH7	O	VSP	Horizontal clock 7 output
CKH8	O	VSP	Horizontal clock 8 output
CKH9	O	VSP	Horizontal clock 9 output
STV1	O	VSP	Vertical start output
STV2	O	VSP	Vertical start output
PRST	O	VSP	Panel reset signal output for 1st frame
CKV	O	VSP	Vertical clock 1 output
ENBV	O	VSP	V enable output
CSV	O	VSP	Switch normal scan (down/up) and reverse scan (up/down)

4.5. Test and Dummy Pins

Symbol	I/O	Type	Functions
Test Pins			
TEST[1:2]	I		Test pins, not accessible to user, must be left open.
TEST[4:7]	I		Test pins, not accessible to user, must be left open.
Dummy Pins			
ALS_MOUT1	I		Dummy input. Please connect to DGND
ALS_EOUT1	I		Dummy input. Please connect to DGND
ALS_MOUT2	I		Dummy input. Please connect to DGND
ALS_EOUT2	I		Dummy input. Please connect to DGND
ALS_MOUT3	I		Dummy input. Please connect to DGND
ALS_EOUT3	I		Dummy input. Please connect to DGND
ALS_SET	O		Dummy output. Please leave it open

5. FUNCTIONS

5.1. RGB Interface

5.1.1. General Description

The OTM3201A provides 8, 16, 18, and 24-bits parallel RGB interface DB[23:0] with control signals : VS(Pin TE_VSYNC_D), HS(Pin HSYNC), DE(Pin E_NRD_PE), PCLK(Pin DCK). The interface is activated after Power On sequence.

Pixel clock (PCLK) is running all the time without stopping and it is used to entering VS, HS, DE and DB[23:0] states when there is a rising edge of the PCLK. The PCLK cannot be used as continues internal clock for other functions of the display module e.g. Sleep In –mode etc. Vertical synchronization (VS) is served as Vertical synchronization signal. This is negative (‘0’, low) active and its state is read to the display module by a rising edge of he PCLK signal. Horizontal synchronization (HS) is served as Horizontal signal. This is negative (‘0’, low) active and its state is read to the display module by a rising edge of the PCLK signal. Data Enable (DE) is served as the valid data period signals. This is a positive (‘1’, high) active and its state is read to the display module by a rising edge of the PCLK signal. D[23:0] (24-bits: R7-R0, G7-G0 and B7-B0; and B5-B0; 16-bits: R4-R0, G5-G0 and B4-B0)and DB[7:0] 8-bits data bus are used to tell what is the information of the image that is transferred on the display (When DE=’1’ and there is a rising edge of PCLK). DB[23:0] can be ‘0’ (low) or ‘1’ (high). These lines are read by a rising edge of the PCLK signal.

The PCLK cycle is described in the following figure.

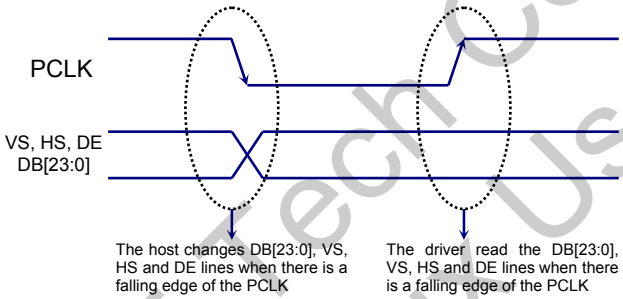


Fig. 5.1.1.1 PCLK cycle

Note: PCLK is an unsynchronized signal (It can be stopped).

5.1.2. General Timing Diagram

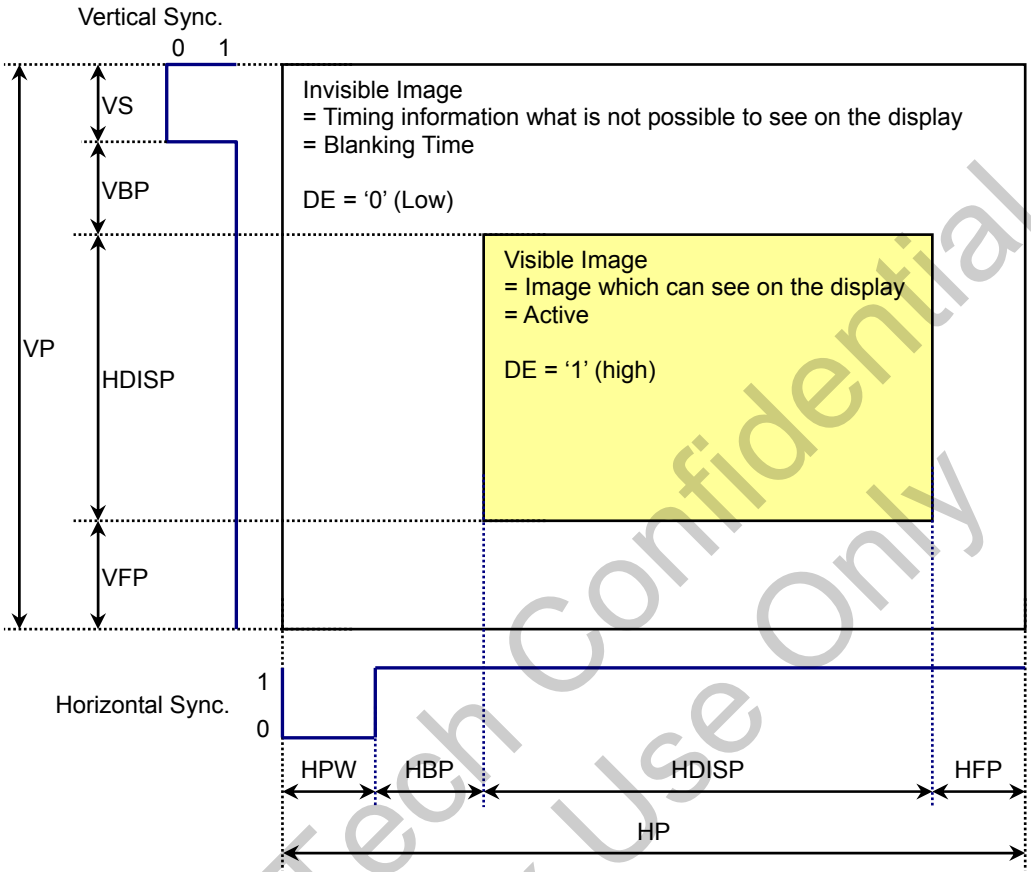


Fig. 5.1.2.1 RGB General Timing diagram

The image information must be correct on the display, when the timings are in range on the interface.

However, the image information can be incorrect on the display, when timings are not out of range on the interface (Out of the range timings cannot on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.) when there is returned from out of the range to in range interface timing.

5.1.3. RGB Interface Bus Width Set

There are four different data bus format available during RGB interface mode. Table 6.4.1 summarized these 4 data bus format.

Table 5.1.3.1 RGB interface Bus Width Set Table

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
	R4	R3	R2	R1	R0	x	x	x	G5	G4	G3	G2	G1	G0	x	x	B4	B3	B2	B1	B0	x	x	x	16-bits data
	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	18-bits data
	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	24-bits data

5.1.4. RGB Interface Timing Diagram

5.1.4.1. General timings for RGB I/F

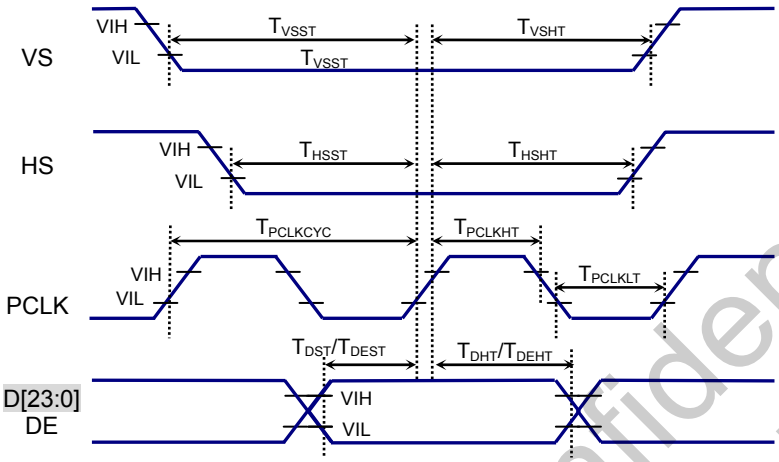


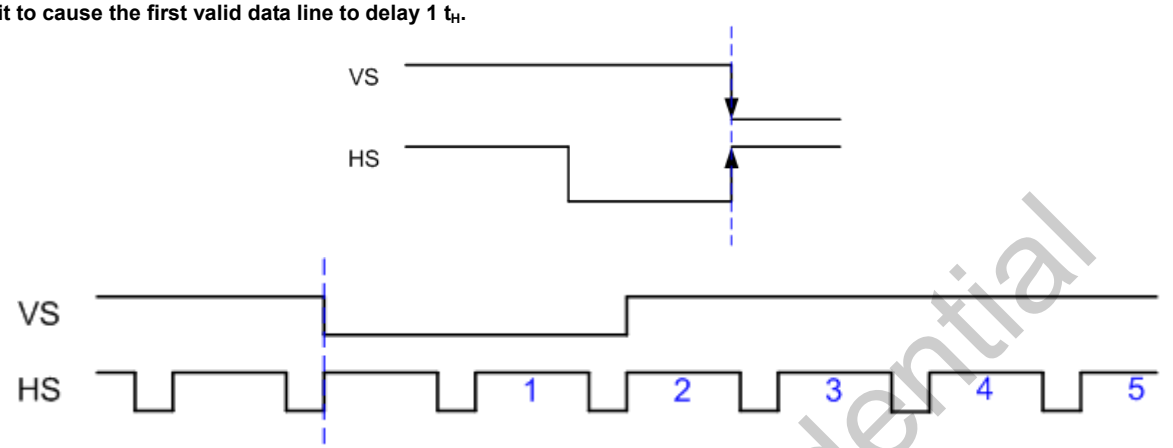
Fig.5.1.4.1.1 General Timing for RGB I/F

General Timing for RGB I/F

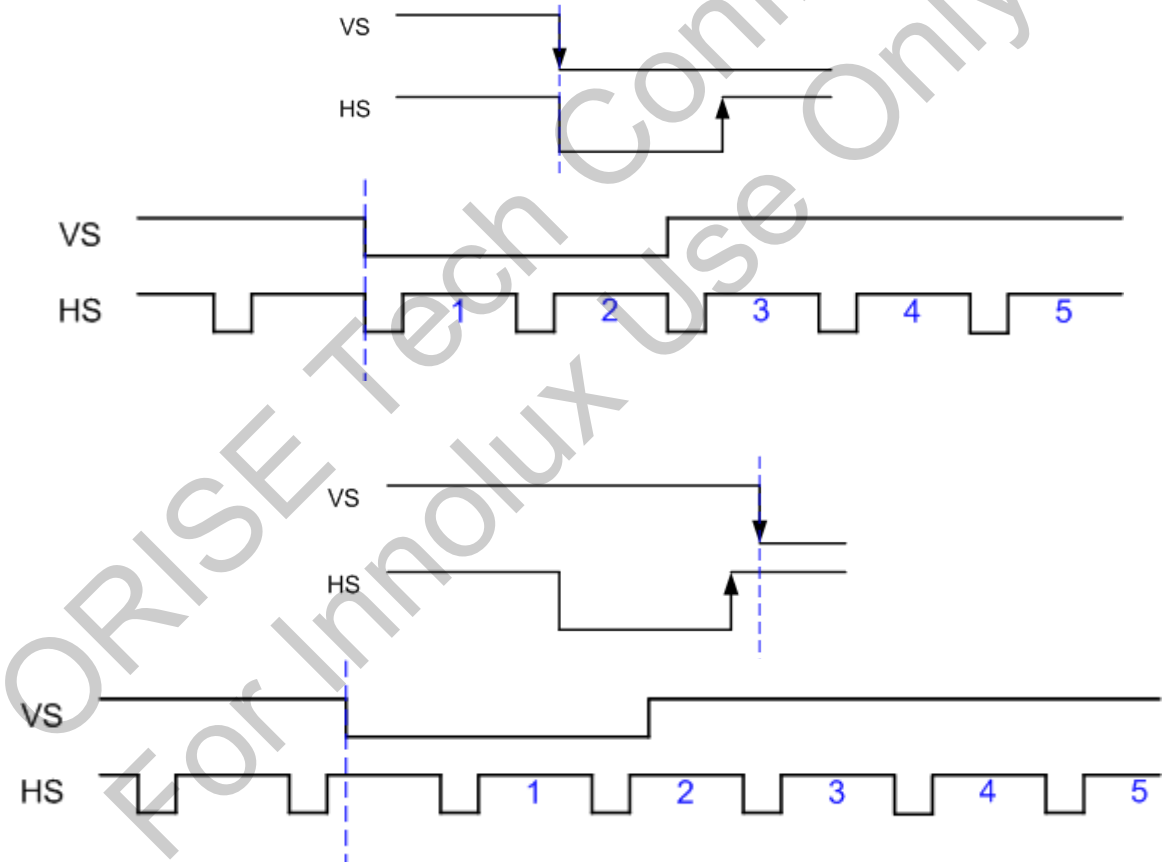
Symbol	Parameter	Related Pins	MIN	TYP	MAX	Unit
tvsys	Vertical Sync Setup Time		20	-	-	ns
tvsyh	Vertical Sync Hold Time		20	-	-	ns
thsys	Horizontal Sync Setup Time		20	-	-	ns
thsyh	Horizontal Sync Hold Time		20			ns
thv	Phase difference of Sync Signal Falling Edge		0	-	240	tPCLK
tPCLK	PCLK cycle time		65			Ns
tCKL	Master Clock Low Period		15	75	-	ns
tCKH	Master Clock High Period		15	75	-	ns
tds	Data Setup Time		20	-	-	ns
tdh	Data Hold Time		20	-	-	ns

Note1: VDDIO=1.6 to 3.6V, VCI=2.3 to 3.6V AGND=0V, DGND=0V, Ta = -40 to 85℃

If VS falling edge and HS rising edge are at same time, it is in the margin and not surely which is the first valid data line. So we want it to cause the first valid data line to delay 1 t_H.



If VS falling edge is late after HS rising edge, it will cause the first valid data line to delay 1 t_H.



5.1.4.2. RGB interface mode timing diagram

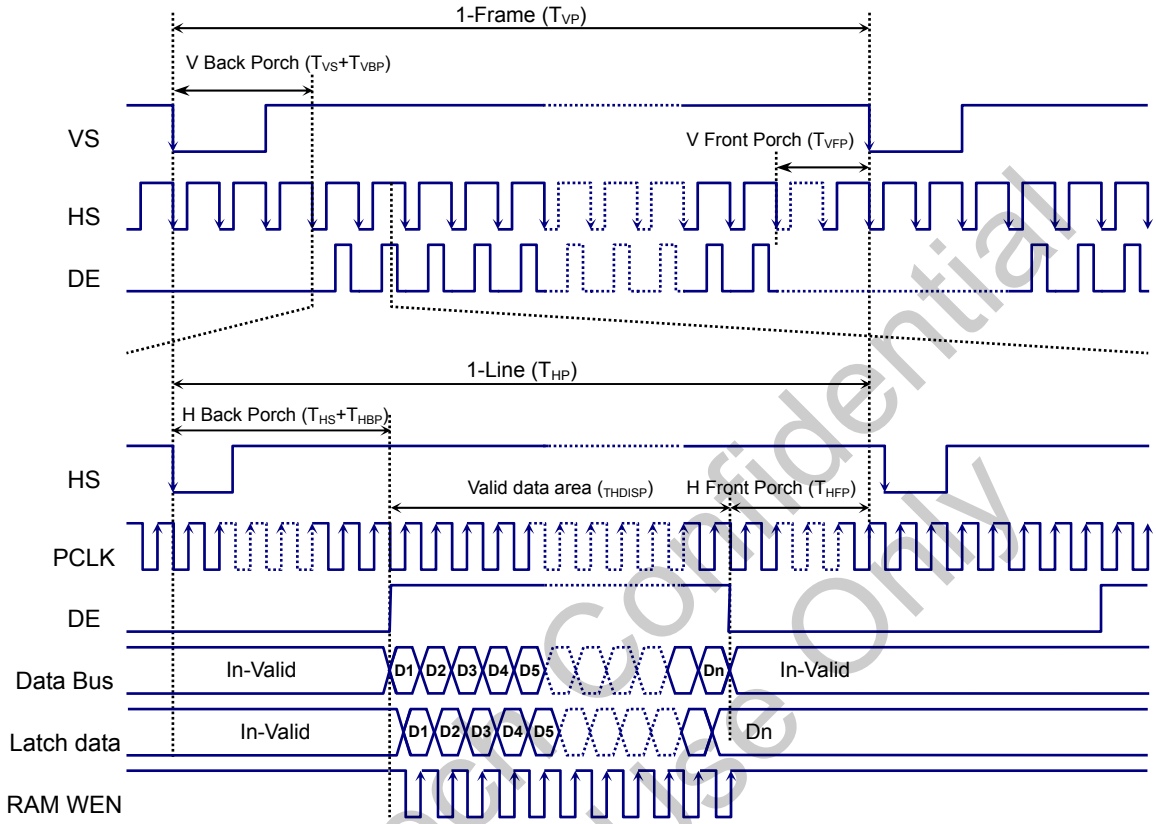
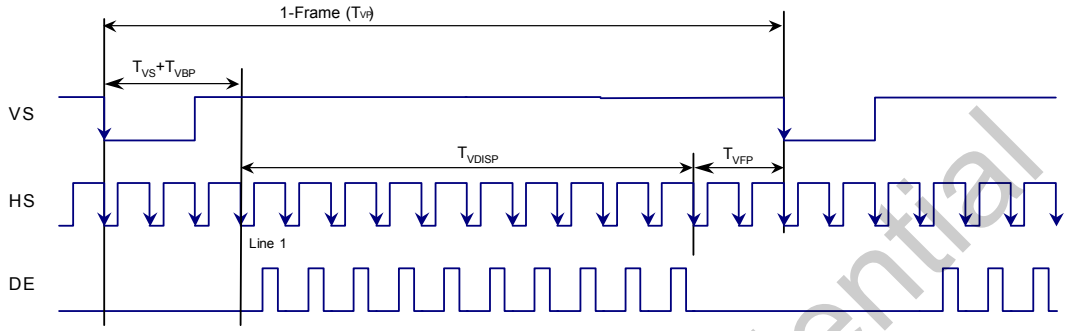


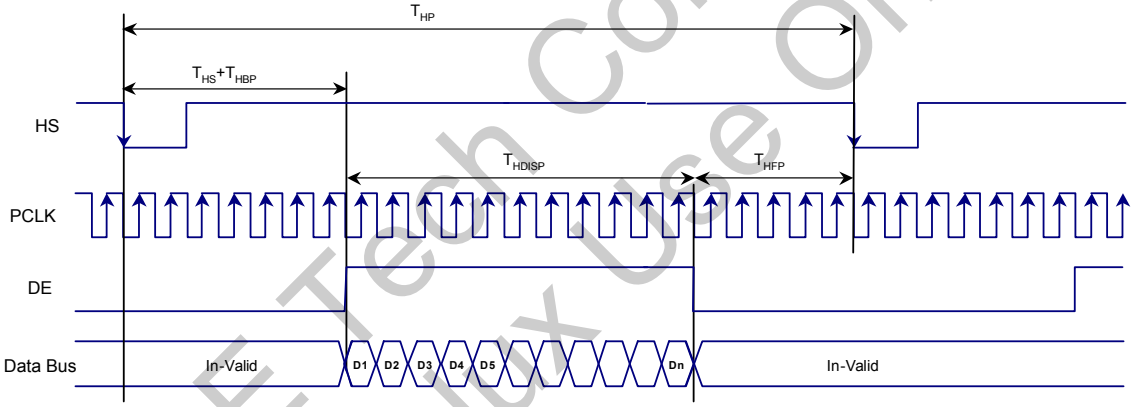
Fig. 5.1.4.2.1 RGB Mode Timing Diagram

IM[1:0]=1x for RGB I/F mode1

Vertical Timing for RGB I /F



Horizontal Timing for RGB I/F



Full color change to Idle mode timing chart

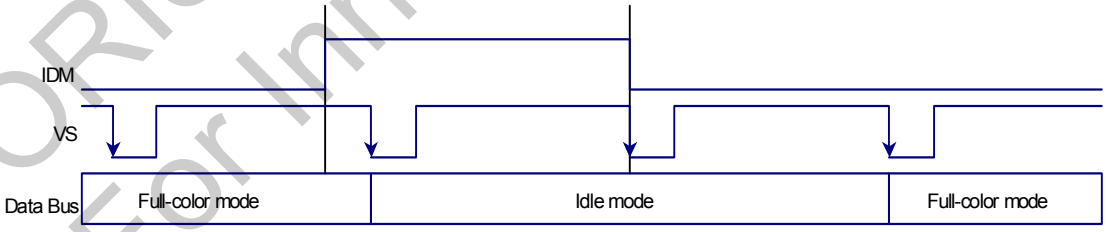


Fig. 5.1.4.2.2 RGB Mode color change timing diagram

Vertical and Horizontal Timing for 240x320 RGB I/F

Item	Symbol	Condition	Specification			Unit
			Min	typical..	Max	
Vertical Frequency		Frame rate	50	60	80	Hz
Horizontal Frequency				19.43		kHz
PCLK Frequency				**5.44**	10	MHz
Vertical Timing						
Vertical cycle period	TVP		324	326	447	HS
Vertical low pulse width	TVS		1	2	6	HS
Vertical front porch	TVFP		2	2	-	HS
Vertical back porch	TVBP		1	2	-	HS
Vertical data start line		TVS+TVBP	2	4	-	HS
Vertical blanking period	TVBL	TVBP + TVFP+ TVS	4	6	127	HS
Vertical active area	TVDISP			320		HS
Horizontal Timing						
Horizontal cycle period	THP		270	280	367	PCLK
Horizontal low pulse width	THS		2	10	-	PCLK
Horizontal front porch	THFP		10	10	-	PCLK
Horizontal back porch	THBP		18	20	-	PCLK
Horizontal data start point		THS + THBP	20	30	-	PCLK
Horizontal blanking period	THBL	THS + THBP+ THFP	30	40	127	PCLK
Horizontal active area	THDISP			240		PCLK

Vertical and Horizontal Timing for 2.0” 320x240 RGB I/F

Item	Symbol	Condition	Specification			Unit
			Min	typical..	Max	
Vertical Frequency		Frame rate	50	60	80	Hz
Horizontal Frequency			18	21.6	28.8	kHz
PCLK Frequency			4.43	5.31	7.08	MHz
Vertical Timing						
Vertical cycle period	TVP		244	246	367	HS
Vertical low pulse width	TVS		1	2	6	HS
Vertical front porch	TVFP		2	2	-	HS
Vertical back porch	TVBP		1	2	-	HS
Vertical data start line		TVS+TVBP	2	4	-	HS
Vertical blanking period	TVBL	TVBP + TVFP+ TVS	4	6	127	HS
Vertical active area	TVDISP			240		HS
Horizontal Timing						
Horizontal cycle period	THP		350	360	447	PCLK
Horizontal low pulse width	THS		2	10	-	PCLK
Horizontal front porch	THFP		10	10	-	PCLK
Horizontal back porch	THBP		18	20	-	PCLK
Horizontal data start point		THS + THBP	20	30	-	PCLK
Horizontal blanking period	THBL	THS + THBP+ THFP	30	40	127	PCLK
Horizontal active area	THDISP			320		PCLK

Note 1. VDDIO=1.6 to 3.6V, VCI=2.3 to 3.6V, AVSS=DVSS=0V, Ta=-40 to 85 ℃

Note 2. Data lines can be set to “High” or “Low” during blanking time – Don’t care.

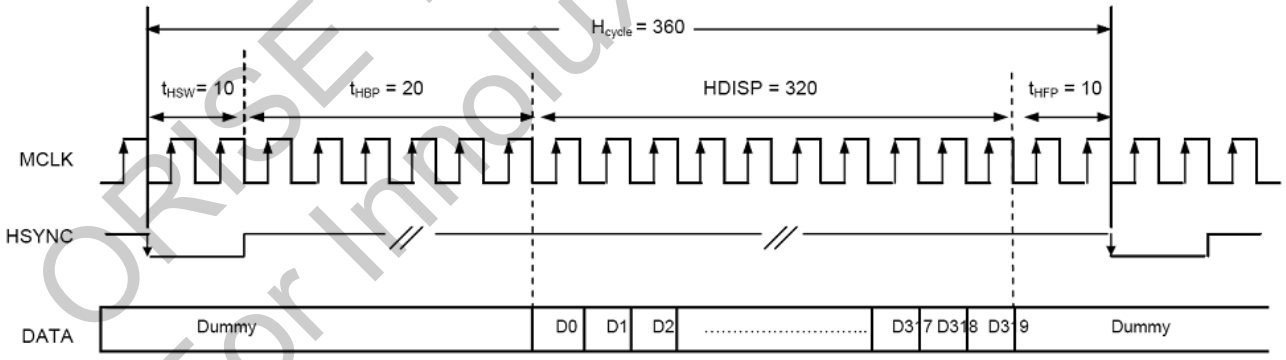


Fig. 5.1.4.2.3 Horizontal Write Timing

Vertical and Horizontal Timing for 240x400 RGB I/F

Item	Symbol	Condition	Specification			Unit
			Min	typical..	Max	
Vertical Frequency		Frame rate	50	60	80	Hz
Horizontal Frequency				16.8		kHz
PCLK Frequency				**6.82**		MHz
Vertical Timing						
Vertical cycle period	TVP		404	406	527	HS
Vertical low pulse width	TVS		1	2	6	HS
Vertical front porch	TVFP		2	2	-	HS
Vertical back porch	TVBP		1	2	-	HS
Vertical data start line		TVS+TVBP	2	4	-	HS
Vertical blanking period	TVBL	TVBP + TVFP+ TVS	4	6	127	HS
Vertical active area	TVDISP			400		HS
Horizontal Timing						
Horizontal cycle period	THP		270	280	367	PCLK
Horizontal low pulse width	THS		2	10	-	PCLK
Horizontal front porch	THFP		10	10	-	PCLK
Horizontal back porch	THBP		18	20	-	PCLK
Horizontal data start point		THS + THBP	20	30	-	PCLK
Horizontal blanking period	THBL	THS + THBP+ THFP	30	40	127	PCLK
Horizontal active area	THDISP			240		PCLK
Horizontal cycle period RGBx3	THP			840		PCLK
Horizontal low pulse width RGBx3	THS			30	-	PCLK
Horizontal front porch RGBx3	THFP			30	-	PCLK
Horizontal back porch RGBx3	THBP			60	-	PCLK
Horizontal data start point RGBx3		THS + THBP		90	-	PCLK
Horizontal blanking period RGBx3	THBL	THS + THBP+ THFP		120		PCLK
Horizontal active area RGBx3	THDISP			720		PCLK

Note 1. VDDIO=1.6 to 3.6V, VCI=2.3 to 3.6V, AVSS=DVSS=0V, Ta=-40 to 85 ℃

Note 2. Data lines can be set to “High” or “Low” during blanking time – Don’t care.

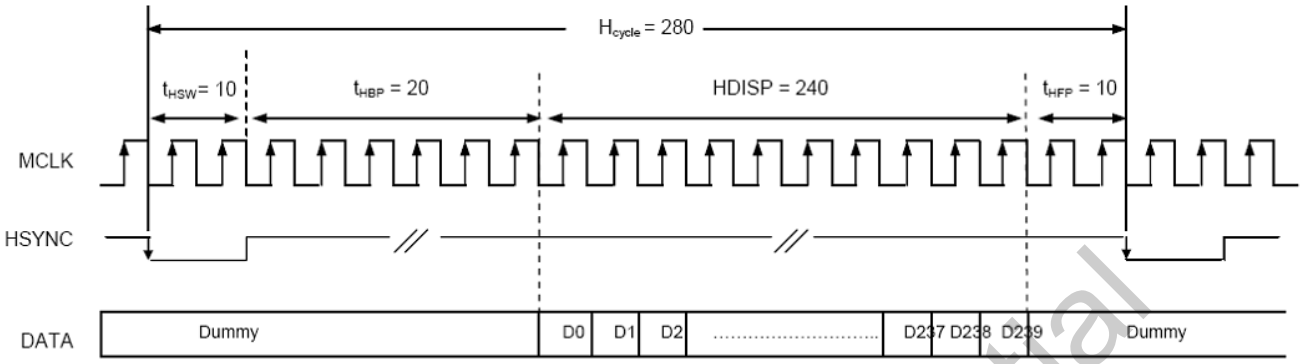


Fig. 5.1.4.2.4 RGB24 Horizontal Wrte Timing

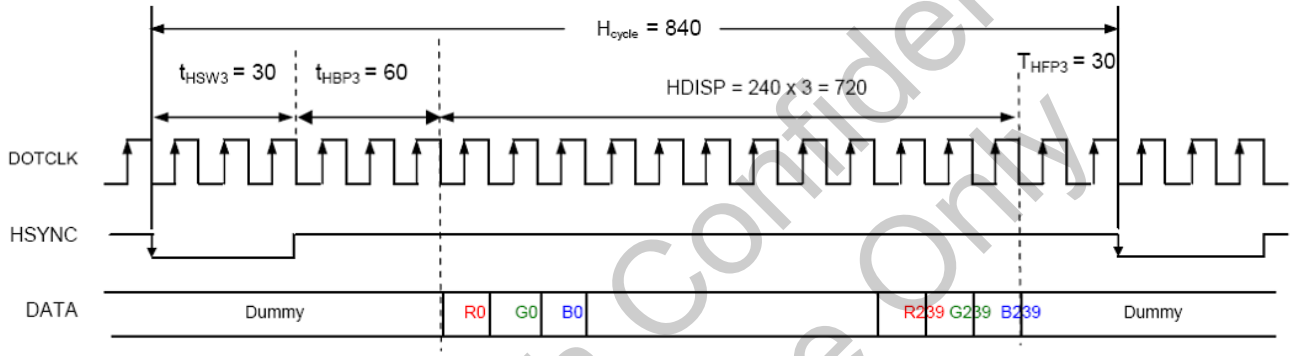


Fig. 5.1.4.2.5 RGB24 Horizontal Wrte Timing RGBX3

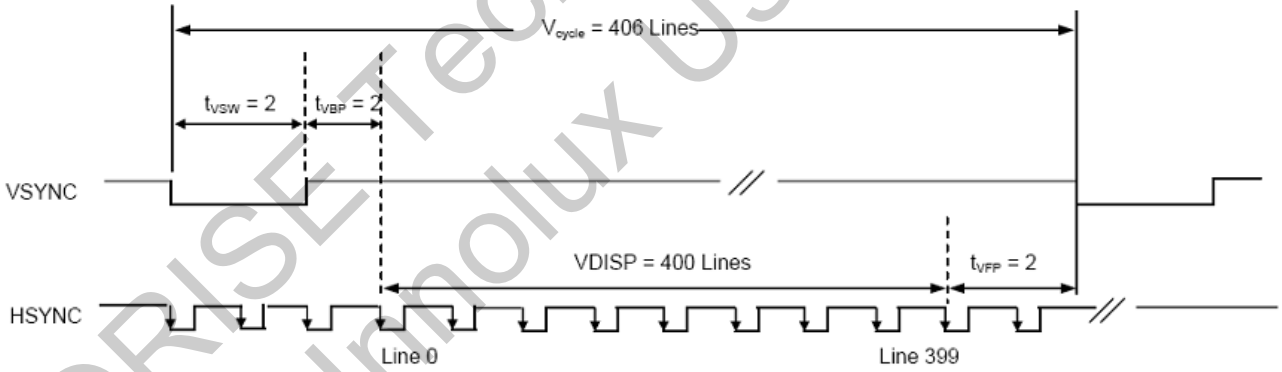
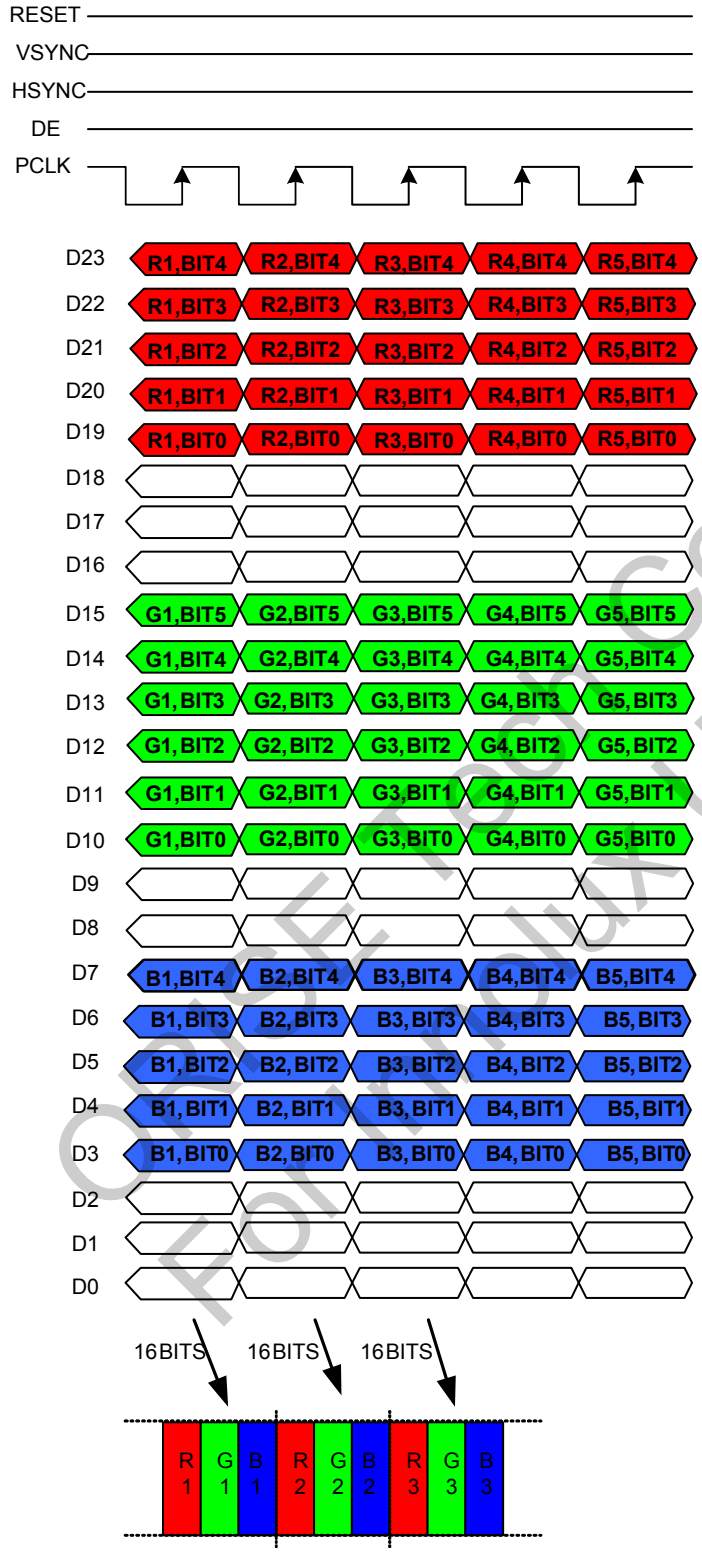


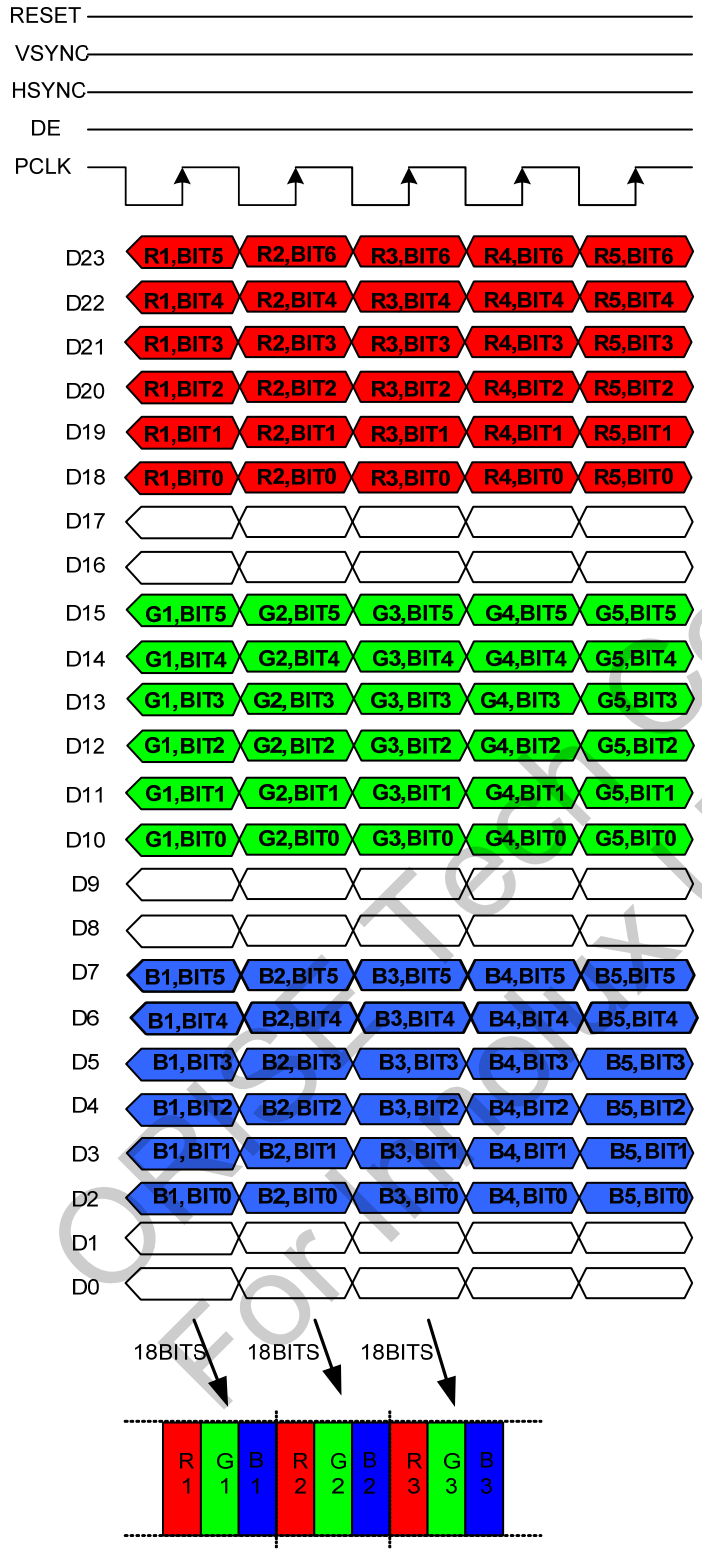
Fig. 5.1.4.2.6 RGB24,RGBx3 Vertical Wrte Timing

5.1.5. RGB Data Color Coding

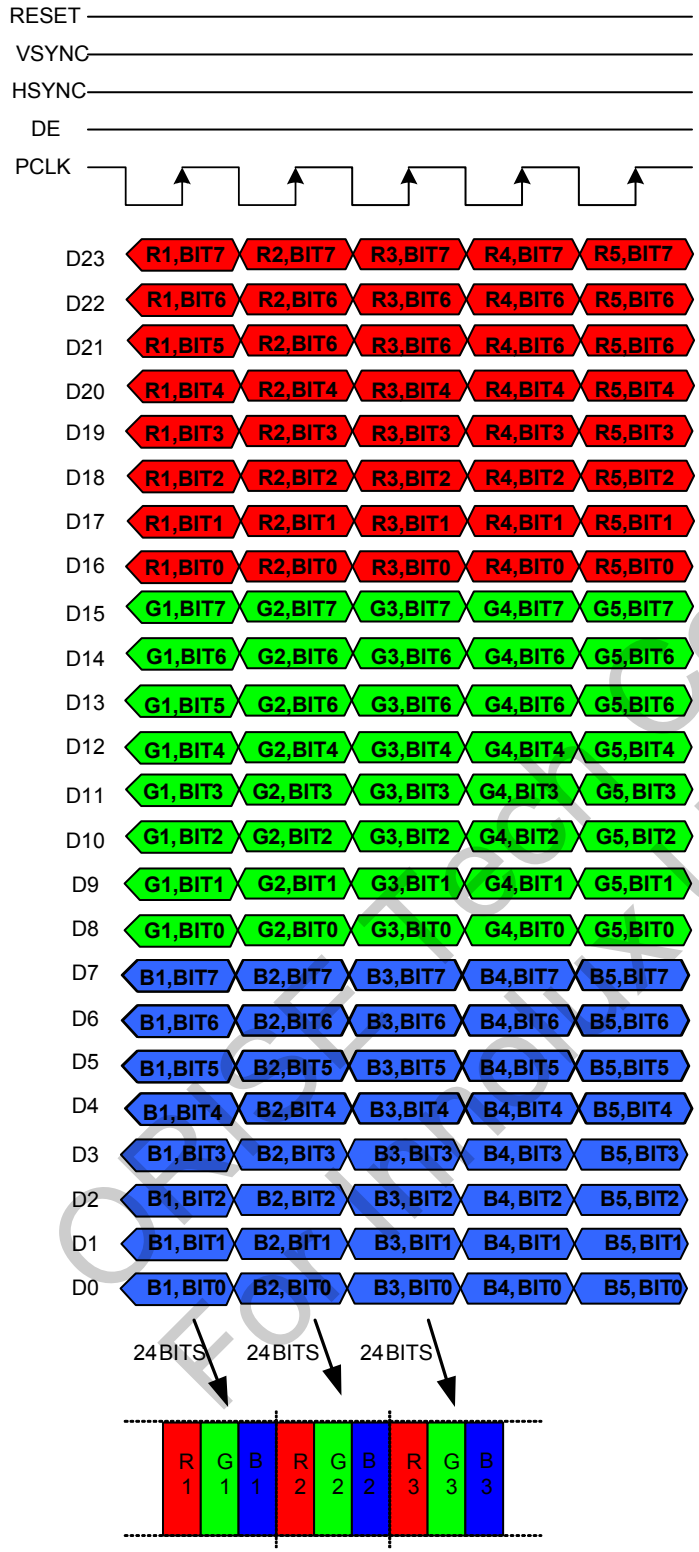
5.1.5.1. 16-bits/pixel Colors Order for the 24-bits Data bus in RGB Interface (RGB 5-6-5-bits input)



5.1.5.2. 18-bits/pixel Colors Order for the 24-bits Data Bus in RGB Interface (RGB 6-6-6-bits input)



5.1.5.3. 24-bits/pixel Colors Order for the 24-bits Data Bus in RGB Interface (RGB 8-8-8-bits input)



5.2. MIPI-DSI Interface

5.2.1. General description

The communication can be separated 2 different levels between the MCU and the display module:

- Interface Level : Low level communication
- Packet level : High level communication

5.2.2. Interface level communication

5.2.2.1. General

The display module uses data and clock lane differential pairs for DSI . Both clock lane and data lane0 can be driven Low Power (LP) or High Speed (HS) mode.

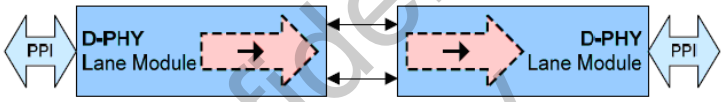
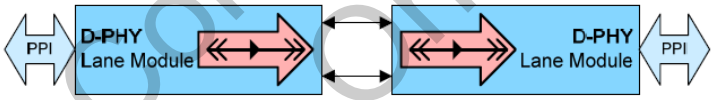
-	Lane support mode	MPU(Host) OTM2501A(Slave)
Clock Lane	Unidirectional lane • High-Speed Clock only • Simplified Escape Mode (ULPS Only)	
Data Lane0	Bi-directional lane • Forward high-speed only • Bi-directional Escape Mode • Bi-direction LPDT	

Table: Lane types and support mode

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.
High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.
There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to the display module and vice versa. The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low-Power (LP)	
	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Table: High Speed and Low-Power Lane Pair State Descriptions

5.2.2.2. DSI-CLK lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM LP-11), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM).

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode(LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

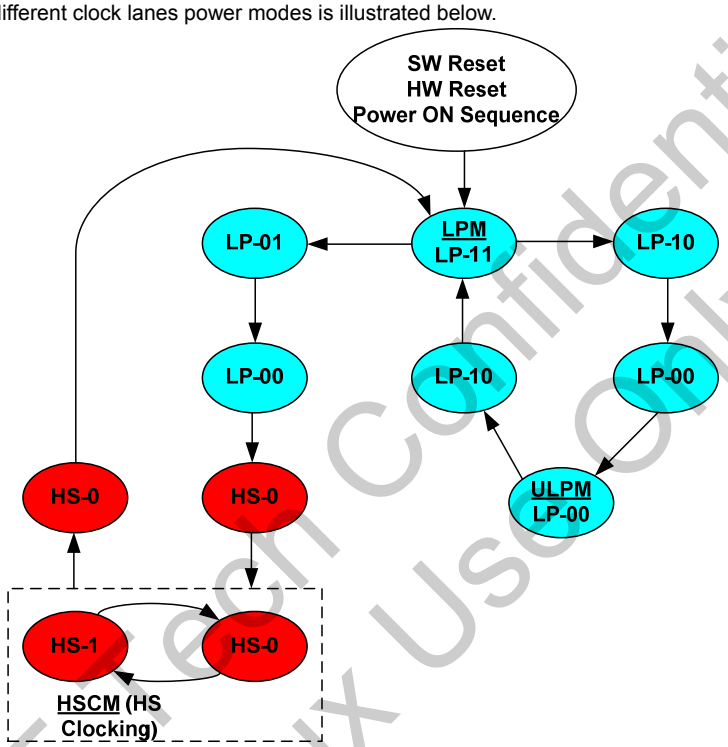


Figure: Clock Lanes Power Modes

Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.
2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

Low Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

1) After SW Reset, HW Reset or Power On Sequence =>LP-11
2) After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.

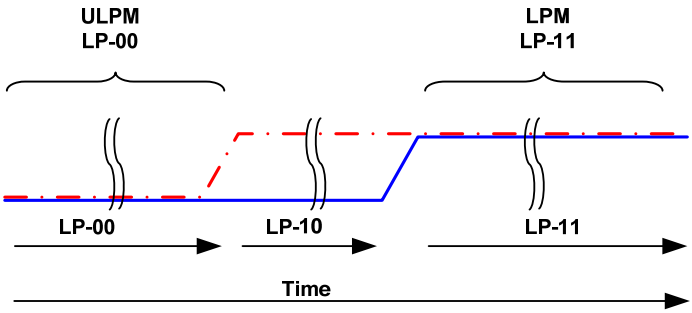


Figure: From ULPM to LPM

3) After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence is illustrated below.

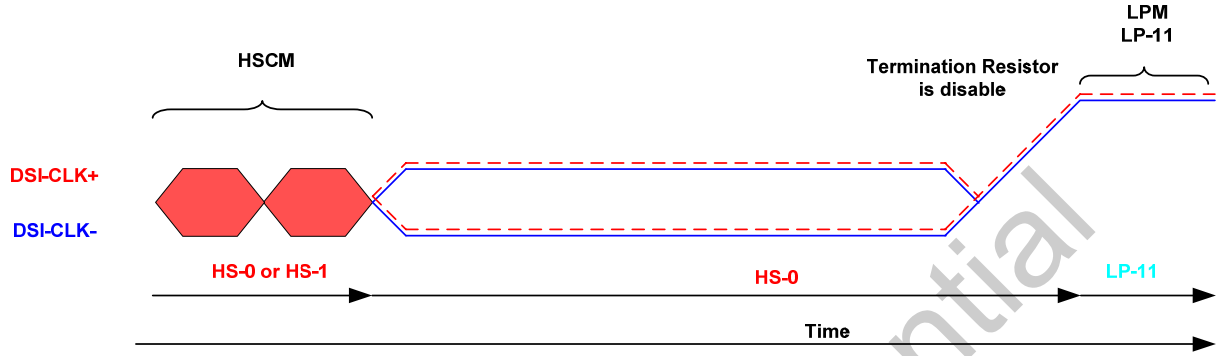


Figure: From HSCM to LPM

All three mode changes are illustrated a flow chart below.

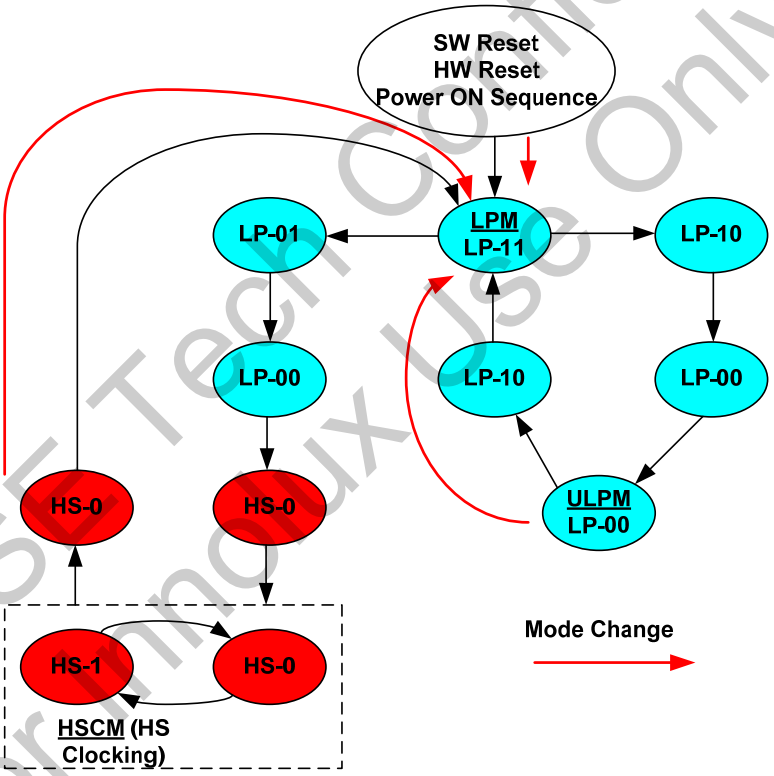


Figure: All three mode changes to LPM

Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM).

This sequence is illustrated below.

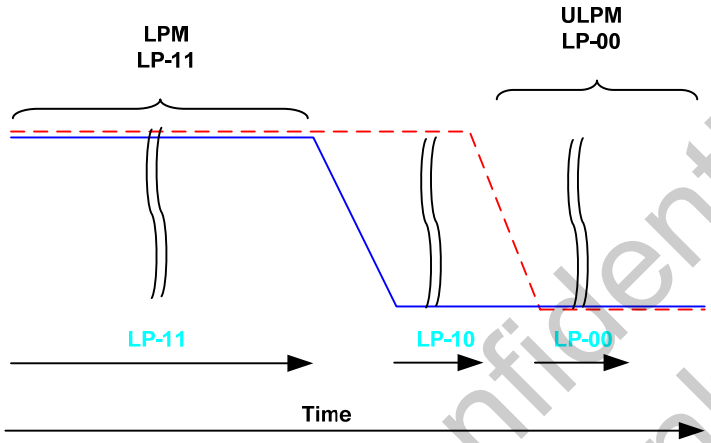


Figure: From LPM to UPLM

The mode change is also illustrated below:

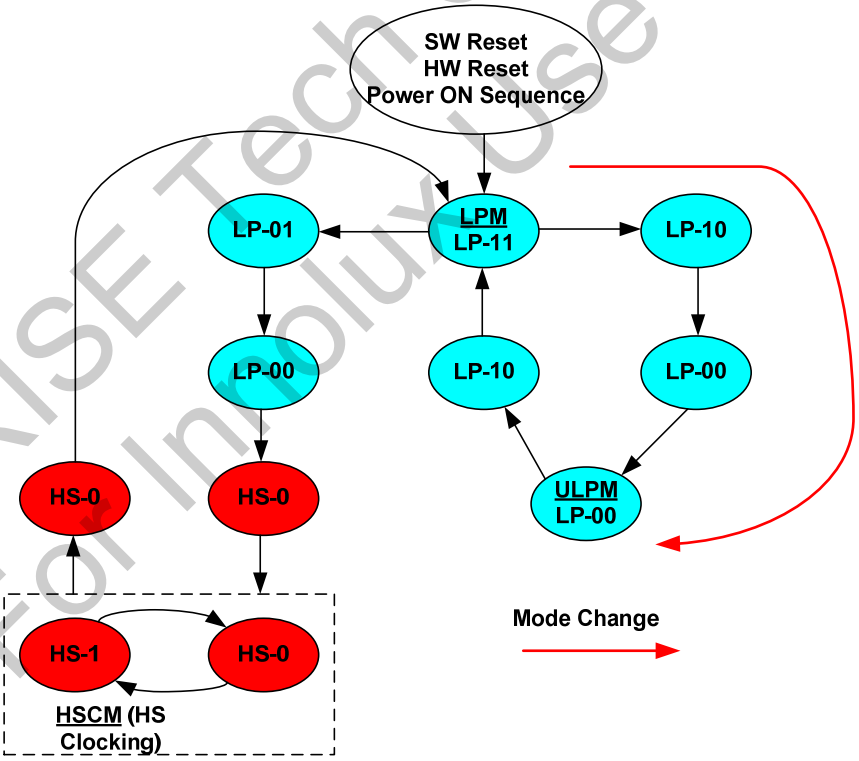


Figure: The mode change from LPM to UPLM

High-speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM).

This sequence is illustrated below.

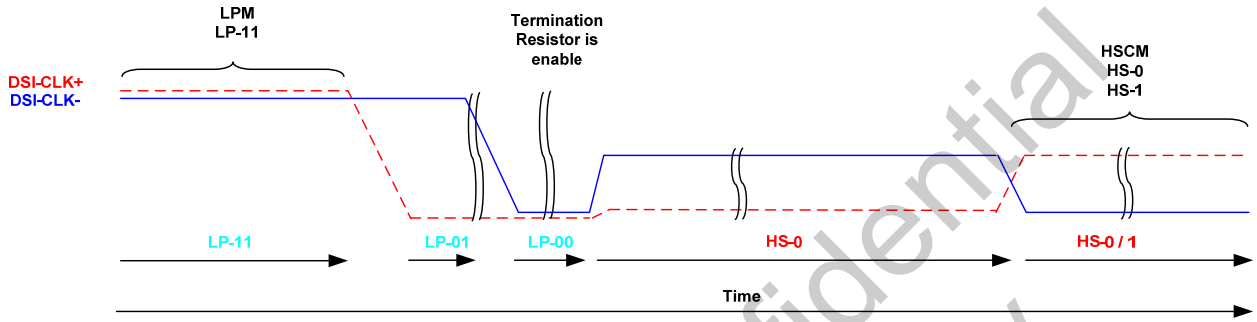


Figure: From LPM to HSCM

The mode change is also illustrated below:

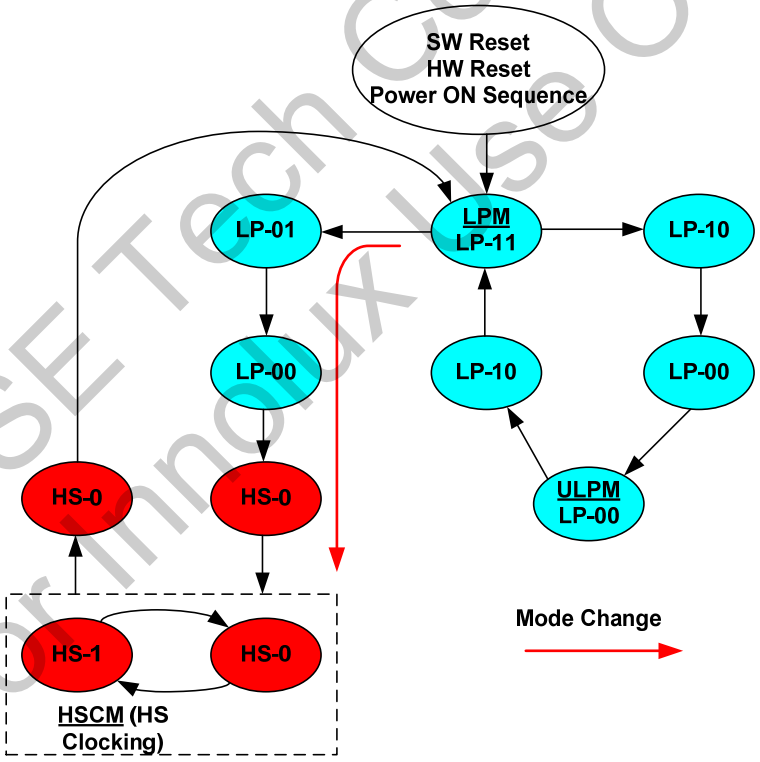


Figure: Mode change from LPM to HSCM

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped

The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0

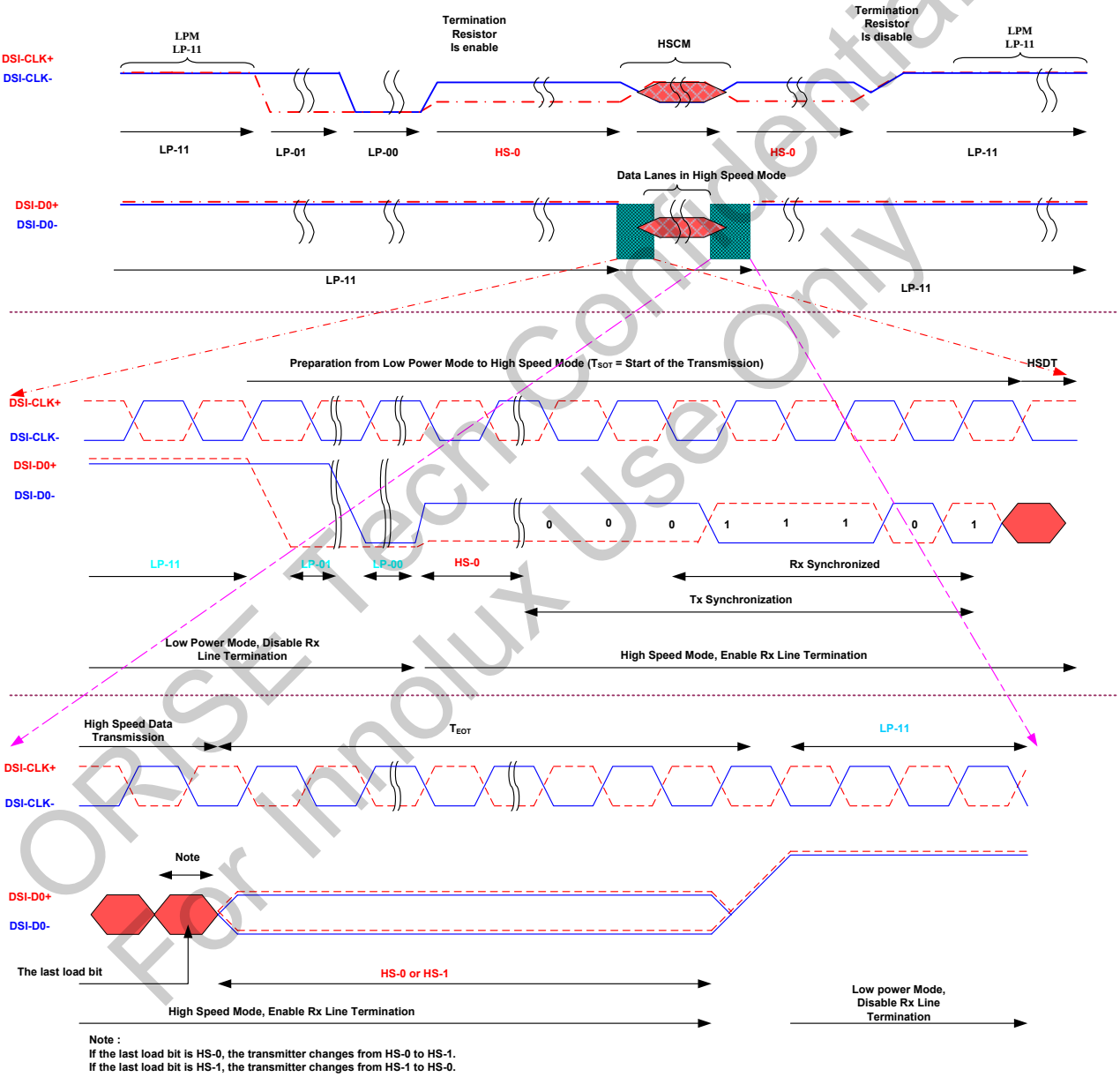


Figure: High speed clock burst

5.2.3. DSI data lanes

5.2.3.1. General

DSI-Dn+/- Data Lanes can be driven in different modes which are:

- Escape Mode (only support DSI_D0 data lane pair)
- High-Speed Data Transmission (support all data lane pairs)
- Bus Turnaround Request (only support DSI_D0 data lane pair)

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00	LP-00 =>LP-10 =>LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 =>LP-01 =>LP-00 =>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11 =>LP-10 =>LP-00 =>LP-10 =>LP-00	High-Z, Note

Table: Entering and leaving sequences

5.2.3.2. Escape modes

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. Escape mode operation shall be supported in the Forward direction and Reverse direction.
The basic sequence of the Escape Mode is as follow

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command , which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit.
- A payload stream if it is needed
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11
- End: LP-11

For Data Lane0, once Escape mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action.
All currently available Escape mode commands and actions are list below.

- Send or receive “Low-Power Data Transmission” (LPDT)
- Drive data lanes to “Ultra-Low Power State” (ULPS)
- Indicate “Remote Application Reset” (RAR), which is resetting the display module (same as S/W Reset function)
- Indicate “Tearing Effect” (TEE), which is used for a TE line event from the display module to the MCU,
- Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MCU.

The Stop state shall be used to exit Escape mode and cannot occur during Escape mode operation because of the Spaced-One-Hot encoding. Stop state immediately returns the Lane to Control mode. If the entry command doesn’t match a supported command, that particular Escape mode action shall be ignored and the receive side waits until the transmit side returns to the Stop state.
For Data Lane1 and 2, only support ULPS Escape mode commands.

- Drive data lanes to “Ultra-Low Power State” (ULPS)

The basic construction is illustrated below:

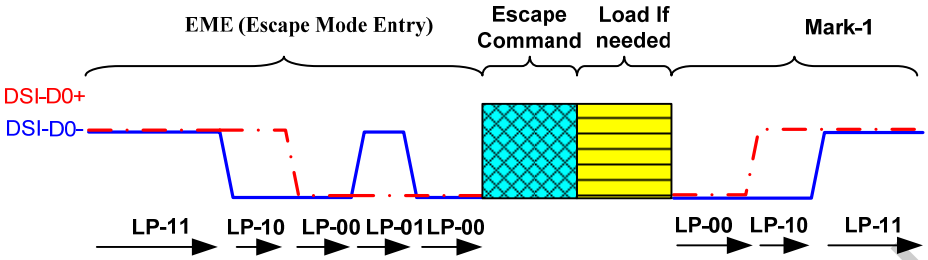


Figure: General Escape mode sequence

The number of the different Escape Commands is eight. These eight different Escape Commands can be divided 2 different groups: Mode or Trigger. Escape command groups are defined below.

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit => Last Bit Transmitted)
Low-Power Data Transmission	Mode	1110 0001bin
Ultra-Low Power Mode	Mode	0001 1110bin
Remote Application Reset	Trigger	0110 0010 bin
Tearing Effect	Trigger	0101 1101 bin
Acknowledge	Trigger	0010 0001 bin

Table: Escape commands

The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode.
The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Payload (Data):
  - One or more bytes
  - Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

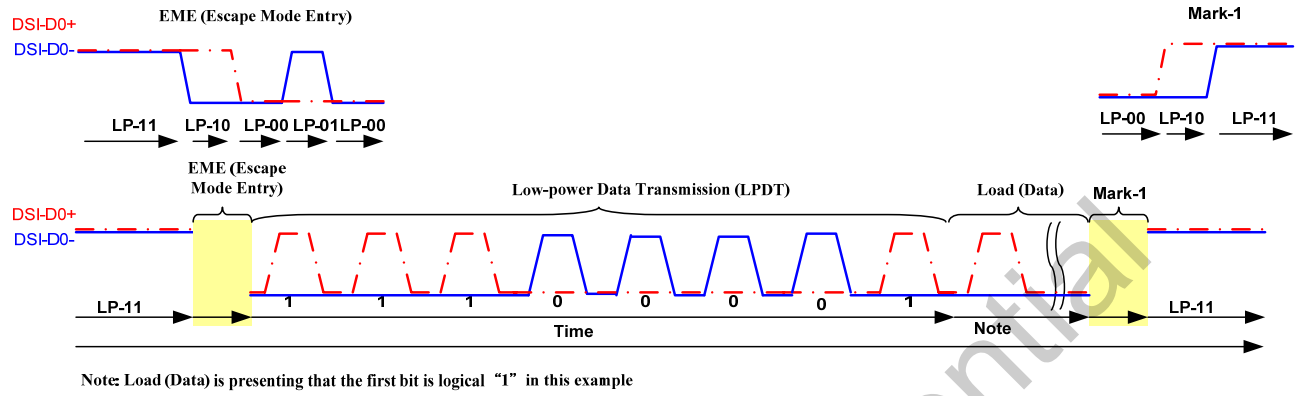


Figure: Low-power data transmission

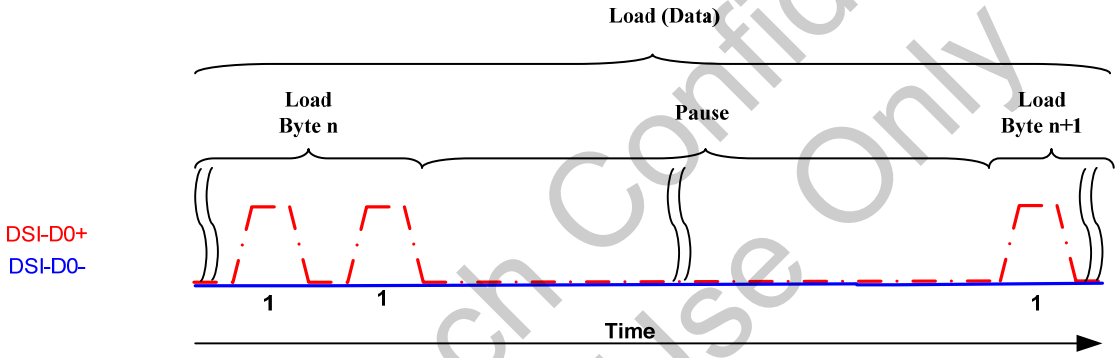


Figure: Pause (example)

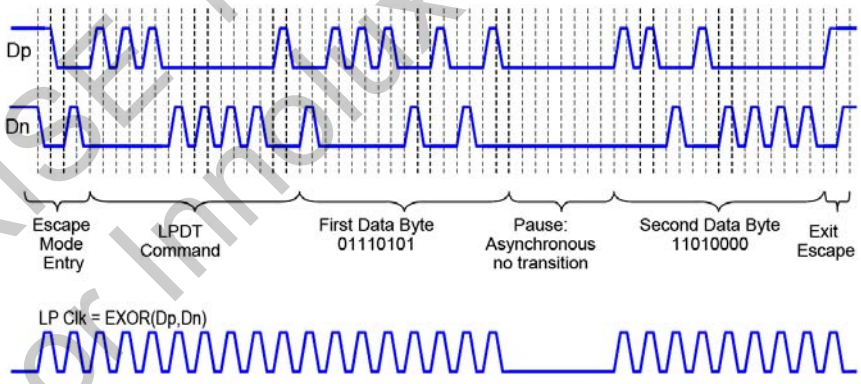


Figure: Two Data Byte Low-Power Data Transmission Example

Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

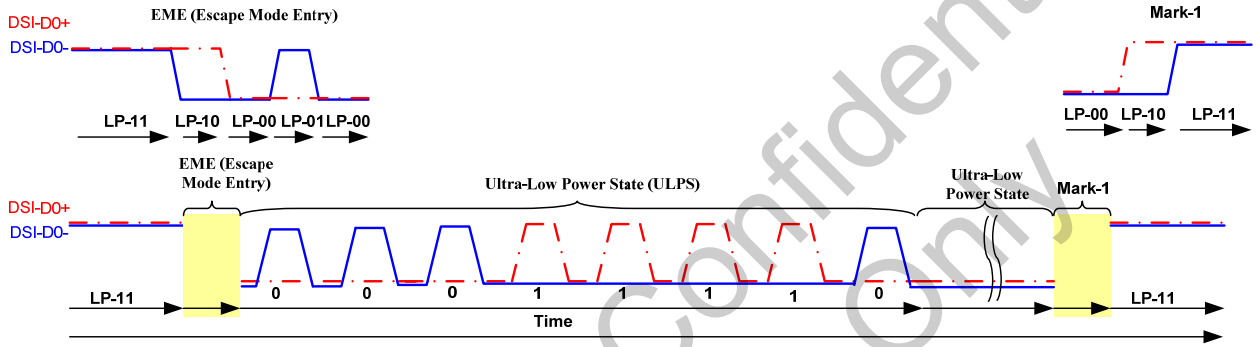


Figure: Ultra-low power state (ULPS)

Acknowledgement (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

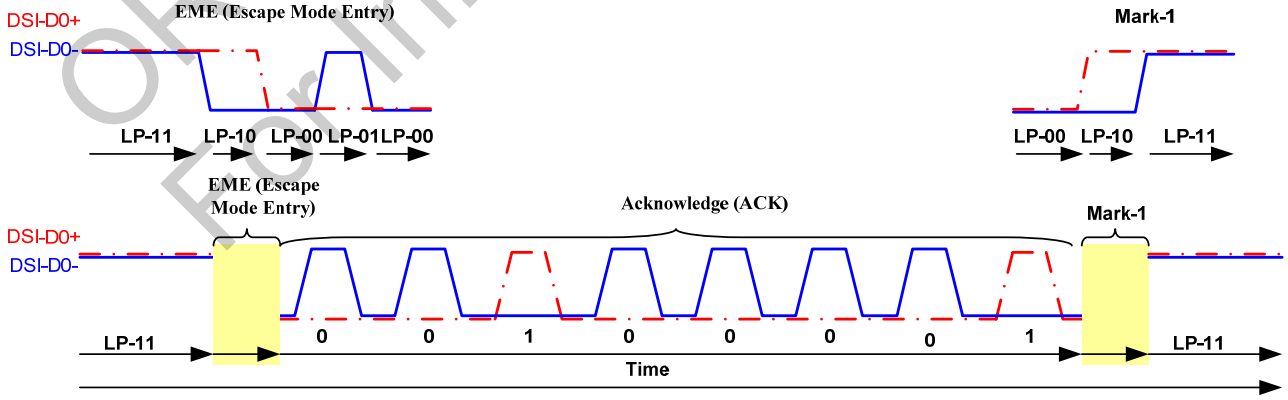


Figure: Acknowledgement (ACK)

5.2.3.3. High-Speed Data Transmission (HSDT)

Entering High-Speed Data Transmission (T_{sot} of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D0+/- of the display module are entering (TSOT) in the High-Speed Data Transmission(HSDT) as follows

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (TSOT of HSDT) sequence is illustrated below.

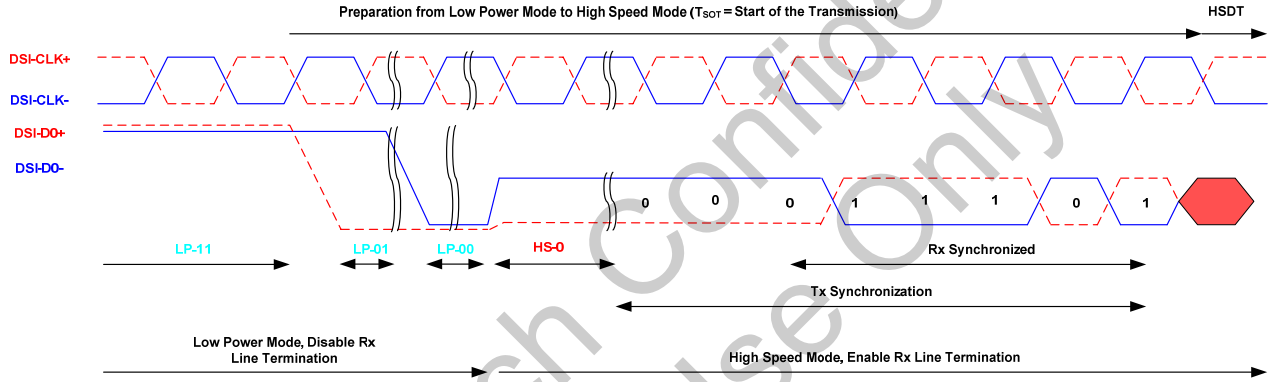


Figure: Tsot of HSDT

Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DSI- CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes

DSI-D0+/- are in LP-11 mode. See more information on chapter “7.2.2 High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D0+/- of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
  - MCU changes to HS-1, if the last load bit is HS-0
  - MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below

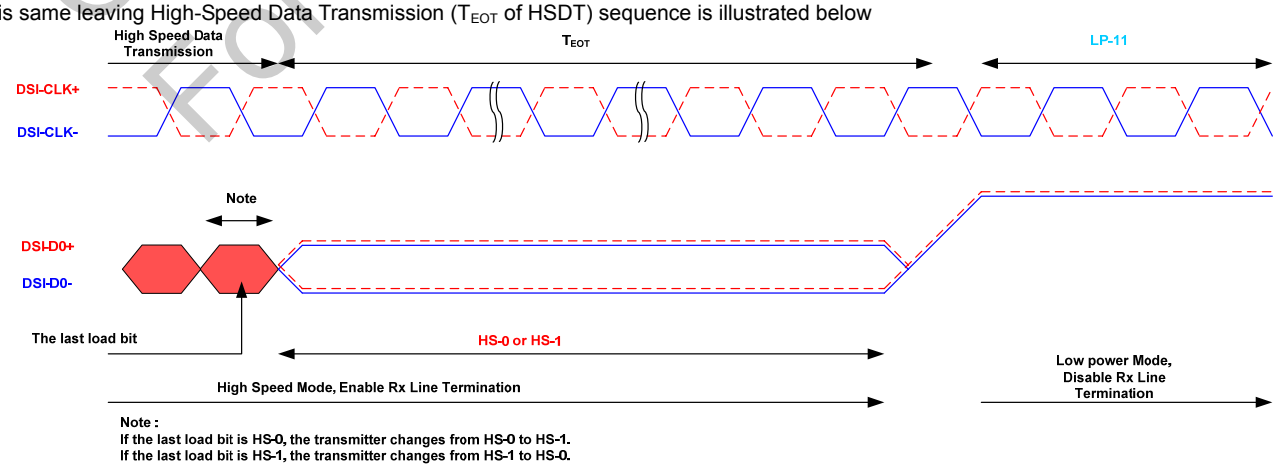


Figure: TEOT of HSDT

Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets.

These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter “Short Packet (SPa) and Long Packet (LPa) Structures“.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

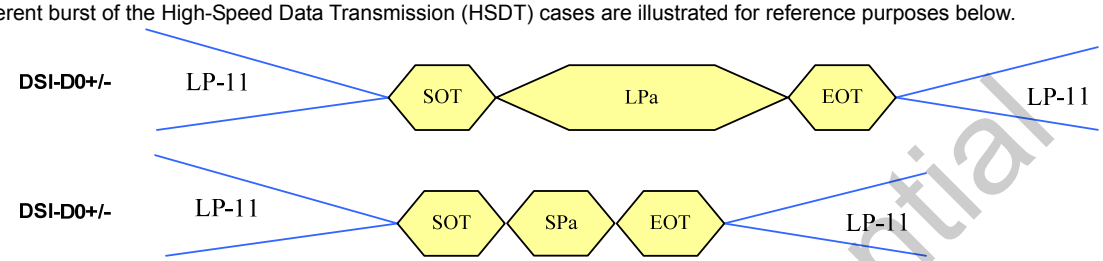


Figure: Single packet in HSDT

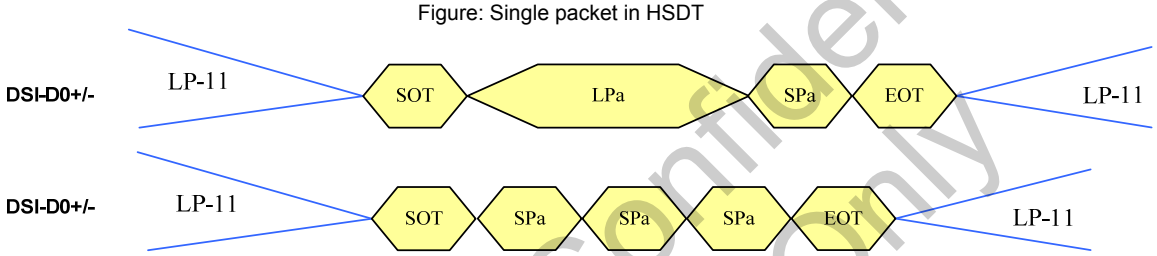


Figure: Multiple packets in HSDT

Figure: Packets with EoT package in HSDT

Abbreviation	Explanation
LP-11	Low Power Mode, Data lanes are ‘1’s (Stop Mode)
SOT	Start of the Transmission
LPa	Long Packet
SPa	Short Packet
EOT	End of the Transmission

Table: Abbreviations

5.2.3.4. Bus Turnaround (BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU and display module are using the same sequence when this bus turnaround procedure is used.

This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follows.

- Start (MCU): LP-11
- Turnaround Request (MCU): LP-11 =>LP-10 =>LP-00
- The MCU waits until the display module is starting to control DSI-D0+/- data lanes and the MCU stops to control DSI-D0+/- data lanes (= High-Z)
- The display module changes to the stop mode: LP-00 =>LP-10 =>LP-11

The same bus turnaround procedure (From the MCU to the display module) is illustrated below.

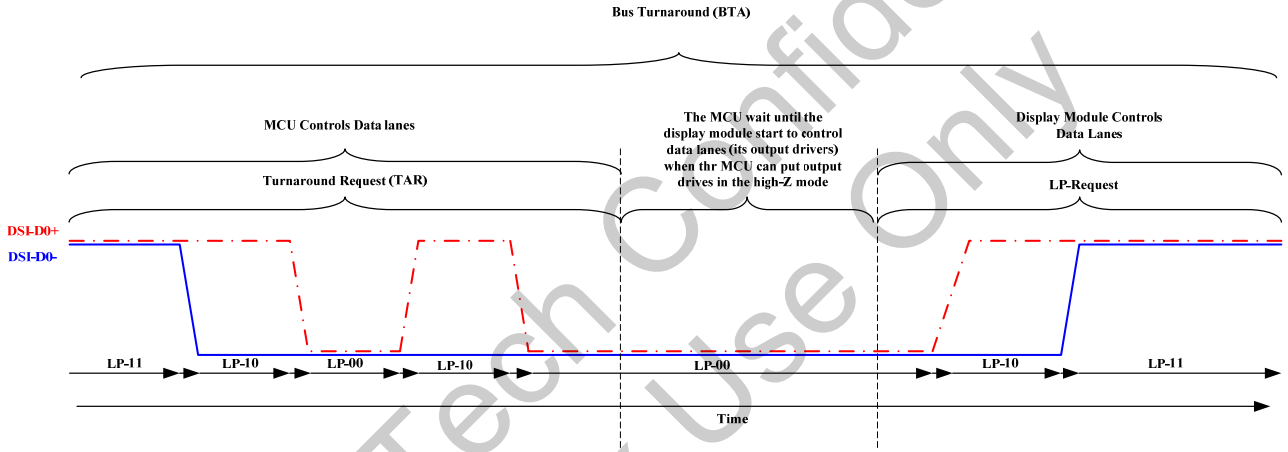


Figure: Bus turnaround procedure

5.2.4. Packet level communication

5.2.4.1. Short Packet (SPa) and Long Packet (LPa) structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

The lengths of the packets are

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

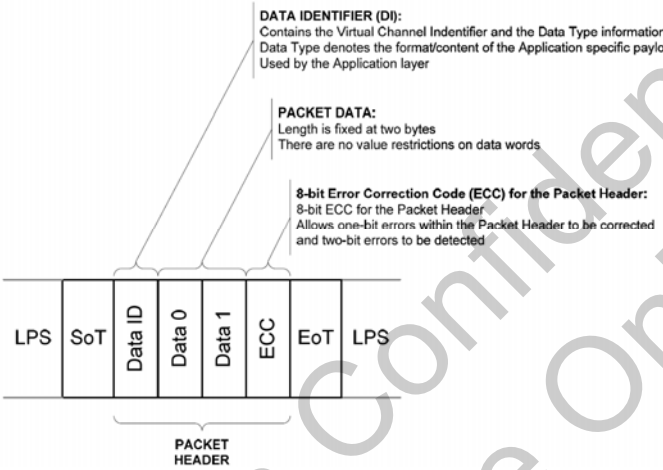


Figure: Short packet structure

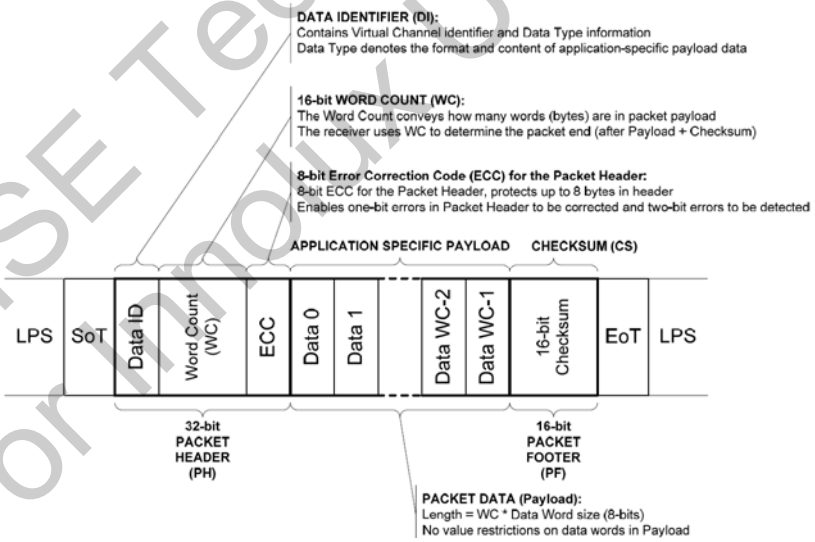


Figure:. Long packet structure

Note: Short Packet (SPa) Structure" and Long Packet (LPa) Structure" are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).

The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format. e.g.:

- LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11
- LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11
- LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11

Bit Order of the Byte on Packets

All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified.

Following figure shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

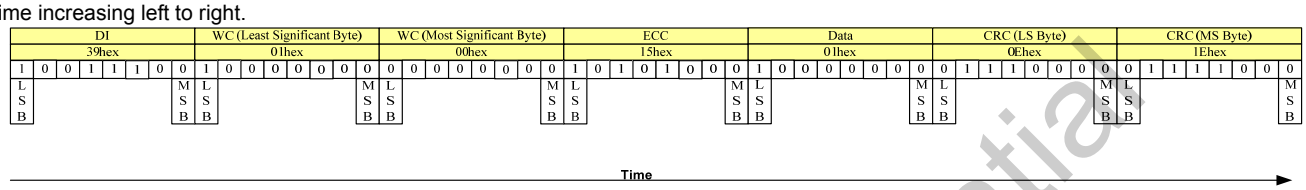


Figure: Bit order of the byte on packets

Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last.

e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

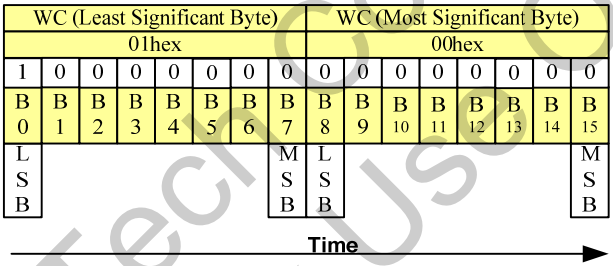


Figure: Byte order of the multiple byte information on packets

Packet Head (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

- 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)

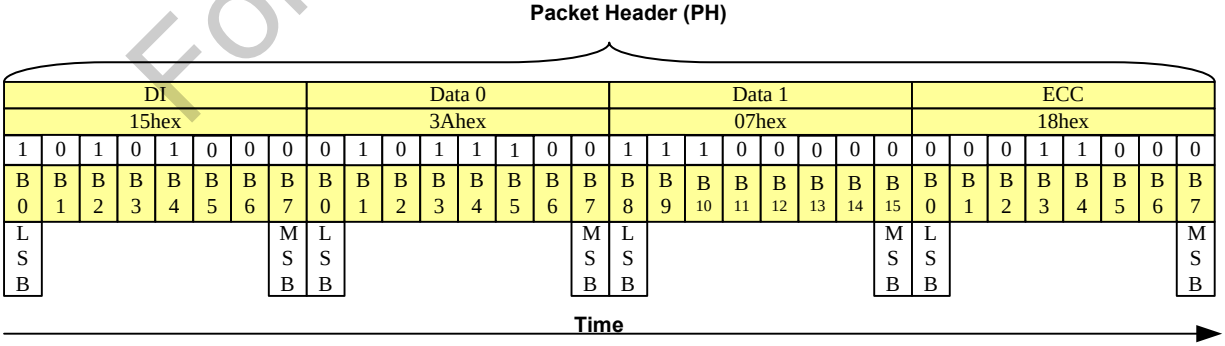


Figure: Packet head on short packet

Long Packet (LPa):

- 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)
- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)

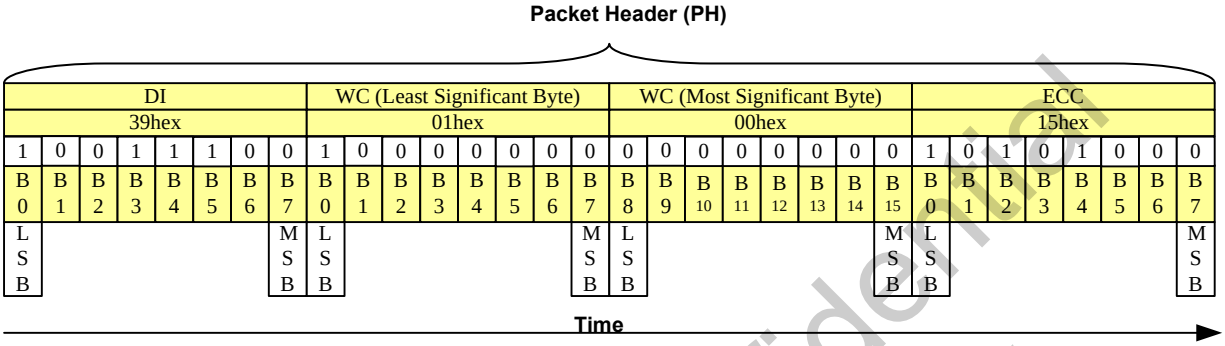


Figure: Packet head on long packet

Data Identification

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI[7...6]
- Data Type (DT), 6 bits, DI[5…0]

The Data Identification (DI) structure is illustrated on a table below.

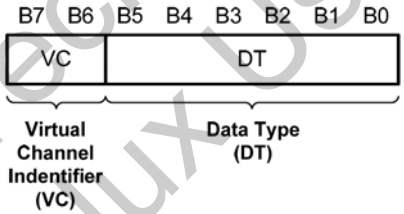


Table: Data identification structure

Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.

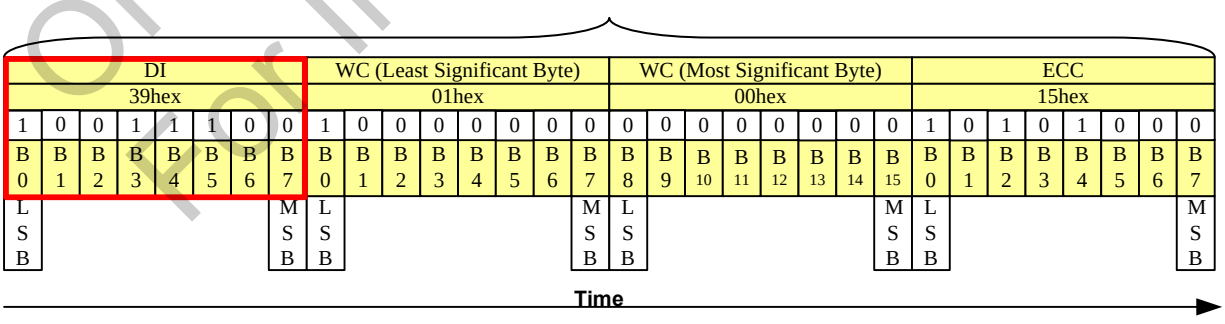


Figure: Data identification of the packet head

Virtual Channel (VC)

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals.

Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the MCU. Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

OTM2501A **only support VC code=00, package with other VC code(01/10/11) will be filter out.**

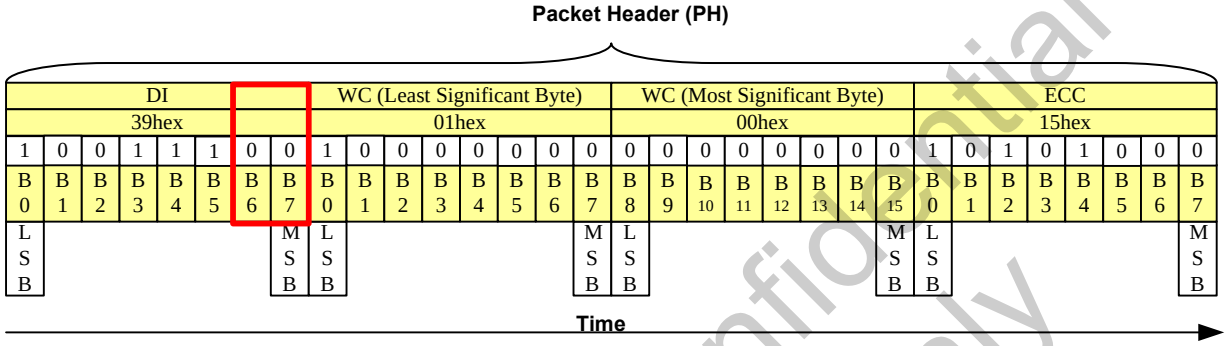


Figure: Virtual channel on the packet head

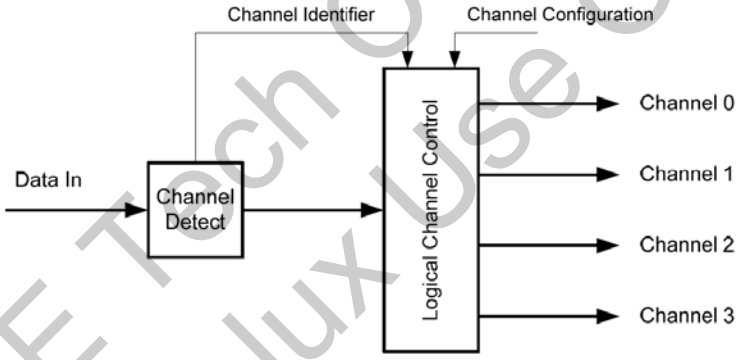


Figure: Virtual channel block diagram (receiver case)

Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.

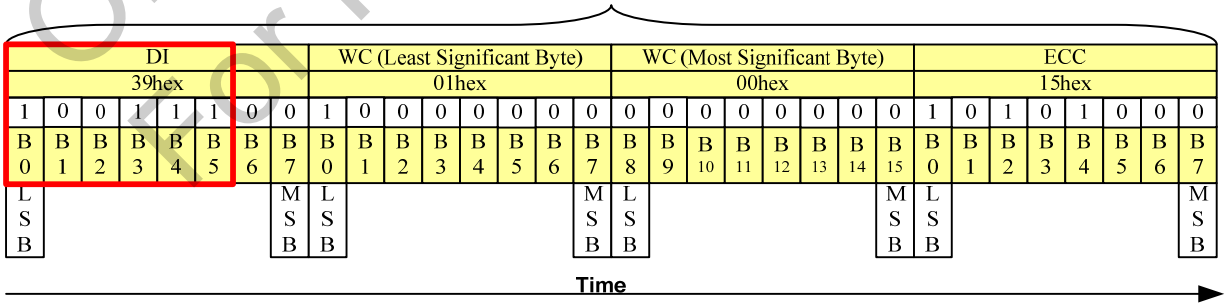


Figure: Data type on the packet head

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. These Data Type (DT) are defined on tables below.

From the MCU to the Display module		
Data Type (HEX)	Data Type (Binary)	Description
01h	00 0001	Sync Event, V Sync Start
11h	01 0001	Sync Event, V Sync End
21h	10 0001	Sync Event, H Sync Start
31h	11 0001	Sync Event, H Sync End
08h	00 1000	End of Transmission (EoT) packet
02h	00 0010	Color Mode (CM) Off Command
12h	01 0010	Color Mode (CM) On Command
22h	10 0010	Shut Down Peripheral Command
32h	11 0010	Turn On Peripheral Command
03h	00 0011	Generic Short WRITE, no parameters
13h	01 0011	Generic Short WRITE, 1 parameters
23h	10 0011	Generic Short WRITE, 2 parameters
04h	00 0100	Generic READ, no parameters
14h	01 0100	Generic READ, 1 parameters
24h	10 0100	Generic READ, 2 parameters
05h	00 0101	DCS WRITE, no parameters
15h	01 0101	DCS WRITE, 1 parameters
06h	00 0110	DCS READ, no parameters
37h	11 0111	Set Maximum Return Packet Size
09h	00 1001	Null Packet, no data
19h	01 1001	Blanking Packet, no data
29h	10 1001	Generic Long Write
39h	11 1001	DCS Long Write/Write_LUT Command packet
0Eh	00 1110	Packet Pixel Stream, 16-bit RGB, 5-6-5 Format
2Eh	10 1110	Loosely Packet Pixel Stream, 18-bit RGB, 6-6-6 Format
3Eh	11 1110	Packet Pixel Stream, 24-bit RGB, 8-8-8 Format

Table: Data type from the MCU to the display module

From the Display Module to the MCU		
Data Type (HEX)	Data Type (Binary)	Description
02h	00 0010	Acknowledge & Error Report
1Ch	01 1100	DCS Long READ Response
21h	10 0001	DCS Short READ Response, 1 byte returned
22h	10 0010	DCS Short READ Response, 2 byte returned

Table: Data type from the display module to the MCU

The receiver is ignored other Data Type (DT) if they are not defined on tables above. Host send “Generic Read” data type, OTM2501A will return DCS Read package to Host.

Packet data on the short packet

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

Bits of Data 1 are set to 00h, if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below.

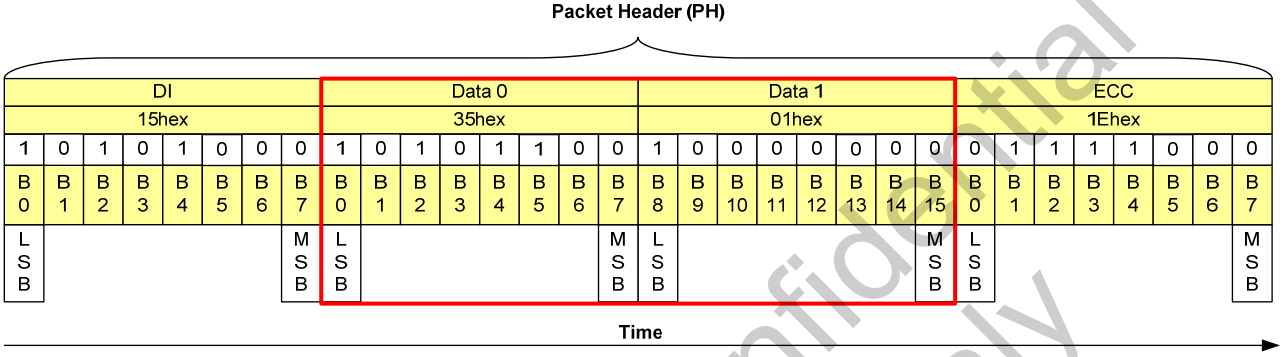


Figure: Packet data on the short packet, 2 bytes information

Packet Data (PD) information:

- Data 0: 10hex
- Data 1: 00hex (Null)

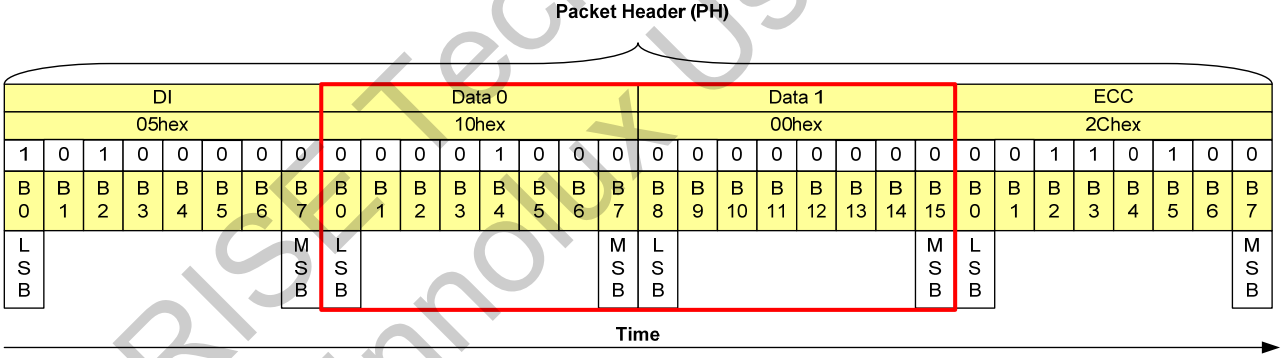


Figure: Packet data on the short packet, 1 bytes information

Word count on the long packet

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI)has indicated that Long Packet (LPa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH).

Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

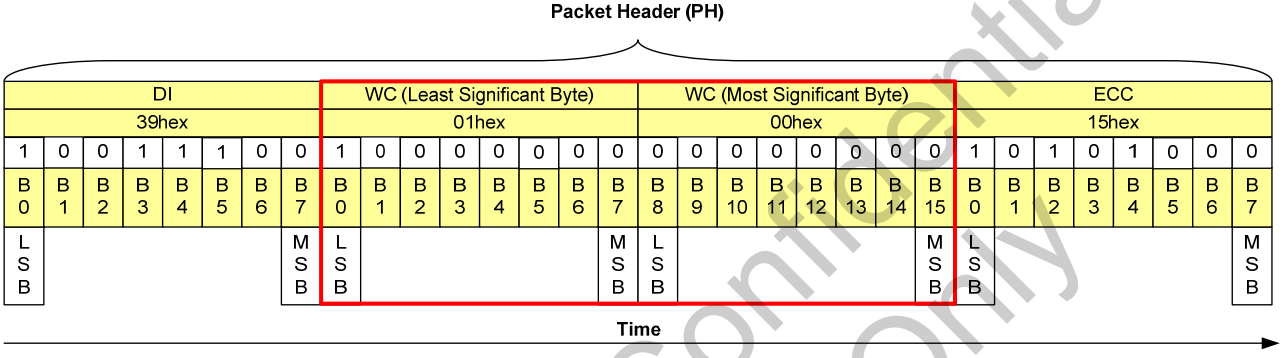


Figure: Word count on the long packet

Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors:

- Short Packet (SPa): Data Identification (DI) and Packet Data (PD) bytes (24 bits: D[23…0])
- Long Packet (LPa): Data Identification (DI) and Word Count (WC) bytes (24 bits: D[23…0])

D[23…0] is illustrated for reference purposes below.

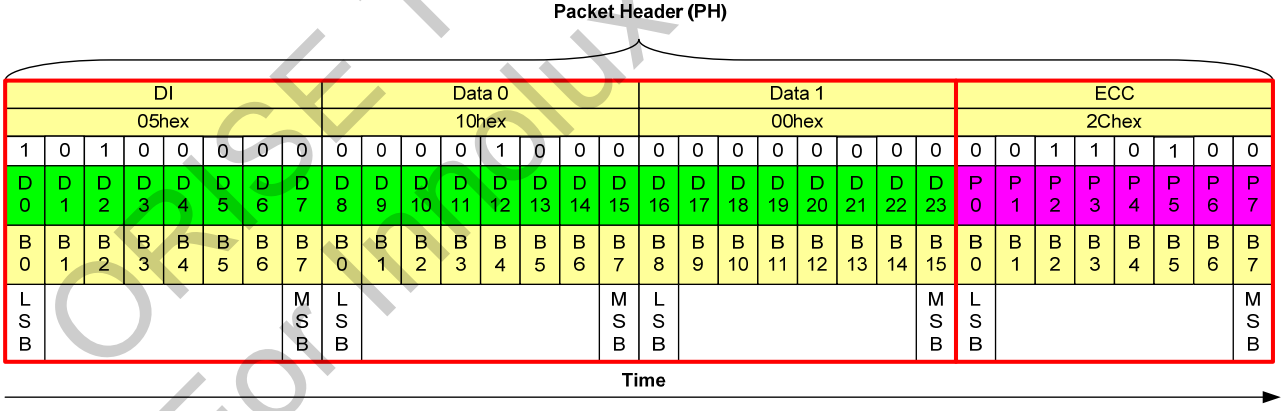


Figure: D[23:0] and P[7:0] on the short packet

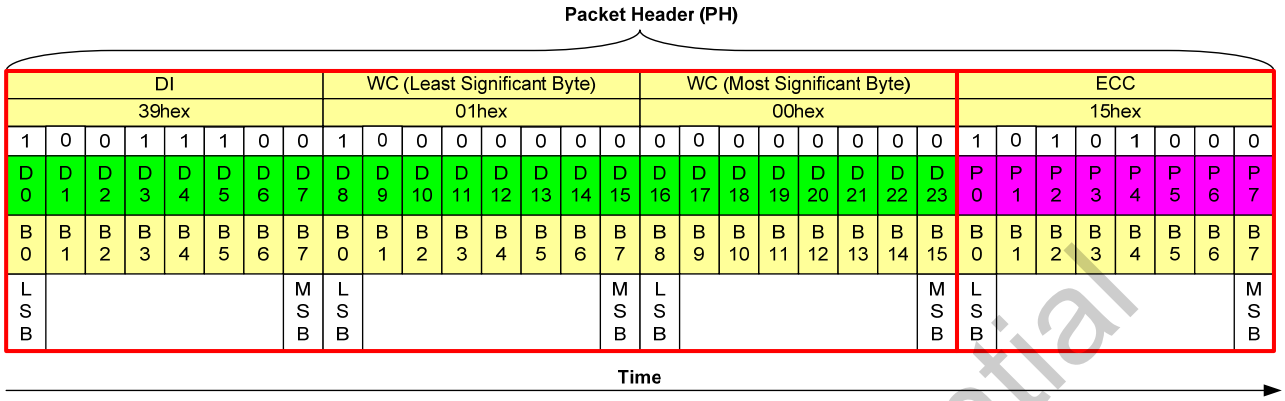


Figure: D[23:0] and P[7:0] on the long packet

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
- P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D[23…0]). Therefore, there is only needed 6 bits (P[5…0]) for Error Correction Code (ECC).

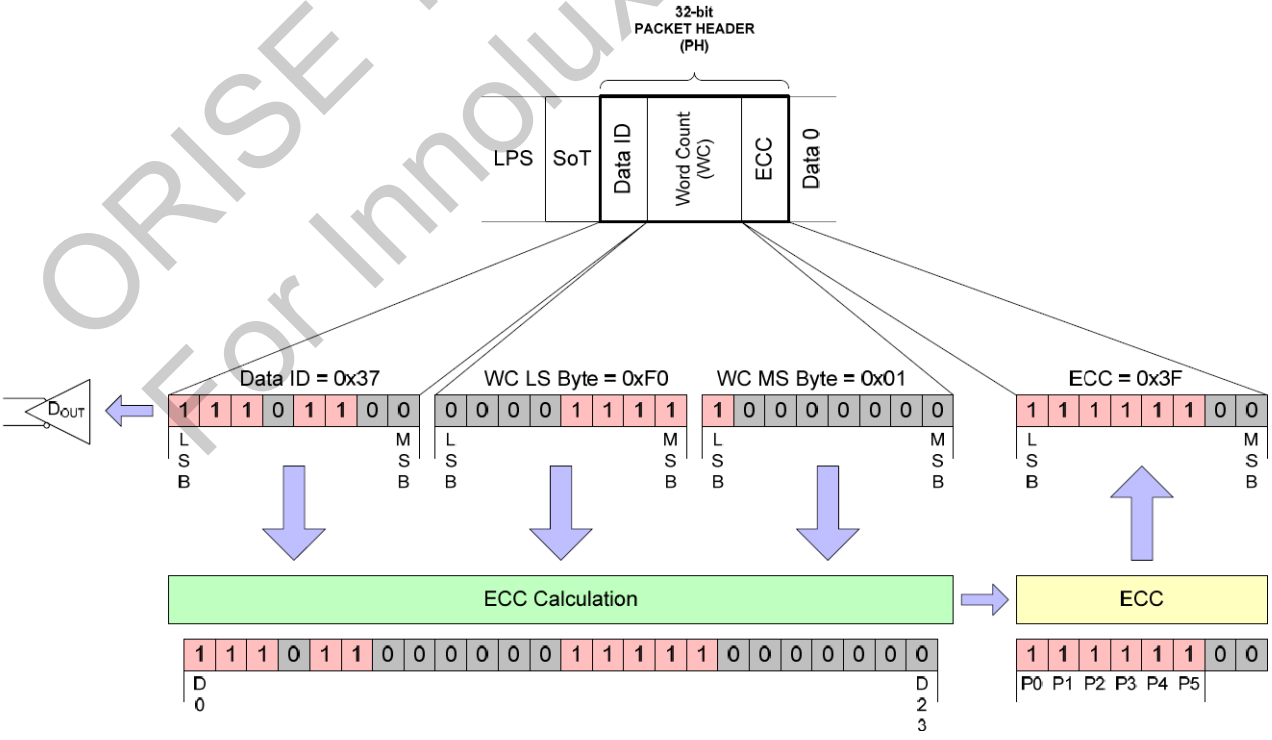


Figure: 24-bit ECC generation on TX side (Example)

Packet footer on the long packet

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa).

The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial X16+X12+X5+X0 as it is illustrated below.

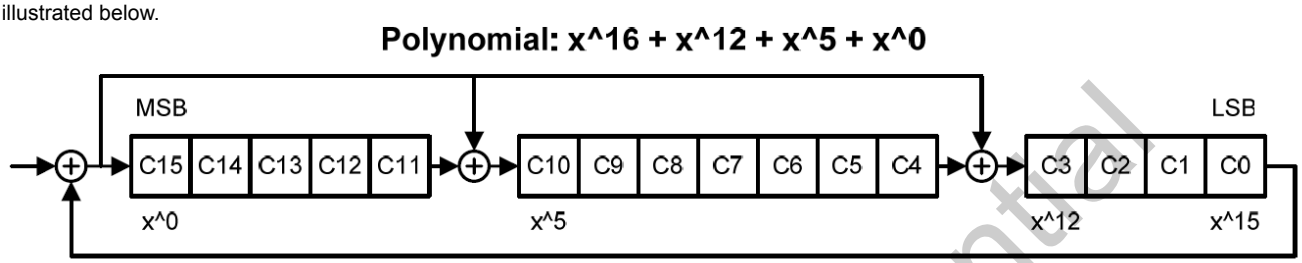


Figure: 16-bit cyclic redundancy check (CRC) calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations.

The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

5.2.4.2. Packet transmissions

Packet from the MCU to the display module

Display Command Set (DCS), which is defined on chapter “Instructions” is used from the MCU to the display module.

This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.

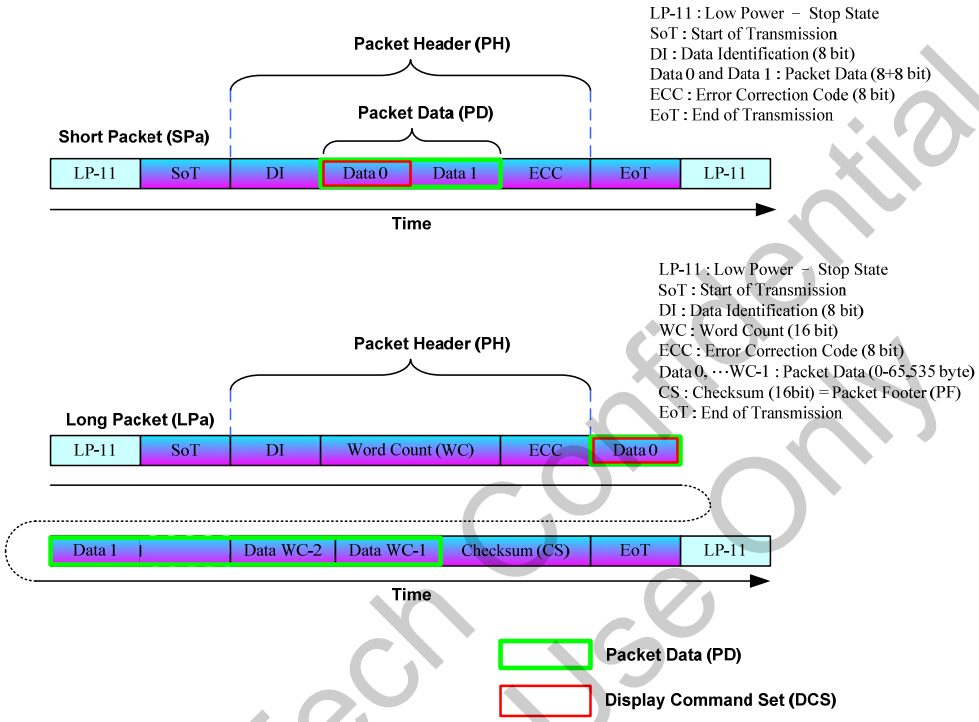


Figure: DCS on the short packet and long packet

Packet from the display module to the MCU

Used packet types

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS).

The used packet type is defined on Data Type (DT).

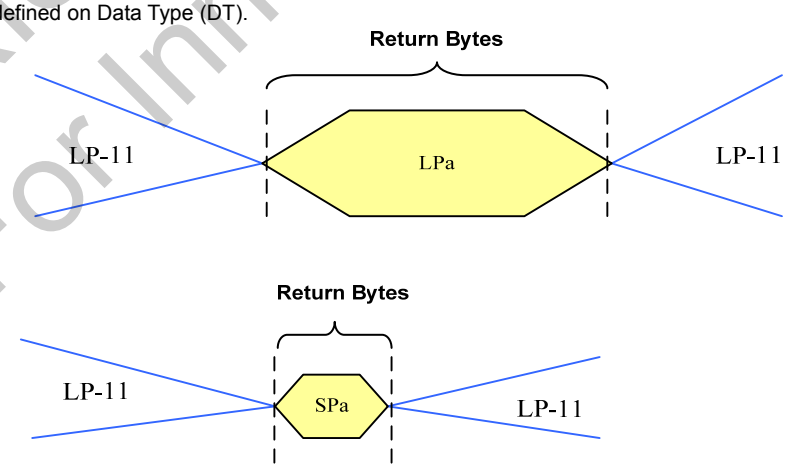


Figure: Return bytes on single packet

Acknowledge with Error Report (AwER)

"Acknowledge with Error Report" (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0010b), from the display module to the MCU.

The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to 1 , as they are defined on the following table.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Protocol Timer Rime-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, signal-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum (CRC) Error (only for Long Packet(LP))
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invaild
13	Invalid Transmission Length
14	Reserved, set to "0" internally
15	DSI Protocol violation

Figure: Acknowledge with error report for long packet response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Protocol Timer Rime-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, signal-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	set to "0" internally
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invaild
13	Invalid Transmission Length
14	Reserved, set to "0" internally
15	DSI Protocol violation

Figure: Acknowledge with error report for short packet response

These errors are only included on the last packet, which has been received from the MCU to the display module, before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 00 0010b
- Packet Data (PD)
  - Bit 8: ECC Error, single-bit (detected and corrected)
  - AwER: 0100h
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

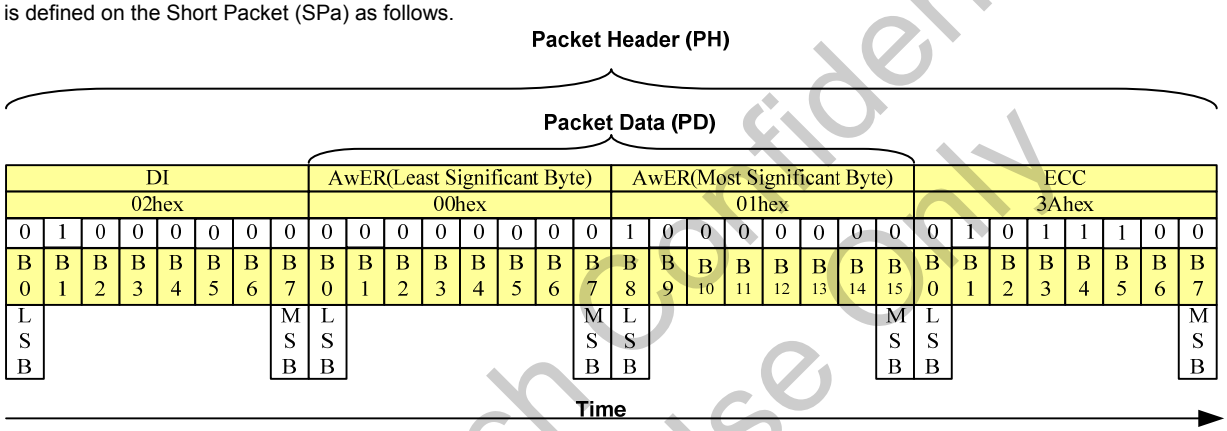


Figure: Acknowledge with error report – example

5.2.5. Customer-defined generic read data type format

The short packet of Data Type 24h (Generic READ, 2 parameters) specifies the register content for read and the Nth parameter that will begin reading. After Data Type 24h is received, BTA is executed. Then, the Nth parameter becomes the first data, and the number of data of WC (word count) value is output.

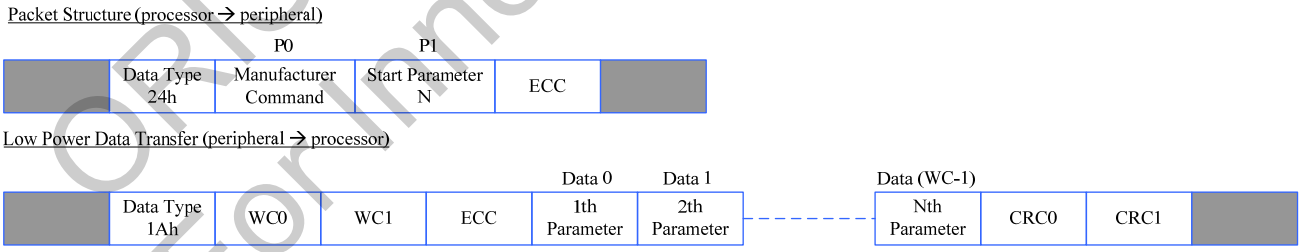


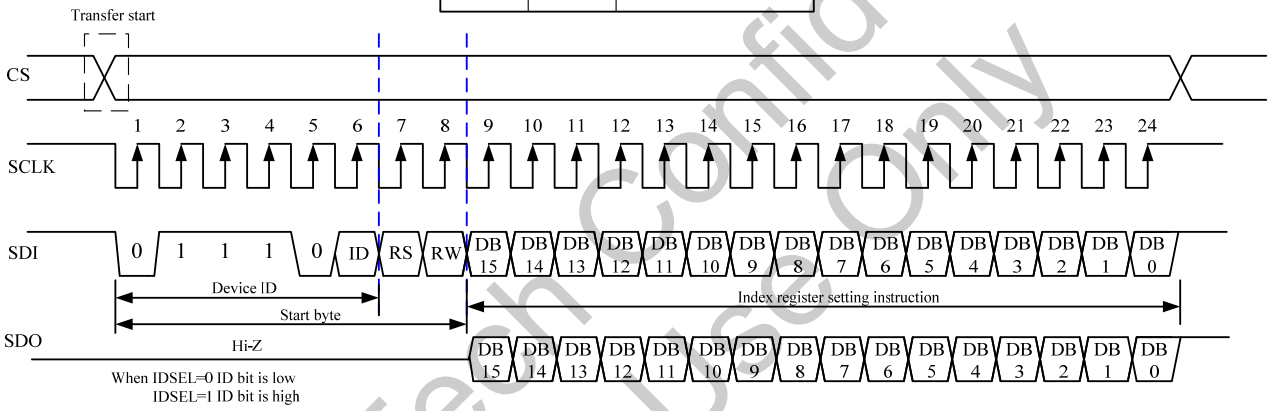
Figure: Generic read data type format

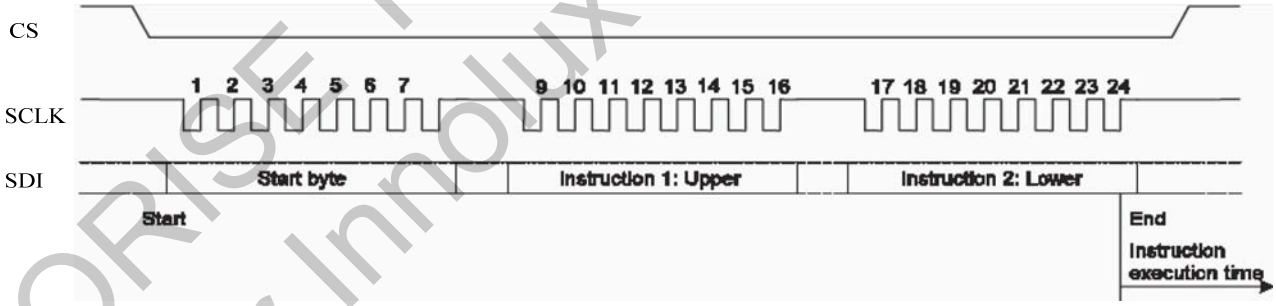
5.3. Series Interface (SPI)

The serial interface is used to communication between the micro controller and the LCD driver chip. It contains CSX (chip select), SCL (serial clock), SDI (serial data input) and SDO (serial data output). Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary. If the host places the SDI line into high-impedance state during the read intervals, then the SDI and SDO can be tied together.

5.3.1. 16bit-index SPI (IM=2'b01)

RS	RW	Function
0	0	Set to index register
0	1	-
1	0	Write to instruction
1	1	Read to ID



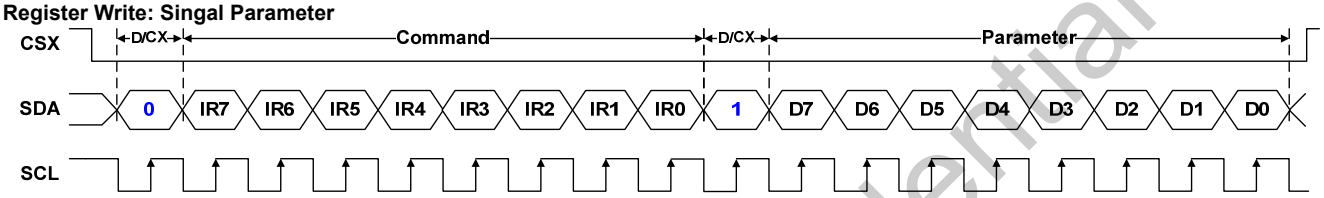


5.3.2. 3-wire 9-bits SPI (IM=2'b10, 2'b11)

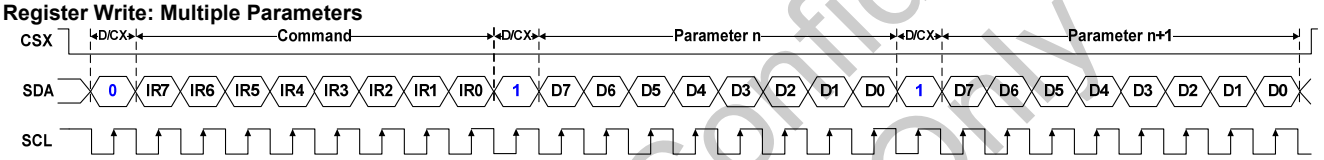
5.3.2.1. SPI Write Mode

The write mode of the interface means the micro controller writes commands and data to the OTM3201A. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. When CSX is high, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling CSX edge, SCL can be high or low. SDI / SDO is sampled at the rising edge of SCL.

Register Write: Singal Parameter



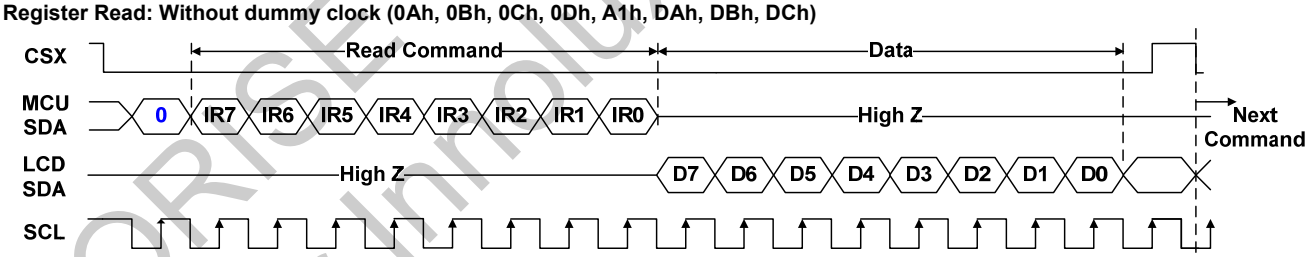
Register Write: Multiple Parameters



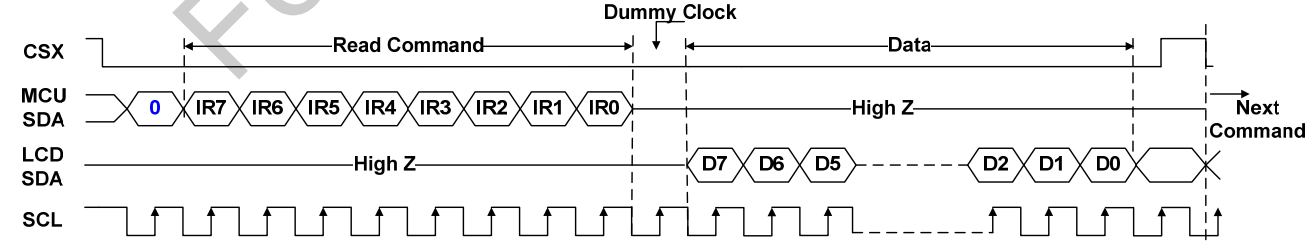
5.3.2.2. SPI Read Mode

The read mode of the interface means that the micro controller reads register value from the OTM3201A. To do so the micro controller first has to send a command and then the following byte is transmitted in the opposite direction. After that CSX is required to go high before a new command is send. The OTM3201A samples the SDI (input data) at the rising edges, but shifts SDO (output data) at the falling SCL edges. Thus the micro controller is supported to read data at the rising SCL edges. After the read status command has been sent, the SDI line must be set to tri-state no later than at the falling SCL edge of the last bit.

Register Read: Without dummy clock (0Ah, 0Bh, 0Ch, 0Dh, A1h, DAh, DBh, DCh)

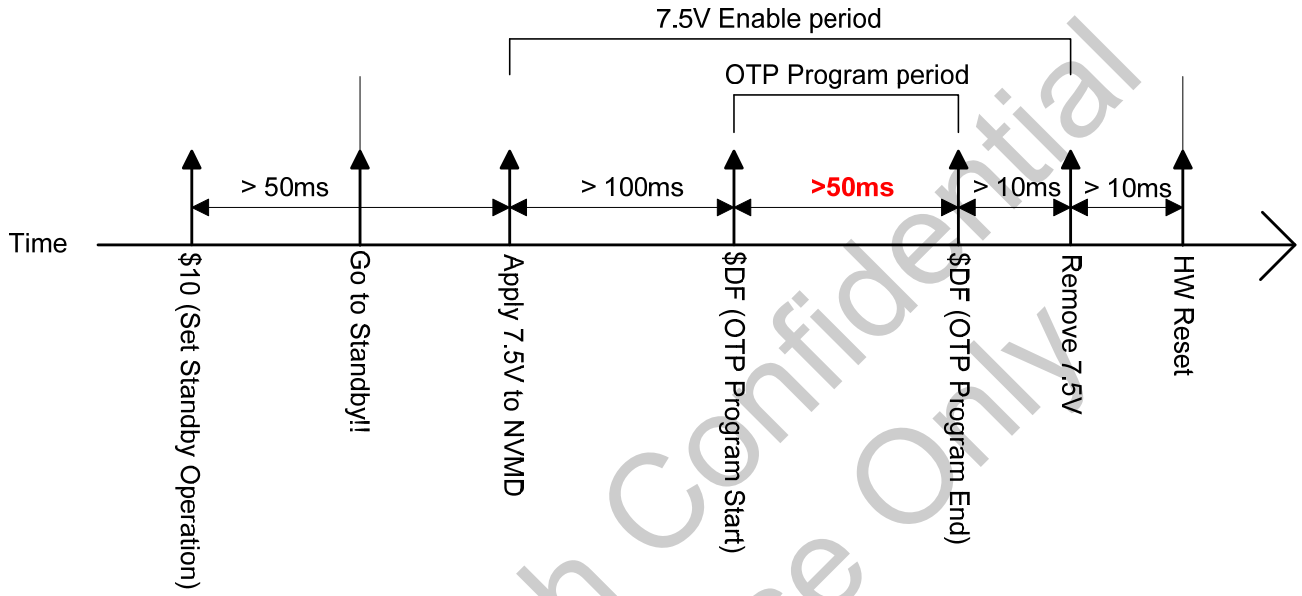


Register Read: With dummy clock (CMD2)

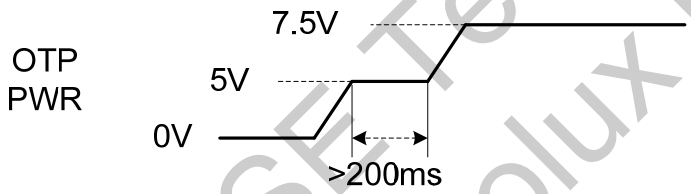


5.4. NVM Programming Sequence

Sequence of NVM is descripted as following. The first step to program NVM is “write Standby operation command”. After this command, overthan 50ms must be hold to make sure that the dirver IC is in Standby mode. Another 100ms is necessary to make sure NVMD is stable to 7.5V. NVM program command can be written after stable 7.5V voltage existed. Then, NVM Program End command is written after **50ms**. 7.5V voltage is removed after Program End command, and then H/W reset to verify the NVM memory.



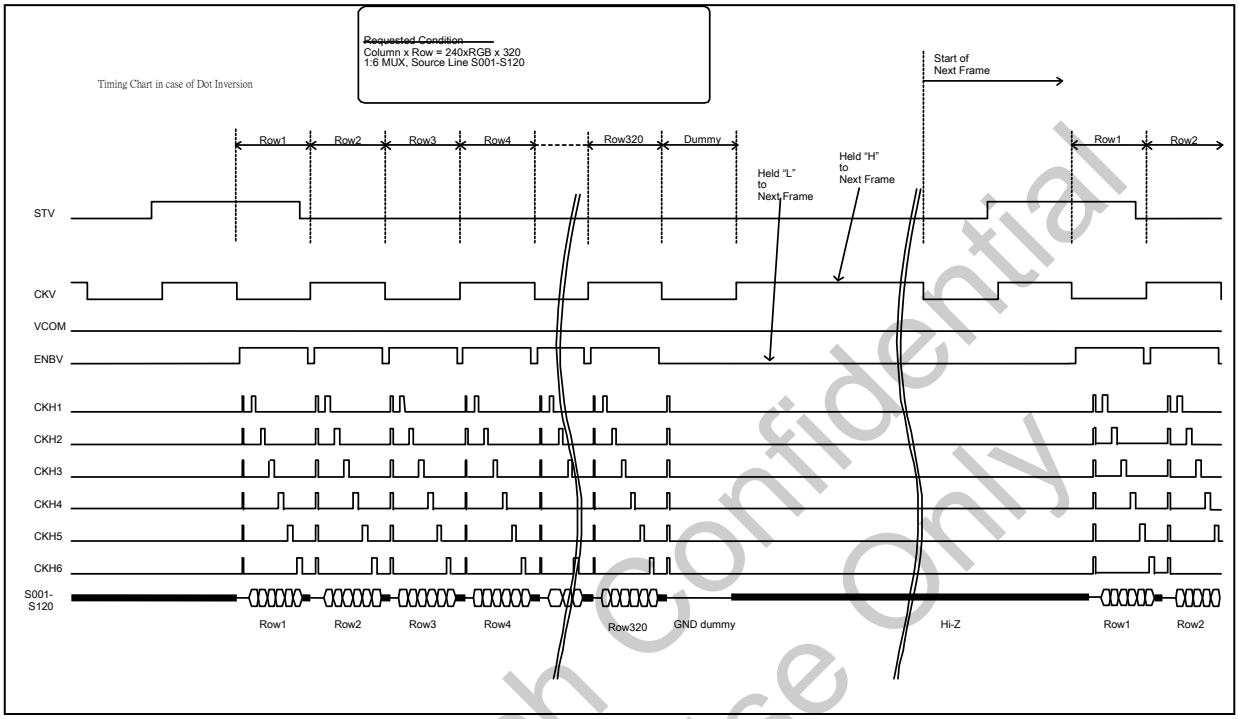
MTP Power on sequence



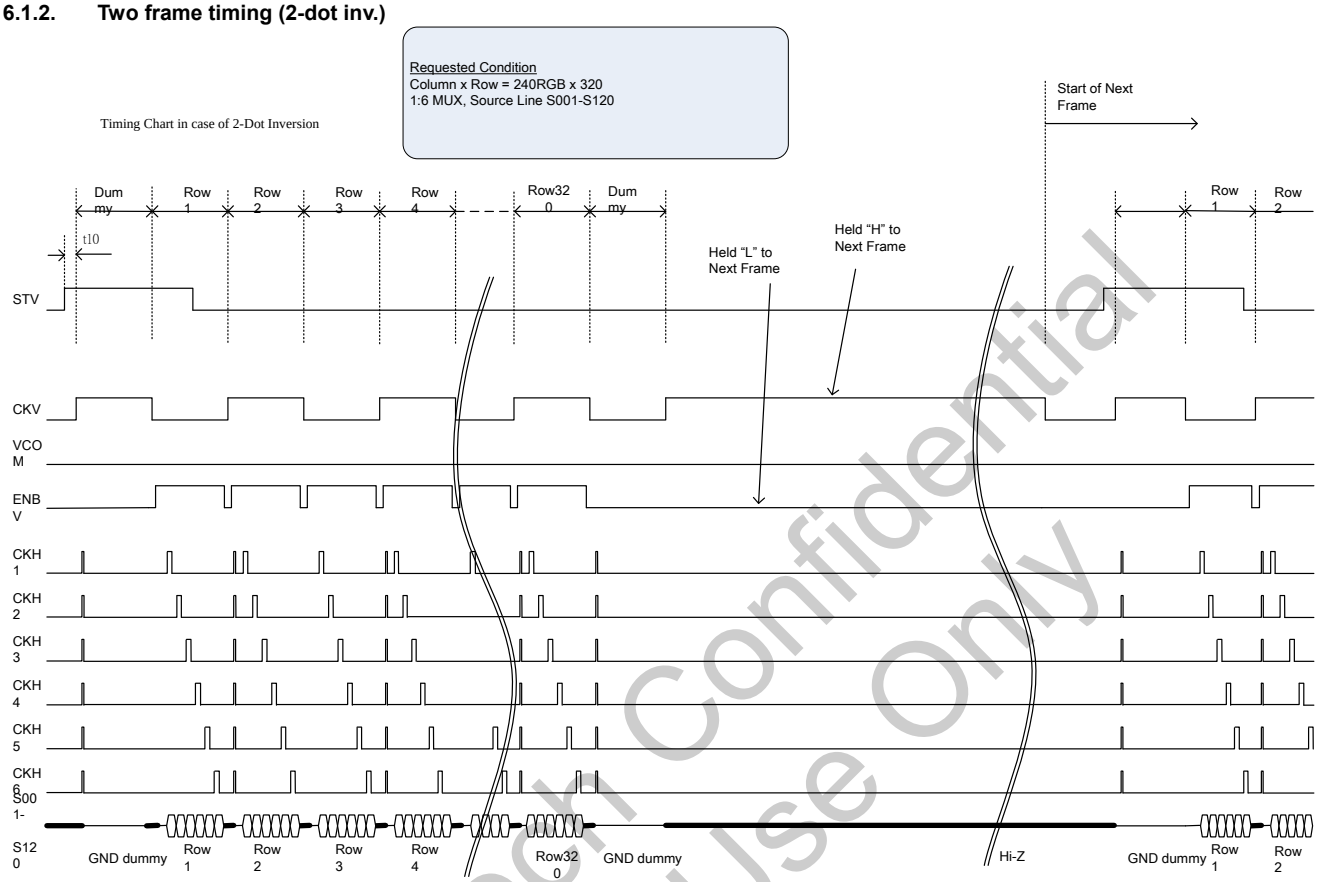
6. TCON TIMING

6.1. Dot Inversion, 2Dot Inversion And Column Inversion

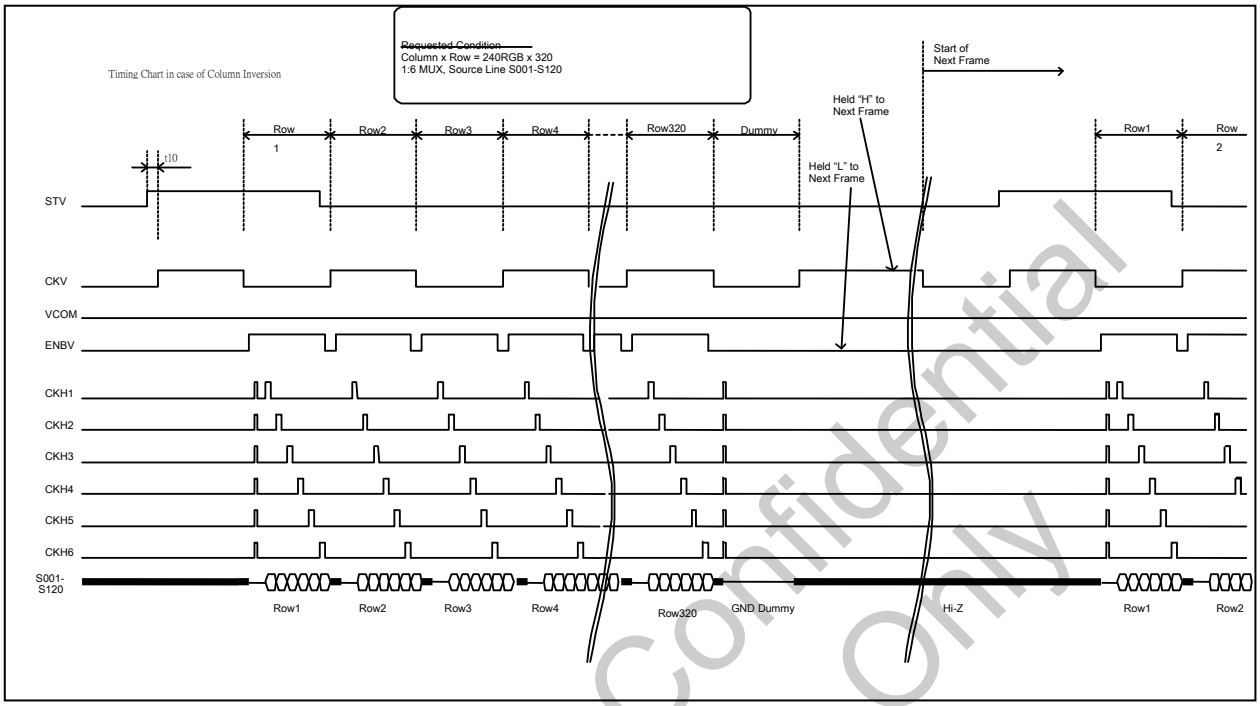
6.1.1. Two frame timing (dot inv.)



6.1.2. Two frame timing (2-dot inv.)

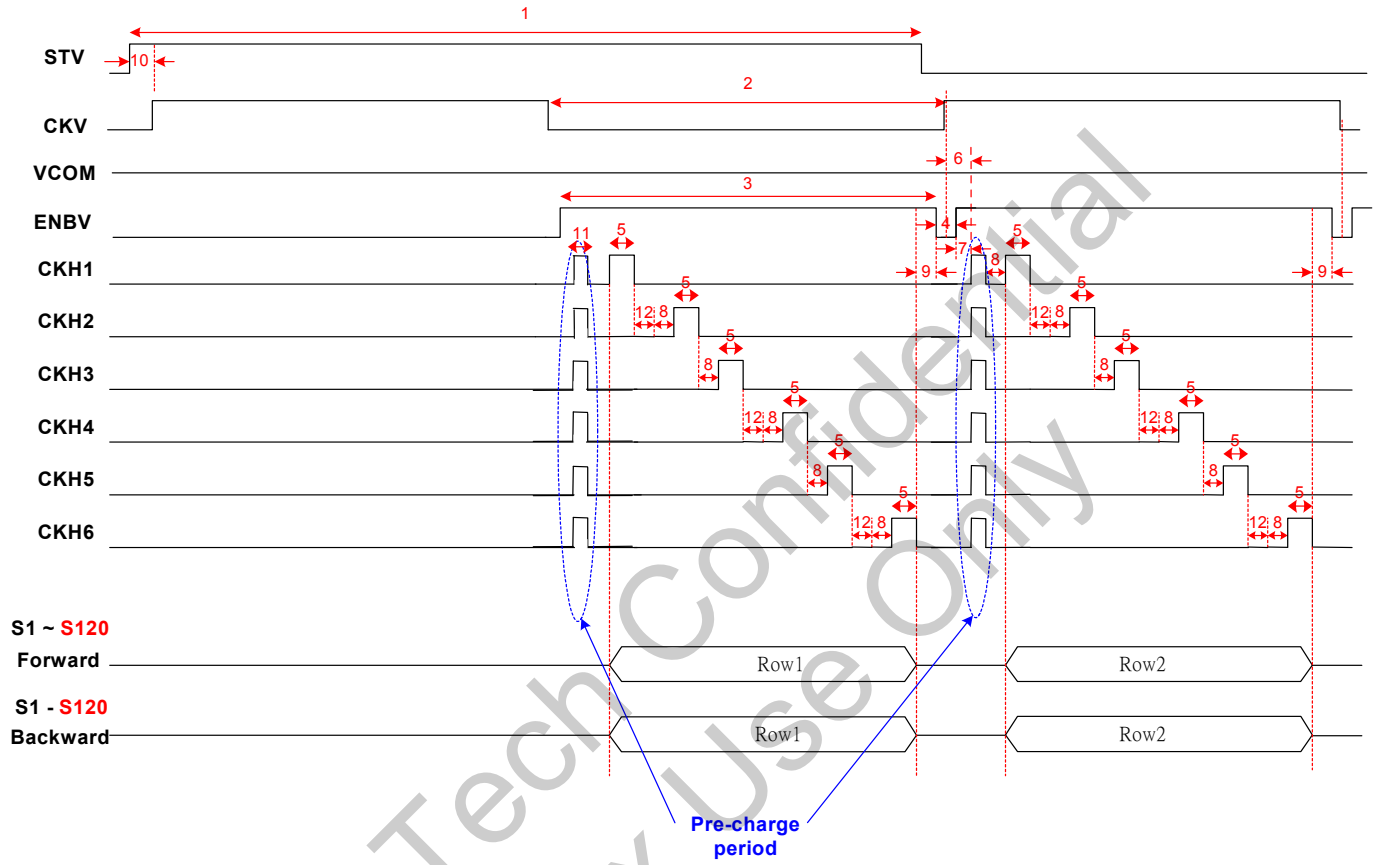


6.1.3. Two frame timing (column inv)



6.2. TCON Control Signals Timing

6.2.1. RESOL[2:0]=000 **(QVGA Portrait type, 1:6 MUX)**



Note：

1. This figure is base on Same Color MUX and t12 must insert every polarity change.
2. The source output is GND in pre-charge period.
3. The pre-charge period (CKH) is settable to turn on/off in normal & idle mode.
4. PRECH signal is settable to turn on/off in normal & idle mode.

Panel requirement (Frame freq. = 60Hz for 240xRGBx320) **(Blanking line: V=6, H=40)** **Unit: DCK**

DCK=182ns	1	2	3	4	5	6	7	8	9	10	11	12
Typical	560	280	264	16	34	8	0	4	19	11	5	4
Typical(us)	101.92	50.96	48.05	2.91	6.19	1.46	0	0.73	3.46	2.00	0.91	0.73
Maximum(us)												
Minimum(us)												
Step(us)												

RESOL[2:0]=001 240xRGBx400(1：6 MUX)

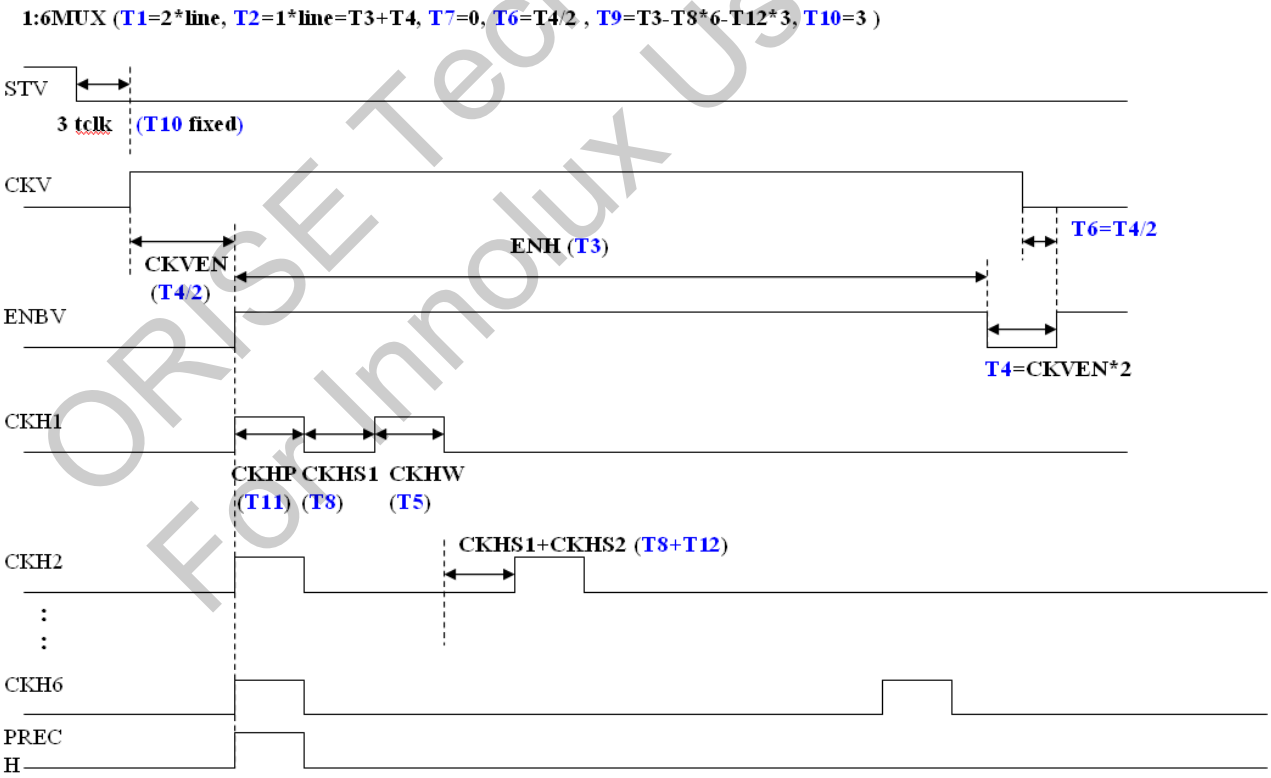
Panel requirement (Frame freq. = 60Hz for 240xRGBx400) (Blanking line: V=6, H=40) Unit: DCK

DCK=146ns	1	2	3	4	5	6	7	8	9	10	11	12
Typical	560	280	260	20	31	10	0	5	22	14	7	5
Typical(us)	81.76	40.88	37.96	2.92	4.53	1.46	0	0.73	3.21	2.04	1.02	0.73
Maximum(us)												
Minimum(us)												
Step(us)												

RESOL[2:0]=010 240xRGBx432(1：6 MUX)

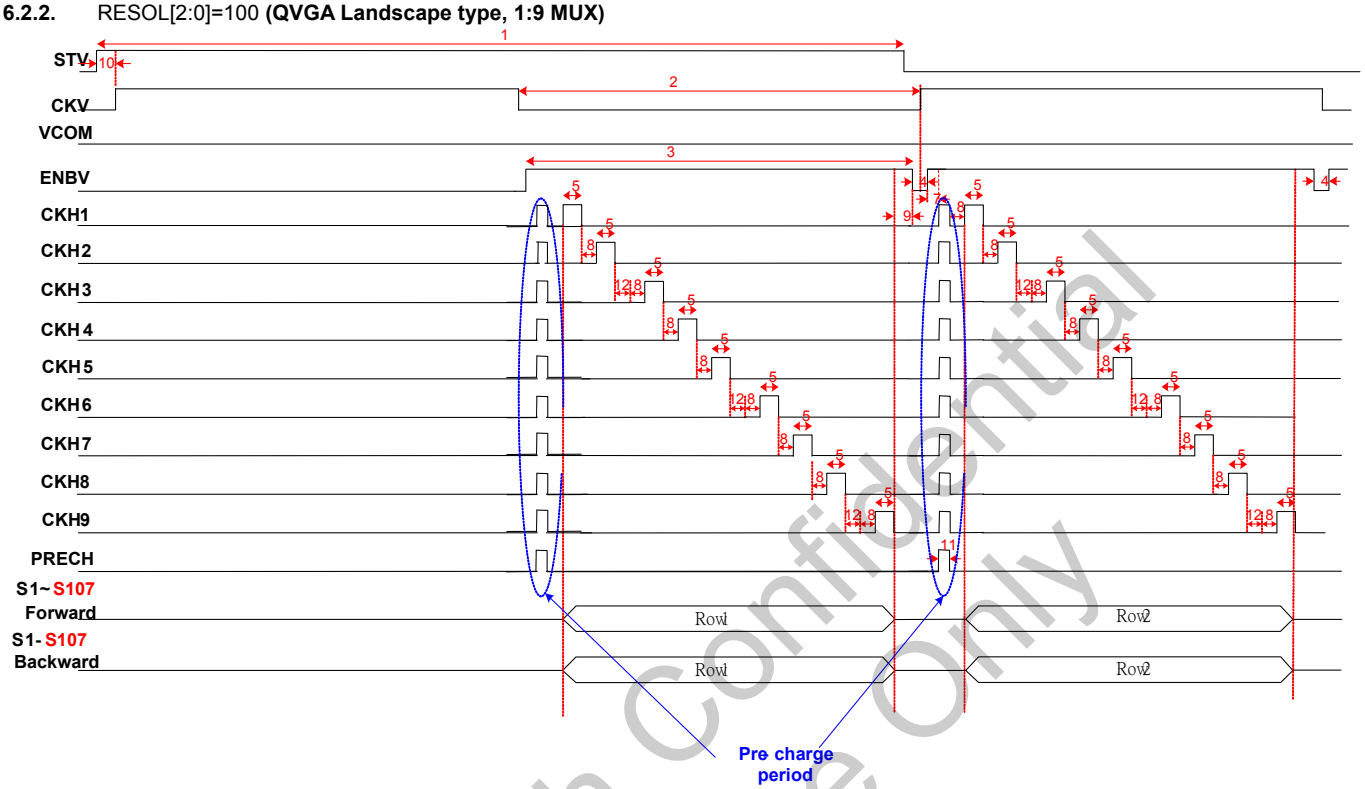
Panel requirement (Frame freq. = 60Hz for 240xRGBx432) (Blanking line: V=6, H=40) Unit: DCK

DCK=135ns	1	2	3	4	5	6	7	8	9	10	11	12
Typical	560	280	258	22	29	11	0	6	23	15	7	6
Typical(us)	75.60	37.80	34.83	2.97	3.92	1.49	0	0.81	3.11	2.03	0.95	0.81
Maximum(us)												
Minimum(us)												
Step(us)												



TCON timing and register mapping.

6.2.2. RESOL[2:0]=100 **(QVGA Landscape type, 1:9 MUX)**



Note：

1. This figure is base on Same Color MUX and t12 must insert every polarity change.
2. The source output is GND in pre-charge period.
3. The pre-charge period (CKH) is settable to turn on/off in normal & idle mode.
4. PRECH signal is settable to turn on/off in normal & idle mode.

Panel requirement (Frame freq. = 60Hz for 320xRGBx320) (Blanking line: V=6, H=40) Unit: DCK

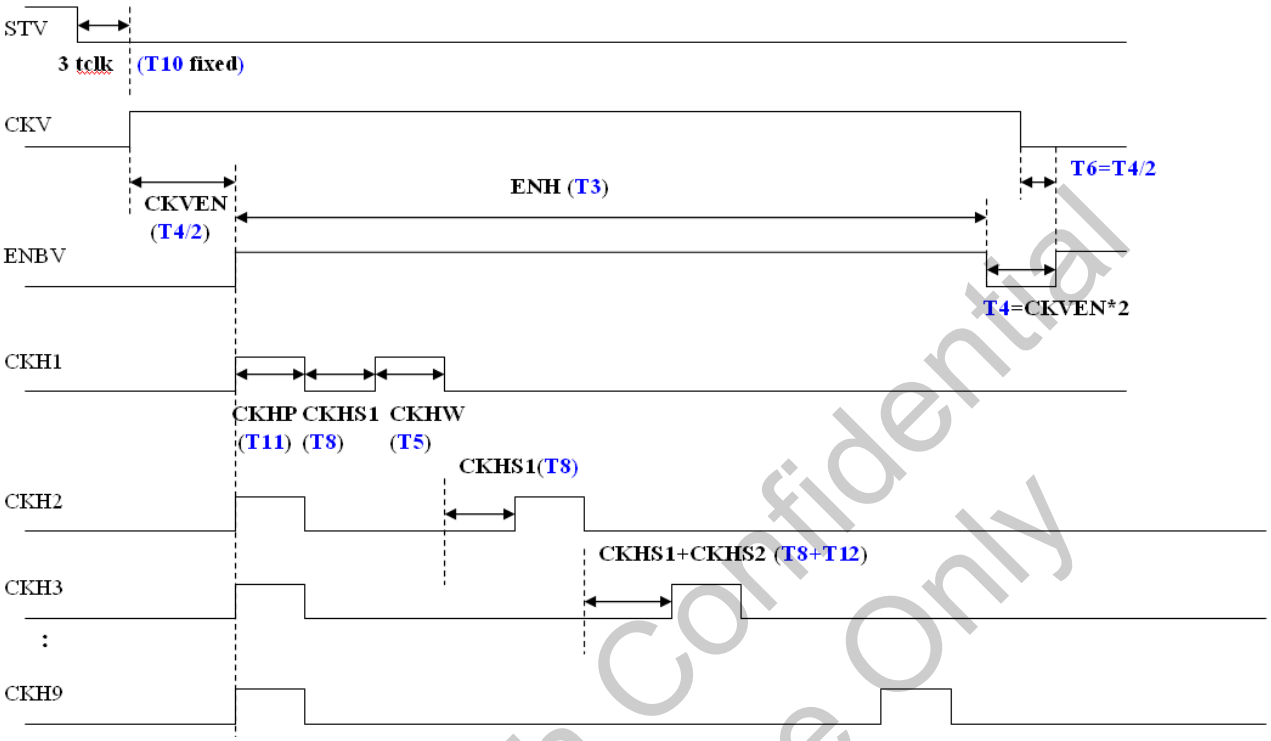
DCK=188ns	1	2	3	4	5	6	7	8	9	10	11	12
Typical	720	360	344	16	30	8	0	4	21	11	5	4
Typical(us)	135.36	67.68	64.67	3.01	5.64	1.50	0.00	0.75	3.95	2.07	0.94	0.75
Maximum(us)												
Minimum(us)												
Step(us)												

RESOL[2:0]=101 320xRGBx320(1：9 MUX)

Panel requirement (Frame freq. = 60Hz for 320xRGBx320) (Blanking line: V=6, H=40) Unit: DCK

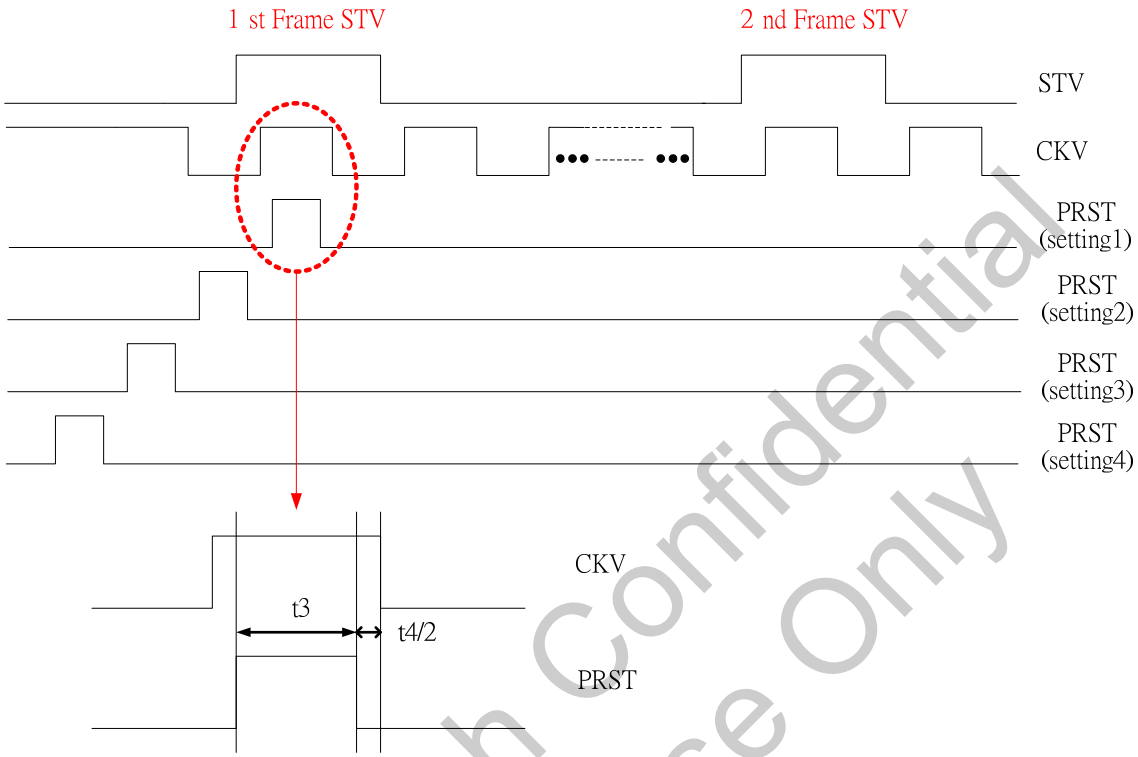
DCK=142ns	1	2	3	4	5	6	7	8	9	10	11	12
Typical	720	360	338	22	26	11	0	6	25	14	7	6
Typical(us)	102.24	51.12	48.00	3.12	3.69	1.56	0.00	0.85	3.55	1.99	0.99	0.85
Maximum(us)												
Minimum(us)												
Step(us)												

1:9MUX (T1=2*line, T2=1*line=T3+T4, T7=0, T6=T4/2 , T9=T3-T8*6-T12*3, T10=3)



TCON timing and register mapping.

6.2.3. Panel Reset function



2-bit register to choose one of 4 kinds setting of reset.

00 => setting 1

01 => setting 2 (default)

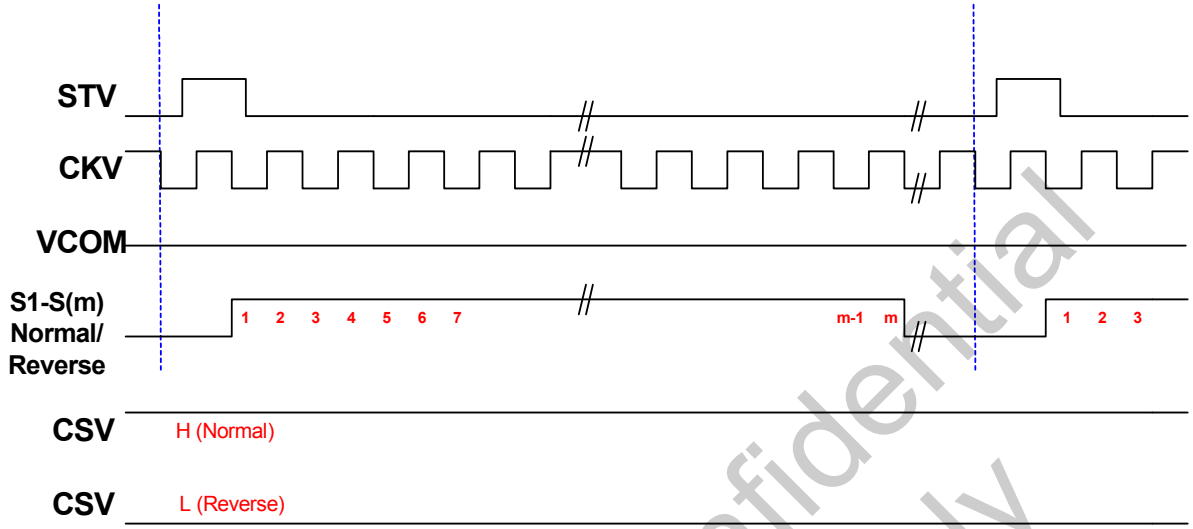
10 => setting 3

11 => setting 4

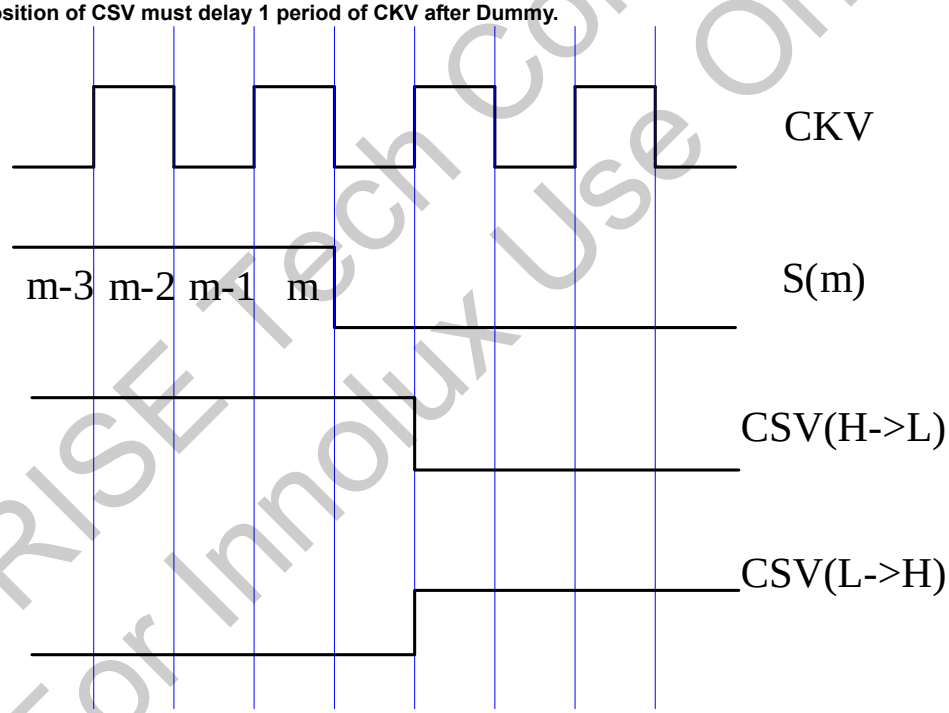
Note: The reset is only active in 1st frame, and it is GND in other frames.

6.2.4. Normal and Reverse scan timing chart:

(a) The other signals must be the same in Normal and Reverse inversion.

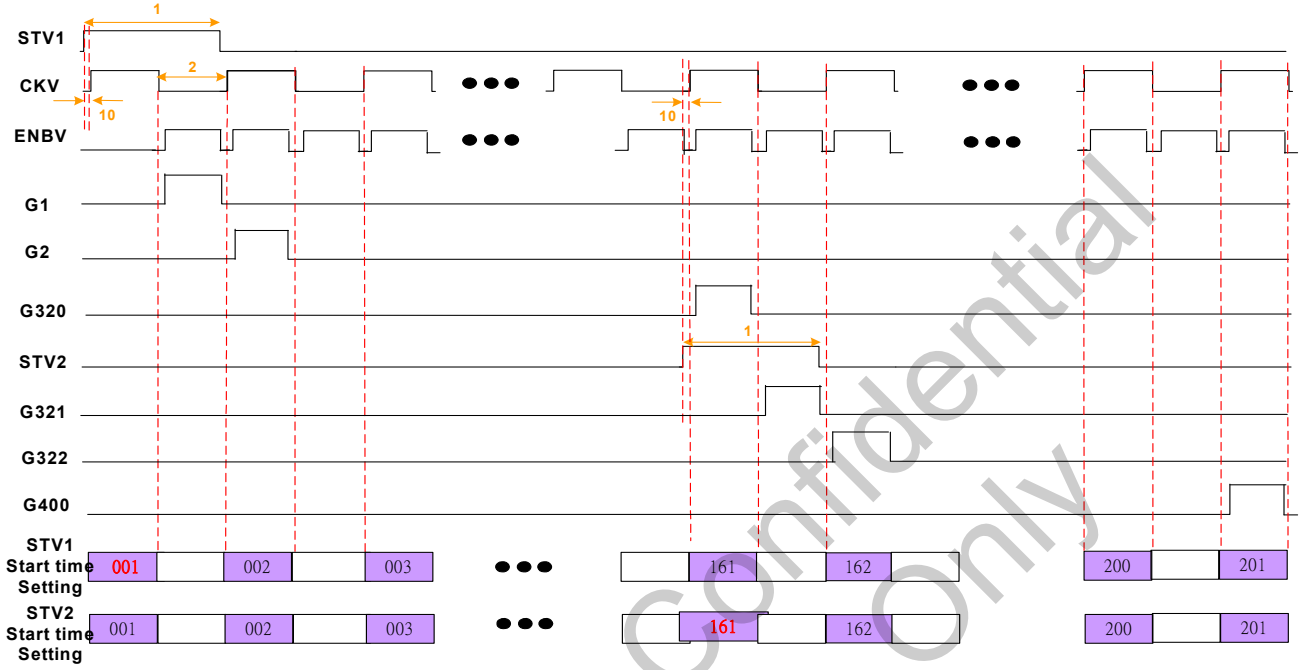


(b) The switch position of CSV must delay 1 period of CKV after Dummy.

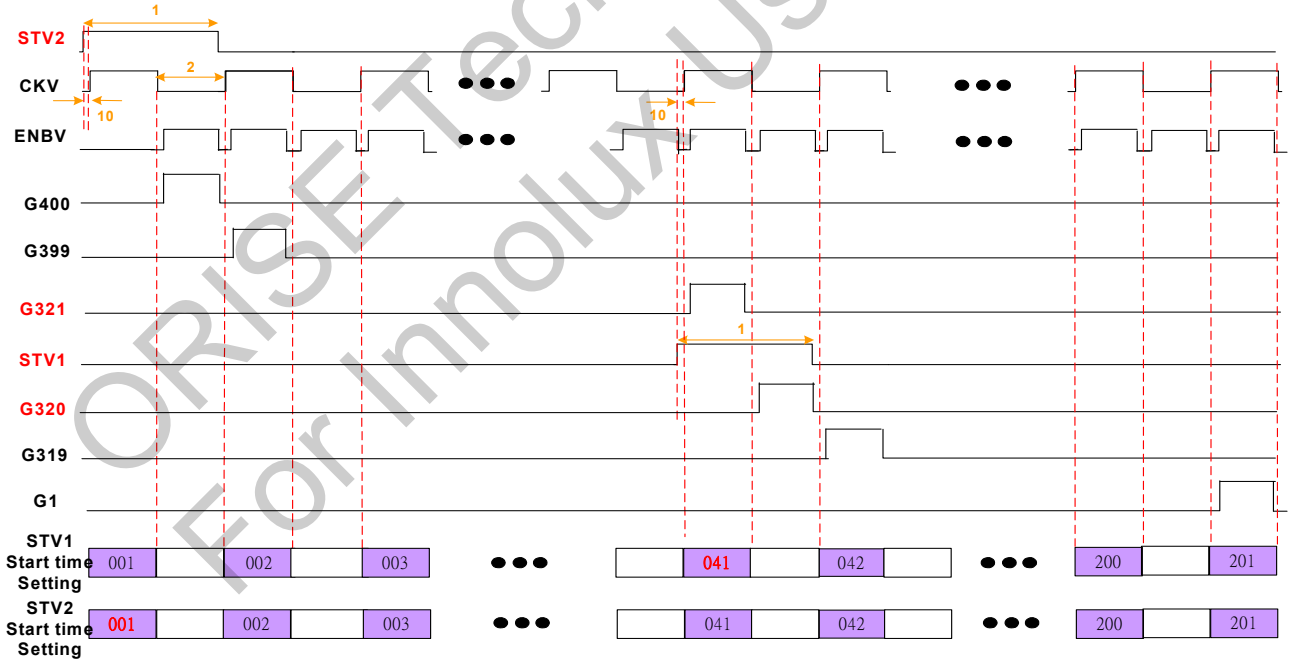


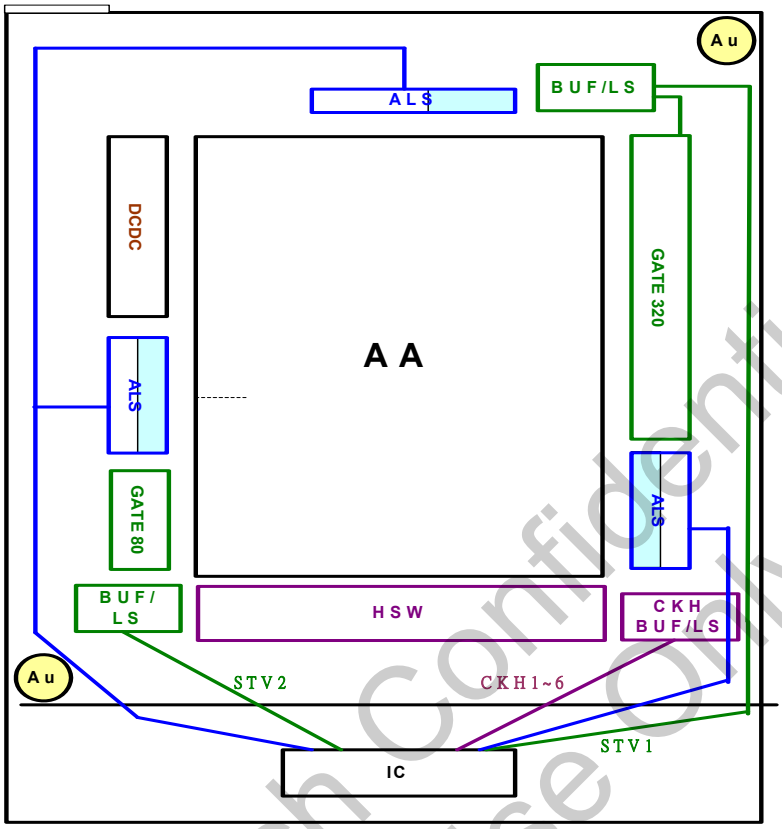
6.2.5. STV1/2 start time setting

Normal Scan



Reverse Scan



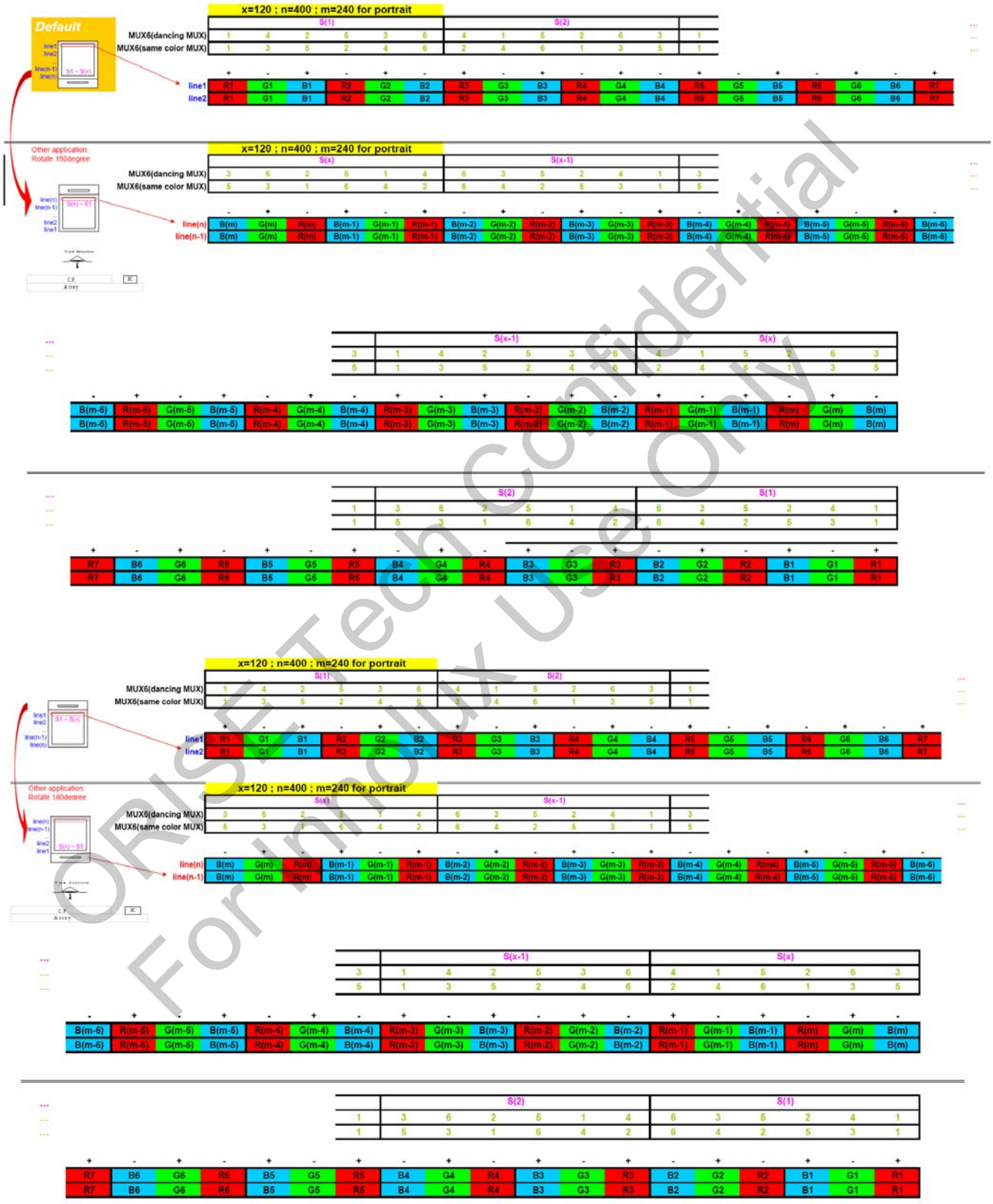


Register table

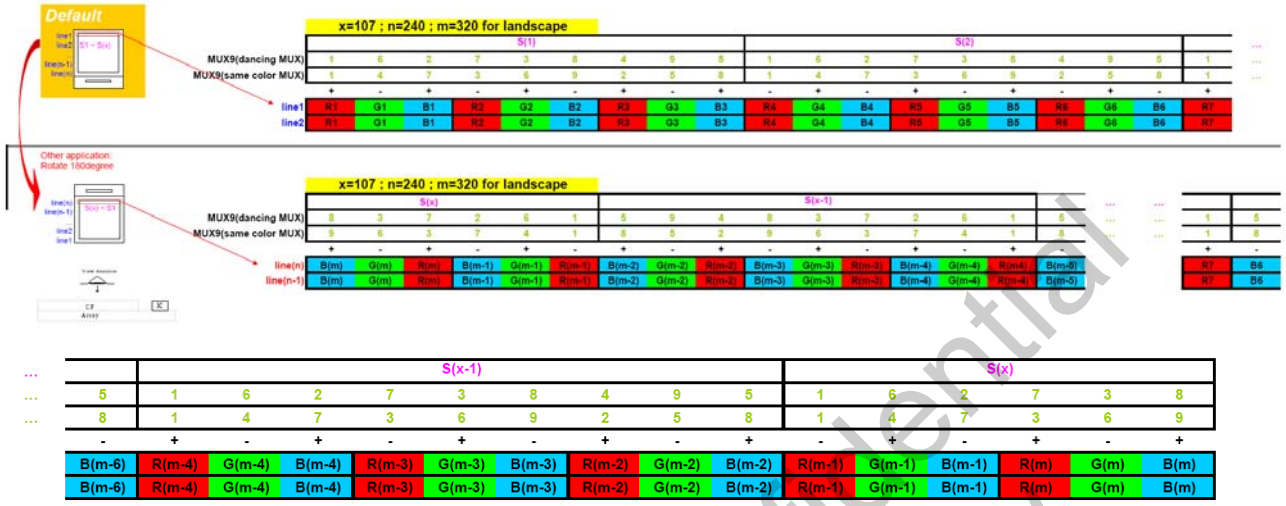
	Setting Range	Default
STV1 (normal)	1~216	001
STV2 (normal)	1~216	161
STV1 (Reverse)	1~216	041
STV2 (Reverse)	1~216	001

6.3. Color MUX

1:6 MUX

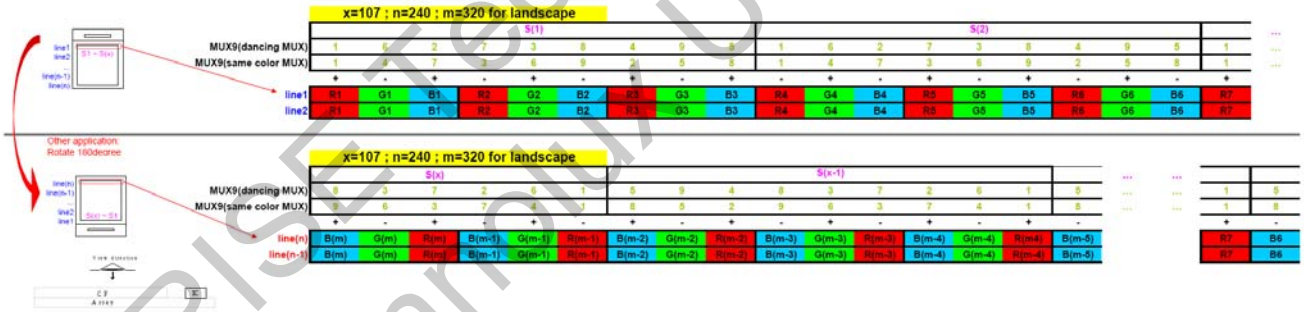


1:9 MUX



	S(x-1)										S(x)						
...																	
...	5	1	6	2	7	3	8	4	9	5	1	6	2	7	3	8	
...	8	1	4	7	3	6	9	2	5	8	1	4	7	3	6	9	
	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	
	B(m-6)	R(m-4)	G(m-4)	B(m-4)	R(m-3)	G(m-3)	B(m-3)	R(m-2)	G(m-2)	B(m-2)	R(m-1)	G(m-1)	B(m-1)	R(m)	G(m)	B(m)	
	B(m-6)	R(m-4)	G(m-4)	B(m-4)	R(m-3)	G(m-3)	B(m-3)	R(m-2)	G(m-2)	B(m-2)	R(m-1)	G(m-1)	B(m-1)	R(m)	G(m)	B(m)	

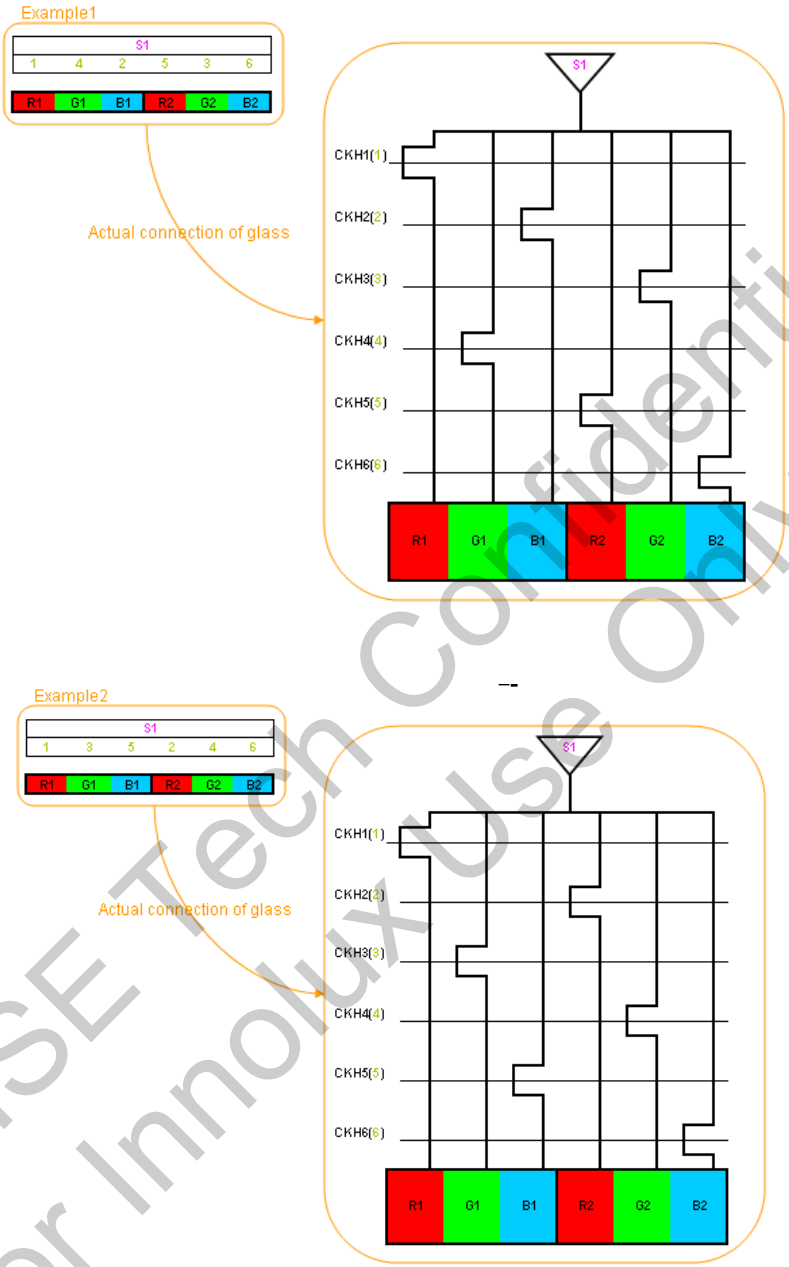
S(2)								S(1)							
9	4	8	3	7	2	6	1	5	9	4	8	3	7	2	6	1
5	2	9	6	3	7	4	1	8	5	2	9	6	3	7	4	1
+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+
G6	R6	B5	G5	R5	B4	G4	R4	B3	G3	R3	B2	G2	R2	B1	G1	R1
G6	R6	B5	G5	R5	B4	G4	R4	B3	G3	R3	B2	G2	R2	B1	G1	R1



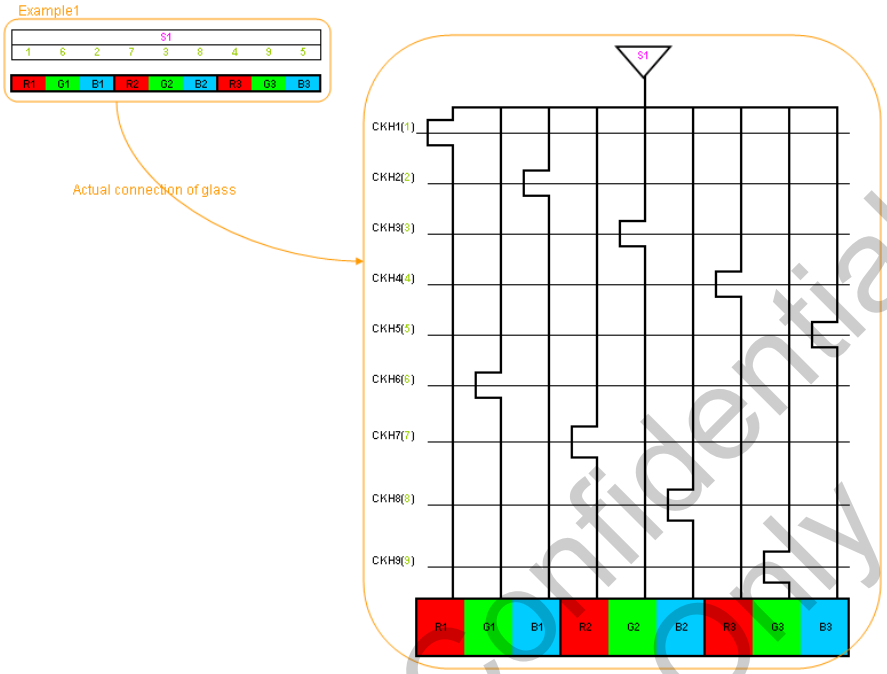
	S(x-1)										S(x)						
...																	
...	5	1	6	2	7	3	8	4	9	5	1	6	2	7	3	8	
...	8	1	4	7	3	6	9	2	5	8	1	4	7	3	6	9	
	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	
	B(m-5)	R(m-4)	G(m-4)	B(m-4)	R(m-3)	G(m-3)	B(m-3)	R(m-2)	G(m-2)	B(m-2)	R(m-1)	G(m-1)	B(m-1)	R(m)	G(m)	B(m)	
	B(m-5)	R(m-4)	G(m-4)	B(m-4)	R(m-3)	G(m-3)	B(m-3)	R(m-2)	G(m-2)	B(m-2)	R(m-1)	G(m-1)	B(m-1)	R(m)	G(m)	B(m)	

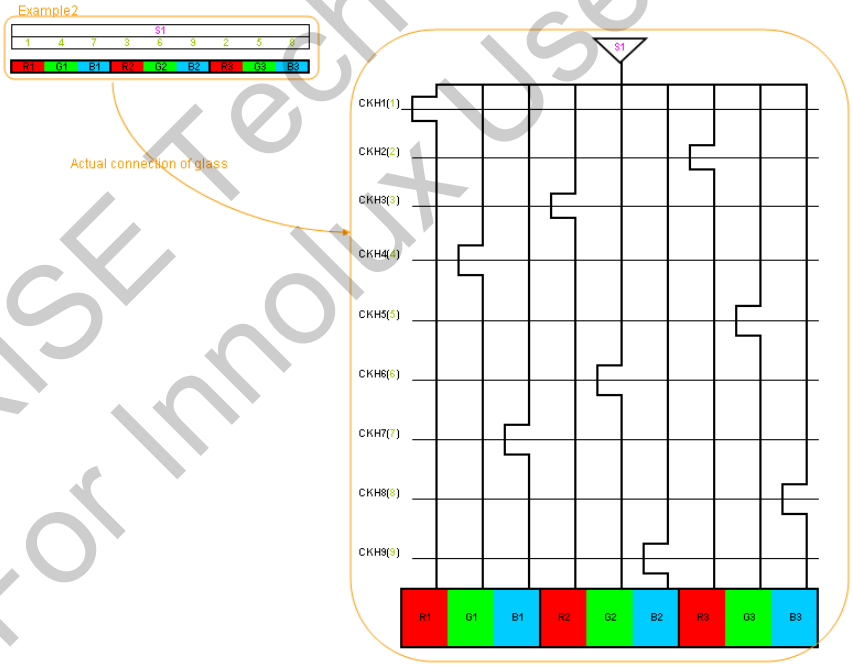
S(2)								S(1)							
9	4	8	3	7	2	6	1	5	9	4	8	3	7	2	6	1
5	2	9	6	3	7	4	1	8	5	2	9	6	3	7	4	1
+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+
G6	R6	B5	G5	R5	B4	G4	R4	B3	G3	R3	B2	G2	R2	B1	G1	R1
G6	R6	B5	G5	R5	B4	G4	R4	B3	G3	R3	B2	G2	R2	B1	G1	R1

MUX6



MUX9

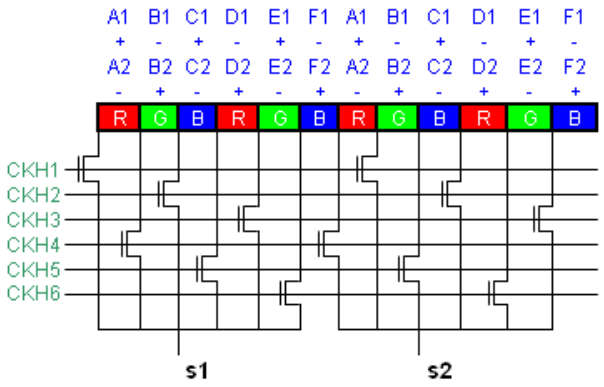




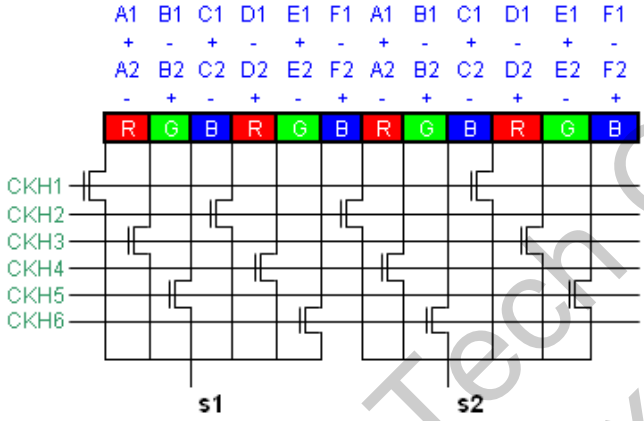
6.4. Source Scan Function

6.4.1. QVGA Portrait type

Dancing Mux



Same Color Mux



Selecting sequence:

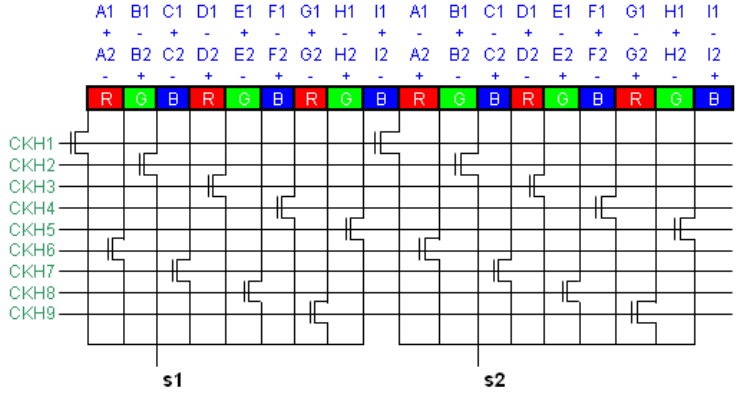
Option1: ckh1 => ckh2 => ckh3 => ckh4 => ckh5 => ckh6
All the sequence should be same every line & every frame

Option2: ckh6 => ckh5 => ckh4 => ckh3 => ckh2 => ckh1
All the sequence should be same every line & every frame

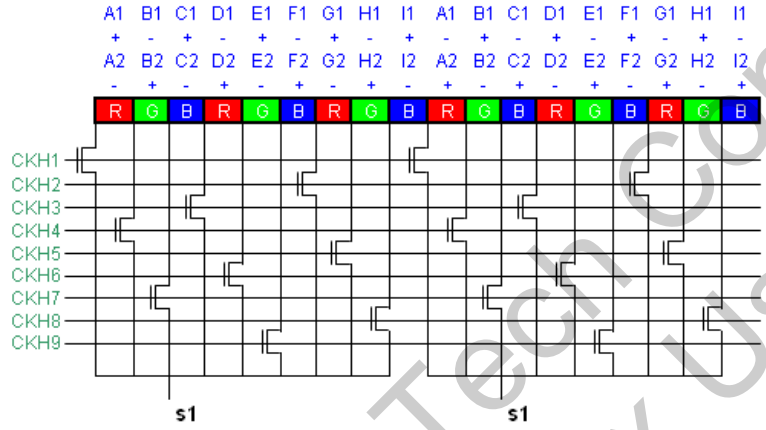
Option3: Frame Odd: ckh1 => ckh2 => ckh3 => ckh4 => ckh5 => ckh6
Frame Even: ckh6 => ckh5 => ckh4 => ckh3 => ckh2 => ckh1
All the sequence should be same every line & every frame

6.4.2. QVGA Landscape type

Dancing Mux



Same Color Mux



Selecting sequence:

Option1: ckh1 => ckh2 => ckh3 => ckh4 => ckh5 => ckh6 => ckh7 => ckh8 => ckh9
All the sequence should be same every line & every frame

Option2: ckh9 => ckh8 => ckh7 => ckh6 => ckh5 => ckh4 => ckh3 => ckh2 => ckh1
All the sequence should be same every line & every frame

Option3: Frame Odd: ckh1 => ckh2 => ckh3 => ckh4 => ckh5 => ckh6 => ckh7 => ckh8 => ckh9
Frame Even: ckh9 => ckh8 => ckh7 => ckh6 => ckh5 => ckh4 => ckh3 => ckh2 => ckh1
All the sequence should be same every line & every frame

6.4.3. Source Scan Setting

The related registers of the source line assignment are specified below. The detail function of the registers are specified on Chapter . Register Settings(MUX6,MUX9)

RESOL2=0 MUX 1:6

Order of source line		S1						S2					
(4n-3) row		A1	B1	C1	D1	E1	F1	A1	B1	C1	D1	E1	F1
		1	2	3	4	5	6	1	2	3	4	5	6
	All inversions	+	-	+	-	+	-	+	-	+	-	+	-
(4n-2) row		A2	B2	C2	D2	E2	F2	A2	B2	C2	D2	E2	F2
	Dot inversion	-	+	-	+	-	+	-	+	-	+	-	+
	2Dot inversion	-	+	-	+	-	+	-	+	-	+	-	+
	Column inversion	+	-	+	-	+	-	+	-	+	-	+	-
(4n-1) row		A1	B1	C1	D1	E1	F1	A1	B1	C1	D1	E1	F1
	Dot inversion	+	-	+	-	+	-	+	-	+	-	+	-
	2Dot inversion	-	+	-	+	-	+	-	+	-	+	-	+
	Column inversion	+	-	+	-	+	-	+	-	+	-	+	-
4n row		A2	B2	C2	D2	E2	F2	A2	B2	C2	D2	E2	F2
	Dot inversion	-	+	-	+	-	+	-	+	-	+	-	+
	2Dot inversion	+	-	+	-	+	-	+	-	+	-	+	-
	Column inversion	+	-	+	-	+	-	+	-	+	-	+	-

Order of output for 1st frame		S1						S2					
(4n-3) row		T1	T2	T3	T4	T5	T6	T1	T2	T3	T4	T5	T6
		Group A			Group B			Group A+1			Group B-1		
	All inversions	+			-			-			+		
(4n-2) row		T7	T8	T9	T10	T11	T12	T7	T8	T9	T10	T11	T12
	Dot inversion	Group C			Group D			Group C+1			Group D-1		
		-			+			+			-		
	2Dot inversion	Group C			Group D			Group C+1			Group D-1		
		-			+			+			-		
	Column inversion	Group D			Group C			Group D-1			Group C+1		
		-			+			+			-		
(4n-1) row		T13	T14	T15	T16	T17	T18	T13	T14	T15	T16	T17	T18
	2Dot inversion	Group A			Group B			Group A+1			Group B-1		
		+			-			-			+		
	2Dot inversion	Group B			Group A			Group B-1			Group A+1		
		+			-			-			+		
	Column inversion	Group A			Group B			Group A+1			Group B-1		
		+			-			-			+		
4n row		T19	T20	T21	T22	T23	T24	T19	T20	T21	T22	T23	T24
	2Dot inversion	Group C			Group D			Group C+1			Group D-1		
		-			+			+			-		
	2Dot inversion	Group D			Group C			Group D-1			Group C+1		
		-			+			+			-		
	Column inversion	Group D			Group C			Group D-1			Group C+1		
		-			+			+			-		

Connection (S1 vs S2)

Group A/C	Group A+1/C+1
1	2
3	4
5	6

Group B/D	Group B-1/D-1
2	1
4	3
6	5

RESOL2=0 MUX 1:9

Order of source line		S1									S2								
(4n-3) row		A1	B1	C1	D1	E1	F1	G1	H1	I1	A1	B1	C1	D1	E1	F1	G1	H1	I1
		1	2	3	4	5	6	7	8	9	1	2	3	4	5	6	7	8	9
	All inversion	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-
(4n-2) row		A2	B2	C2	D2	E2	F2	G2	H2	I2	A2	B2	C2	D2	E2	F2	G2	H2	I2
	Dot inversion	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+
	2Dot inversion	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+
	Column inversion	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-
(4n-1) row		A1	B1	C1	D1	E1	F1	G1	H1	I1	A1	B1	C1	D1	E1	F1	G1	H1	I1
	Dot inversion	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-
	2Dot inversion	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+
	Column inversion	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-
(4n) row		A2	B2	C2	D2	E2	F2	G2	H2	I2	A2	B2	C2	D2	E2	F2	G2	H2	I2
	Dot inversion	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+
	2Dot inversion	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-
	Column inversion	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-

Order of output for 1st frame		S1									S2								
(4n-3) row		T1	T2	T3	T4	T5	T6	T7	T8	T9	T1	T2	T3	T4	T5	T6	T7	T8	T9
		Group X					Group Y				Group X					Group Y			
	All inversion	+					-				-					+			
(4n-2) row		T10	T11	T12	T13	T14	T15	T16	T17	T18	T10	T11	T12	T13	T14	T15	T16	T17	T18
	Dot inversion	Group Z					Group AA				Group Z					Group AA			
		-					+				+					-			
	2Dot inversion	Group Z					Group AA				Group Z					Group AA			
		-					+				+					-			
	Column inversion	Group AA					Group Z				Group AA					Group Z			
		-					+				+					-			
(4n-1) row		T19	T20	T21	T22	T23	T24	T25	T26	T27	T19	T20	T21	T22	T23	T24	T25	T26	T27
	Dot inversion	Group X					Group Y				Group X					Group Y			
		+					-				-					+			
	2Dot inversion	Group Y					Group X				Group Y					Group X			
		+					-				-					+			
	Column inversion	Group X					Group Y				Group X					Group Y			
		+					-				-					+			
(4n) row		T28	T29	T30	T31	T32	T33	T34	T35	T36	T28	T29	T30	T31	T32	T33	T34	T35	T36
	Dot inversion	Group Z					Group AA				Group Z					Group AA			
		-					+				+					-			
	2Dot inversion	Group AA					Group Z				Group AA					Group Z			
		-					+				+					-			
	Column inversion	Group AA					Group Z				Group AA					Group Z			
		-					+				+					-			

Amplifier offset canceration

a Negative amp mode a

b Negative amp mode b

Cancel

a Positive amp mode a

b Positive amp mode b

Cancel

Dot inversion

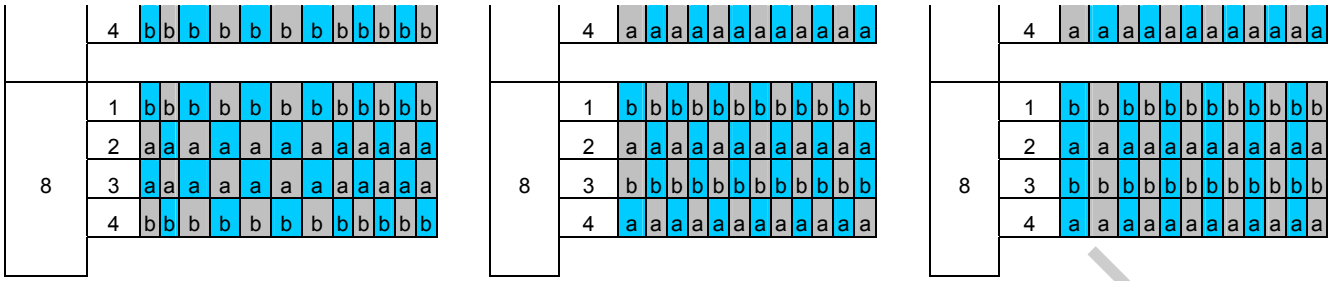
Frame	Line	Columns
1	1	a a a a a a a a a a a a a a
	2	b b b b b b b b b b b b b b
	3	b b b b b b b b b b b b b b
	4	a a a a a a a a a a a a a a
2	1	a a a a a a a a a a a a a a
	2	b b b b b b b b b b b b b b
	3	b b b b b b b b b b b b b b
	4	a a a a a a a a a a a a a a
3	1	b b b b b b b b b b b b b b
	2	a a a a a a a a a a a a a a
	3	a a a a a a a a a a a a a a
	4	b b b b b b b b b b b b b b
4	1	b b b b b b b b b b b b b b
	2	a a a a a a a a a a a a a a
	3	a a a a a a a a a a a a a a
	4	b b b b b b b b b b b b b b
5	1	a a a a a a a a a a a a a a
	2	b b b b b b b b b b b b b b
	3	b b b b b b b b b b b b b b
	4	a a a a a a a a a a a a a a
6	1	a a a a a a a a a a a a a a
	2	b b b b b b b b b b b b b b
	3	b b b b b b b b b b b b b b
	4	a a a a a a a a a a a a a a
7	1	b b b b b b b b b b b b b b
	2	a a a a a a a a a a a a a a
	3	a a a a a a a a a a a a a a

2dot inversion

Frame	Line	Columns
1	1	a a a a a a a a a a a a a a
	2	b b b b b b b b b b b b b b
	3	a a a a a a a a a a a a a a
	4	b b b b b b b b b b b b b b
2	1	a a a a a a a a a a a a a a
	2	b b b b b b b b b b b b b b
	3	a a a a a a a a a a a a a a
	4	b b b b b b b b b b b b b b
3	1	b b b b b b b b b b b b b b
	2	a a a a a a a a a a a a a a
	3	b b b b b b b b b b b b b b
	4	a a a a a a a a a a a a a a
4	1	b b b b b b b b b b b b b b
	2	a a a a a a a a a a a a a a
	3	b b b b b b b b b b b b b b
	4	a a a a a a a a a a a a a a
5	1	a a a a a a a a a a a a a a
	2	b b b b b b b b b b b b b b
	3	a a a a a a a a a a a a a a
	4	b b b b b b b b b b b b b b
6	1	a a a a a a a a a a a a a a
	2	b b b b b b b b b b b b b b
	3	a a a a a a a a a a a a a a
	4	b b b b b b b b b b b b b b
7	1	b b b b b b b b b b b b b b
	2	a a a a a a a a a a a a a a
	3	b b b b b b b b b b b b b b

Column inversion

Frame	Line	Columns
1	1	a a a a a a a a a a a a a a
	2	b b b b b b b b b b b b b b
	3	a a a a a a a a a a a a a a
	4	b b b b b b b b b b b b b b
2	1	a a a a a a a a a a a a a a
	2	b b b b b b b b b b b b b b
	3	a a a a a a a a a a a a a a
	4	b b b b b b b b b b b b b b
3	1	b b b b b b b b b b b b b b
	2	a a a a a a a a a a a a a a
	3	b b b b b b b b b b b b b b
	4	a a a a a a a a a a a a a a
4	1	b b b b b b b b b b b b b b
	2	a a a a a a a a a a a a a a
	3	b b b b b b b b b b b b b b
	4	a a a a a a a a a a a a a a
5	1	a a a a a a a a a a a a a a
	2	b b b b b b b b b b b b b b
	3	a a a a a a a a a a a a a a
	4	b b b b b b b b b b b b b b
6	1	a a a a a a a a a a a a a a
	2	b b b b b b b b b b b b b b
	3	a a a a a a a a a a a a a a
	4	b b b b b b b b b b b b b b
7	1	b b b b b b b b b b b b b b
	2	a a a a a a a a a a a a a a
	3	b b b b b b b b b b b b b b



7. INSTRUCTIONS

7.1. Outline

The OTM3201A supports 24-bit data bus interface to configure system via accessing command register. When the command register is executed, sending the command information to specify which index register would be accessed and following the data to that control register.

Table 7.1.1 System Function command1 List (IM[1:0] = 00, 10, 11)

Command	(Hex)	Write/Read /Command	Function	Parameter Number
NOP	00	**C**	No Operation	0
SWRESET	01	**C**	Software reset	0
RDDPM	0A	**R**	Read Display Power Mode	1
RDDMADCTL	0B	**R**	Read Display MADCTL	1
RDDCOLMOD	0C	**R**	Read Display Pixel Format	1
RDDIM	0D	**R**	Read Display Image Mode	1
SLPIN	10	**C**	Sleep in	0
SLPOUT	11	**C**	Sleep out	0
INVOFF	20	**C**	Display Inversion Off	0
INVON	21	**C**	Display Inversion On	0
DISPOFF	28	**C**	Display off	0
DISPON	29	**C**	Display on	0
MADCTL	36	**W**	Memory Access Control	1
IDMOFF	38	**C**	Idle Mode off	0
IDMON	39	**C**	Idle Mode on	0
COLMOD	3A	**C**	Interface Pixel Format	1
RDDDBS	A1	**R**	Read DDB Start	5
RDID1	DA	**R**	Read ID1	1
RDID2	DB	**R**	Read ID2	1
RDID3	DC	**R**	Read ID3	1

7.2. Command1 Description (IM[1:0] = 00, 10, 11)

7.2.1. NOP (00h) : No Operation

00H	NOP (No Operation)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NOP	Write	0	0	0	0	0	0	0	0	(00H)
Parameter	No Parameter									-

Description	- This command is empty command. It does not have effect on the display module.
Restriction	-
Default	

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

7.2.2. SWRESET (01h): Software Reset

01H	SWRESET (Software Reset)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SWRESET	Write	0	0	0	0	0	0	0	1	(01H)
Parameter	No Parameter									-

Description	- When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all source & gate outputs are set to VSS (display off).
Restriction	- It will be necessary to wait 5msec before sending new command following software reset. - The display module loads all display supplier's factory default values to the registers during 5msec. - If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command. - Software Reset command cannot be sent during Sleep Out sequence.
Default	

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

7.2.3. RDDPM (0AH): Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDPM	Write	0	0	0	0	1	0	1	0	(0AH)
1st Parameter	Read	0	IDMON	0	SLP OUT	1	DISON	0	0	08h

Description

- This command indicates the current status of the display as described in the table below:

Bit	Description	Value
IDMON	Idle Mode On/Off	"1" = Idle Mode On, "0" = Idle Mode Off
SLPON	Sleep In/Out	"1" = Sleep Out, "0" = Sleep In
DISON	Display On/Off	"1" = Display On, "0" = Display Off

.

Restriction

-

Default

Status	Default Value (D7 to D0)
Power On Sequence	08h
S/W Reset	08h
H/W Reset	08h

7.2.4. RDDMADCTR (0BH): Read Display MADCTR

0BH	RDDMADCTR (Read Display MADCTR)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDMADCTR	Write	0	0	0	0	1	0	1	1	(0BH)
1st Parameter	Read	0	0	0	ML	RGB	0	0	0	00h

Description

- This command indicates the current status of the display as described in the table below:.

Bit	Description	Value
ML	Vertical Refresh Order	LCD vertical refresh direction control '0' = LCD vertical refresh Top to Bottom '1' = LCD vertical refresh Bottom to Top
RGB	RGB-BGR ORDER	Color selector switch control '0' =RGB color filter panel, '1' =BGR color filter panel

.

Restriction

-

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

7.2.5. RDDCOLMOD (0CH): Read Display Pixel Format

0CH	RDDCOLMOD (Read Display Pixel Format)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDCOLMOD	Write	0	0	0	0	1	1	0	0	(0CH)
1st Parameter	Read	0	VIPF2	VIPF1	VIPF0	0	IFPF2	IFPF1	IFPF0	77h

Description

- This command indicates the current status of the display as described in the table below:

VIPF[2:0]		RGB Interface Color Format
101	5	16-bits/pixel
110	6	18-bits/pixel
111	7	24-bits/pixel

Others are no define and invalid

.

IFPF[2:0]		MCU Interface Color Format
101	5	16-bits/pixel
110	6	18-bits/pixel
111	7	24-bits/pixel

Others are no define and invalid

.

Restriction

-

Default

Status	Default Value	
-	VFPF[2:0]	IFPF[2:0]
Power On Sequence	111 (24-bits/pixel)	111 (24-bits/pixel)
S/W Reset	111 (24-bits/pixel)	111 (24-bits/pixel)
H/W Reset	111 (24-bits/pixel)	111 (24-bits/pixel)

7.2.6. RDDIM (0DH): Read Display Image Mode

0DH	RDDIM (Read Display Image Mode)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDIM	Write	0	0	0	0	1	1	0	1	(0DH)
1st Parameter	Read	0	0	INVON	0	0	0	0	0	00h

Description

- This command indicates the current status of the display as described in the table below:

Bit	Description	Value
INVON	Inversion On/Off	"1" = Inversion is On, "0" = Inversion is Off

.

Restriction

-

Default

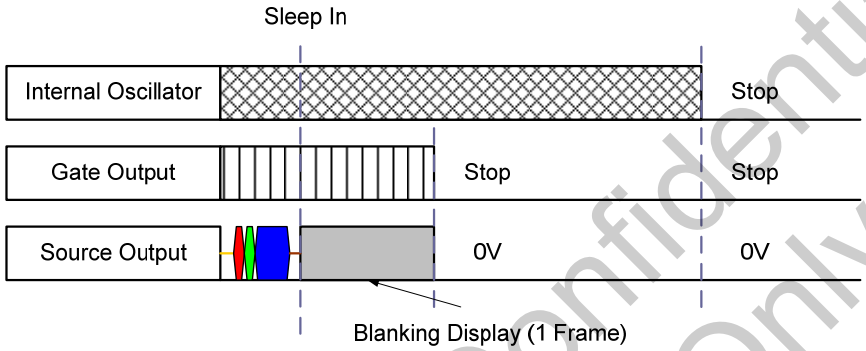
Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

7.2.7. SLPIN (10H): Sleep In

10H	SLPIN (Sleep In)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPIN	Write	0	0	0	1	0	0	0	0	(10H)
Parameter	No Parameter									-

Description

- This command causes the LCD module to enter the minimum power consumption mode.
- In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.



- MCU interface and memory are still working and the memory keeps its contents

Restriction

- This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11H).
- It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.
- It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Default

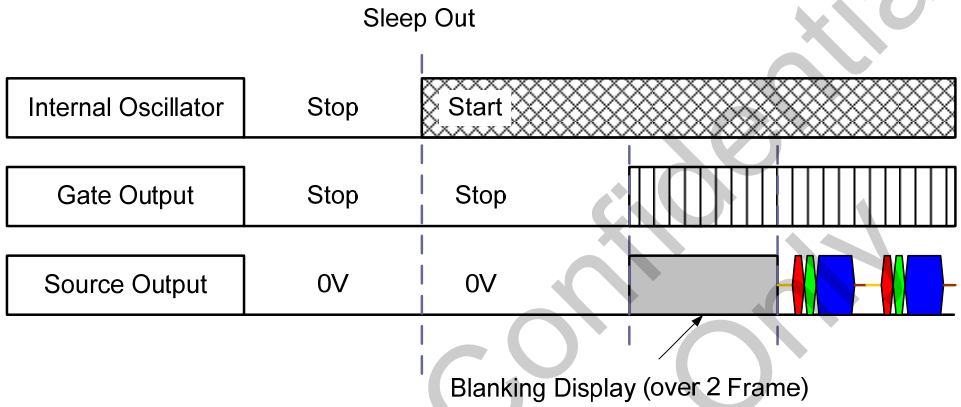
Status	Default Value
Power On Sequence	Sleep In mode
S/W Reset	Sleep In mode
H/W Reset	Sleep In mode

7.2.8. SLPOUT (11H): Sleep Out

11H	SLPOUT (Sleep Out)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPOUT	Write	0	0	0	1	0	0	0	1	(11H)
Parameter	No Parameter									-

Description

- This command turns off sleep mode.
- In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.



Restriction

- This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10H).
- It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.
- DRIVER loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the DRIVER is already Sleep Out mode.
- DRIVER is doing self-diagnostic functions during this 5msec.
- It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent

Default

Status	Default Value
Power On Sequence	Sleep In mode
S/W Reset	Sleep In mode
H/W Reset	Sleep In mode

7.2.9. INVOFF (20h) : Display Inversion Off

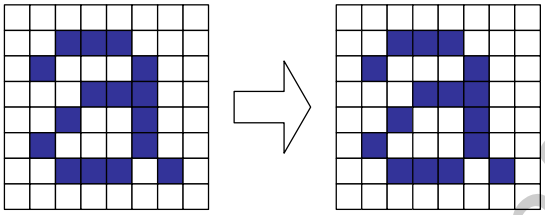
20H	INVOFF (Display Inversion Off)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVOFF	Write	0	0	1	0	0	0	0	0	(20H)
Parameter	No Parameter									-

Description

- This command is used to recover from display inversion mode.
- This command does not change any other status.

(Example)

MCU → Display



Restrictions

- This command has no effect when module is already in inversion off mode.

Default

Status	Default value
Power On Sequence	Display Inversion Off
SW Reset	Display Inversion Off
HW Reset	Display Inversion Off

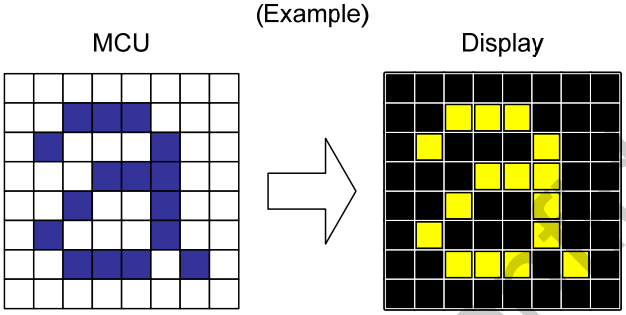
7.2.10. INVON (21h) : Display Inversion On

21H	INVON (Display Inversion On)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVON	Write	0	0	1	0	0	0	0	1	(21H)
Parameter	No Parameter									-

Description

- This command is used to enter into display inversion mode.
- This command does not change any other status.

(Example)



Restrictions

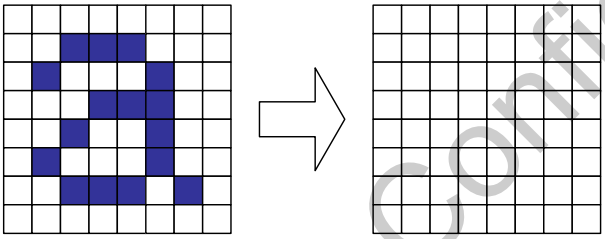
- This command has no effect when module is already in inversion on mode.

Default

Status	Default value
Power On Sequence	Display Inversion Off
SW Reset	Display Inversion Off
HW Reset	Display Inversion Off

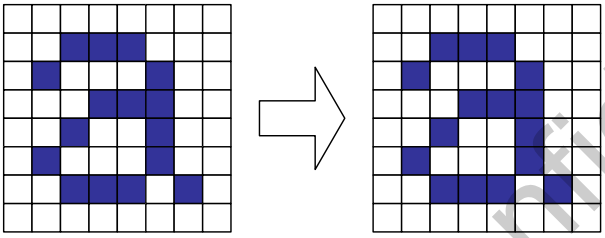
7.2.11. DISPOFF (28H): Display Off

28H	DISPOFF (Display Off)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPOFF	Write	0	0	1	0	1	0	0	0	(28H)
Parameter	No Parameter									-

Description	- This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disables and blank page inserted. - This command does not change any other status. - There will be no abnormal visible effect on the display. - Exit from this command by Display On (29H) (Example) MCU Display  .
Restriction	-This command has no effect when module is already in Display Off mode.
Default	**Status** / **Default Value** Power On Sequence: Display off S/W Reset: Display off H/W Reset: Display off

7.2.12. DISPON (29H): Display On

29H	DISPON (Display On)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPON	Write	0	0	1	0	1	0	0	1	(29H)
Parameter	No Parameter									-

Description	- This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. - This command does not change any other status. (Example) MCU Display  .
Restriction	- This command has no effect when module is already in Display On mode.
Default	.

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

7.2.13. MADCTR (36H): Memory Data Access Control

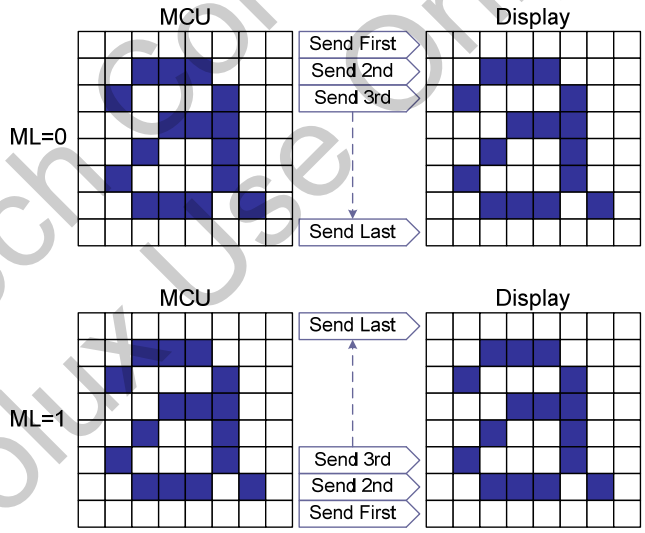
36H	MADCTR (Memory Data Access Control)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
MADCTR	Write	0	0	1	1	0	1	1	0	(36H)
1st Parameter	Write	0	0	0	ML	RGB	0	0	0	00h

Description

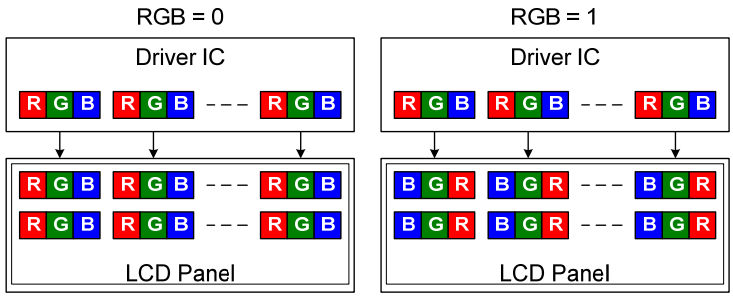
- This command has no effect for driver output, only register value is updated.
- This command makes no change on the other driver status.

Bit	Description	Value
ML	Vertical Refresh Order	LCD vertical refresh direction control '0' = LCD vertical refresh Top to Bottom '1' = LCD vertical refresh Bottom to Top
RGB	RGB-BGR ORDER	Color selector switch control '0' =RGB color filter panel, '1' =BGR color filter panel

ML: Vertical Refresh Order



RGB: RGB-BGR Order



Restriction

-

Default

Status	Default Value
Power On Sequence	ML=0,RGB=0,
S/W Reset	ML=0,RGB=0,
H/W Reset	ML=0,RGB=0,

7.2.14. IDMOFF (38H): Idle Mode Off

38H	IDMOFF (Idle Mode Off)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMOFF	Write	0	0	1	1	1	0	0	0	(38H)
Parameter	No Parameter									-

Description	- This command is used to recover from Idle mode on. - There will be no abnormal visible effect on the display mode change transition. - In the idle off mode, 1. LCD can display 65k, 262k and 16.7M – colors. 2. Normal frame frequency is applied.
Restriction	- This command has no effect when module is already in idle off mode.
Default	

	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

7.2.15. IDMON (39H): Idle Mode On

39H	IDMON (Idle Mode On)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMON	Write	0	0	1	1	1	0	0	1	(39H)
Parameter	No Parameter									-

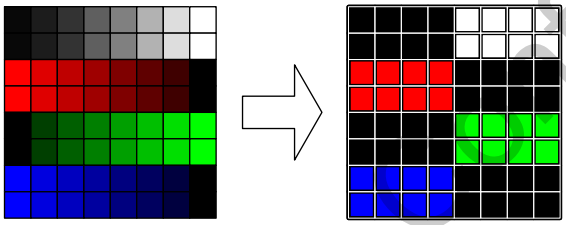
Description

- This command is used to enter into Idle mode on.
- There will be no abnormal visible effect on the display mode change transition.
- In the idle on mode,

1. Color expression is reduced.
2. 8-Color mode frame frequency is applied.
3. Exit from IDMON by Idle Mode Off (38H) command

(Example)

MCU Display



Color	R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	G_7 G_6 G_5 G_4 G_3 G_2 G_1 G_0	B_7 B_6 B_5 B_4 B_3 B_4 B_1 B_0
Black	0xxxxxxx	0xxxxxxx	0xxxxxxx
Blue	0xxxxxxx	0xxxxxxx	1xxxxxxx
Red	1xxxxxxx	0xxxxxxx	0xxxxxxx
Magenta	1xxxxxxx	0xxxxxxx	1xxxxxxx
Green	0xxxxxxx	1xxxxxxx	0xxxxxxx
Cyan	0xxxxxxx	1xxxxxxx	1xxxxxxx
Yellow	1xxxxxxx	1xxxxxxx	0xxxxxxx
White	1xxxxxxx	1xxxxxxx	1xxxxxxx

Restriction

- This command has no effect when module is already in idle on mode.

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

7.2.16. COLMOD (3AH): Interface Pixel Format

3AH	COLMOD (Interface Pixel Format)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
COLMOD	Write	0	0	1	1	1	0	1	0	(3AH)
1st Parameter	Write	0	VIPF2	VIPF1	VIPF0	0	IFPF2	IFPF1	IFPF0	77h

Description

- This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface and RGB interface. The formats are shown in the table:

VIPF[2:0]		RGB Interface Color Format
101	5	16-bits/pixel
110	6	18-bits/pixel
111	7	24-bits/pixel

Others are no define and invalid

.

IFPF[2:0]		MCU Interface Color Format
101	5	16-bits/pixel
110	6	18-bits/pixel
111	7	24-bits/pixel

Others are no define and invalid

Note1: In 16-bits/Pixel, 18-bits/Pixel or 24-bits/Pixel mode, the LUT is applied to transfer data into the source.

Restriction

-

Default

Status	Default Value	
-	VIPF[2:0]	IFPF[2:0]
Power On Sequence	111 (24-bits/pixel)	111 (24-bits/pixel)
S/W Reset	111 (24-bits/pixel)	111 (24-bits/pixel)
H/W Reset	111 (24-bits/pixel)	111 (24-bits/pixel)

.

7.2.17. RDDDBSTR (A1H): Read DDB Start

A1H	RDDDBSTR (Read DDB Start)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDDBSTR	Write	1	0	1	0	0	0	0	1	(A1H)
1st Parameter	Read	0	0	0	0	0	0	0	0	00h
2nd Parameter	Read	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	E3h
3rd Parameter	Read	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80h
4th Parameter	Read	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	6Ch
5th Parameter	Read	1	1	1	1	1	1	1	1	FFh

Description	- The command reads identifying and descriptive information from the peripheral. This information is organized in the Device Descriptor Block(DDB) stored on the peripheral. - The format of returned data is as follows: Parameter 1: Reserved (00h) Parameter 2: ID1 Parameter 3: ID2 Parameter 4: ID3 Parameter 5: Reserved (FFh)
Restriction	-
Default	

Status	Default Value
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

7.2.18. RDID1 (DAH): Read ID1

DAH	RDID1 (Read ID1)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID1	Write	1	1	0	1	1	0	1	0	(DAH)
1st Parameter	Read	ID1 7	ID1 6	ID1 5	ID1 4	ID1 3	ID1 2	ID1 1	ID1 0	E3h

Description	- This read byte identifies the display module's manufacturer.
Restriction	- None
Default	

Status	Default Value
Power On Sequence	E3h
S/W Reset	E3h
H/W Reset	E3h

7.2.19. RDID2 (DBH): Read ID2

DBH	RDID2 (Read ID2)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID2	Write	1	1	0	1	1	0	1	1	(DBH)
1st Parameter	Read	1	ID2 6	ID2 5	ID2 4	ID2 3	ID2 2	ID2 1	ID2 0	80h

Description	- This read byte is used to track the display module/driver version. It is defined by display supplier (with agreement) and changes each time a revision is made to the display, material or construction specifications.
Restriction	-
Default	

Status	Default Value
Power On Sequence	80h
S/W Reset	80h
H/W Reset	80h

7.2.20. RDID3 (DCH): Read ID3

DCH	RDID3 (Read ID3)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID3	Write	1	1	0	1	1	1	0	0	(DCH)
1st Parameter	Read	ID3 7	ID3 6	ID3 5	ID3 4	ID3 3	ID3 2	ID3 1	ID3 0	6Ch

Description	- This read byte is used to track the display module/driver version. It is defined by display supplier (with agreement) and changes each time a revision is made to the display, material or construction specifications.
Restriction	-
Default	

Status	Default Value	
	Landscape	Portrait
Power On Sequence	6Ch	5Dh
S/W Reset	6Ch	5Dh
H/W Reset	6Ch	5Dh

7.3. Command1 Description (IM[1:0]=01)

7.3.1. Index(IR)

IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	R/W	Default
									ID6	ID5	ID4	ID3	ID2	ID1	ID0		

Index register format

7.3.2. Version management register 1,2 (R0)

IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	R/W	Default
VER 7	VER 6	VER 5	VER 4	VER 3	VER 2	VER 1	VER 0	VER 27	VER 26	VER 25	VER 24	VER 23	VER 22	VER 21	VER 20	R	1100H

Bit 8 to 16 shows a product name(default: 11H). Bit 0 to 7 shows a product version(default: 00)

Register 00h – Product name and version. This cannot be changed without Motorola's written permission.

7.3.3. Each setting register (R1)

IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	R/W	Default
						TB	RL									R/W	0300H

Register 01h – Set scan direction (see section 6.3.4 for scan direction relative to display layout)

•R01h = 0x0300, Normal scan direction

•R01h = 0x0000, Inverted scan direction

Sets direction of TB (top / bottom), or RL (right / left)

7.3.4. Line/frame inversion register (R2)

IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	R/W	Default
						B/C										R/W	0200H

Register 02h – Line inversion / Frame inversion selection.

• R02h = 0x0200, Dot inversion, default.

• R02h = 0x0000, Column inversion.

7.3.5. ENTRY MODE (R03)

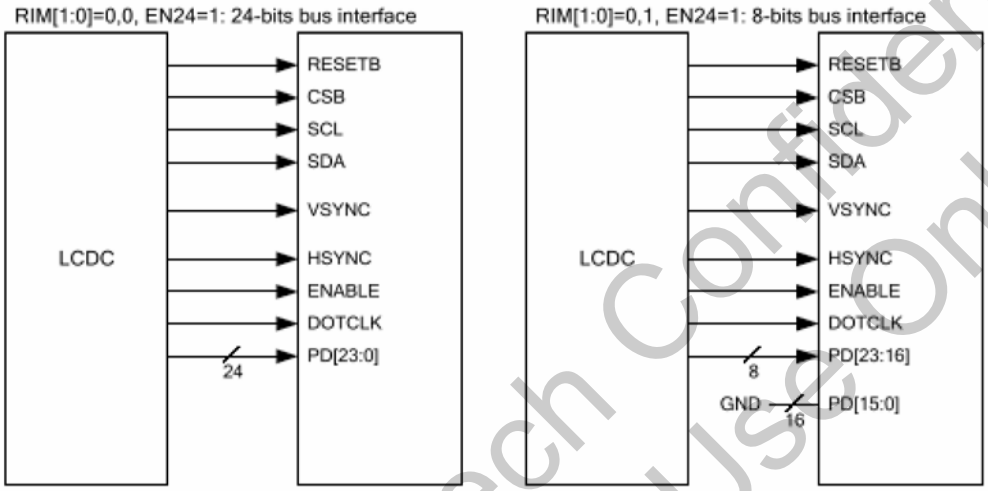
R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	BGR							RIM1	RIM0
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register 03h – RGB Interface select

• R03h = 0x0000, 24 bit interface, RGB24 (default)

• R03h = 0x0001, 8 bit interface, RGBx3

Note: State of BGR bit as related to color filter selection is unknown at this time. Its value shall be logically OR'd to the values here.



7.3.6. Command reset register (R28H)

IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	R/W	Default
Software Reset																R/W	0000H

Register 0x28h – Software Reset. Note: Only register restorations to defaults are performed.

• R28h = 0x0000, Reset Release, normal operation.

• R28h = 0x000E, Software Reset.

7.3.7. General input register (R51H)

IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	R/W	Default
				GPI3	GPI2	GPI1	GPI0									R	-

Register 0x51h – GPI input. These inputs are configured based upon glass size

• R051h = 0x0000 – 2.0" display. (for reference only)

• R051h = 0x0100 – 2.2" display. (for reference only)

• R051h = 0x0200 – 2.4" display. (for reference only)

• R051h = 0x0400 – 2.8" display. Identifies this display

7.3.8. 8-color mode register (R53H)

IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	R/W	Default
															HCL	R/W	0000

Register 0x53h – Color Mode

• R53h = 0x0000, 262,144 color mode

• R53h = 0x0001, 8 color mode

7.3.9. Temperature sensor read register (R70H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	X	X	X	X	X	X	X	X	X	X	TES5	TES4	TES3	TES2	TES1	TES0
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R80H is temperature sensor read value register function. The senor range is **(-40~86°C)** and TES[5:0] are parameter of temperature value.

TES[5:0]		Temper°C	TES[5:0]		Temper°C
000000	**0**	**-40**	:	:	:
000001	1	**-38**	011110	30	**20**
000010	2	**-36**	011111	31	**22**
000011	3	**-34**	:	:	:
000100	4	**-32**	101000	40	**40**
000101	5	**-30**	:	:	:
:	:	:	:	:	:
010010	18	**-4**	:	:	:
010011	19	**-2**	:	:	:
010100	20	**0**	:	:	:
:	:	:	111011	59	**78**
:	:	:	111100	60	**80**
:	:	:	111101	61	**82**
:	:	:	:	:	:
:	:	:	111111	63	**86**

7.4. Command2 Description

7.4.1. Orise Engineering Mode Enable (RF0h)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
F000h	W	OPW[15:8]								00h
F001h	W	OPW[7:0]								00h

This command is used to enter into Orise engineering mode for analog gamma read and other internal testing register use only. When OPW[15:8]=0x54 & PW[7:0]=0x47, DrIC will enter into Orise engeering mode.

7.4.2. SPI Register Read Mode Enable (RA0h)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
A000h	W	RD_MOD	0	0	0	0	0	0	0	00h

This command is used to enter read mode when interface is set to SPI I/F. Before setting this command, please enable Orise engineering mode first.

- RD_MOD: Read mode enable

RD_MOD	Description
0	SPI I/F write command mode
1	SPI I/F read command mode

7.4.3. CHIPID (RB0h)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
B000h	R	0	0	0	1	1	VEN[2:0]			1Ch

VER [2:0]: ASIC version (trimming in supplier)

000: A
001: B
010: C /D
100: E

7.4.4. Display Inversion Control (RB1h)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
B100h	W/R	0	0	NLA[1:0]		0	0	NLB[1:0]		22h

Display Inversion mode control

-NLA[1:0]: Inversion setting in full colors normal mode (Normal mode)

NLA	Inversion setting in full colors normal mode
00	1-dot Inversion
01	2-dot Inversion
10	Column Inversion
11	Setting disable

-NLB[1:0]: Inversion setting in Idle mode (Idle mode).

NLB[1:0]	Inversion setting in full colors normal mode
00	1-dot Inversion
01	2-dot Inversion
10	Column Inversion
11	Setting disable

This register can be MTP program.

7.4.5. RGB Signal Control (RB2h)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
B200h	W/R	0	0	0	0	EP	DP	HSP	VSP	00h

Symbol	Name	Clock polarity set for RGB Interface
EP	DE polarity set	'1' = Low enable for RGB I/F '0' = High enable for RGB I/F (Default)
DP	PCLK polarity set	'1' = data fetched at the falling edge '0' = data fetched at the rising edge (Default)
HSP	Hsync polarity set	'1' = High level sync clock '0' = Low level sync clock (Default)
VSP	Vsync polarity set	'1' = High level sync clock '0' = Low level sync clock (Default)

This command is used for RGB I/F only.

Notes: Make sure that the data is transferred in dot units (RGB) in synchronization with DOTCLK in 6- bit interface operation.

This register can be MTP program.

7.4.6. RGB Interface Blanking Porch setting (RB3h)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
B300h	W/R	0	0	VFP[5:0]						02h
B301h	W/R	0	0	VBP[5:0]						02h
B302h	W/R	0	0	HFP[5:0]						0Ah
B303h	W/R	0	0	HBP[5:0]						14h
B304h	W/R	0	VSW[2:0]			HSW[3:0]				2Ah

VBP[5:0]: Set the delay period from falling edge of Vsync signal to first valid line. This register is used for RGB I/F and MIPI I/F.

VBP[5:0]	No. of lines of Hsync
00d	(invalid)
01d	1
02d	**2**
:	:
08d	8
:	:
63d	63

VFP [5:0]: Set the delay period from last valid line to falling edge of Vsync signal. This register is used for RGB I/F only.

VFP[5:0]	No. of lines of Hsync
00d	(invalid)
01d	1
02d	**2**
:	:
08d	8
:	:
63d	63

VSW [2:0]: Set the Vsync low pulse width. This register is used for RGB I/F only.

VSW[2:0]	No. of clock cycle of Hsync
0d	(invalid)
1d	(invalid)
2d	**2**
:	:
7d	7

HSW[3:0]: Set the Hsync low pulse width. This register is used for RGB I/F only.

HSW[3:0]	No. of clock cycle of PCLK
00d	(invalid)
01d	(invalid)
02d	2
:	:
10d	**10**
:	:
15d	15

HBP [5:0]: Set the delay period from falling edge of Hsync signal to first valid line. This register is used for RGB I/F only.

HBP[5:0]	No. of clock cycle of PCLK
00d	(invalid)
:	:
17d	(invalid)
18d	18
19d	19
20d	**20**
:	:
62d	62
63d	63

HFP [5:0]: Set the delay period from last valid line to falling edge of Hsync signal. This register is used for RGB I/F only.

HBP[5:0]	No. of clock cycle of PCLK
00d	(invalid)
:	:
9d	(invalid)
10d	**10**
:	:
62d	62
63d	63

This register can be MTP program.

7.4.7. PFM/Charge Pump power control(RB4h)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
B400h	W/R	0	0	0	VSPC	CVP[3:0]				02h
B401h	W/R	0	0	0	VSNC	CVN[3:0]				02h

VSPC: VSP on/off control

0: on

1: off

CVP [2:0]: VSP clamping voltage

CVP[3:0]		VSP(V)	CVP[3:0]		VSP(V)
0000	0	6.5	1000	8	4.9
0001	1	6.3	1001	9	4.7
0010	2	6.1	1010	10	4.5
0011	3	5.9	1011	11	disable
0100	4	5.7	1100	12	disable
0101	5	5.5	1101	13	disable
0110	6	5.3	1110	14	disable
0111	7	5.1	1111	15	disable

VSNC: VSN on/off control

0: on

1: off

CVN [2:0]: VSN clamping voltage

CVN[3:0]		VSN(V)	CVN[3:0]		VSN(V)
0000	0	-6.5	1000	8	-4.9
0001	1	-6.3	1001	9	-4.7
0010	2	-6.1	1010	10	-4.5
0011	3	-5.9	1011	11	disable
0100	4	-5.7	1100	12	disable
0101	5	-5.5	1101	13	disable
0110	6	-5.3	1110	14	disable
0111	7	-5.1	1111	15	disable

This register can be MTP program.

7.4.8. Gamma Voltage adjust Control (RB5h)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
B500h	W/R	VRP[7:0]								8Ah
B501h	W/R	VRN[7:0]								C0h
B502h	W/R	0	VRGP[6:0]							04h
B503h	W/R	NVM1	VRGN[6:0]							2Fh

NVM1: Register access enable. Setting value is valid when NVM1=1.

VRP[7:0]: The positive polarity gamma amplitude voltage setting (VGMP).

VRP[7:0]	VGMP(V)	VRP[7:0]	VGMP(V)	VRP[7:0]	VGMP(V)	VRP[7:0]	VGMP(V)	VRP[7:0]	VGMP(V)	VRP[7:0]	VGMP(V)	VRP[7:0]	VGMP(V)	VRP[7:0]	VGMP(V)
0	6.3000	32	5.9000	64	5.5000	96	5.1000	128	4.7000	160	4.3000	192	3.9000	224	3.5000
1	6.2875	33	5.8875	65	5.4875	97	5.0875	129	4.6875	161	4.2875	193	3.8875	225	disable
2	6.2750	34	5.8750	66	5.4750	98	5.0750	130	4.6750	162	4.2750	194	3.8750	..	disable
3	6.2625	35	5.8625	67	5.4625	99	5.0625	131	4.6625	163	4.2625	195	3.8625	255	disable
4	6.2500	36	5.8500	68	5.4500	100	5.0500	132	4.6500	164	4.2500	196	3.8500		
5	6.2375	37	5.8375	69	5.4375	101	5.0375	133	4.6375	165	4.2375	197	3.8375		
6	6.2250	38	5.8250	70	5.4250	102	5.0250	134	4.6250	166	4.2250	198	3.8250		
7	6.2125	39	5.8125	71	5.4125	103	5.0125	135	4.6125	167	4.2125	199	3.8125		
8	6.2000	40	5.8000	72	5.4000	104	5.0000	136	4.6000	168	4.2000	200	3.8000		
9	6.1875	41	5.7875	73	5.3875	105	4.9875	137	4.5875	169	4.1875	201	3.7875		
10	6.1750	42	5.7750	74	5.3750	106	4.9750	138	4.5750	170	4.1750	202	3.7750		
11	6.1625	43	5.7625	75	5.3625	107	4.9625	139	4.5625	171	4.1625	203	3.7625		
12	6.1500	44	5.7500	76	5.3500	108	4.9500	140	4.5500	172	4.1500	204	3.7500		
13	6.1375	45	5.7375	77	5.3375	109	4.9375	141	4.5375	173	4.1375	205	3.7375		
14	6.1250	46	5.7250	78	5.3250	110	4.9250	142	4.5250	174	4.1250	206	3.7250		
15	6.1125	47	5.7125	79	5.3125	111	4.9125	143	4.5125	175	4.1125	207	3.7125		
16	6.1000	48	5.7000	80	5.3000	112	4.9000	144	4.5000	176	4.1000	208	3.7000		
17	6.0875	49	5.6875	81	5.2875	113	4.8875	145	4.4875	177	4.0875	209	3.6875		
18	6.0750	50	5.6750	82	5.2750	114	4.8750	146	4.4750	178	4.0750	210	3.6750		
19	6.0625	51	5.6625	83	5.2625	115	4.8625	147	4.4625	179	4.0625	211	3.6625		
20	6.0500	52	5.6500	84	5.2500	116	4.8500	148	4.4500	180	4.0500	212	3.6500		
21	6.0375	53	5.6375	85	5.2375	117	4.8375	149	4.4375	181	4.0375	213	3.6375		
22	6.0250	54	5.6250	86	5.2250	118	4.8250	150	4.4250	182	4.0250	214	3.6250		
23	6.0125	55	5.6125	87	5.2125	119	4.8125	151	4.4125	183	4.0125	215	3.6125		
24	6.0000	56	5.6000	88	5.2000	120	4.8000	152	4.4000	184	4.0000	216	3.6000		
25	5.9875	57	5.5875	89	5.1875	121	4.7875	153	4.3875	185	3.9875	217	3.5875		
26	5.9750	58	5.5750	90	5.1750	122	4.7750	154	4.3750	186	3.9750	218	3.5750		
27	5.9625	59	5.5625	91	5.1625	123	4.7625	155	4.3625	187	3.9625	219	3.5625		
28	5.9500	60	5.5500	92	5.1500	124	4.7500	156	4.3500	188	3.9500	220	3.5500		
29	5.9375	61	5.5375	93	5.1375	125	4.7375	157	4.3375	189	3.9375	221	3.5375		
30	5.9250	62	5.5250	94	5.1250	126	4.7250	158	4.3250	190	3.9250	222	3.5250		
31	5.9125	63	5.5125	95	5.1125	127	4.7125	159	4.3125	191	3.9125	223	3.5125		

VRN[7:0]: The Negative polarity gamma amplitude voltage setting (VGMN).

VRN[7:0]	VGMN(V)	VRN[7:0]	VGMN(V)	VRN[7:0]	VGMN(V)	VRN[7:0]	VGMN(V)	VRN[7:0]	VGMN(V)	VRN[7:0]	VGMN(V)	VRN[7:0]	VGMN(V)	VRN[7:0]	VGMN(V)
0	-6.3000	32	-5.9000	64	-5.5000	96	-5.1000	128	-4.7000	160	-4.3000	192	-3.9000	224	-3.5000
1	-6.2875	33	-5.8875	65	-5.4875	97	-5.0875	129	-4.6875	161	-4.2875	193	-3.8875	225	disable
2	-6.2750	34	-5.8750	66	-5.4750	98	-5.0750	130	-4.6750	162	-4.2750	194	-3.8750	..	disable
3	-6.2625	35	-5.8625	67	-5.4625	99	-5.0625	131	-4.6625	163	-4.2625	195	-3.8625	255	disable
4	-6.2500	36	-5.8500	68	-5.4500	100	-5.0500	132	-4.6500	164	-4.2500	196	-3.8500		
5	-6.2375	37	-5.8375	69	-5.4375	101	-5.0375	133	-4.6375	165	-4.2375	197	-3.8375		
6	-6.2250	38	-5.8250	70	-5.4250	102	-5.0250	134	-4.6250	166	-4.2250	198	-3.8250		
7	-6.2125	39	-5.8125	71	-5.4125	103	-5.0125	135	-4.6125	167	-4.2125	199	-3.8125		
8	-6.2000	40	-5.8000	72	-5.4000	104	-5.0000	136	-4.6000	168	-4.2000	200	-3.8000		
9	-6.1875	41	-5.7875	73	-5.3875	105	-4.9875	137	-4.5875	169	-4.1875	201	-3.7875		
10	-6.1750	42	-5.7750	74	-5.3750	106	-4.9750	138	-4.5750	170	-4.1750	202	-3.7750		
11	-6.1625	43	-5.7625	75	-5.3625	107	-4.9625	139	-4.5625	171	-4.1625	203	-3.7625		
12	-6.1500	44	-5.7500	76	-5.3500	108	-4.9500	140	-4.5500	172	-4.1500	204	-3.7500		
13	-6.1375	45	-5.7375	77	-5.3375	109	-4.9375	141	-4.5375	173	-4.1375	205	-3.7375		
14	-6.1250	46	-5.7250	78	-5.3250	110	-4.9250	142	-4.5250	174	-4.1250	206	-3.7250		
15	-6.1125	47	-5.7125	79	-5.3125	111	-4.9125	143	-4.5125	175	-4.1125	207	-3.7125		
16	-6.1000	48	-5.7000	80	-5.3000	112	-4.9000	144	-4.5000	176	-4.1000	208	-3.7000		
17	-6.0875	49	-5.6875	81	-5.2875	113	-4.8875	145	-4.4875	177	-4.0875	209	-3.6875		
18	-6.0750	50	-5.6750	82	-5.2750	114	-4.8750	146	-4.4750	178	-4.0750	210	-3.6750		
19	-6.0625	51	-5.6625	83	-5.2625	115	-4.8625	147	-4.4625	179	-4.0625	211	-3.6625		
20	-6.0500	52	-5.6500	84	-5.2500	116	-4.8500	148	-4.4500	180	-4.0500	212	-3.6500		
21	-6.0375	53	-5.6375	85	-5.2375	117	-4.8375	149	-4.4375	181	-4.0375	213	-3.6375		
22	-6.0250	54	-5.6250	86	-5.2250	118	-4.8250	150	-4.4250	182	-4.0250	214	-3.6250		
23	-6.0125	55	-5.6125	87	-5.2125	119	-4.8125	151	-4.4125	183	-4.0125	215	-3.6125		
24	-6.0000	56	-5.6000	88	-5.2000	120	-4.8000	152	-4.4000	184	-4.0000	216	-3.6000		
25	-5.9875	57	-5.5875	89	-5.1875	121	-4.7875	153	-4.3875	185	-3.9875	217	-3.5875		
26	-5.9750	58	-5.5750	90	-5.1750	122	-4.7750	154	-4.3750	186	-3.9750	218	-3.5750		
27	-5.9625	59	-5.5625	91	-5.1625	123	-4.7625	155	-4.3625	187	-3.9625	219	-3.5625		
28	-5.9500	60	-5.5500	92	-5.1500	124	-4.7500	156	-4.3500	188	-3.9500	220	-3.5500		
29	-5.9375	61	-5.5375	93	-5.1375	125	-4.7375	157	-4.3375	189	-3.9375	221	-3.5375		
30	-5.9250	62	-5.5250	94	-5.1250	126	-4.7250	158	-4.3250	190	-3.9250	222	-3.5250		
31	-5.9125	63	-5.5125	95	-5.1125	127	-4.7125	159	-4.3125	191	-3.9125	223	-3.5125		

VRGP[6:0]: The positive polarity gamma amplitude voltage setting (VGSP).

VRGP[6:0]	VGSP(V)	VRGP[6:0]	VGSP(V)	VRGP[6:0]	VGSP(V)	VRGP[6:0]	VGSP(V)
0	1.8750	32	1.4750	64	1.0750	96	0.6750
1	1.8625	33	1.4625	65	1.0625	97	0.6625
2	1.8500	34	1.4500	66	1.0500	98	0.6500
3	1.8375	35	1.4375	67	1.0375	99	0.6375
4	1.8250	36	1.4250	68	1.0250	100	0.6250
5	1.8125	37	1.4125	69	1.0125	101	0.6125
6	1.8000	38	1.4000	70	1.0000	102	0.6000
7	1.7875	39	1.3875	71	0.9875	103	0.5875
8	1.7750	40	1.3750	72	0.9750	104	0.5750
9	1.7625	41	1.3625	73	0.9625	105	0.5625
10	1.7500	42	1.3500	74	0.9500	106	0.5500
11	1.7375	43	1.3375	75	0.9375	107	0.5375
12	1.7250	44	1.3250	76	0.9250	108	0.5250
13	1.7125	45	1.3125	77	0.9125	109	0.5125
14	1.7000	46	1.3000	78	0.9000	110	0.5000
15	1.6875	47	1.2875	79	0.8875	111	0.4875
16	1.6750	48	1.2750	80	0.8750	112	0.4750
17	1.6625	49	1.2625	81	0.8625	113	0.4625
18	1.6500	50	1.2500	82	0.8500	114	0.4500
19	1.6375	51	1.2375	83	0.8375	115	0.4375
20	1.6250	52	1.2250	84	0.8250	116	0.4250
21	1.6125	53	1.2125	85	0.8125	117	0.4125
22	1.6000	54	1.2000	86	0.8000	118	0.4000
23	1.5875	55	1.1875	87	0.7875	119	0.3875
24	1.5750	56	1.1750	88	0.7750	120	0.3750
25	1.5625	57	1.1625	89	0.7625	121	0.3625
26	1.5500	58	1.1500	90	0.7500	122	0.3500
27	1.5375	59	1.1375	91	0.7375	123	0.3375
28	1.5250	60	1.1250	92	0.7250	124	0.3250
29	1.5125	61	1.1125	93	0.7125	125	0.3125
30	1.5000	62	1.1000	94	0.7000	126	0.3000
31	1.4875	63	1.0875	95	0.6875	127	0.0000

VRGN[6:0]: The negative polarity gamma amplitude voltage setting (VGSN).

VRGP[6:0]	VGSP(V)	VRGP[6:0]	VGSP(V)	VRGP[6:0]	VGSP(V)	VRGP[6:0]	VGSP(V)
0	-1.8750	32	-1.4750	64	-1.0750	96	-0.6750
1	-1.8625	33	-1.4625	65	-1.0625	97	-0.6625
2	-1.8500	34	-1.4500	66	-1.0500	98	-0.6500
3	-1.8375	35	-1.4375	67	-1.0375	99	-0.6375
4	-1.8250	36	-1.4250	68	-1.0250	100	-0.6250
5	-1.8125	37	-1.4125	69	-1.0125	101	-0.6125
6	-1.8000	38	-1.4000	70	-1.0000	102	-0.6000
7	-1.7875	39	-1.3875	71	-0.9875	103	-0.5875
8	-1.7750	40	-1.3750	72	-0.9750	104	-0.5750
9	-1.7625	41	-1.3625	73	-0.9625	105	-0.5625
10	-1.7500	42	-1.3500	74	-0.9500	106	-0.5500
11	-1.7375	43	-1.3375	75	-0.9375	107	-0.5375
12	-1.7250	44	-1.3250	76	-0.9250	108	-0.5250
13	-1.7125	45	-1.3125	77	-0.9125	109	-0.5125
14	-1.7000	46	-1.3000	78	-0.9000	110	-0.5000
15	-1.6875	47	-1.2875	79	-0.8875	111	-0.4875
16	-1.6750	48	-1.2750	80	-0.8750	112	-0.4750
17	-1.6625	49	-1.2625	81	-0.8625	113	-0.4625
18	-1.6500	50	-1.2500	82	-0.8500	114	-0.4500
19	-1.6375	51	-1.2375	83	-0.8375	115	-0.4375
20	-1.6250	52	-1.2250	84	-0.8250	116	-0.4250
21	-1.6125	53	-1.2125	85	-0.8125	117	-0.4125
22	-1.6000	54	-1.2000	86	-0.8000	118	-0.4000
23	-1.5875	55	-1.1875	87	-0.7875	119	-0.3875
24	-1.5750	56	-1.1750	88	-0.7750	120	-0.3750
25	-1.5625	57	-1.1625	89	-0.7625	121	-0.3625
26	-1.5500	58	-1.1500	90	-0.7500	122	-0.3500
27	-1.5375	59	-1.1375	91	-0.7375	123	-0.3375
28	-1.5250	60	-1.1250	92	-0.7250	124	-0.3250
29	-1.5125	61	-1.1125	93	-0.7125	125	-0.3125
30	-1.5000	62	-1.1000	94	-0.7000	126	-0.3000
31	-1.4875	63	-1.0875	95	-0.6875	127	0.0000

This register can be MTP program.

7.4.9. VPDC power control setting (RB7h)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
B700h	W/R	0	0	0	VPDC2ON	0	VPDC2[2:0]			04h
B701h	W/R	0	0	0	VPDC1ON	VPDC1[3:0]				08h

[VPDC2ON]: VPDC2 on/off control
0: on (Default)
1: off

VPDC2 [2:0]: VPDC voltage control (0.2 V per step)
000: 1.0 V
001: 1.2 V
:
111: 2.4 V

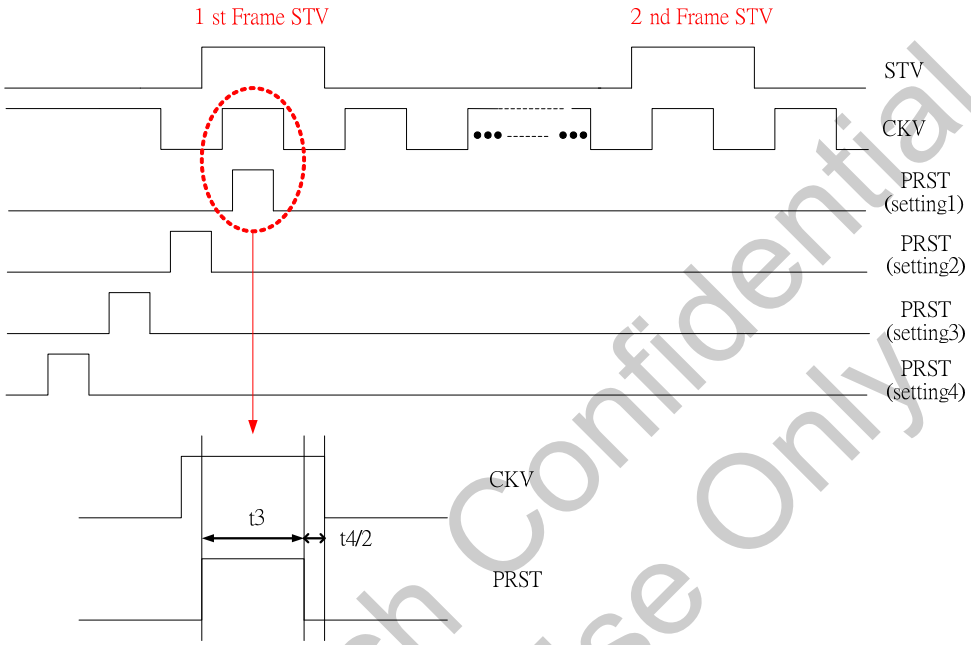
[VPDC1ON]: VPDC1 on/off control
0: on (Default)
1: off

VPDC1 [3:0]: VPDC voltage control (0.2 V per step)
0000: 2.2 V
0001: 2.4 V
:
0011: 2.8V
:
1110: 5 V
1111: disable

This register can be MTP program.

7.4.10. Panel reset and STV1/2 function setting (RB8h)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
B800h	W/R	0	0	0	0	0	PRSTON	PRST[1:0]		01h
B801h	W/R	STV[7:0]								A1h



- PRSTON: Panel reset pin on/off control

PRSTON	set
0	ON
1	Off

- PRST [1:0]: Panel reset pin control

PRST[1:0]	set
00	Setting1
01	Setting2(default)
10	Setting3
11	Setting4

- STV[7:0]: STV1 to STV2 Start timing setting(1H/bit)

ALSON=1 (STV1 on, STV2 on)					
	CSV	STV1 Start Line	STV2 Start Line	STV1to2[7:0]	Gate output direction
TB=1	"H"	First (1)	Second (((STV1to2[7:0]-1) x 2)+1)	((Gate Black1 line number)/2) +1	Gate normal scan T-->B (G1-->Gn)
TB=0	"L"	Second ((Gn-((STV1to2[7:0]-1) x 2))+1)	First (1)	((Gate Black1 line number)/2) +1	Gate reverse scan B-->T (Gn-->G1)

STV[7:0] default value = 161

ALSON=0 (STV1 on, STV2 off(keep GND))					
	CSV	STV1 Start Line	STV2 Start Line	STV1to2[7:0]	Gate output direction
TB=1	"H"	First	-	Don't care	Gate normal scan T-->B (G1-->Gn)
TB=0	"L"	First	-	Don't care	Gate reverse scan B-->T (Gn-->G1)

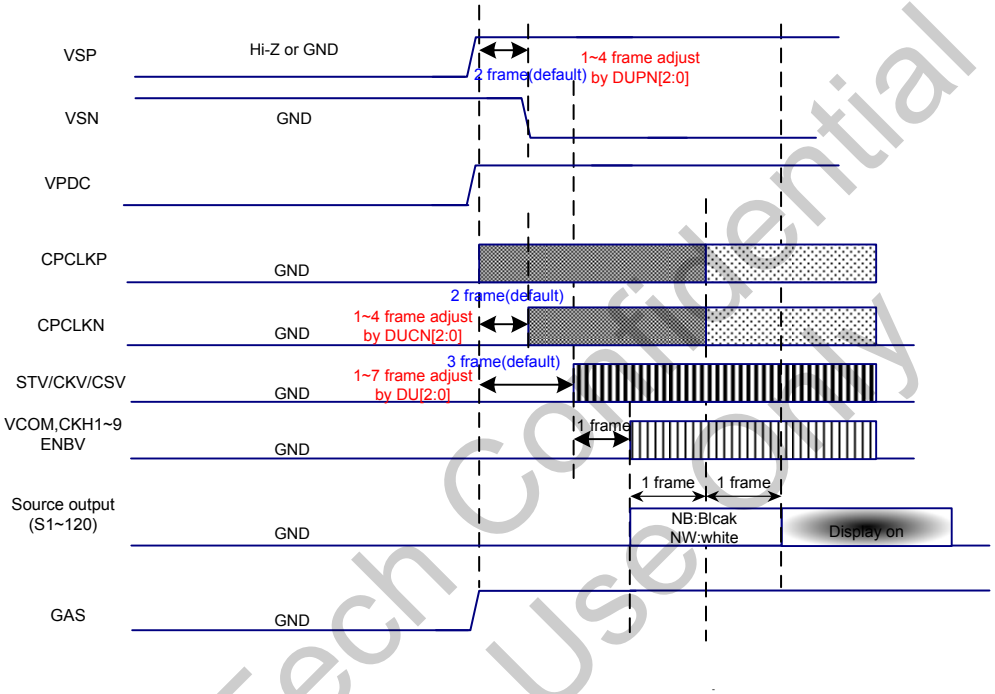
Note: Gn by RESOL[2:0]

RESOL[2:0]	Gn	
0	320	
1	400	default
2	432	
3	240	
4	320	

This register can be MTP program.

7.4.11. Dummy frame control setting (RB9h)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
B900h	W/R	0	0	DN[1:0]		DCPN[1:0]		DUPN[1:0]		35h
B901h	W/R	0	0	0	0	0	CPFR[2:0]			05h
B902h	W/R	CNON	CNF[2:0]			CPON	CPF[2:0]			33h



[DUCN1:DUCN0]: Power on sequence Dummy frame from VSP to CPCLKP signal start stage

00: 1 frame

01: 2 frame (default)

10: 3 frame

11: 4frame

[DU2:DU0]: Power on sequence Dummy frame from XVDD to panel control signal start stage

000: 0 frame

001: 1 frame

010: 2 frame

011: 3 frame (default)

.....

111: 7 frame

[DUPN1:DUPN0]: Power on sequence Dummy frame from VSP to VSN signal start stage

00: 1 frame

01: 2 frame (default)

10: 3 frame

11: 4frame

CPON/CNON: CPCLKP/N on/off control

0: ON(default)

1:OFF

CPF[2:0]: CPCLKN frequency control

000: 10 kHz

001: 20 kHz

010: 30 kHz

011: 40 kHz(default)

100: 50 kHz

101: 60 kHz

110: 70 kHz

111: 80 kHz

CNF[2:0]: CPCLKN frequency control

000: 10 kHz

001: 20 kHz

010: 30 kHz

011: 40 kHz(default)

100: 50 kHz

101: 60 kHz

110: 70 kHz

111: 80 kHz

CPFR[2:0]: CPCLKP/N Prepare frequency control

000: 10 kHz

001: 20 kHz

010: 30 kHz

011: 40 kHz

100: 50 kHz

101: 60 kHz (default)

110: 70 kHz

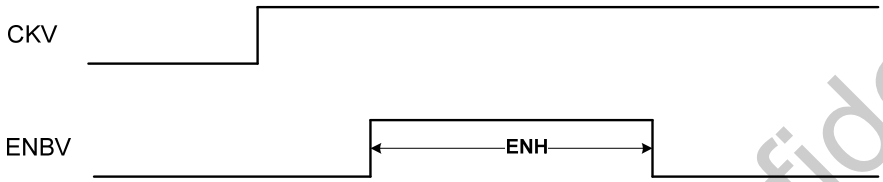
111: 80 kHz

This register can be MTP program.

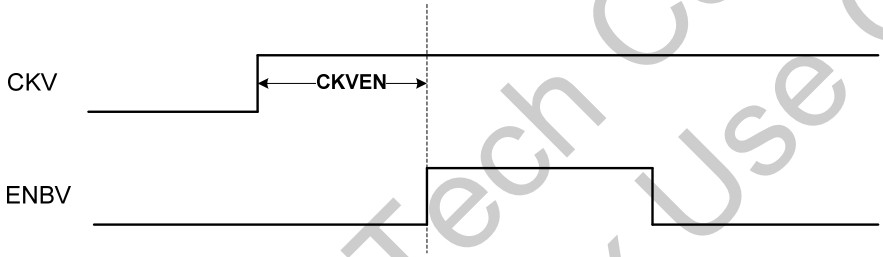
7.4.12. Display Waveform Cycle setting (RBAh)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
BA00h	W/R	0	0	0	0	0	CKHW[2:0]			07h
BA01h	W/R	0	CKHP[2:0]			CKHS2[1:0]		CKHS1[1:0]		26h
BA02h	W/R	0	ENH[6:0]							3Ch
BA03h	W/R	0	0	0	0	0	0	CKVEN[1:0]		01h

ENH



CKVEN



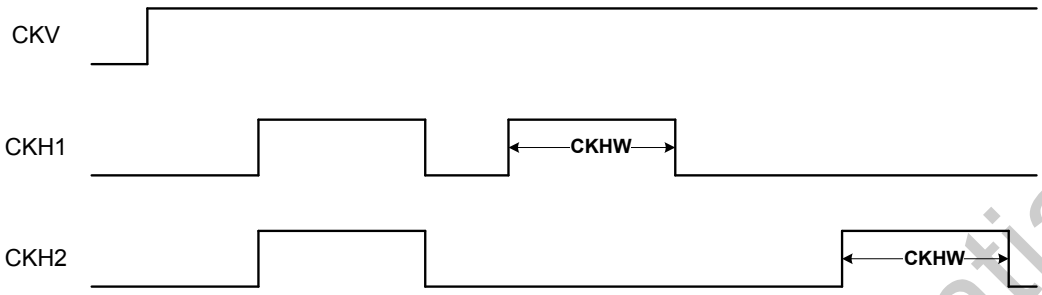
- ENBV High Time

ENH[6:0]	ENBV high pulse width(1 clk/step)
0d	27
1d	28
--	--
41d	68
--	--
127d	154

- CKVEN

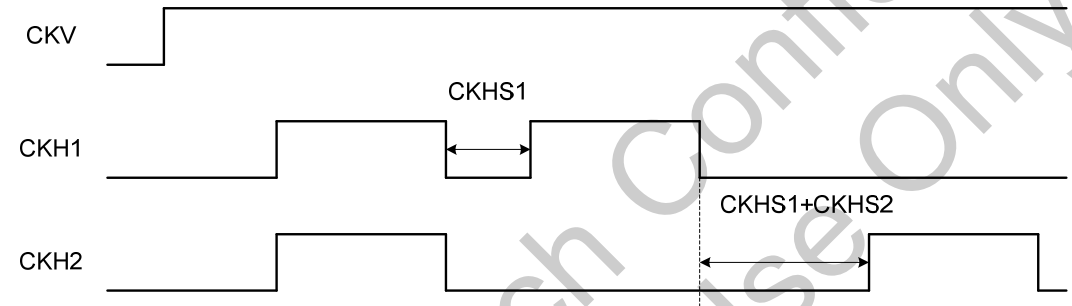
CKVEN[1:0]	CKV to ENBV Space(1 clk/step)
0d	Invalid
1d	1
2d	2
3d	3

CKHW & CKHS

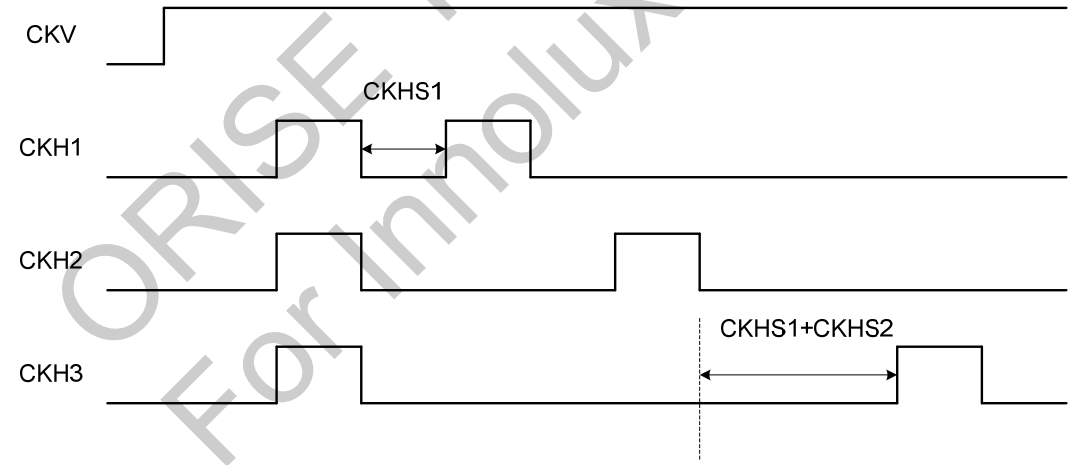


CKHS1 & CKHS2

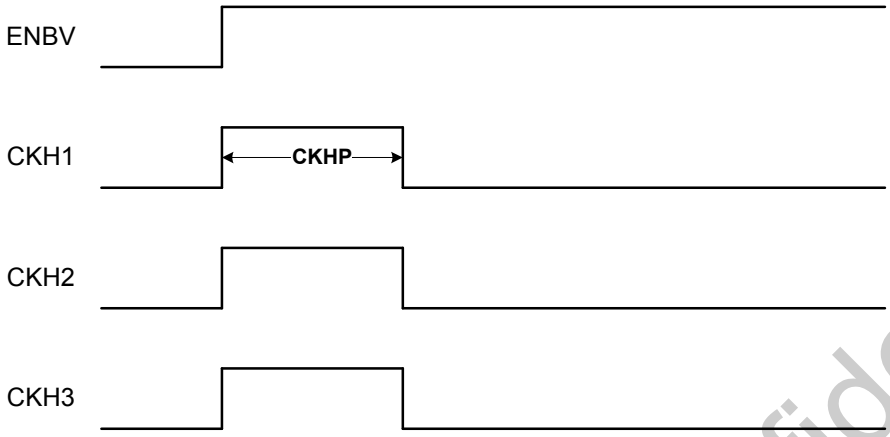
1:6 MUX



1:9 MUX



ENBV & CKHP



-CKHW[2:0] : CKH1/CKH2/CKH3/CKH4/CKH5/CKH6/CKH7/CKH8/CKH9

-CKHS[1:0] : CKH1_CKH2/CKH2_CKH3 … CKH8_CKH9/

CKH pulse width

CKHW[2:0]	CKH pulse width (1 clk/step)
0d	Invalid
1d	1
2d	2
--	--
5d	5
--	--
7d	7

CKH Space1 / CKH Space2

CKHS1[1:0] **CKHS2[1:0]**	CKH Space (1 clk/step)
0d	Invalid
1d	1
2d	2
3d	3

Pre-charge pulse width

CKHP[2:0]	Pre-charge pulse width(1 clk/step)
0d	Invalid
1d	1
2d	2
3d	3
4d	4
5d	5
6d	6

This register can be MTP program

7.4.13. Write Command reset register (RBBH)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
BB00h	W/R	0	0	0	0	GPI[3:0]				00h

Register 0xBBh –Write Command reset register for R51H. These inputs are configured based upon glass size

• R051h = 0x0000 -- 2.0” display. (for reference only)

• R051h = 0x0100 – 2.2” display. (for reference only)

• R051h = 0x0200 – 2.4” display. (for reference only)

• R051h = 0x0400 – 2.8” display. Identifies this display

For R51H read register, RBBH is MTP to set the glass size information.

This register can be MTP program.

7.4.14. Mux1 to 6 CKH timing structure register (RBCH)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
BC00h	W/R	0	GA[2:0]			0	GB[2:0]			00h
BC01h	W/R	0	GC[2:0]			0	GD[2:0]			44h

GA[2:0] Order of Group A (dot, 2dot, col inv)

GA2	GA1	GA0							
0	0	0	A1	C1	E1	1	3	5	default
0	0	1	A1	E1	C1	1	5	3	
0	1	0	C1	E1	A1	3	5	1	
0	1	1	C1	A1	E1	3	1	5	
1	0	0	E1	A1	C1	5	1	3	
1	0	1	E1	C1	A1	5	3	1	

GB[2:0] Order of Group B (dot, 2dot, col inv)

GB2	GB1	GB0							
0	0	0	B1	D1	F1	2	4	6	default
0	0	1	B1	F1	D1	2	6	4	
0	1	0	D1	F1	B1	4	6	2	
0	1	1	D1	B1	F1	4	2	6	
1	0	0	F1	B1	D1	6	2	4	
1	0	1	F1	D1	B1	6	4	2	

GC[2:0] Order of Group C (dot, 2dot, col inv)

GC:

GC2	GC1	GC0							
0	0	0	A2	C2	E2	1	3	5	
0	0	1	A2	E2	C2	1	5	3	
0	1	0	C2	E2	A2	3	5	1	
0	1	1	C2	A2	E2	3	1	5	
1	0	0	E2	A2	C2	5	1	3	default
1	0	1	E2	C2	A2	5	3	1	

GD[2:0] Order of Group D (dot, 2dot, col inv)

GD2	GD1	GD0							
0	0	0	B2	D2	F2	2	4	6	
0	0	1	B2	F2	D2	2	6	4	
0	1	0	D2	F2	B2	4	6	2	
0	1	1	D2	B2	F2	4	2	6	
1	0	0	F2	B2	D2	6	2	4	default
1	0	1	F2	D2	B2	6	4	2	

This register can be MTP program.

7.4.15. Mux1 to 9 CKH timing structure register (RBDH)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
BD00h	W/R	0	GX[2:0]			0	GY[2:0]			00h
BD01h	W/R	0	GZ[2:0]			0	GAA[2:0]			11h
BD02h	W/R	OF9[3:0]				0	0	M9C[1:0]		32h

GX[2:0] Order of Group X (dot, 2dot, col inv)

GX2	GX1	GX0											
0	0	0	A1	C1	E1	G1	I1	1	3	5	7	9	default
0	0	1	I1	G1	E1	C1	A1	9	7	5	3	1	
0	1	0	E1	C1	A1	I1	G1	5	3	1	9	7	
0	1	1	G1	I1	A1	C1	E1	7	9	1	3	5	
1	0	0	A1	G1	E1	C1	I1	1	7	5	3	9	
1	0	1	I1	C1	E1	G1	A1	9	3	5	7	1	
1	1	0	C1	I1	A1	G1	E1	3	9	1	7	5	
1	1	1	E1	G1	A1	I1	C1	5	7	1	9	3	

GY[2:0] Order of Group Y (dot, 2dot, col inv)

GY2	GY1	GY0									
0	0	0	B1	D1	F1	H1	2	4	6	8	default
0	0	1	H1	F1	D1	B1	8	6	4	2	
0	1	0	D1	B1	H1	F1	4	2	8	6	
0	1	1	F1	H1	B1	D1	6	8	2	4	
1	0	0	B1	F1	D1	H1	2	6	4	8	
1	0	1	H1	D1	F1	B1	8	4	6	2	
1	1	0	D1	H1	B1	F1	4	8	2	6	
1	1	1	F1	B1	H1	D1	6	2	8	4	

GZ[2:0] Order of Group Z (dot, 2dot, col inv)

GZ2	GZ1	GZ0										
0	0	0	A2	C2	E2	G2	I2	1	3	5	7	9	
0	0	1	I2	G2	E2	C2	A2	9	7	5	3	1	default
0	1	0	E2	C2	A2	I2	G2	5	3	1	9	7	
0	1	1	G2	I2	A2	C2	E2	7	9	1	3	5	
1	0	0	A2	G2	E2	C2	I2	1	7	5	3	9	
1	0	1	I2	C2	E2	G2	A2	9	3	5	7	1	
1	1	0	C2	I2	A2	G2	E2	3	9	1	7	5	
1	1	1	E2	G2	A2	I2	C2	5	7	1	9	3	

GAA[2:0] Order of Group AA (dot, 2dot, col inv)

GAA2	GAA1	GAA0									
0	0	0	B2	D2	F2	H2	2	4	6	8	
0	0	1	H2	F2	D2	B2	8	6	4	2	default
0	1	0	D2	B2	H2	F2	4	2	8	6	
0	1	1	F2	H2	B2	D2	6	8	2	4	
1	0	0	B2	F2	D2	H2	2	6	4	8	
1	0	1	H2	D2	F2	B2	8	4	6	2	
1	1	0	D2	H2	B2	F2	4	8	2	6	
1	1	1	F2	B2	H2	D2	6	2	8	4	

OF90

OF0	P.S. Amp. Offset cancellation	
0	4 frame cancellation	
1	8 frame cancellation	default

OF9[3:1]

OF3	OF2	OF1		
0	0	0	offset0	
0	0	1	offset1	default
0	1	0	offset2	
0	1	1	offset3	
1	0	0	offset4	
1	0	1	offset5	

M9C[1:0]

M6C1	M6C0	
0	0	Dancing MUX
0	1	Same Color MUX (option1, default for Normally white)
1	0	Same Color MUX (option2, defult for Normally black)
1	1	

Selecting sequence:

Option1: ckh1 => ckh2 => ckh3 => ckh4 => ckh5 => ckh6 => ckh7 => ckh8 => ckh9

All the sequence should be same every line & every frame

Option2: ckh9 => ckh8 => ckh7 => ckh6 => ckh5 => ckh4 => ckh3 => ckh2 => ckh1

All the sequence should be same every line & every frame

Option3: Frame Odd: ckh1 => ckh2 => ckh3 => ckh4 => ckh5 => ckh6 => ckh7 => ckh8 => ckh9

Frame Even: ckh9 => ckh8 => ckh7 => ckh6 => ckh5 => ckh4 => ckh3 => ckh2 => ckh1

All the sequence should be same every line

This register can be MTP program.

7.4.16. Gamma (‘+’polarity) Correction Characteristics Setting R gamma (RC0h)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
C000h	W/R	0	0	VP0[5:0]						-
C001h	W/R	0	0	VP1[5:0]						-
C002h	W/R	0	0	VP8[5:0]						-
C003h	W/R	0	0	0	VP16[4:0]					-
C004h	W/R	0	0	0	VP24[4:0]					-
C005h	W/R	0	0	VP52[5:0]						-
C006h	W/R	0	0	0	VP80[4:0]					-
C007h	W/R	0	0	0	VP108[4:0]					-
C008h	W/R	0	0	0	VP128[4:0]					-
C009h	W/R	0	0	0	VP147[4:0]					-
C00Ah	W/R	0	0	0	VP175[4:0]					-
C00Bh	W/R	0	0	VP203[5:0]						-
C00Ch	W/R	0	0	0	VP231[4:0]					-
C00Dh	W/R	0	0	0	VP239[4:0]					-
C00Eh	W/R	0	0	VP247[5:0]						-
C00Fh	W/R	0	0	VP254[5:0]						-
C010h	W/R	0	0	VP255[5:0]						-

Note: Analog gamma setting value can not be read out unless registers have been written or programmed.

This register can be MTP program.

7.4.17. Gamma ('-'polarity) Correction Characteristics Setting R gamma (RC1h)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
C100h	W/R	0	0	VN0[5:0]						-
C101h	W/R	0	0	VN1[5:0]						-
C102h	W/R	0	0	VN8[5:0]						-
C103h	W/R	0	0	0	VP16[4:0]					-
C104h	W/R	0	0	0	VP24[4:0]					-
C105h	W/R	0	0	VN52[5:0]						-
C106h	W/R	0	0	0	VP80[4:0]					-
C107h	W/R	0	0	0	VP108[4:0]					-
C108h	W/R	0	0	0	VP128[4:0]					-
C109h	W/R	0	0	0	VP147[4:0]					-
C10Ah	W/R	0	0	0	VP175[4:0]					-
C10Bh	W/R	0	0	VN203[5:0]						-
C10Ch	W/R	0	0	0	VP231[4:0]					-
C10Dh	W/R	0	0	0	VP239[4:0]					-
C10Eh	W/R	0	0	VN247[5:0]						-
C10Fh	W/R	0	0	VN254[5:0]						-
C110h	W/R	0	0	VN255[5:0]						-

Note: Analog gamma setting value can not be read out unless registers have been written or programmed.

This register can be MTP program.

7.4.18. Gamma (‘+’polarity) Correction Characteristics Setting G gamma (RC2h)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
C200h	W/R	0	0	VP0[5:0]						-
C201h	W/R	0	0	VP1[5:0]						-
C202h	W/R	0	0	VP8[5:0]						-
C203h	W/R	0	0	0	VP16[4:0]					-
C204h	W/R	0	0	0	VP24[4:0]					-
C205h	W/R	0	0	VP52[5:0]						-
C206h	W/R	0	0	0	VP80[4:0]					-
C207h	W/R	0	0	0	VP108[4:0]					-
C208h	W/R	0	0	0	VP128[4:0]					-
C209h	W/R	0	0	0	VP147[4:0]					-
C20Ah	W/R	0	0	0	VP175[4:0]					-
C20Bh	W/R	0	0	VP203[5:0]						-
C20Ch	W/R	0	0	0	VP231[4:0]					-
C20Dh	W/R	0	0	0	VP239[4:0]					-
C20Eh	W/R	0	0	VP247[5:0]						-
C20Fh	W/R	0	0	VP254[5:0]						-
C210h	W/R	0	0	VP255[5:0]						-

Note: Analog gamma setting value can not be read out unless registers have been written or programmed.

This register can be MTP program.

7.4.19. Gamma ('-'polarity) Correction Characteristics Setting G gamma (RC3h)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
C300h	W/R	0	0	VN0[5:0]						-
C301h	W/R	0	0	VN1[5:0]						-
C302h	W/R	0	0	VN8[5:0]						-
C303h	W/R	0	0	0	VP16[4:0]					-
C304h	W/R	0	0	0	VP24[4:0]					-
C305h	W/R	0	0	VN52[5:0]						-
C306h	W/R	0	0	0	VP80[4:0]					-
C307h	W/R	0	0	0	VP108[4:0]					-
C308h	W/R	0	0	0	VP128[4:0]					-
C309h	W/R	0	0	0	VP147[4:0]					-
C30Ah	W/R	0	0	0	VP175[4:0]					-
C30Bh	W/R	0	0	VN203[5:0]						-
C30Ch	W/R	0	0	0	VP231[4:0]					-
C30Dh	W/R	0	0	0	VP239[4:0]					-
C30Eh	W/R	0	0	VN247[5:0]						-
C30Fh	W/R	0	0	VN254[5:0]						-
C310h	W/R	0	0	VN255[5:0]						-

Note: Analog gamma setting value can not be read out unless registers have been written or programmed.

This register can be MTP program.

7.4.20. Gamma (‘+’polarity) Correction Characteristics Setting B gamma (RC4h)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
C400h	W/R	0	0	VP0[5:0]						-
C401h	W/R	0	0	VP1[5:0]						-
C402h	W/R	0	0	VP8[5:0]						-
C403h	W/R	0	0	0	VP16[4:0]					-
C404h	W/R	0	0	0	VP24[4:0]					-
C405h	W/R	0	0	VP52[5:0]						-
C406h	W/R	0	0	0	VP80[4:0]					-
C407h	W/R	0	0	0	VP108[4:0]					-
C408h	W/R	0	0	0	VP128[4:0]					-
C409h	W/R	0	0	0	VP147[4:0]					-
C40Ah	W/R	0	0	0	VP175[4:0]					-
C40Bh	W/R	0	0	VP203[5:0]						-
C40Ch	W/R	0	0	0	VP231[4:0]					-
C40Dh	W/R	0	0	0	VP239[4:0]					-
C40Eh	W/R	0	0	VP247[5:0]						-
C40Fh	W/R	0	0	VP254[5:0]						-
C410h	W/R	0	0	VP255[5:0]						-

Note: Analog gamma setting value can not be read out unless registers have been written or programmed.

This register can be MTP program.

7.4.21. Gamma (‘-’polarity) Correction Characteristics Setting B gamma (RC5h)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
C500h	W/R	0	0	VN0[5:0]						-
C501h	W/R	0	0	VN1[5:0]						-
C502h	W/R	0	0	VN8[5:0]						-
C503h	W/R	0	0	0	VP16[4:0]					-
C504h	W/R	0	0	0	VP24[4:0]					-
C505h	W/R	0	0	VN52[5:0]						-
C506h	W/R	0	0	0	VP80[4:0]					-
C507h	W/R	0	0	0	VP108[4:0]					-
C508h	W/R	0	0	0	VP128[4:0]					-
C509h	W/R	0	0	0	VP147[4:0]					-
C50Ah	W/R	0	0	0	VP175[4:0]					-
C50Bh	W/R	0	0	VN203[5:0]						-
C50Ch	W/R	0	0	0	VP231[4:0]					-
C50Dh	W/R	0	0	0	VP239[4:0]					-
C50Eh	W/R	0	0	VN247[5:0]						-
C50Fh	W/R	0	0	VN254[5:0]						-
C510h	W/R	0	0	VN255[5:0]						-

Note: Analog gamma setting value can not be read out unless registers have been written or programmed.

This register can be MTP program.

7.4.22. Write the version management register 1,2 (RCBh)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
CB00h	W/R	VER[15:8]								20h
CB01h	W/R	VER[7:0]								89h

For R0h Write the version management register 1,2. This register can setting by MTP function.
Bit 8 to 16 shows a product name(default: 11H). Bit 0 to 7 shows a product version(default: 00)
Register 00h – Product name and version. This cannot be changed without Motorola's written permission.

This register can be MTP program.

7.4.23. Oscillator Divided Adjustment (RCFh)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
CF00h	W/R	0	0	0	0	0	0	1	1	03h
CF01h	W/R	FIX_ENA	OSCDIV[6:0]							0Eh

This command is used to set MCLK/PCLK divided ratio manully.
- FIX_ENA: Enable OSCDIV[7:0] valid to control MCLK/PCLK ratio.
- OSCDIV[6:0]: MCLK/PCLK ratio setting

This register can be MTP program.

7.4.24. Write ID2 (RD1h)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
D100h	W/R	1	ID2[6:0]							80h

This command is used to set ID2

This register can be MTP program.

7.4.25. Write ID3 (RD2h)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
D200h	W/R	ID3[7:0]								6Ch

This command is used to set ID3

Resolution	ID3[7:0] Default
Landscape	0x6C
Portrait	0x5D

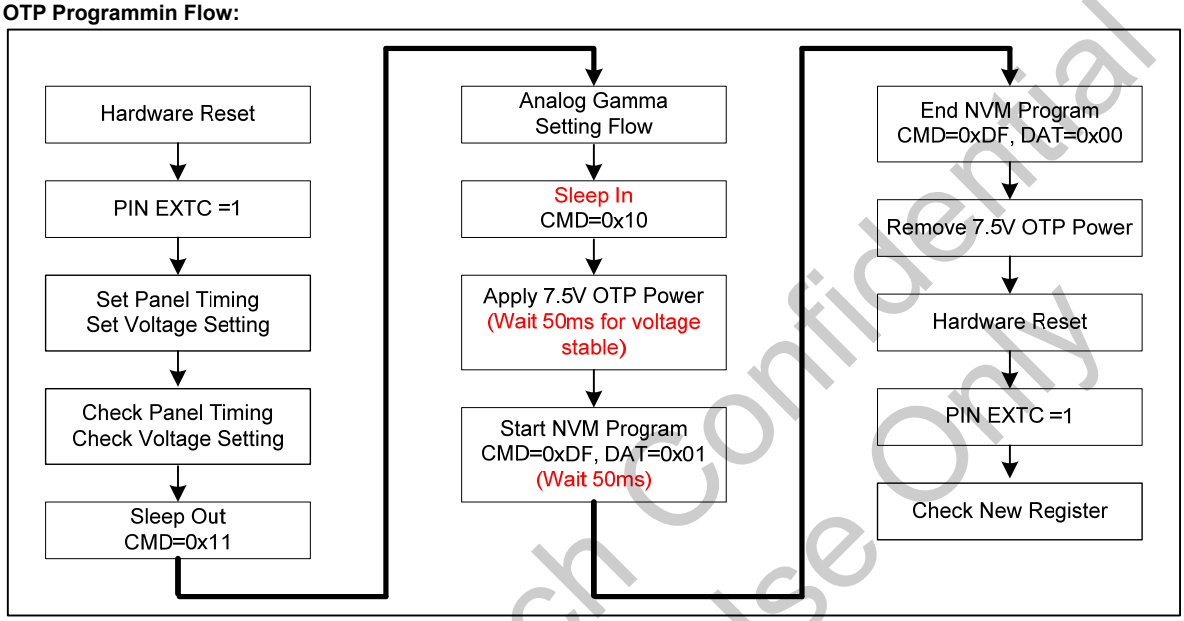
This register can be MTP program.

7.4.26. OTP Write Mode (RDFh)

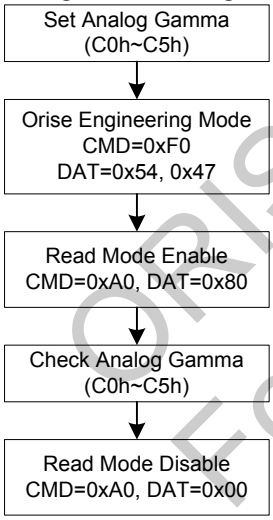
Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
DF00h	W	0	0	0	0	0	0	0	NVM_PGM	00h

This command is used to program OTP.

OTP Programmin Flow:



Analog Gamma Setting Flow:



7.4.27. MIPI RX Delay Setting (RE2h)

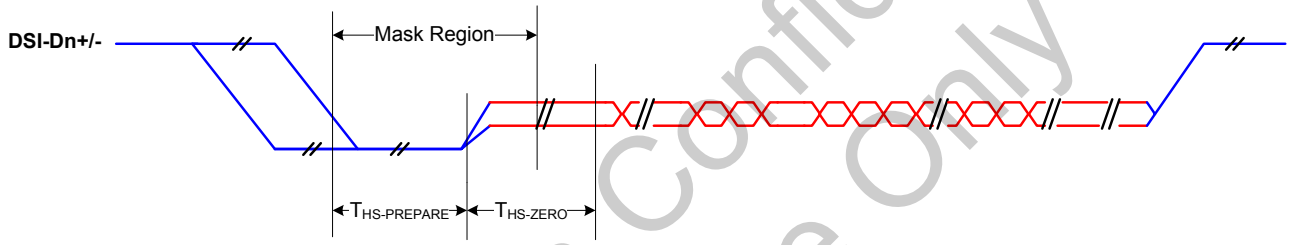
Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
E200h	W/R	RCDLY_EN	RCDLY_SEL[2:0]			SKEW_N[1:0]		SKEW_P[1:0]		C0h

This command is used to set MIPI RX timing

- RCDLY_EN: Enable mask length adjusting function
- RCDLY_SEL[2:0]: Set mask length and valid when RCDLY_EN =1

RCDLY_EN	Mask Length Setting
0	Fixed value
1	RCDLY_SEL[2:0]

For MIPI state from LP-11 to high speed mode, an internal mask is need to ignore noise from analog circuit. The mask length can be set by register RCDLY_SEL[2:0] when RCDLY_EN = 1



- SKEW_N[1:0]: Negative data lane data delay setting
- SKEW_P[1:0]: Postive data lane data delay setting

SKEW_N/P[1:0]	Delay Select (ns)
0h	+ 0.6
1h	+ 1.2
2h	+ 1.8
3h	+ 2.4

This register can be MTP program.

7.4.28. Landscape MIPI Video Mode One Line Clock Number (RE9h)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
E900h	W/R	0	LSCP_RTN[6:0]							5Ah

This command is used to set internal clock number within oen line at landscape resolution.

This register can be MTP program.

7.4.29. Portrait MIPI Video Mode One Line Clock Number (REAh)

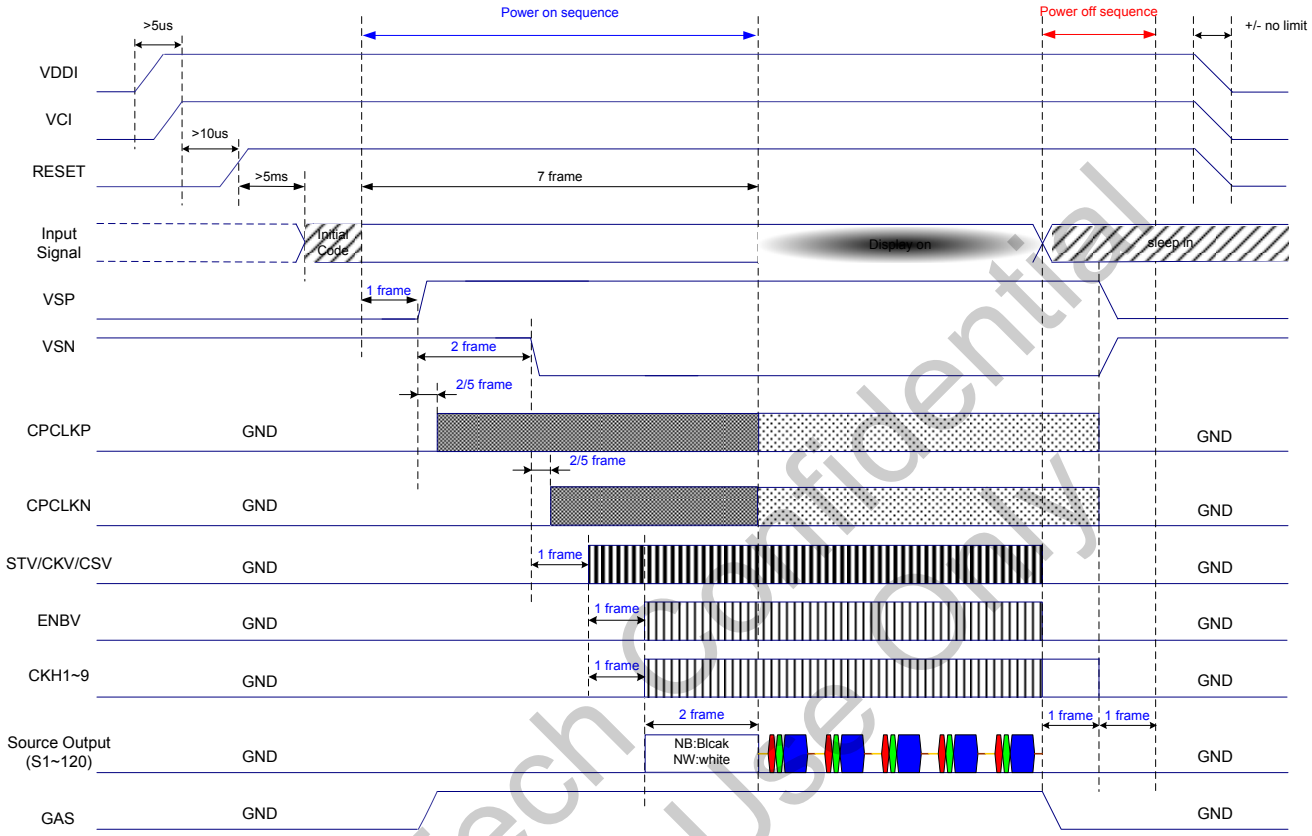
Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
EA00h	W/R	0	PORT_RTN[6:0]							46h

This command is used to set internal clock number within oen line at portrait resolution.

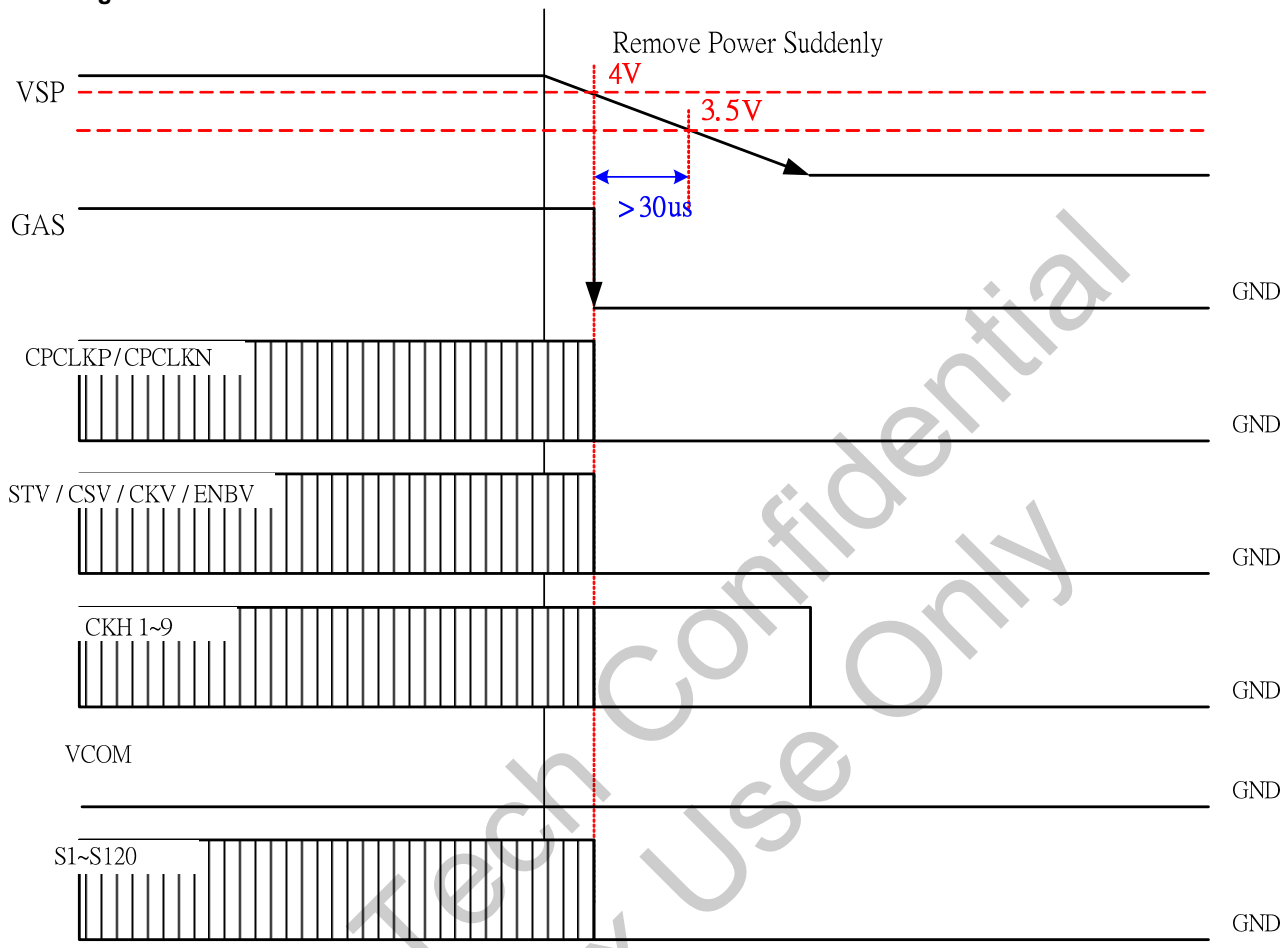
This register can be MTP program.

8. POWER ON/OFF SEQUENC

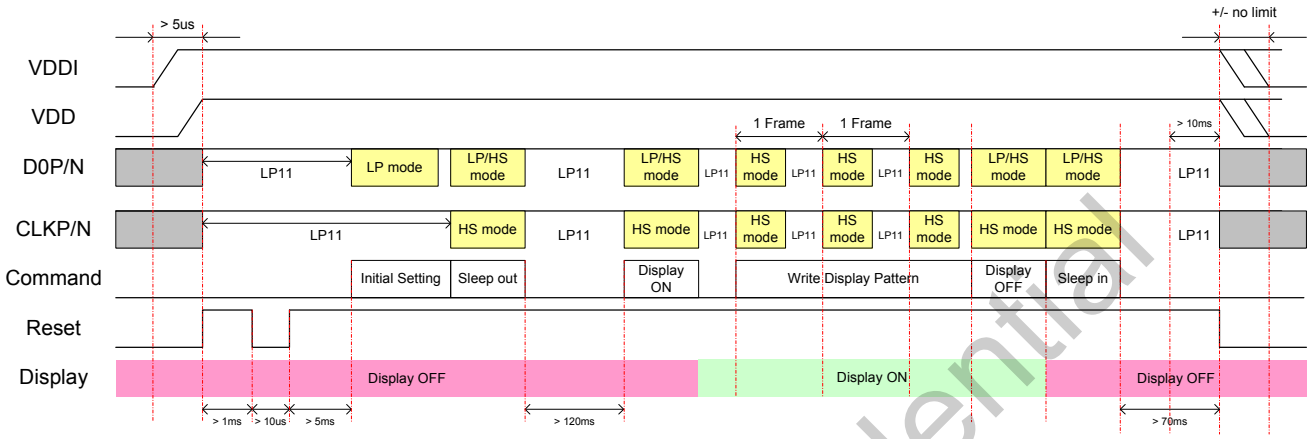
8.1. Power On/Off Timing Chart



8.2. Timing Chart Of Abnormal Power Off



8.3. Power-on/off sequence for MIPI interface



Note : We proposed using non-continue CLK with Burst mode

9. ELECTRICAL SPECIFICATIONS

9.1. Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	VCI	- 0.3 ~ +4.6	V
Supply voltage (Logic I/F)	VDDIO	- 0.3 ~ +4.6	V
Logic Input voltage range	V_{IN}	- 0.3 ~ VDDIO + 0.3	V
Logic Output voltage range	V_O	- 0.3 ~ VDDIO + 0.3	V
Operating temperature range	T_{OPR}	-30 ~ +80	℃
Storage Temperature range	T_{STG}	-40 ~ +85	℃

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

9.2. DC Characteristics

Parameter	Symbol	Conditions	Specification			Unit	Related Pins
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	VCI	Operating Voltage	2.3	2.775	3.6	V	
Logic Operating voltage	VDDIO	I/O supply voltage-	1.6	1.875	3.6	V	
Input / Output							
Logic High level input voltage	VIH		0.7VDDIO		VDDIO	V	Note1
Logic Low level input voltage	VIL	-	0		0.3VDDIO	V	Note1
Logic High level output voltage	VOH	IOH = -1.0mA	0.8VDDIO		VDDIO	V	
Logic Low level output voltage	VOL	IOL = +1.0mA	0		0.2VDDIO	V	
Logic High level input current	IIH				1	μA	
Logic Low level input current	IIL		-1			μA	
Logic Input leakage current	IIL	VIN = VDDIO or VSS	-0.1	-	0.1	μA	
Booster Operation							
Internal reference voltage	V_{REF}			1.8		V	
Positive system voltage	VSP		3		6.6	V	
Negative system voltage	VSN		-6.6		-3	V	
Source Driver							
Source output settling time	Tr	Below with 99% precision		**2.3**	**2.8**	us	Note 4,
Output deviation voltage (Source output channel)	V,dev				**15**	mV	Note 4
					6	mV	
Output offset voltage	VOFSET				**25**	mV	Note 5

Note 1: VDDIO=1.6 to 3.6V, VCI=2.3 to 3.6V, VSSA=VSS=0V, Ta=-40 to 85℃ (to +85℃ no damage)

Note 2, 3, 4: When the measurements are performed with LCD module, Measurement Points are like below.

Note 3: D[23:0], RESET, IM[1:0], PCLK, VSync, HSync, DE and Test pins

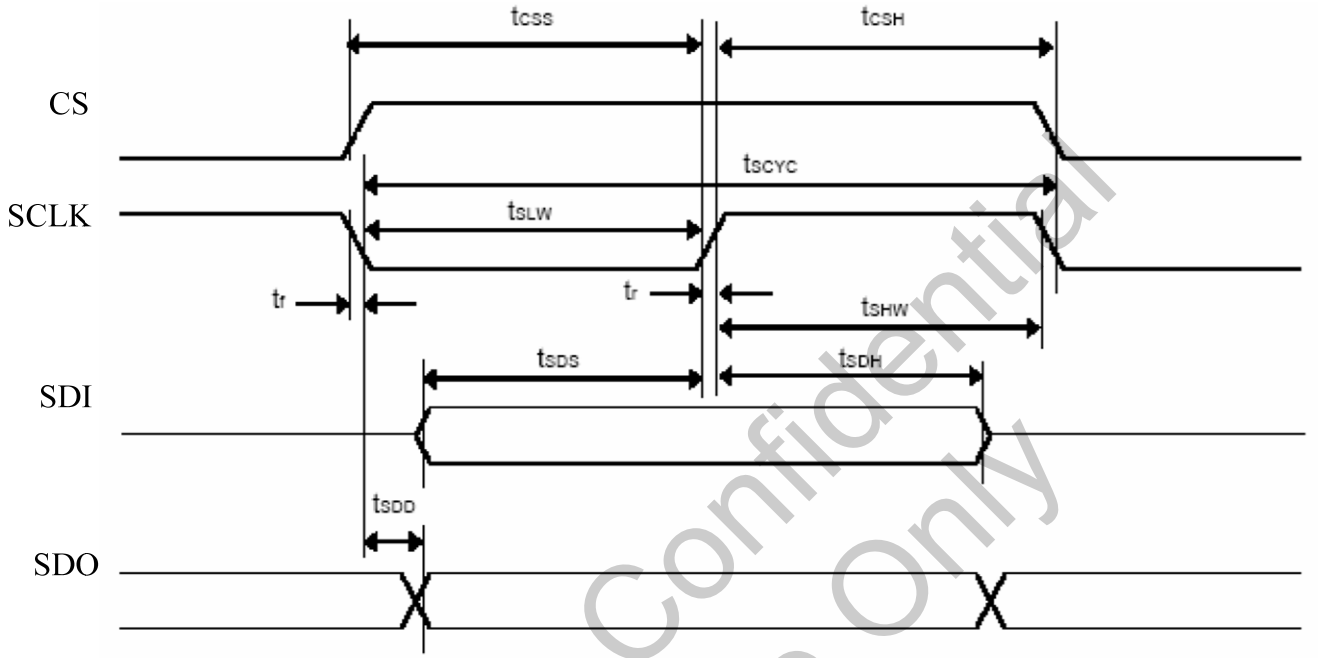
Note 4, Panel loading refer panel information

Note 5, The Max. value is between with Note 4 measure point and Gamma setting value.

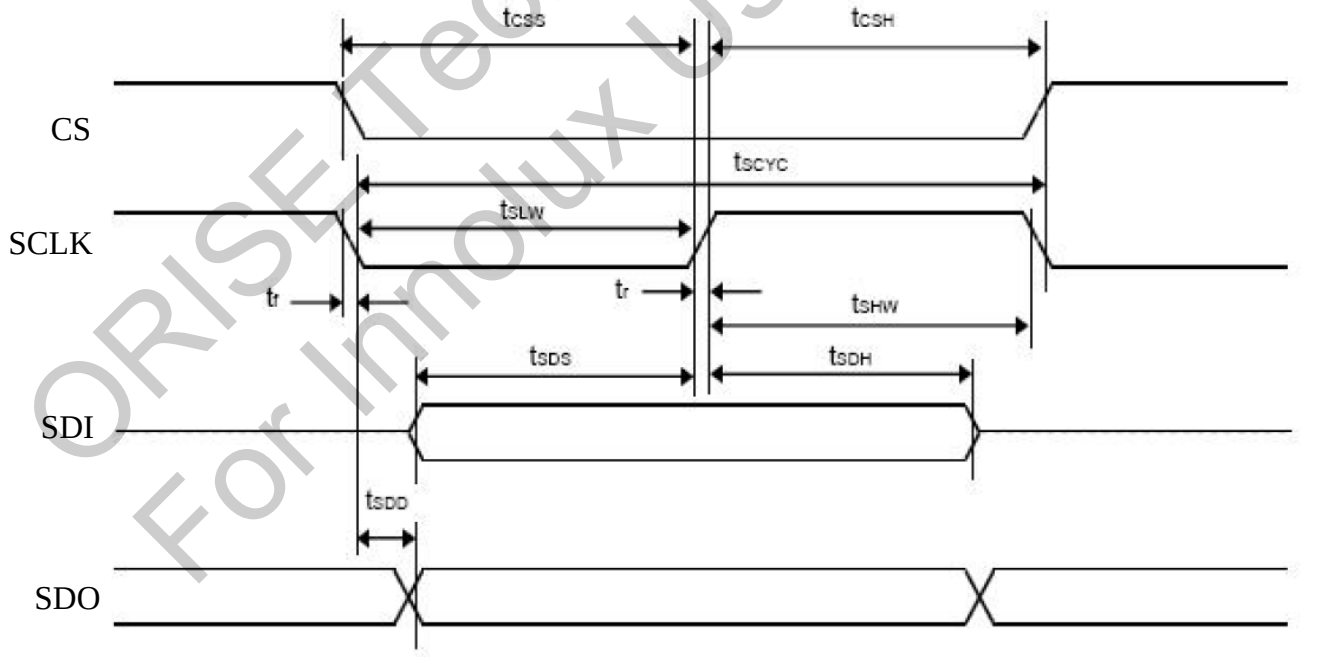
9.3. Timing Charts

9.3.1. Serial interface characteristics

When CSTROL=1



When CSTROL=0



T_A=-40 to +85℃, VDDIO=1.6 to 3.6V, VCI=2.3 to 3.6V, VSS=0V

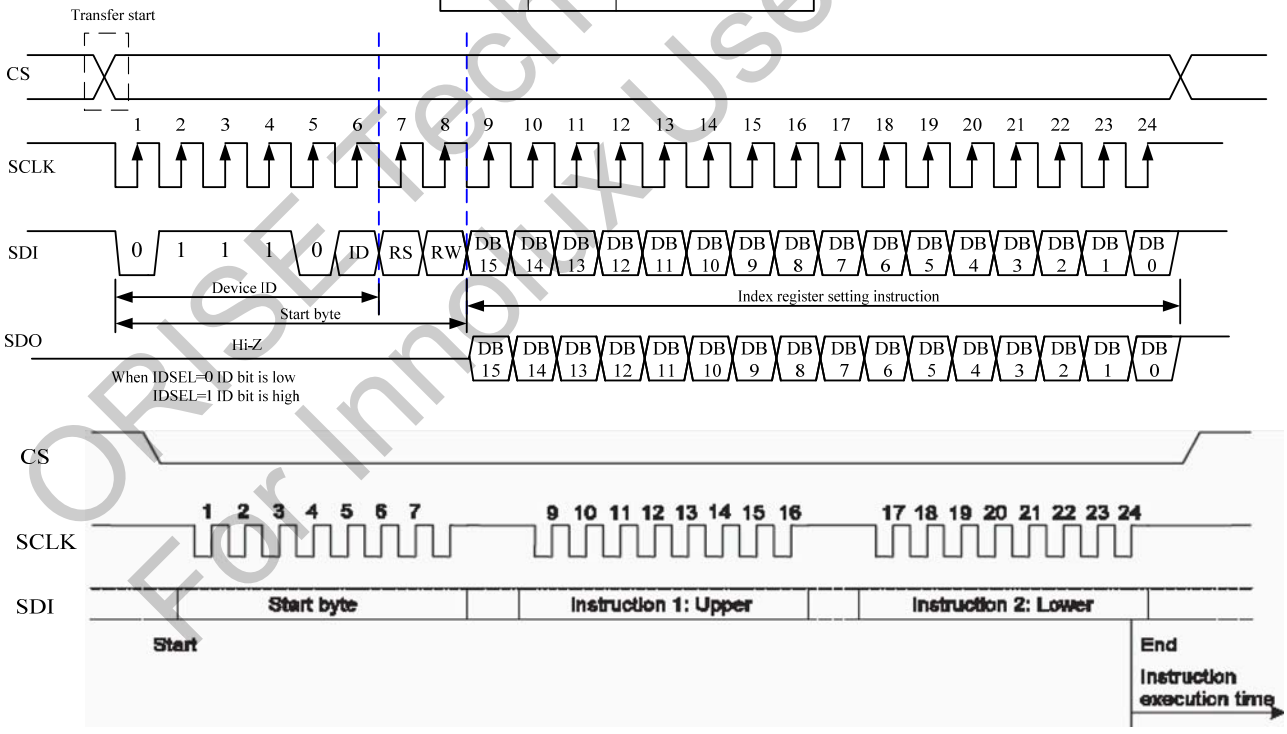
Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Serial clock cycle	t_{SCYC}		210			ns
SCLK high level pulse width	t_{SHW}		90			ns
SCLK low level pulse width	t_{SLW}		90			ns
Data setup time	t_{SDS}		90			ns
Data hold time	t_{SDH}		90			ns
LCDCS - SCLK time	t_{CSS}		120			ns
	t_{CSH}		120			ns
SCLK↓→SO output delay time	t_{SDO}				105	ns

Note TYP. value are reference value when T_A = 25°C.

Remarks 1. The input signal rise/fall times (t_r, t_f) are rated as 25 ns or less.

2. All timing is rated based on 20 to 80% of VDDIO.

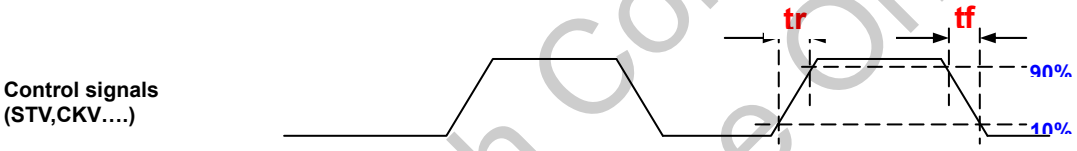
RS	RW	Function
0	0	Set to index register
0	1	-
1	0	Write to instruction
1	1	Read to ID



9.3.2. AC Characteristics of DC/DC Converter

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
VCSW1 rising time	Tr	period from 0.1*VCI to 0.9*VCI (external component load is around 150pf)			20	nS
VCSW1 falling time	Tf	Period from 0.9*VCI to 0.1*VCI (external component load is around 150pf)			20	nS
VCSW1 Ron	Ron	Connect a voltage source “0.7V” at this pad and observe the current through voltage source.		20		Ω
VCSW2 rising time	Tr	period from 0.1*VCI to 0.9*VCI			20	nS
VCSW2 falling time	Tf	Period from 0.9*VCI to 0.1*VCI			20	nS
VCSW2 Ron	Ron	Connect a voltage source “0.7V” at this pad and observe the current through voltage source.		20		Ω

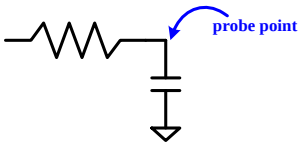
9.3.3. AC Characteristic of Panel Control Signal



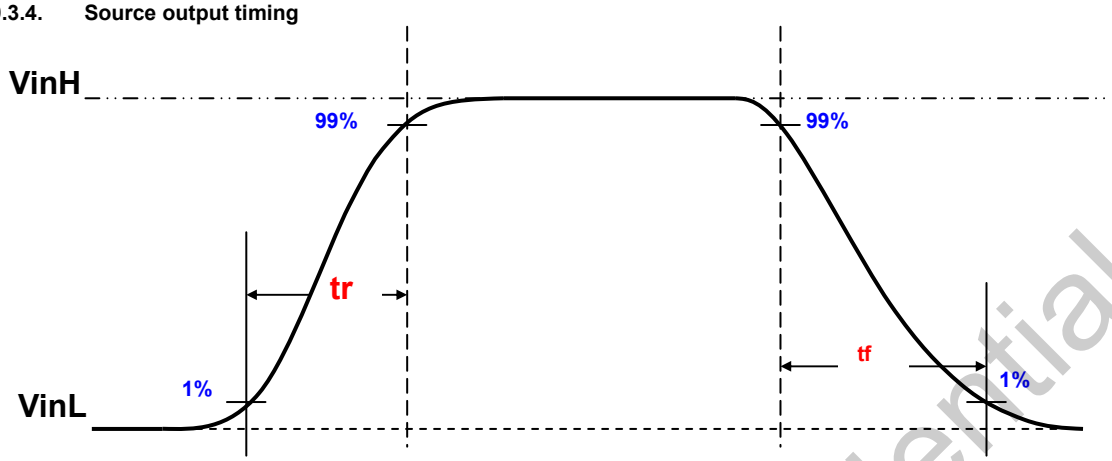
Item	Symbol	Min.	Typ.	Max.	unit
STV, CKV, ENBV, CSV, GAS, DCCLKP/N	Vil	-	0-	0.1VSP	V
	Vih	-0.9VSP	VSP-	-	V
CKH1/2/3/4/5/6 (CKH1/2/3/4/5/6/7/8/9)	Vil	-	0	0.1VSP	V
	vih	0.9VSP	VSP-	-	V

Item	Symbol	Min.	Typ.	Max.	unit
STV, CKV, ENBV, CSV, GAS, DCCLKP/N	tr	-	-	100	ns
	tf	-	-	100	ns
CKH1/2/3/4/5/6 (CKH1/2/3/4/5/6/7/8/9)	tr	-	-	100	ns
	tf	-	-	100	ns

Remark: Probe point of Control signal’s Loading



9.3.4. Source output timing



RGB output characteristic

Item	symbol	Conditions	240xRGBx400	320xRGBx240	Unit
Rise time	tr	1% - 99%	2.3	2.8	us
fall time	tf	99% - 1%	2.3	2.8	us

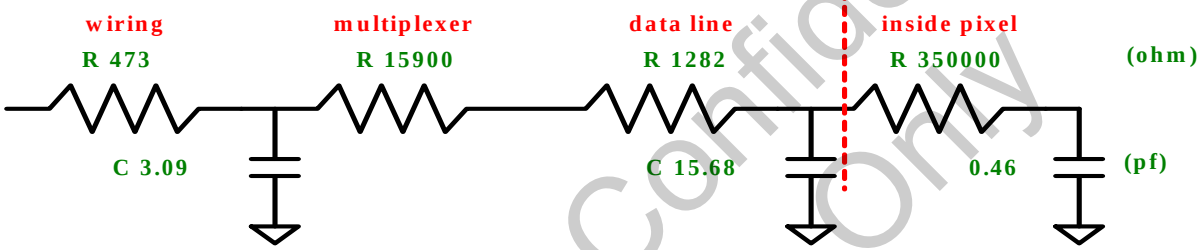
Remark: Probe point of RGB & VCOM Loading

9.3.5. Panel Loading

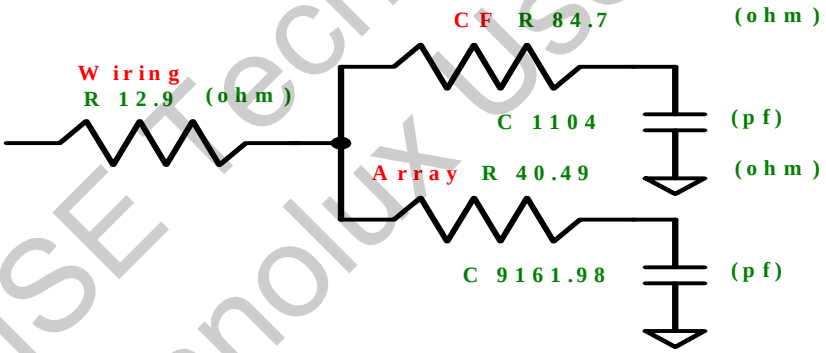
(a) 2.8" 240x400 NB (for portrait)

Pin Name	R(Ω)	C(pf)	Pin Name	R(Ω)	C(pf)
RGB	See blow		CKH1	186.5	6.98
CKV	617	26.78	CKH2	186.5	6.98
STV	617	26.78	CKH3	186.5	6.98
ENBV	617	26.78	CKH4	186.5	6.98
CSV	617	26.78	CKH5	186.5	6.98
GAS	617	26.78	CKH6	186.5	6.98
CPCLKN	339	**0.2uF**	VCOM	See blow	
CPCLKP	339	**0.2uF**			

RGB Loading



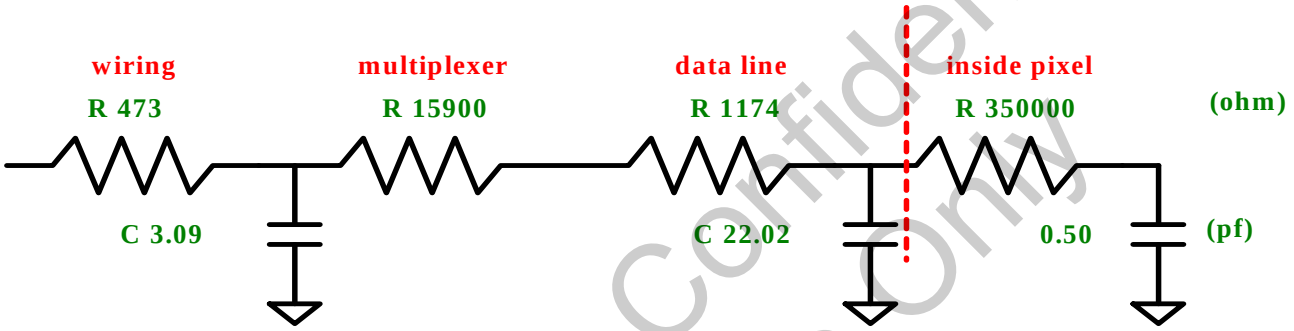
VCOM Loading



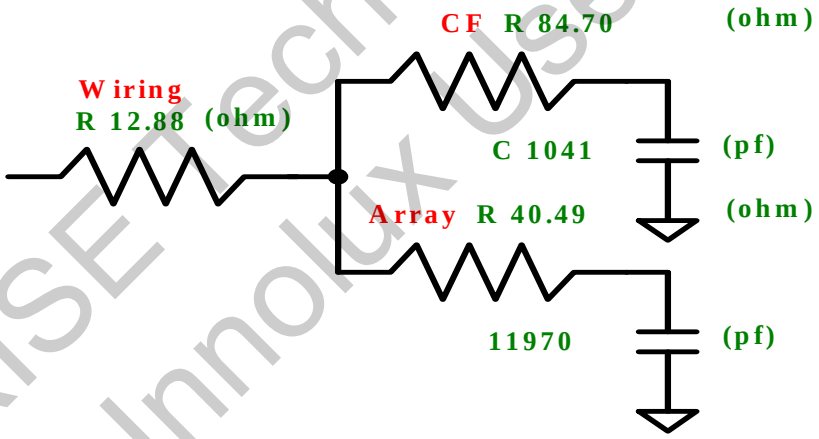
(b) 2.8" 240x400 NW (for portrait)

Pin Name	R(Ω)	C(pf)	Pin Name	R(Ω)	C(pf)
RGB	See blow		CKH1	186.4	6.98
CKV	617	26.77	CKH2	186.4	6.98
STV	617	26.77	CKH3	186.4	6.98
ENBV	617	26.77	CKH4	186.4	6.98
CSV	617	26.77	CKH5	186.4	6.98
GAS	617	26.77	CKH6	186.4	6.98
CPCLKN	339	**0.2uF**	VCOM	See blow	
CPCLKP	339	**0.2uF**			

RGB Loading



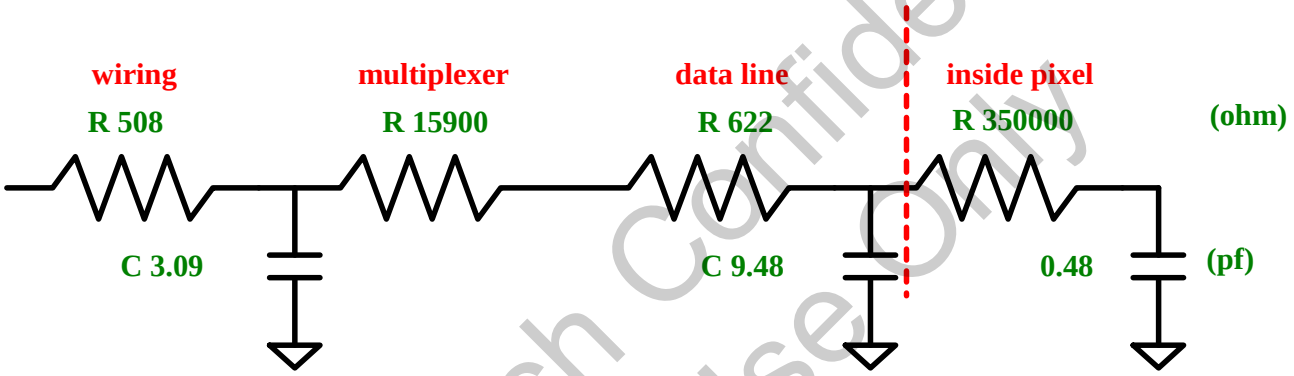
VCOM Loading



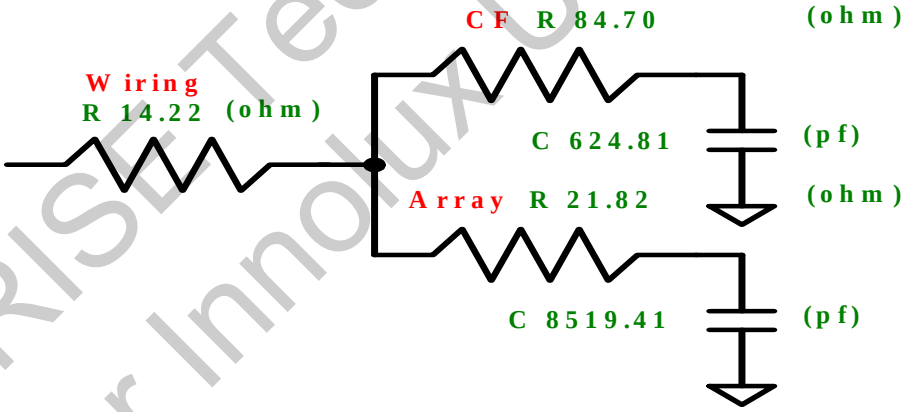
(c) 2.0" 320x240 NB (for landscape)

Pin Name	R(Ω)	C(pf)	Pin Name	R(Ω)	C(pf)
RGB	See blow		CKH1	160.84	5.37
CKV	500.58	21.12	CKH2	160.84	5.37
STV	500.58	21.12	CKH3	160.84	5.37
ENBV	500.58	21.12	CKH4	160.84	5.37
CSV	500.58	21.12	CKH5	160.84	5.37
GAS	500.58	21.12	CKH6	160.84	5.37
CPCLKN	237.56	**0.2uF**	VCOM	See blow	
CPCLKP	237.56	**0.2uF**			

RGB Loading



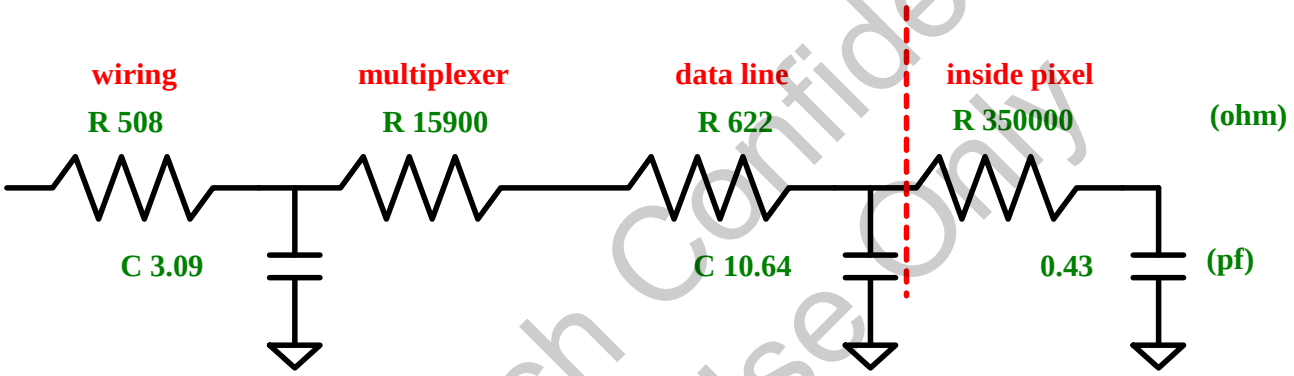
VCOM Loading



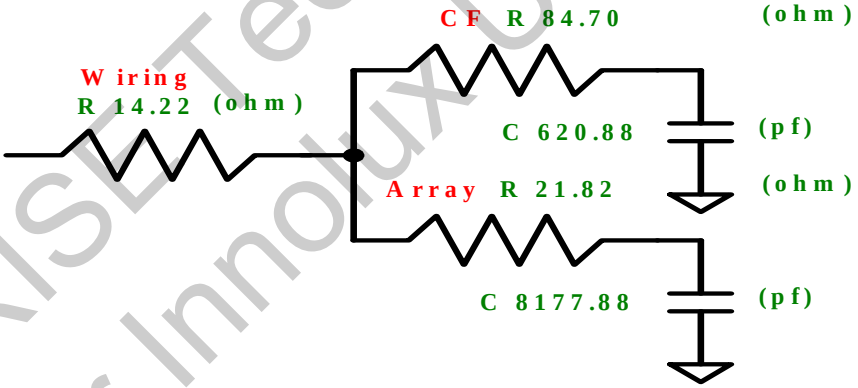
(d) Minimum case (2.0'' 320x240 NW) (for landscape)

Pin Name	R(Ω)	C(pf)	Pin Name	R(Ω)	C(pf)
RGB	See blow		CKH1	160.84	5.37
CKV	500.58	21.12	CKH2	160.84	**5.37**
STV	500.58	21.12	CKH3	160.84	**5.37**
ENBV	500.58	21.12	CKH4	160.84	**5.37**
CSV	500.58	21.12	CKH5	160.84	**5.37**
GAS	500.58	21.12	CKH6	160.84	**5.37**
CPCLKN	237.56	**0.2uF**	VCOM	See blow	
CPCLKP	237.56	**0.2uF**			

RGB Loading



VCOM Loading



9.3.6. MIPI-DSI characteristics

9.3.6.1. High speed mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Mode						
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	8	-	25	ns
DSI-CLK+/-	UI_{INSTA} , UI_{INSTB}	UI instantaneous Halfs	4	-	12.5	ns
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3UI	ps

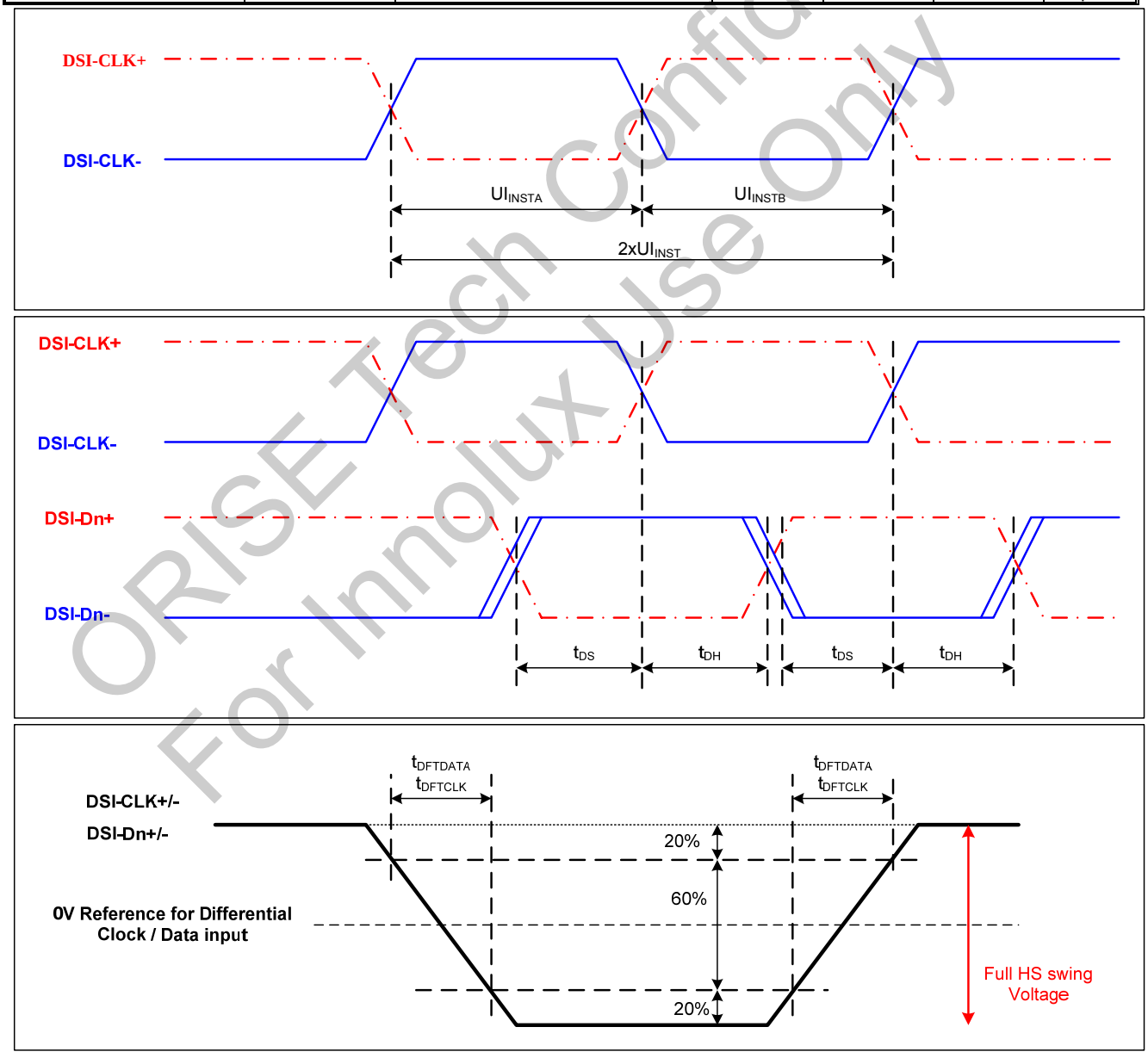


Figure: AC characteristics for MIPI-DSI High speed mode

9.3.6.2. Low power mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power mode						
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU Display Module	50	-	-	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module MPU	58	-	-	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2XT_{LPXD}$	ns
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	$5XT_{LPXD}$	-	-	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	$4XT_{LPXD}$	-	-	ns
DSI-D0+/-	Ratio T_{LPX}	Ratio of T_{LPXM} / T_{LPXD} between MCU and display module	2/3	-	3/2	

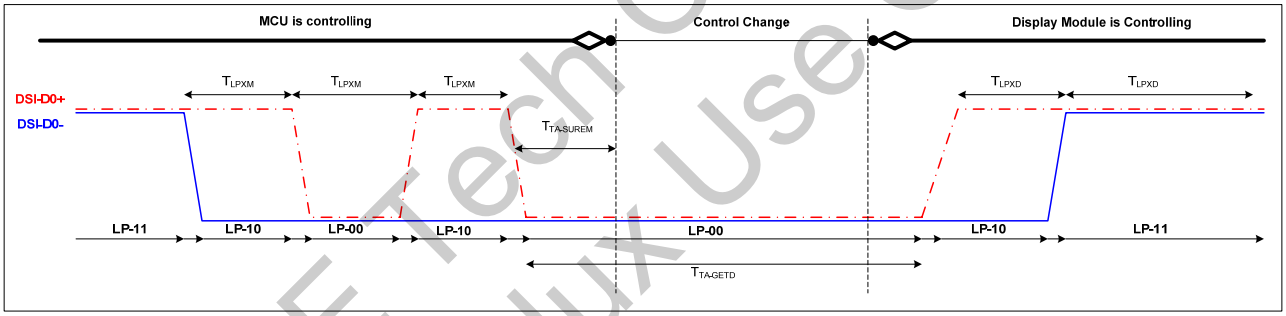


Figure: BTA from the MCU to the Display Module

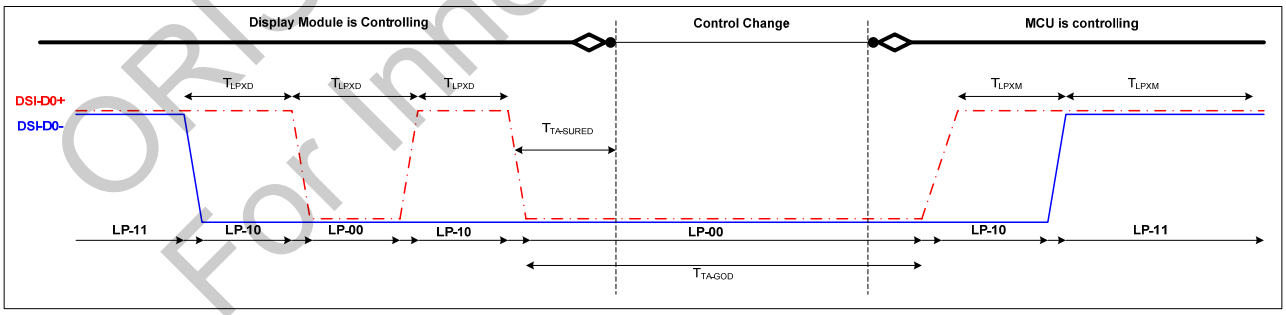


Figure: BTA from the Display Module to the MCU

9.3.6.3. Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	T_{LPX}	Length of any low-power state period	50	-	-	ns
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4UI	-	85ns + 6UI	ns
DSI-Dn+/-	$T_{HS-PREPARE}$ +$T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time to drive HS-0 before the sync sequence	145ns + 10UI	-	-	ns
DSI-Dn+/-	$T_{D-TERM-EN}$	Time to enable Data Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	35ns + 4UI	ns
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns + 4UI	ns
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns
DSI-Dn+/-	T_{EoT}	Time from start of $T_{HS-TRAIL}$ period to start of LP-11 state	-	-	105ns + 12UI	ns

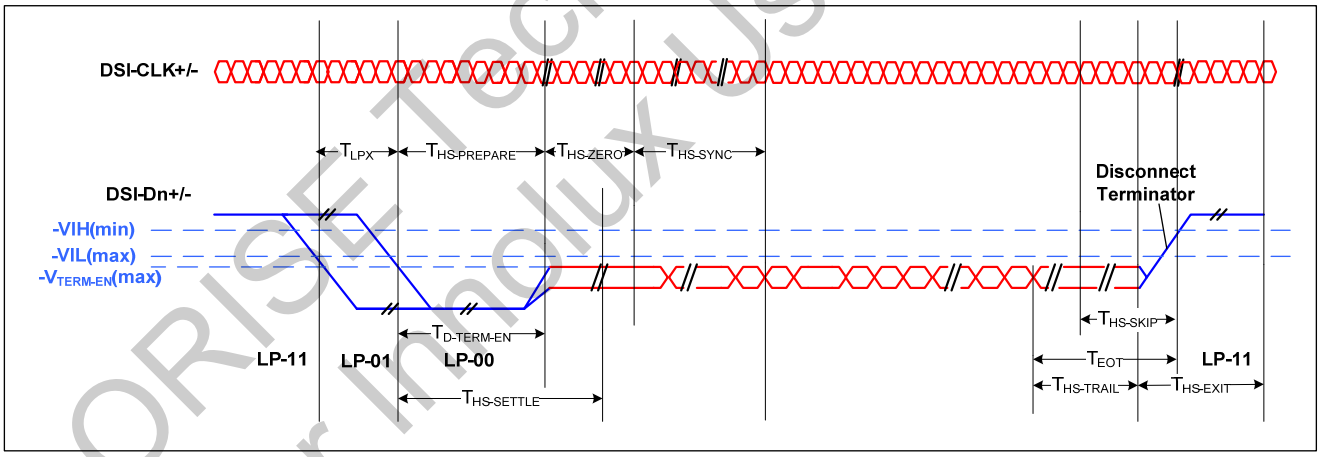


Figure: High Speed Data Transmission Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	$T_{CLK-POST}$	**Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode**	60ns + 52UI	-	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	**Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode**	8	-	-	UI
DSI-CLK+/-	$T_{CLK-PREPARE}$	**Time to drive LP-00 to prepare for HS clock transmission**	38	-	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	**Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$**	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$ **+$T_{CLK-ZERO}$**	**$T_{CLK-PREPARE}$ + time for lead HS-0 drive period before starting Clock**	300	-	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	**Time to drive HS differential state after last payload clock bit of a HS transmission burst**	60	-	-	ns
DSI-CLK+/-	T_{EoT}	**Time from start of $T_{CLK-TRAIL}$ period to start of LP-11 state**	-	-	105ns + 12UI	ns

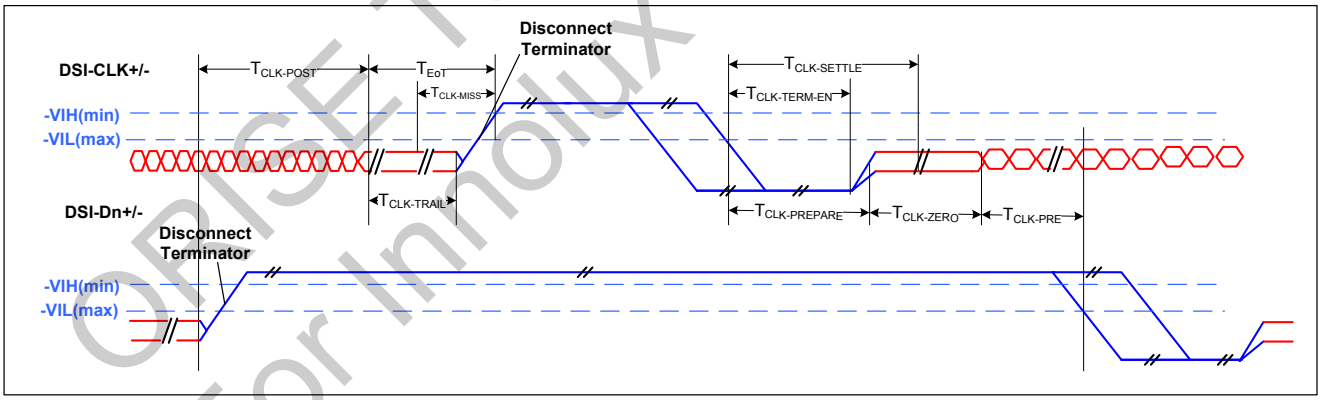


Figure: Switching the clock Lane between clock Transmission and Low Power Mode

9.3.6.4. LP-11 between High Speed and Low Power Modes

DSI-D0 High Speed or Low Power modes are starting or finishing from/to Stop State (SS, LP-11) when 4 different combinations, what are listed below, are possible:

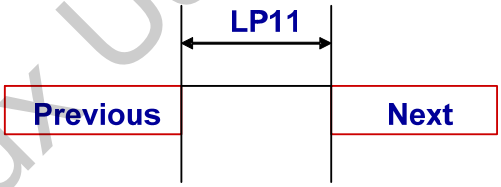
1. High Speed Mode => Stop State (SS, LP-11) => High Speed Mode
2. High Speed Mode => Stop State (SS, LP-11) => Low Power Mode
3. Low Power Mode => Stop State (SS, LP-11) => High Speed Mode
4. Low Power Mode => Stop State (SS, LP-11) => Low Power Mode

The Low Power Mode is also including 2 different functions:

1. Escape
2. Bus Turnaround (BTA)

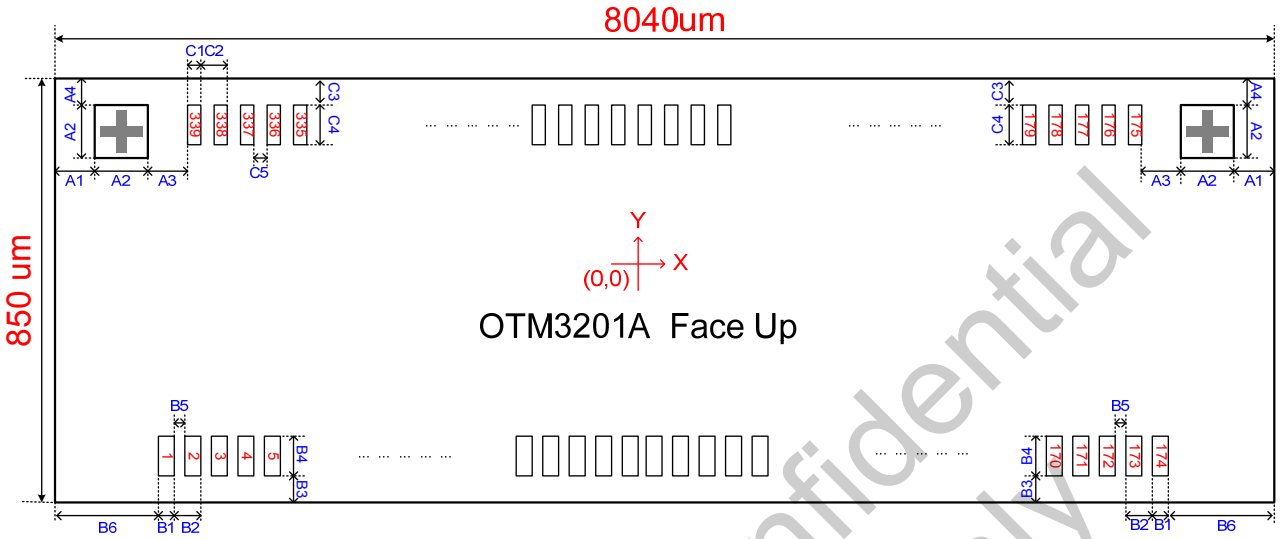
Stop State (SS, LP-11) Timings from Previous mode to Next mode

Previous \ Next	Escape mode		HSDT		BTA	
	Min	Max	Min	Max	Min	Max
Escape mode	100 ns	-	100 ns	-	100 ns	-
HSDT	60ns + 52UI	-	60ns + 52UI	-	60ns + 52UI	-
BTA	100 ns	-	100 ns	-	100 ns	-



10. CHIP INFORMATION

10.1. Pad Assignment



Symbol	Size	Symbol	Size	Symbol	Size
A1	81.5	B1	30	C1	33
A2	100	B2	45	C2	46
A3	50	B3	65	C3	65
A4	65	B4	100	C4	100
-	-	B5	15	C5	13
-	-	B6	112.5	C6	112.5

Note1: Dummy bump design is stated on the individual product approval sheet.

Note2: There is no temperature compensation design

10.2. Pad Dimension

Item	PAD No.	Size		Unit
		X	Y	
Chip Size	-	8040	850	μm
Chip thickness	-	150 ± 10 (OTM3201A-C1、C2)		
Pad pitch	1-174	45	-	
	175-339	46	-	
Pad size	1-174	30	100	
	175-339	33	100	

Note1: Chip size included scribe line.

10.3. Pad Locations

Input Side (Left to Right)

PAD NO.	PAD Name	X	Y
1	Dummy	-3892.5	-295
2	TEST1	-3847.5	-295
3	TEST2	-3802.5	-295
4	IDSEL	-3757.5	-295
5	TEST4	-3712.5	-295
6	TEST5	-3667.5	-295
7	TEST6	-3622.5	-295
8	TEST7	-3577.5	-295
9	DGNDOUT	-3532.5	-295
10	IM0	-3487.5	-295
11	IM1	-3442.5	-295
12	VDDIOUT	-3397.5	-295
13	RESOL0	-3352.5	-295
14	RESOL1	-3307.5	-295
15	RESOL2	-3262.5	-295
16	ALSON	-3217.5	-295
17	LCM	-3172.5	-295
18	EXTC	-3127.5	-295
19	DCMOD	-3082.5	-295
20	VDDIOUT	-3037.5	-295
21	RESET	-2992.5	-295
22	SCLK	-2947.5	-295
23	SDI	-2902.5	-295
24	CS	-2857.5	-295
25	D/CX(CSTROL)	-2812.5	-295
26	SDO	-2767.5	-295
27	DGNDOUT	-2722.5	-295
28	VSync	-2677.5	-295
29	DE	-2632.5	-295
30	HSync	-2587.5	-295
31	PCLK	-2542.5	-295
32	D23	-2497.5	-295
33	D22	-2452.5	-295
34	D21	-2407.5	-295
35	D20	-2362.5	-295
36	D19	-2317.5	-295
37	D18	-2272.5	-295
38	D17	-2227.5	-295
39	D16	-2182.5	-295
40	DGNDOUT	-2137.5	-295
41	D15	-2092.5	-295
42	D14	-2047.5	-295
43	D13	-2002.5	-295
44	D12	-1957.5	-295
45	D11	-1912.5	-295
46	D10	-1867.5	-295
47	D9	-1822.5	-295
48	D8	-1777.5	-295
49	DGNDOUT	-1732.5	-295
50	D7	-1687.5	-295
51	D6	-1642.5	-295
52	D5	-1597.5	-295
53	D4	-1552.5	-295
54	D3	-1507.5	-295
55	D2	-1462.5	-295
56	D1	-1417.5	-295
57	D0	-1372.5	-295
58	DGNDOUT	-1327.5	-295
59	CM	-1282.5	-295
60	SD	-1237.5	-295
61	RL	-1192.5	-295
62	TB	-1147.5	-295
63	VDDIOUT	-1102.5	-295
64	REV	-1057.5	-295
65	FCS	-1012.5	-295
66	VDDIO	-967.5	-295
67	VDDIO	-922.5	-295
68	DGND	-877.5	-295
69	DGND	-832.5	-295
70	DGND	-787.5	-295
71	DGND	-742.5	-295
72	DVDD	-697.5	-295
73	DVDD	-652.5	-295
74	VSSAM	-607.5	-295
75	RX_D0P(DATA+)	-562.5	-295
76	RX_D0P(DATA+)	-517.5	-295
77	RX_D0N(DATA-)	-472.5	-295
78	RX_D0N(DATA-)	-427.5	-295
79	VSSAM	-382.5	-295
80	VSSAM	-337.5	-295
81	RX_CP(Clock+)	-292.5	-295
82	RX_CP(Clock+)	-247.5	-295
83	RX_CN(Clock-)	-202.5	-295
84	RX_CN(Clock-)	-157.5	-295
85	VSSAM	-112.5	-295
86	VSSIM	-67.5	-295
87	VSSIM	-22.5	-295
88	VDDAM	22.5	-295
89	VDDAM	67.5	-295
90	VDDIM	112.5	-295
91	VDDIM	157.5	-295
92	VC12	202.5	-295
93	VC12	247.5	-295
94	VGSP	292.5	-295
95	VGMP	337.5	-295
96	VGMN	382.5	-295
97	VGSN	427.5	-295
98	DVDDN	472.5	-295
99	VSN	517.5	-295
100	VSN	562.5	-295
101	VSN	607.5	-295
102	VSN	652.5	-295
103	VSN	697.5	-295
104	VSN	742.5	-295
105	VSN	787.5	-295
106	VSN	832.5	-295
107	VSN	877.5	-295
108	VSN	922.5	-295
109	VSP(AVDD)	967.5	-295
110	VSP(AVDD)	1012.5	-295
111	VSP(AVDD)	1057.5	-295
112	VSP(AVDD)	1102.5	-295
113	VSP(AVDD)	1147.5	-295
114	VSP(AVDD)	1192.5	-295
115	VSP(AVDD)	1237.5	-295
116	VSP(AVDD)	1282.5	-295
117	VSP(AVDD)	1327.5	-295
118	VSP(AVDD)	1372.5	-295
119	AGND	1417.5	-295
120	AGND	1462.5	-295
121	AGND	1507.5	-295
122	VCI	1552.5	-295
123	VCI	1597.5	-295
124	VCI	1642.5	-295
125	VCI	1687.5	-295
126	VCI	1732.5	-295
127	VCI	1777.5	-295
128	VCI	1822.5	-295
129	VCI	1867.5	-295
130	VCI	1912.5	-295
131	VCI	1957.5	-295
132	VCI	2002.5	-295

PAD NO.	PAD Name	X	Y
133	CVSS(AGND)	2047.5	-295
134	CVSS(AGND)	2092.5	-295
135	CVSS(AGND)	2137.5	-295
136	CVSS(AGND)	2182.5	-295
137	CVSS(AGND)	2227.5	-295
138	CVSS(AGND)	2272.5	-295
139	CVSS(AGND)	2317.5	-295
140	CVSS(AGND)	2362.5	-295
141	C21N	2407.5	-295
142	C21N	2452.5	-295
143	C21N	2497.5	-295
144	C21P	2542.5	-295
145	C21P	2587.5	-295
146	C21P	2632.5	-295
147	C12P	2677.5	-295

PAD NO.	PAD Name	X	Y
148	C12P	2722.5	-295
149	C12P	2767.5	-295
150	C12P	2812.5	-295
151	C12N	2857.5	-295
152	C12N	2902.5	-295
153	C12N	2947.5	-295
154	C12N	2992.5	-295
155	C11P	3037.5	-295
156	C11P	3082.5	-295
157	C11P	3127.5	-295
158	C11P	3172.5	-295
159	C11N	3217.5	-295
160	C11N	3262.5	-295
161	C11N	3307.5	-295
162	C11N	3352.5	-295

PAD NO.	PAD Name	X	Y
163	VCSW1	3397.5	-295
164	VCSW1	3442.5	-295
165	VCSW2	3487.5	-295
166	VCSW2	3532.5	-295
167	VPDC1	3577.5	-295
168	VPDC1	3622.5	-295
169	VREF	3667.5	-295
170	VPDC2	3712.5	-295
171	VDD_OTP	3757.5	-295
172	VDD_OTP	3802.5	-295
173	VDD_OTP	3847.5	-295
174	Dummy	3892.5	-295

Output Side (Right to Left)

PAD NO.	PAD Name	X	Y
175	DUMMY(TESTA1)	3772	295
176	DUMMY(TESTA2)	3726	295
177	ALS_EOUT1	3680	295
178	ALS_MOUT1	3634	295
179	ALS_SET	3588	295
180	ALS_EOUT3	3542	295
181	ALS_MOUT3	3496	295
182	DUMMY	3450	295
183	CPCLKP	3404	295
184	CPCLKN	3358	295
185	GAS	3312	295
186	ENBV	3266	295
187	CSV	3220	295
188	CKV	3174	295
189	STV1	3128	295
190	STV2	3082	295
191	PRST	3036	295
192	DUMMY	2990	295
193	S1	2944	295
194	S2	2898	295
195	S3	2852	295
196	S4	2806	295
197	S5	2760	295
198	S6	2714	295
199	S7	2668	295
200	S8	2622	295
201	S9	2576	295

PAD NO.	PAD Name	X	Y
202	S10	2530	295
203	S11	2484	295
204	S12	2438	295
205	S13	2392	295
206	S14	2346	295
207	S15	2300	295
208	S16	2254	295
209	S17	2208	295
210	S18	2162	295
211	S19	2116	295
212	S20	2070	295
213	S21	2024	295
214	S22	1978	295
215	S23	1932	295
216	S24	1886	295
217	S25	1840	295
218	S26	1794	295
219	S27	1748	295
220	S28	1702	295
221	S29	1656	295
222	S30	1610	295
223	S31	1564	295
224	S32	1518	295
225	S33	1472	295
226	S34	1426	295
227	S35	1380	295
228	S36	1334	295

PAD NO.	PAD Name	X	Y
229	S37	1288	295
230	S38	1242	295
231	S39	1196	295
232	S40	1150	295
233	S41	1104	295
234	S42	1058	295
235	S43	1012	295
236	S44	966	295
237	S45	920	295
238	S46	874	295
239	S47	828	295
240	S48	782	295
241	S49	736	295
242	S50	690	295
243	S51	644	295
244	S52	598	295
245	S53	552	295
246	S54	506	295
247	S55	460	295
248	S56	414	295
249	S57	368	295
250	S58	322	295
251	S59	276	295
252	S60	230	295
253	DUMMY	184	295
254	S61	138	295
255	S62	92	295

PAD NO.	PAD Name	X	Y
256	S63	46	295
257	S64	0	295
258	S65	-46	295
259	S66	-92	295
260	S67	-138	295
261	S68	-184	295
262	S69	-230	295
263	S70	-276	295
264	S71	-322	295
265	S72	-368	295
266	S73	-414	295
267	S74	-460	295
268	S75	-506	295
269	S76	-552	295
270	S77	-598	295
271	S78	-644	295
272	S79	-690	295
273	S80	-736	295
274	S81	-782	295
275	S82	-828	295
276	S83	-874	295
277	S84	-920	295
278	S85	-966	295
279	S86	-1012	295
280	S87	-1058	295
281	S88	-1104	295
282	S89	-1150	295
283	S90	-1196	295
284	S91	-1242	295

PAD NO.	PAD Name	X	Y
285	S92	-1288	295
286	S93	-1334	295
287	S94	-1380	295
288	S95	-1426	295
289	S96	-1472	295
290	S97	-1518	295
291	S98	-1564	295
292	S99	-1610	295
293	S100	-1656	295
294	S101	-1702	295
295	S102	-1748	295
296	S103	-1794	295
297	S104	-1840	295
298	S105	-1886	295
299	S106	-1932	295
300	S107	-1978	295
301	S108	-2024	295
302	S109	-2070	295
303	S110	-2116	295
304	S111	-2162	295
305	S112	-2208	295
306	S113	-2254	295
307	S114	-2300	295
308	S115	-2346	295
309	S116	-2392	295
310	S117	-2438	295
311	S118	-2484	295
312	S119	-2530	295
313	S120	-2576	295

PAD NO.	PAD Name	X	Y
314	DUMMY	-2622	295
315	CKH1	-2668	295
316	CKH2	-2714	295
317	CKH3	-2760	295
318	CKH4	-2806	295
319	CKH5	-2852	295
320	CKH6	-2898	295
321	CKH7	-2944	295
322	CKH8	-2990	295
323	CKH9	-3036	295
324	PRST	-3082	295
325	STV2	-3128	295
326	STV1	-3174	295
327	CKV	-3220	295
328	CSV	-3266	295
329	ENBV	-3312	295
330	GAS	-3358	295
331	CPCLKN	-3404	295
332	CPCLKP	-3450	295
333	DUMMY	-3496	295
334	ALS_EOUT2	-3542	295
335	ALS_MOUT2	-3588	295
336	DUMMY	-3634	295
337	ALS_SET	-3680	295
338	DUMMY	-3726	295
339	DUMMY	-3772	295

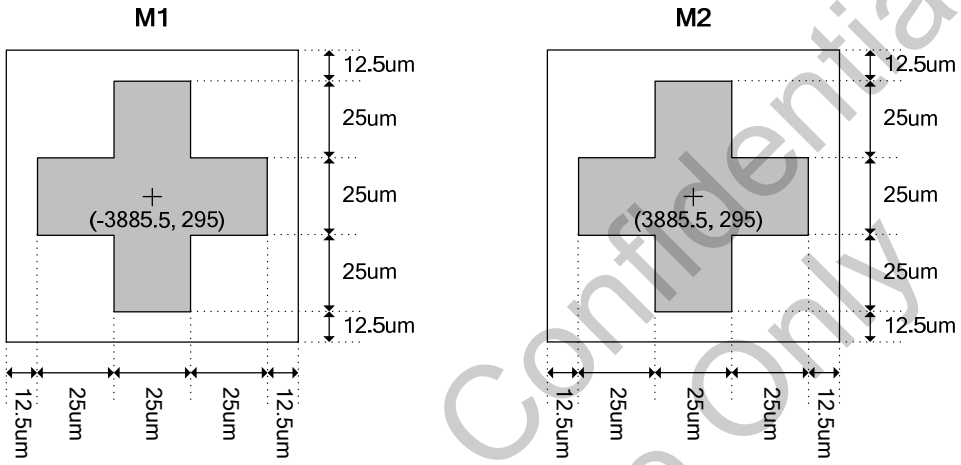
10.4. Alignment Mark

--Alignment Mark coordinate

M1 (-3885.5, 295)

M2 (3885.5, 295)

--Alignment Mark size



11. DISCLAIMER

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12. REVISION HISTORY

Date	Revision #	Description	Page	Auditor
AUG. 12, 2014	0.3	Add command for MIPI RX delay setting	138	Showmin.Hsiao
APR. 30, 2014	0.2	1. Modify MIPI feature description	3	Showmin.Hsiao
		2. Modify power supply circuit	13	
		3. Add power block diagram and BOM list	14 -15	
		4. Modify IM[1:0], VDD_OTP and D[23:0] description	16 - 18	
		5. Add MIPI-DSI interface description	35 - 59	
		6. Add series interface description	60 - 61	
		7. Add NVM programming flow	62	
		8. Modify Color MUX description	74 - 75	
		9. Add command 1 for MIPI I/F	84 - 103	
		10. Modify and add command 2	107 -138	
		11. Modify power-on/off sequence	139 - 141	
		12. Add MIPI-DSI characteristics	151 - 155	
		13. Modify PAD assignment and dimension	156	
MAY. 28, 2008	0.1	Original	110	LC.Chen