REV. A: 08/10/2010

- Original Release

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Drawing Title:

i.MX28 REFERENCE SCHEMATICS

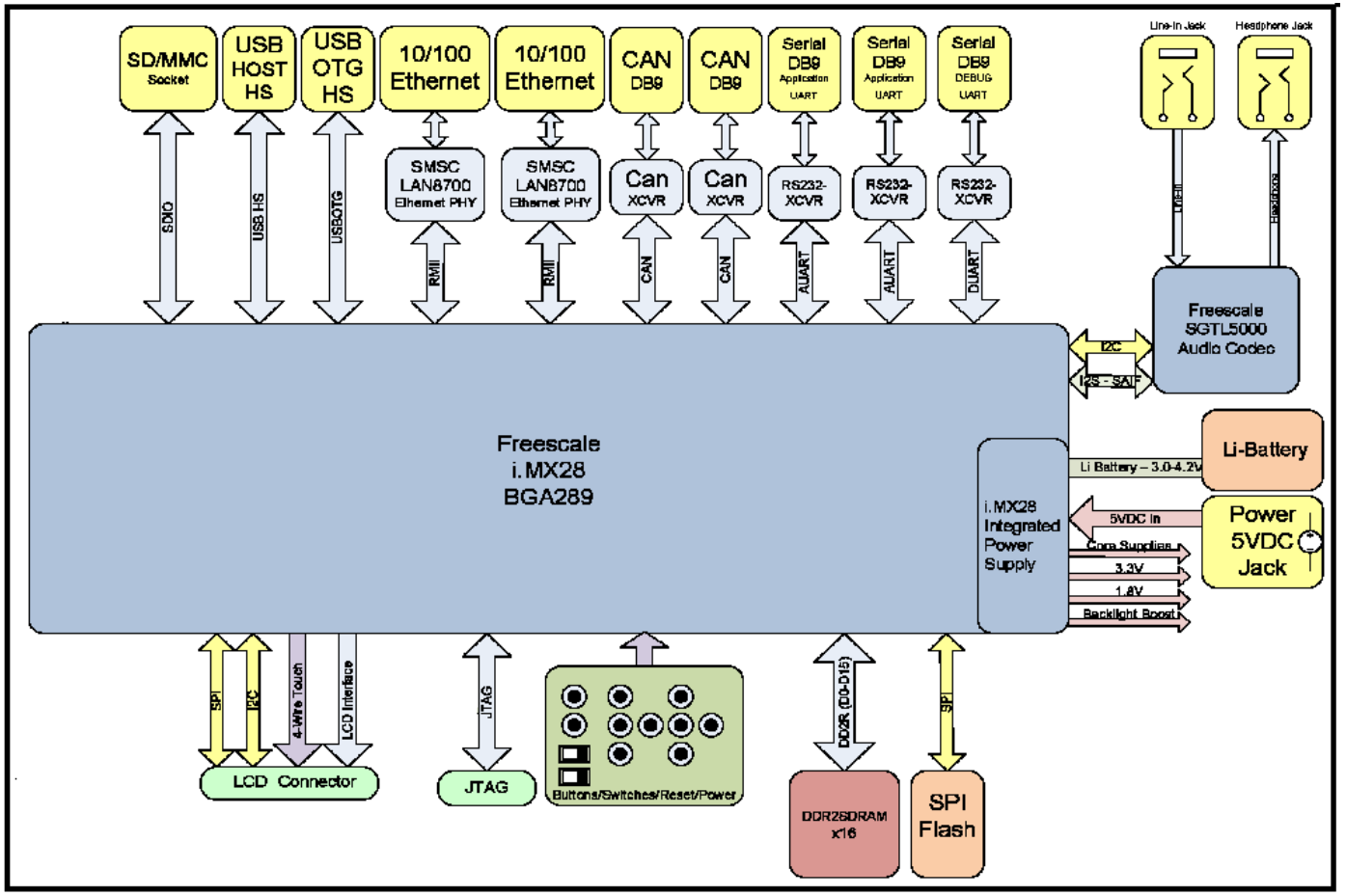
Page Title:

REVISION HISTORY

Size	Document Number	Rev
A	N/A	A

Date: Tuesday, August 10, 2010

i.MX28 Reference Schematics Rev. A



NOTE: These schematics are subject to change.

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Drawing Title: i.MX28 REFERENCE SCHEMATICS

Page Title: BLOCK DIAGRAM

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i.MX28 EXAMPLE COMPONENTS

DCDC Inductor

For best battery life, the DCDC inductor should have a low DC resistance. The current rating of the inductor should be higher than the measured peak current through the inductor, which will be application-specific. The inductor value is recommended to be between 4.7uH and 15uH.

Note that inductors with a higher DC resistance may be used, but may impact battery life.

Reference Designator	Description	Manufacturer	Manufacturer Part Number
L1	15uH, 900mA, 213mOhm RDC	Sumida	CDRH3D28NP-150N
L1	10uH, 690mA, 18mOhm RDC	Panasonic	ELL4LM100M
L1	15uH, 500mA, 520mOhm RDC	Nantong Meda (MEDAFA)	MAH 32-150

DCDC Output Capacitors

The C36, C37, C52, C53, C60, C61, C67, and C68 output capacitors should have an ESR less than 400mOhms. Ceramic capacitors are recommended (Y5V capacitors should not be used).

24MHz Crystal

Reference Designator	Description	Manufacturer	Manufacturer Part Number
Y1	24MHz 30ppm Crystal	Jing Feng	24.000MHz Jing Feng Crystal 2x6mm cylinder, +/- 30ppm, CL = 10pF

32kHz Crystal

Reference Designator	Description	Manufacturer	Manufacturer Part Number
Y2	32kHz 20ppm Crystal	Seiko	VT200FA-6PF20PPM
Y2	32kHz 20ppm Crystal	Seiko	SSPT7FA-7PF20PPM

USB Ferrites and ESD Protection

Reference Designator	Description	Recommended Manufacturer	Manufacturer Part Number
L4, L6	Ferrite, DCR < 100mOhm, 68 ohms @ 100MHz, 1A	Steward	MI0603J680R-10
L5	Ferrite, DCR < 400mOhm, 1500 ohms @ 100MHz, 400mA	Steward	HZ0805D152R-10
D4, D5	ESD Protection Diode	ON Semi.	NZL6V8AXV3T1

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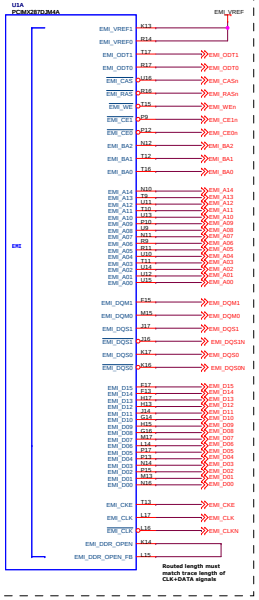
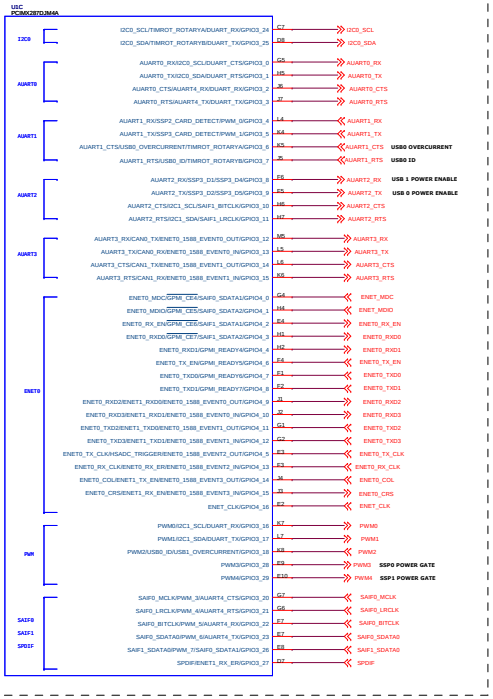
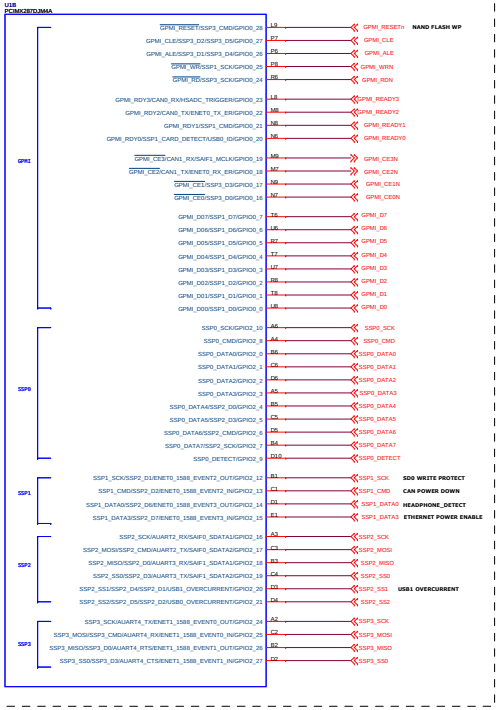
i.MX28 EMI - DDR2 and mDDR



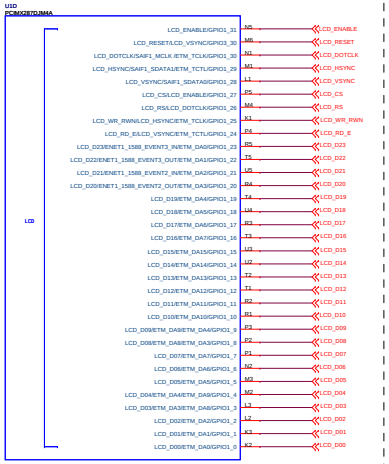
i.MX28 ENET, UART, PWM, & SAIF0



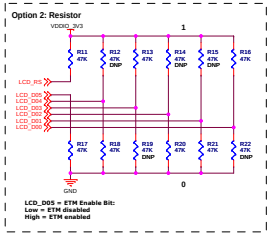
i.MX28 GPMI & SSP



i.MX28 LCD & SAIF1



i.MX28 Bootmode Resistor Selection



LCD_DATA[3]	VOLTAGE SELECT: OR: LCD_DATA[4]	BM3: LCD_DATA[3]	BM2: LCD_DATA[2]	BM1: LCD_DATA[1]	BM0: LCD_DATA[0]	PORT	BOOT MODE
x	x	0	0	0	0	USB0	USB (unencrypted vs. encrypted is under OTP control)
x	0	0	0	0	1	I2C0	I2C0 master, 3.3 V
x	1	0	0	0	1	I2C0	I2C0 master, 1.8 V
x	0	0	0	1	0	SPI2	SPI master SSP2 boot from flash, 3.3 V
x	1	0	0	1	0	SPI2	SPI master SSP2 boot from flash, 1.8 V
x	0	0	0	1	1	SPI3	SPI master SSP3 boot from flash, 3.3 V
x	1	0	0	1	1	SPI3	SPI master SSP3 boot from flash, 1.8 V
x	0	0	1	0	0	GPMI	NAND, 3.3 V
x	1	0	1	0	0	GPMI	NAND, 1.8 V
x	0	0	1	0	1		Reserved
x	0	0	1	1	0	JTAG	Alair JTAG connection mode
x	0	0	1	1	1		Reserved
x	0	1	0	0	0	SPI3	SPI master SSP3 boot from EEPROM, 3.3 V
x	1	1	0	0	0	SPI3	SPI master SSP3 boot from EEPROM, 1.8 V
x	0	1	0	0	1	SSP3	SD/MMC master on SSP3, 3.3 V
x	1	1	0	0	1	SSP3	SD/MMC master on SSP3 1.8 V
x	0	1	0	1	0	SSP1	SD/MMC master on SSP1, 3.3 V
x	1	1	0	1	0	SSP1	SD/MMC master on SSP1, 1.8 V

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Drawing Title: **i.MX28 REFERENCE SCHEMATICS**

Page Title: **i.MX28 DIGITAL**

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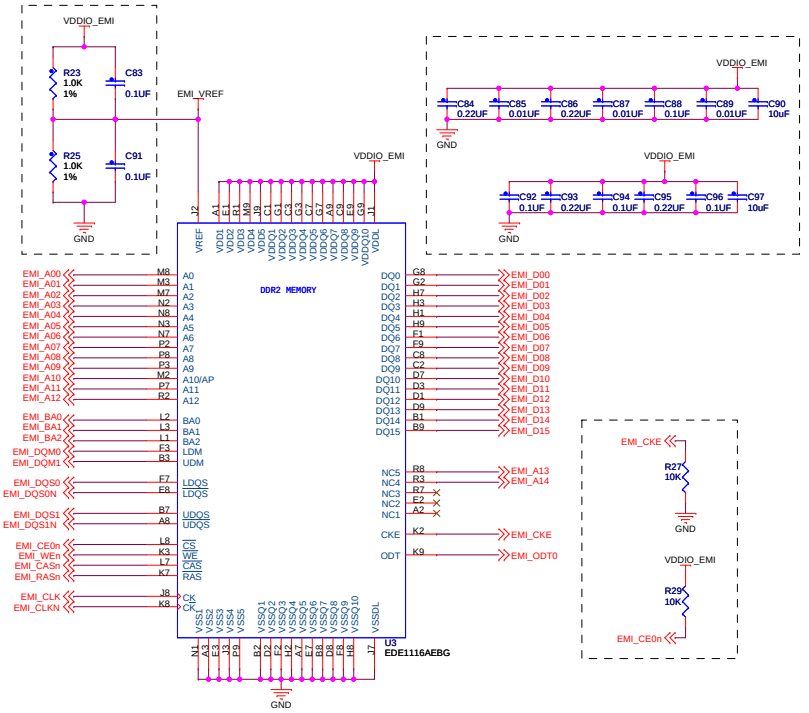
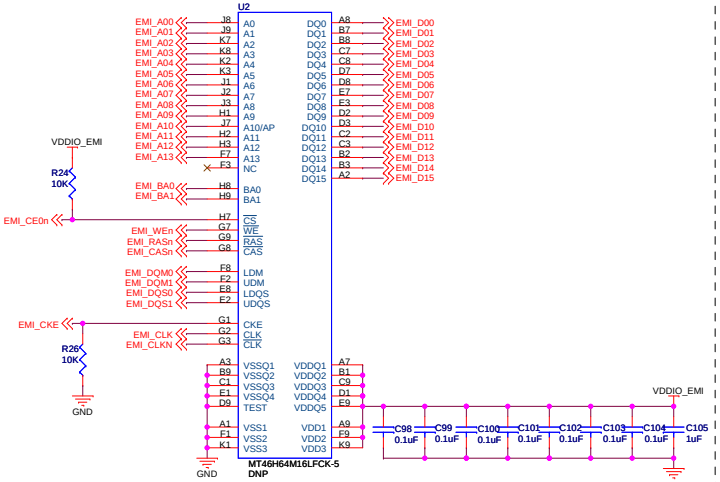
DDR2 (1.5V and 1.8V)

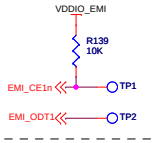


1.8V Mobile DDR



Unused Nets

These nets are currently not used in the reference schematics. However, they are required for systems with 2 DRAM components. The additional DDR2 component requires ODT1 and CE1n. The additional mDDR components requires CE1n.



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Drawing Title: i.MX28 REFERENCE SCHEMATICS

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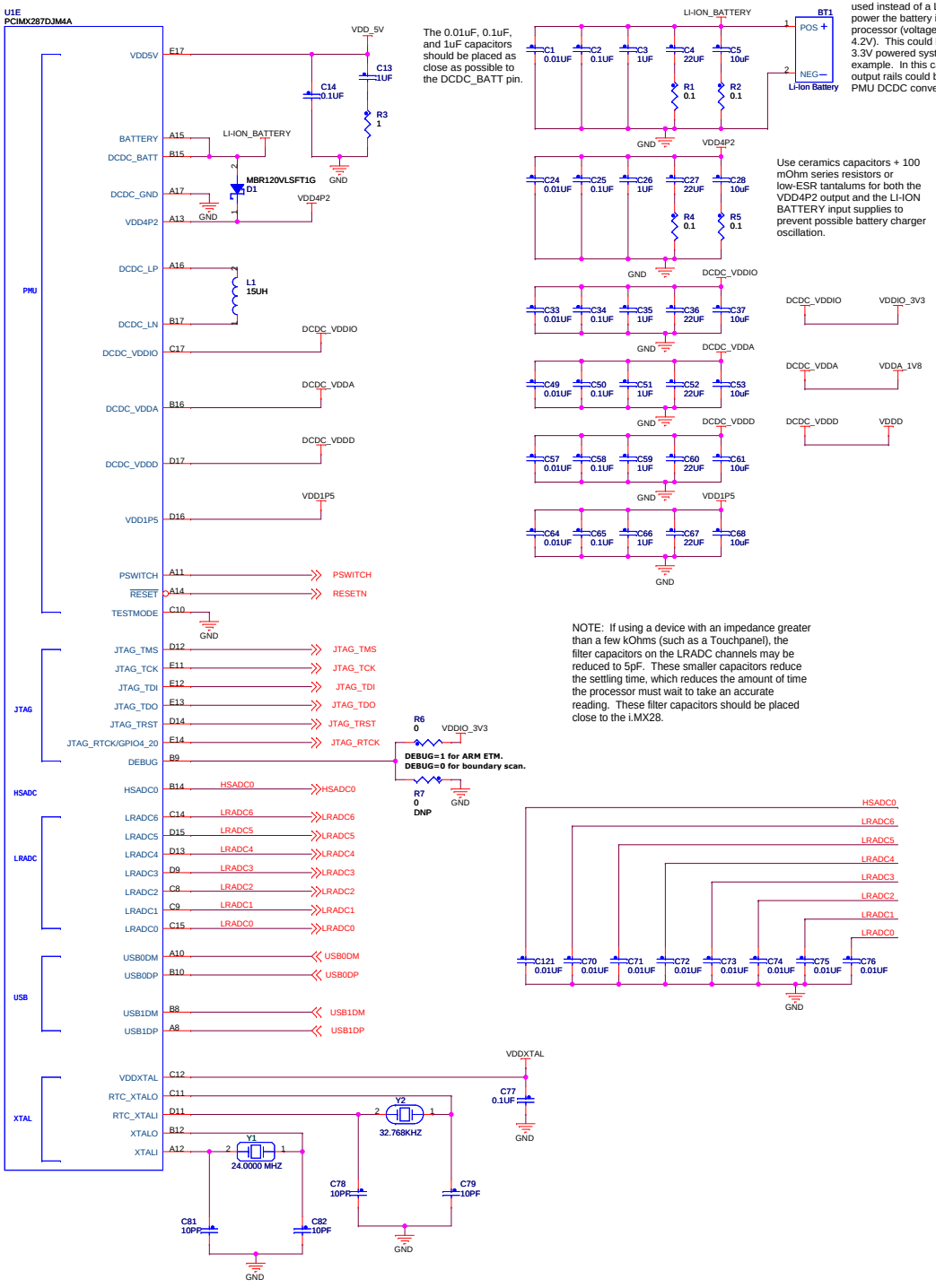
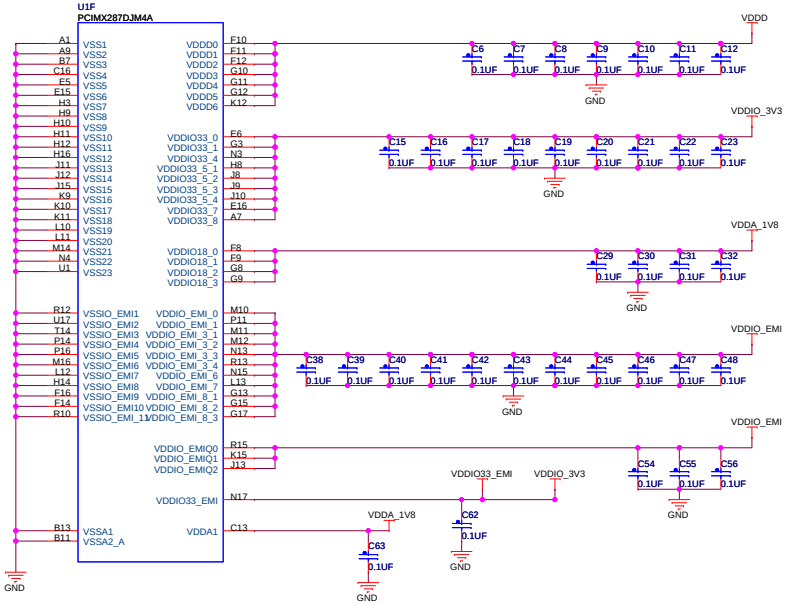
i.MX28 DC-DC / Power Management and Analog



i.MX28 CPU Power Inputs



EMI / DRAM Power Connections

1.5V DDR2 (low voltage)

VDD1P5 — VDDIO_EMI

1.8V DDR2 and mDDR

VDDA_1V8 — VDDIO_EMI

High Speed ADC Test Points

HSADC0 — TP12

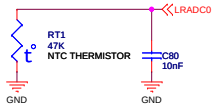
High Speed ADC Trigger

HSADC_TRIGGER ENET0_TX_CLK — TP13

OR

HSADC_TRIGGER GPMI_READY3 — TP14

OPTIONAL TEMPERATURE SENSE



IMPORTANT LAYOUT DESIGN NOTES

1) The crystals should be placed as close as possible to the i.MX28.

2) For best USB jitter performance, the VDDXTAL capacitor and the crystal load capacitors should NOT connect to the ground plane near the DRAM bus routing and grounds. These ground connections should preferably be close to the VSSA1 ground pin.

3) All DCDC input & output capacitors should be located close to the i.MX28.

IMPORTANT CRYSTAL DESIGN NOTES

The 24 MHz crystal should be located close to the i.MX28. Consult crystal manufacturer datasheet for recommended load capacitor values (typically 10-18pF).

Cload = [(C26*C27) / (C26+C27)] + Cstray

where Cstray = stray PCB capacitance, typically 4 - 6 pF

Note: For Microsoft DRM applications use a 30 ppm crystal.

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Drawing Title: **i.MX28 REFERENCE SCHEMATICS**

Page Title: **i.MX28 POWER AND ANALOG**

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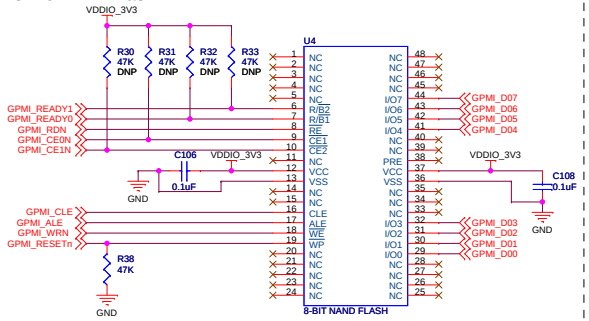
NAND FLASH

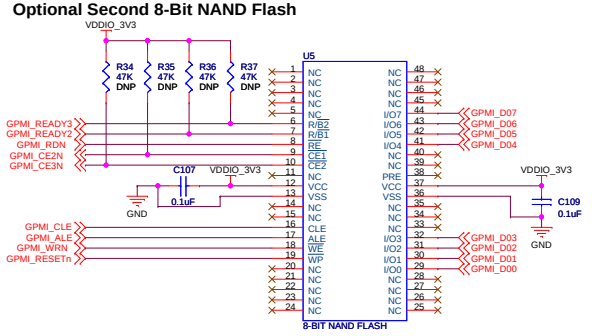
Important Design Notes

1) The WP# pull-down resistor is required to protect the flash memory from inadvertent writes during power transitions.
2) All CE# and R/B# pins require pull up resistors. Note that the i.MX28 has integrated CE# and R/B# pull-up resistors that must be enabled by OTP.
3) The circuits below show dual-CE NAND flash. If using a single-CE NAND flash, change pins 6 and 10 to NO CONNECT.

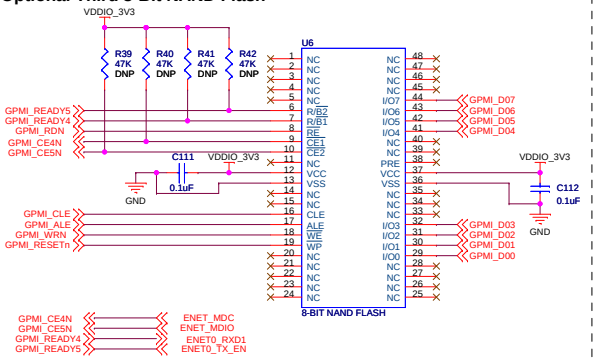
8-Bit NAND Flash



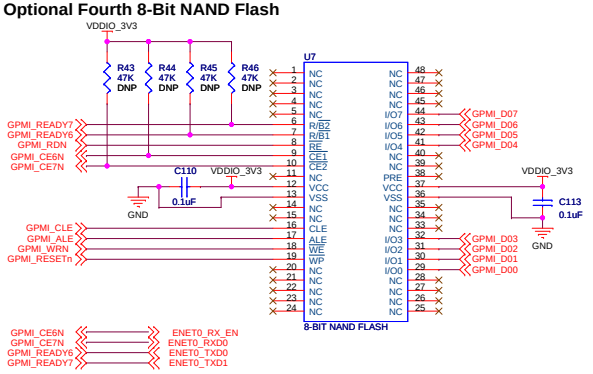
Optional Second 8-Bit NAND Flash



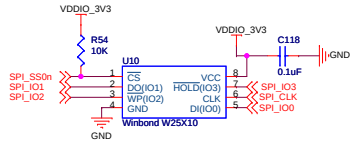
Optional Third 8-Bit NAND Flash



Optional Fourth 8-Bit NAND Flash



SPI FLASH



Reference Designator	Description	Manufacturer	Manufacturer Part Number
U10	SPI Flash, 3.0V	Winbond	W25X10

SPI Flash Pin Assignment Options

Option 1: SSP2 (BSP Default Configuration)

On Page Net Name	i.MX28 Pin Assignment	Alternate SSP2 pins:	
SPI_SS0n	SSP2_SS0	SSP0_DATA5	SSP2_SS0
SPI_CLK	SSP2_SCK	SSP0_DATA7	SSP2_SCK
SPI_IO0	SSP2_MOSI	SSP0_DATA6	SSP2_CMD
SPI_IO1	SSP2_MISO	SSP0_DATA4	SSP2_DATA0
SPI_IO2	SSP2_SS1	SSP1_SCK	SSP2_DATA1
SPI_IO3	SSP2_SS2	SSP1_CMD	SSP2_DATA2

Option 2: SSP3

On Page Net Name	i.MX28 Pin Assignment	Alternate SSP3 pins:	
SPI_SS0n	SSP3_SS0	GPMI_CE1N	SSP3_SS0
SPI_CLK	SSP3_SCK	GPMI_RDN	SSP3_SCK
SPI_IO0	SSP3_MOSI	GPMI_RESETn	SSP3_CMD
SPI_IO1	SSP3_MISO	GPMI_CE0N	SSP3_DATA0
SPI_IO2	AUART2_RX	GPMI_ALE	SSP3_DATA1
SPI_IO3	AUART2_TX	GPMI_CLE	SSP3_DATA2

Option 3: SSP1

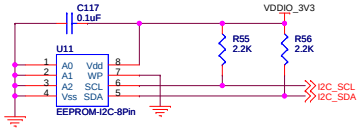
On Page Net Name	i.MX28 Pin Assignment	
SPI_SS0n	GPMI_D3	SSP1_SS0
SPI_CLK	GPMI_WRN	SSP1_SCK
SPI_IO0	GPMI_READY1	SSP1_CMD
SPI_IO1	GPMI_D0	SSP1_DATA0
SPI_IO2	GPMI_D1	SSP1_DATA1
SPI_IO3	GPMI_D2	SSP1_DATA2

Option 4: SSP0

On Page Net Name	i.MX28 Pin Assignment	
SPI_SS0n	SSP0_DATA3	SSP1_SS0
SPI_CLK	SSP0_SCK	SSP1_SCK
SPI_IO0	SSP0_CMD	SSP1_CMD
SPI_IO1	SSP0_DATA0	SSP1_DATA0
SPI_IO2	SSP0_DATA1	SSP1_DATA1
SPI_IO3	SSP0_DATA2	SSP1_DATA2

I2C EEPROM

Use 24LCxx-I/P or Equivalent



Option 1: I2C0 (BSP Default Configuration)

On Page Net Name	i.MX28 Pin Assignment	
I2C_SCL	I2C0_SCL	
I2C_SDA	I2C0_SDA	

I2C0 Alternate Connections

I2C_SCL	AUART0_RX	I2C0_SCL
I2C_SDA	AUART0_TX	I2C0_SDA

Option 2: I2C1

On Page Net Name	i.MX28 Pin Assignment	
I2C_SCL	AUART2_CTS	I2C1_SCL
I2C_SDA	AUART2_RTS	I2C1_SDA

I2C1 Alternate Connections

I2C_SCL	PWM0	I2C1_SCL
I2C_SDA	PWM1	I2C1_SDA

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Drawing Title: **i.MX28 REFERENCE SCHEMATICS**

Page Title: **NON-VOLATILE MEMORY**

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SD/MMC/MMCPlus

SD/MMC/MMCPlus Pin Assignment Options

Option 1: SSP0 (BSP Default Configuration)

On Page Net Name	i.MX28 Pin Assignment
SSP_CMD	SSP0_CMD
SSP_SCK	SSP0_SCK
SSP_DATA0	SSP0_DATA0
SSP_DATA1	SSP0_DATA1
SSP_DATA2	SSP0_DATA2
SSP_DATA3	SSP0_DATA3
SSP_DATA4	SSP0_DATA4
SSP_DATA5	SSP0_DATA5
SSP_DATA6	SSP0_DATA6
SSP_DATA7	SSP0_DATA7
SSP_DETECT	SSP0_DETECT
WRITE_PROTECT#	SSP1_SCK

WRITE_PROTECT# refers to the user-selectable slide switch on SD/MMC cards. This support is optional and can be assigned to any free GPIO pin (BSP default GPIO used is shown above).

Option 2: SSP1 (Alternate Configuration)

On Page Net Name	i.MX28 Pin Assignment	
SSP_CMD	GPMI_READY1	SSP1_CMD
SSP_SCK	GPMI_WRN	SSP1_SCK
SSP_DATA0	GPMI_D0	SSP1_DATA0
SSP_DATA1	GPMI_D1	SSP1_DATA1
SSP_DATA2	GPMI_D2	SSP1_DATA2
SSP_DATA3	GPMI_D3	SSP1_DATA3
SSP_DATA4	GPMI_D4	SSP1_DATA4
SSP_DATA5	GPMI_D5	SSP1_DATA5
SSP_DATA6	GPMI_D6	SSP1_DATA6
SSP_DATA7	GPMI_D7	SSP1_DATA7
SSP_DETECT	GPMI_READY0	SSP1_CARD_DETECT
WRITE_PROTECT#	GPMI_RESETn	

Alternate SSP1 pins for CMD, CLK, DATA0 and DATA3:

SSP_CMD	SSP1_CMD
SSP_SCK	SSP1_SCK
SSP_DATA0	SSP1_DATA0
SSP_DATA3	SSP1_DATA3

WRITE_PROTECT# refers to the user-selectable slide switch on SD/MMC cards. This support is optional and can be assigned to any free GPIO pin (BSP default GPIO used is shown above).

Option 3: SSP2 (Alternate Configuration)

On Page Net Name	i.MX28 Pin Assignment	
SSP_CMD	SSP2_MOSI	SSP2_CMD
SSP_SCK	SSP2_SCK	SSP2_SCK
SSP_DATA0	SSP2_MISO	SSP2_DATA0
SSP_DATA1	SSP1_SCK	SSP2_DATA1
SSP_DATA2	SSP1_CMD	SSP2_DATA2
SSP_DATA3	SSP2_SS0	SSP2_DATA3
SSP_DATA4	SSP2_SS1	SSP2_DATA4
SSP_DATA5	SSP2_SS2	SSP2_DATA5
SSP_DATA6	SSP1_DATA0	SSP2_DATA6
SSP_DATA7	SSP1_DATA3	SSP2_DATA7
SSP_DETECT	AUART1_RX	SSP2_CARD_DETECT
WRITE_PROTECT#	GPMI_RESETn	

Alternate SSP2 pins for CMD, CLK, DATA0-3:

SSP_CMD	SSP0_DATA6
SSP_SCK	SSP0_DATA7
SSP_DATA0	SSP0_DATA4
SSP_DATA1	SSP2_SS1
SSP_DATA2	SSP2_SS2
SSP_DATA3	SSP0_DATA5

WRITE_PROTECT# refers to the user-selectable slide switch on SD/MMC cards. This support is optional and can be assigned to any free GPIO pin.

Option 4: SSP3 (Alternate Configuration) 4 bit SDIO maximum

On Page Net Name	i.MX28 Pin Assignment	
SSP_CMD	SSP3_MOSI	SSP3_CMD
SSP_SCK	SSP3_SCK	SSP3_SCK
SSP_DATA0	SSP3_MISO	SSP3_DATA0
SSP_DATA1	AUART2_RX	SSP3_DATA1
SSP_DATA2	AUART2_TX	SSP3_DATA2
SSP_DATA3	SSP3_SS0	SSP3_DATA3
WRITE_PROTECT#	SSP1_SCK	

Alternate SSP3 pins for CMD, CLK, DATA0-3:

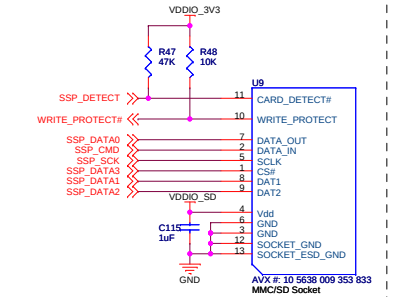
SSP_CMD	GPMI_RESETn
SSP_SCK	GPMI_RDN
SSP_DATA0	GPMI_CE0N
SSP_DATA1	GPMI_ALE
SSP_DATA2	GPMI_CLE
SSP_DATA3	GPMI_CE1N

WRITE_PROTECT# refers to the user-selectable slide switch on SD/MMC cards. This support is optional and can be assigned to any free GPIO pin.

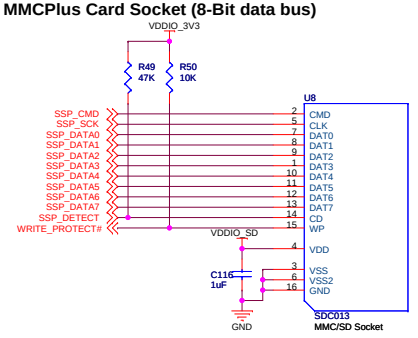
Important Design Notes

1) The SD/MMC socket should have an integrated, normally-open, mechanical CARD DETECT switch.
2) The i.MX28 has integrated pull up resistors for the SD/MMC DATA and CMD signals that must be enabled by setting a register.

SD / MMC Card Socket (4-Bit data bus)

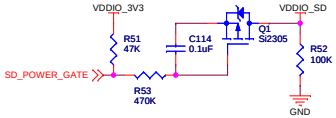


MMCPlus Card Socket (8-Bit data bus)

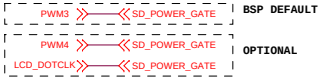


Required Power Switch for Removable SD/MMC Media

This circuitry gates power to the SD/MMC/MMCPlus socket. This ensures reliable operation with some SD/MMC/MMCPlus cards that require large amounts of current at insertion.
At start-up, SD_POWER_GATE is high and VDDIO_SD is unpowered. When CARD_DETECT goes low due to card insertion, firmware will drive SD_POWER_GATE low to connect VDDIO_3V3 to VDDIO_SD. After waiting 30 msec to allow the VDDIO_SD supply to stabilize, the firmware will enable the internal SSP_DATA and SSP_CMD pull-up resistors and begin communicating with the SD/MMC card. When the card is removed and CARD_DETECT goes high, SD_POWER_GATE will be driven high again.



If the application does not need to boot from the SSP port, the SD_POWER_GATE function can be assigned to any free GPIO pin (not just PWM3). However, if the SD/MMC/MMCPlus device is the boot device, SD_POWER_GATE must be driven by the ROM, which supports 3 OTP-selectable options: PWM3, PWM4, or LCD_DOTCLK.



Drawing Title: i.MX28 REFERENCE SCHEMATICS

Page Title: SDIO (SD & MMC)

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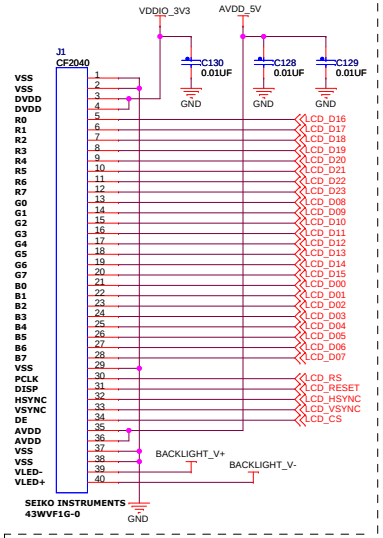
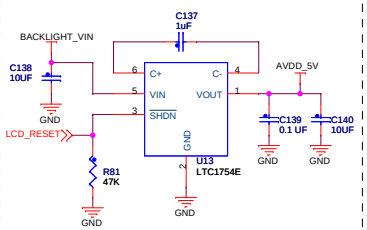
LCD & LED DISPLAY OPTIONS

BSP Default:
24-bit RGB WVGA LCD



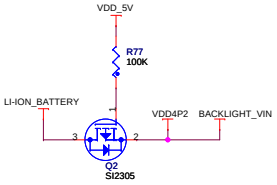
5V Charge Pump

This circuit supplies power to the 5V analog pins of the Seiko display.



Recommended Backlight Power Circuit

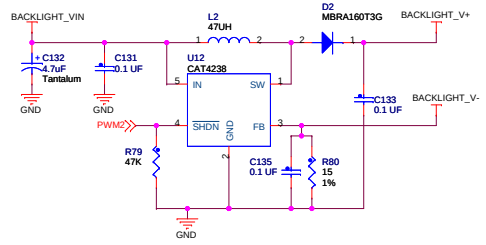
This circuit can be used, but the total system load on the MX28 VDD4P2 output must not exceed the maximum allowable. Please consult the MX28 datasheet and/or reference manual for maximum current outputs and programmable current limit settings.



Option 1:
External Backlight Boost Circuit for up to 10 series LEDs

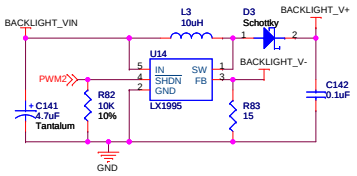
This circuit should be used if up to 10 series LED are used for the LCD backlight or a high voltage (30V or higher) is required.

This circuit is required for the Seiko WVGA display.

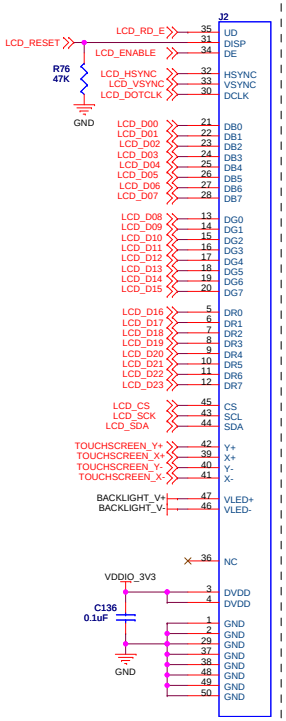


Option 2:
External Backlight Boost Circuit for 3 - 6 series LEDs

Backlight should have 3 - 6 LEDs in series. If the backlight has fewer than 3 LEDs, the backlight may draw power even if the player is powered off.



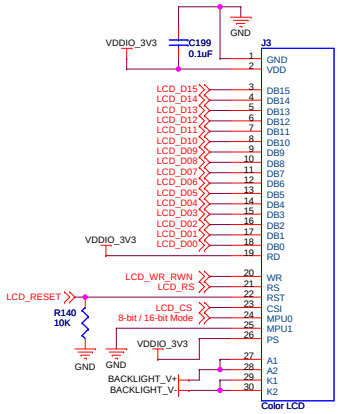
Optional:
24-bit DOTCLK Mode LCD



LCD SPI Interface Pin Assignments

On Page Net Name	i.MX28 Pin Assignment
LCD_SDA	LCD_WR_RWN
LCD_SCK	LCD_RS
LCD_CS	LCD_CS

Optional:
8-bit or 16-bit 8080 System Mode LCD



Connect the 8-bit / 16-bit Mode net either high or low to select 8 bit or 16 bit LCD bus.

Drawing Title: i.MX28 REFERENCE SCHEMATICS

Page Title: LCD AND BACKLIGHT

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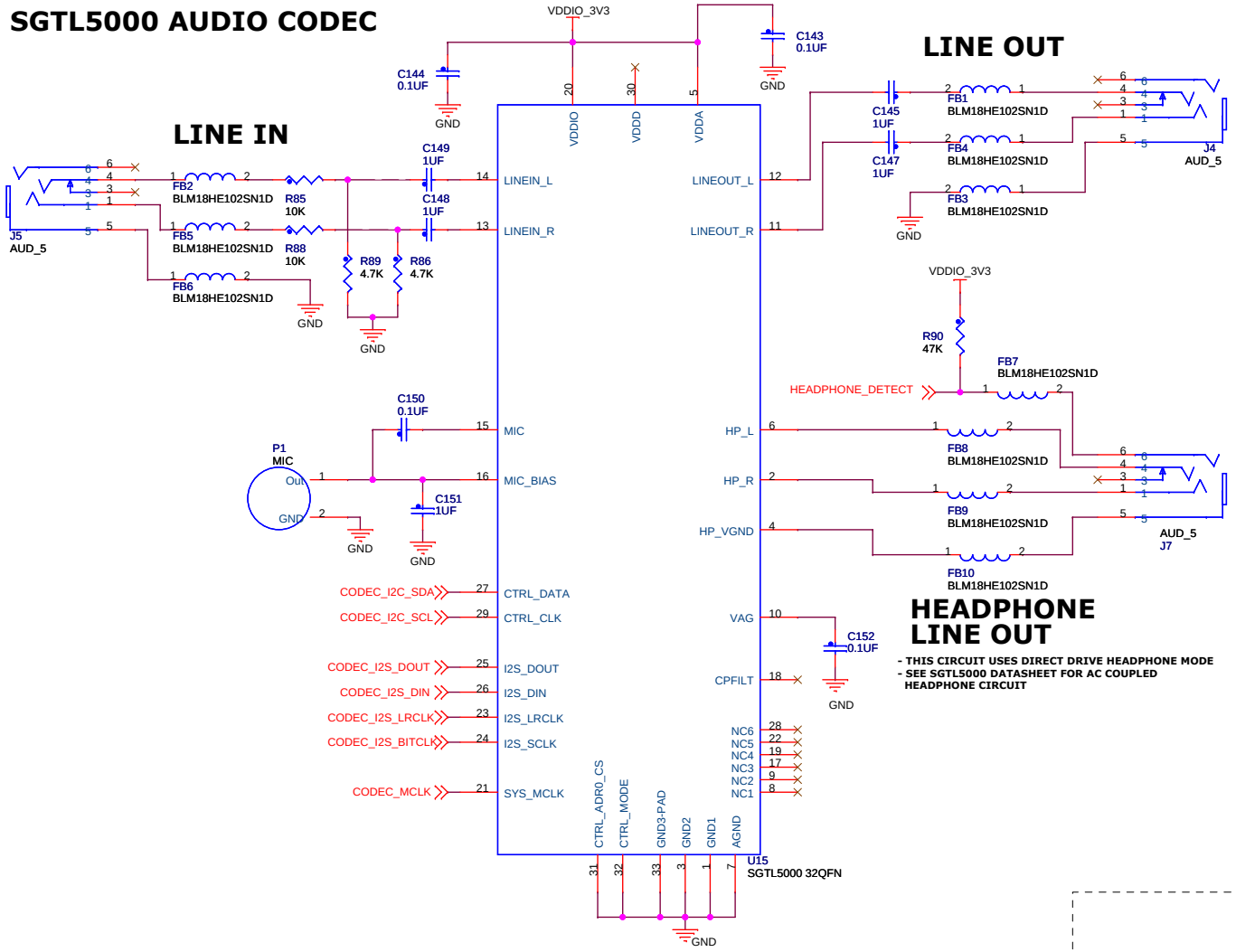
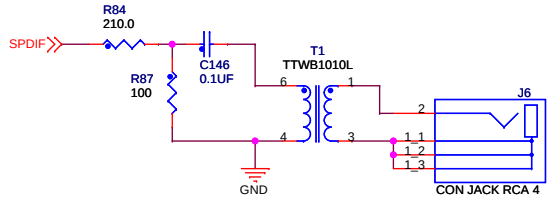
SGTL5000 AUDIO CODEC



- THIS CIRCUIT USES DIRECT DRIVE HEADPHONE MODE
- SEE SGTL5000 DATASHEET FOR AC COUPLED HEADPHONE CIRCUIT

S/PDIF OUTPUT



DEFAULT BSP CONNECTIONS

On Page Net Name	i.MX28 Pin Assignment	
HEADPHONE_DETECT	SSP1_DATA0	
CODEC_I2C_SCL	I2C0_SCL	
CODEC_I2C_SDA	I2C0_SDA	
CODEC_I2S_DOUT	SAIF1_SDATA0	SAIF0_SDATA1
CODEC_I2S_DIN	SAIF0_SDATA0	SAIF0
CODEC_I2S_LRCLK	SAIF0_LRCLK	
CODEC_I2S_BITCLK	SAIF0_BITCLK	
CODEC_MCLK	SAIF0_MCLK	

OPTIONAL I2C CONNECTIONS

On Page Net Name	i.MX28 Pin Assignment	
CODEC_I2C_SCL	AUART0_RX	I2C0_SCL
CODEC_I2C_SDA	AUART0_TX	I2C0_SDA
CODEC_I2C_SCL	AUART2_CTS	I2C1_SCL
CODEC_I2C_SDA	AUART2_RTS	I2C1_SDA
CODEC_I2C_SCL	PWM0	I2C1_SCL
CODEC_I2C_SDA	PWM1	I2C1_SDA

OPTIONAL I2S CONNECTIONS

CODEC_I2S_DOUT	SSP2_SCK	SAIF0_DATA1
CODEC_I2S_DOUT	ENET_MDC	SAIF0_DATA1
CODEC_MCLK	GPMI_CE3N	SAIF1_MCLK
CODEC_MCLK	LCD_DOTCLK	SAIF1_MCLK
CODEC_I2S_LRCLK	AUART2_RTS	SAIF1_LRCLK
CODEC_I2S_BITCLK	AUART2_CTS	SAIF1_BITCLK
CODEC_I2S_DIN	LCD_VSYNC	SAIF1_SDATA0
CODEC_I2S_DIN	SAIF1_SDATA0	SAIF1_SDATA0
CODEC_I2S_DOUT	SSP2_MISO	SAIF1_SDATA1
CODEC_I2S_DOUT	ENET0_RX_EN	SAIF1_SDATA1
CODEC_I2S_DOUT	LCD_HSYNC	SAIF1_SDATA1

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Drawing Title: **i.MX28 REFERENCE SCHEMATICS**

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USB 2.0 Connectors

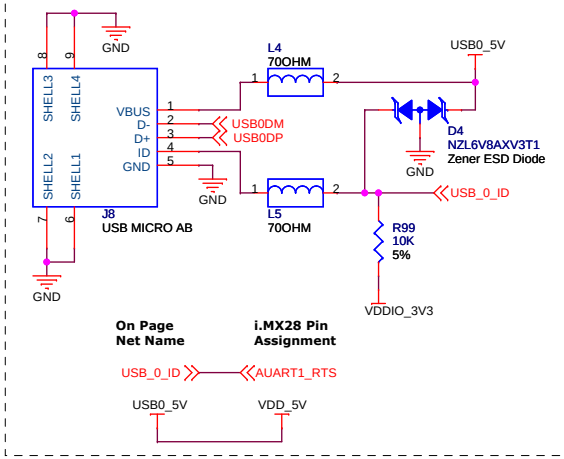
Route USB D+ and D- according to the High Speed USB2.0 Design Guidelines. D+ and D- should have a 90 ohm differential trace impedance and the PCB should have a 20 mil minimum spacing between the USB data lines (D+ and D-) and other signal lines.

In order to maximize ESD immunity, the industrial design plastics should expose the USB Connector as little as possible.

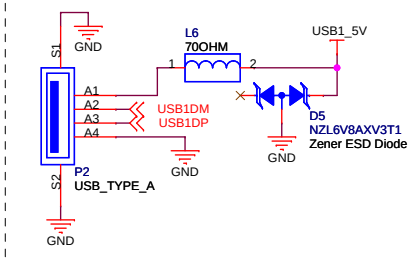
The L4, L5, and L6 ferrites are recommended for ESD immunity. Note that any ferrite in series with the USB 5V supply should have a low DCR (<100mOhms) and be rated for 1A.

The D4 Zener Diode is strongly recommended to protect the VDD5V pin of the i.MX28 from damaging overvoltage conditions that can result from USB cable attachments or from ESD events.

USB0: Device or OTG HOST



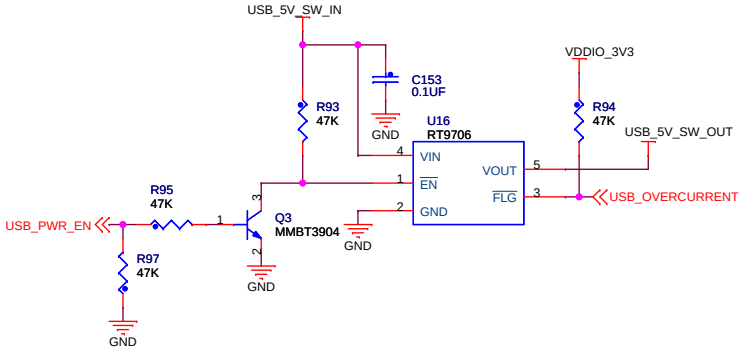
USB1: HOST



USB 5V Power and Overcurrent Detect Switch

This circuit is used to enable 5V power to the USB connector and also to allow for overcurrent detection when the USB 5V bus current exceeds 500mA.

This circuit is needed for each USB connector, so 2 circuits would be needed if supplying 5V power to both USB connnectors.



USB0 Connection Assignments

On Page Net Name	i.MX28 Pin Assignment	
USB_PWR_EN	AUART2_TX	USB_0_PWR_EN
USB_OVERCURRENT	AUART1_CTS	USB_0_OC

Power Connection

USB_5V_SW_OUT — USB0_5V

USB1 Connection Assignments

On Page Net Name	i.MX28 Pin Assignment	
USB_PWR_EN	AUART2_RX	USB_1_PWR_EN
USB_OVERCURRENT	SSP2_SS1	USB_1_OC

Power Connection

USB_5V_SW_OUT — USB1_5V

Switch Power Input

5V Charge Pump (from Li-ion Battery)

USB_5V_SW_IN — CP_5V

OR

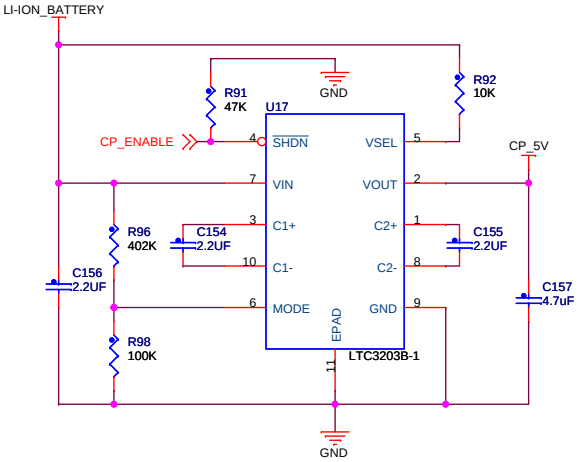
5V DC Adapter Supply

USB_5V_SW_IN — VDD_5V

Optional USB 5V Charge Pump

The USB 5V charge pump can be used to provide a 5V supply to the USB connectors from a Li-ion battery powered device. The maximum 5V output current is 500mA.

One circuit for each USB connector.



USB0 Connection Assignment

On Page Net Name	i.MX28 Pin Assignment	
CP_ENABLE	AUART2_TX	USB_0_PWR_EN

USB1 Connection Assignment

On Page Net Name	i.MX28 Pin Assignment	
CP_ENABLE	AUART2_RX	USB_1_PWR_EN

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Drawing Title: **i.MX28 REFERENCE SCHEMATICS**

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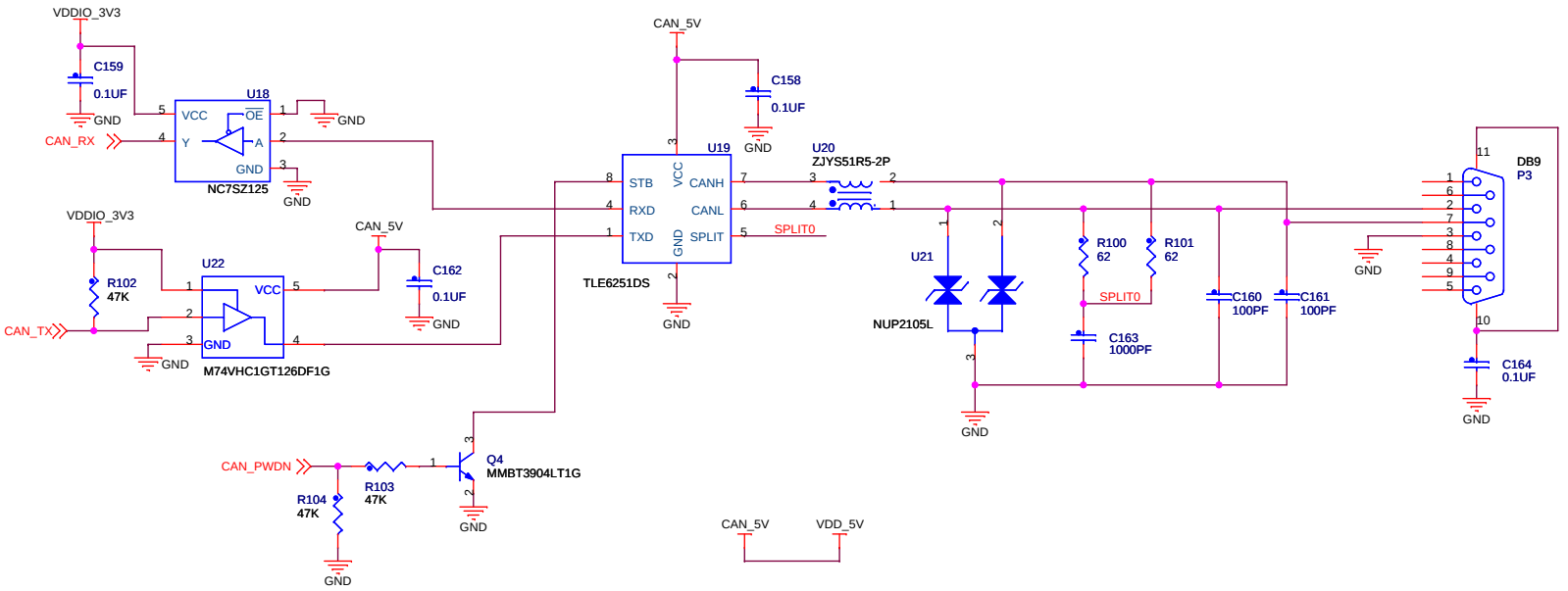
CAN (Controller Area Network) Port

One circuit for each CAN port



MX28 CAN0 Pin Assignments

On Page Net Name	i.MX28 Pin Assignment		
CAN_RX	GPMI_READY3	CAN0_RX	BSP DEFAULT
CAN_TX	GPMI_READY2	CAN0_TX	
CAN_PWDN	SSP1_CMD		
CAN_RX	AUART3_TX	CAN0_RX	OPTIONAL
CAN_TX	AUART3_RX	CAN0_TX	

MX28 CAN1 Pin Assignments

On Page Net Name	i.MX28 Pin Assignment		
CAN_RX	GPMI_CE3N	CAN1_RX	BSP DEFAULT
CAN_TX	GPMI_CE2N	CAN1_TX	
CAN_PWDN	SSP1_CMD		
CAN_RX	AUART3_RTS	CAN1_RX	OPTIONAL
CAN_TX	AUART3_CTS	CAN1_TX	

Note:

If both CAN ports are used, they currently share the same GPIO pin for power down. If the CAN ports need to be powered down individually, then a different GPIO pin should be selected for CAN1.

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Drawing Title: **i.MX28 REFERENCE SCHEMATICS**

Page Title: **CAN**

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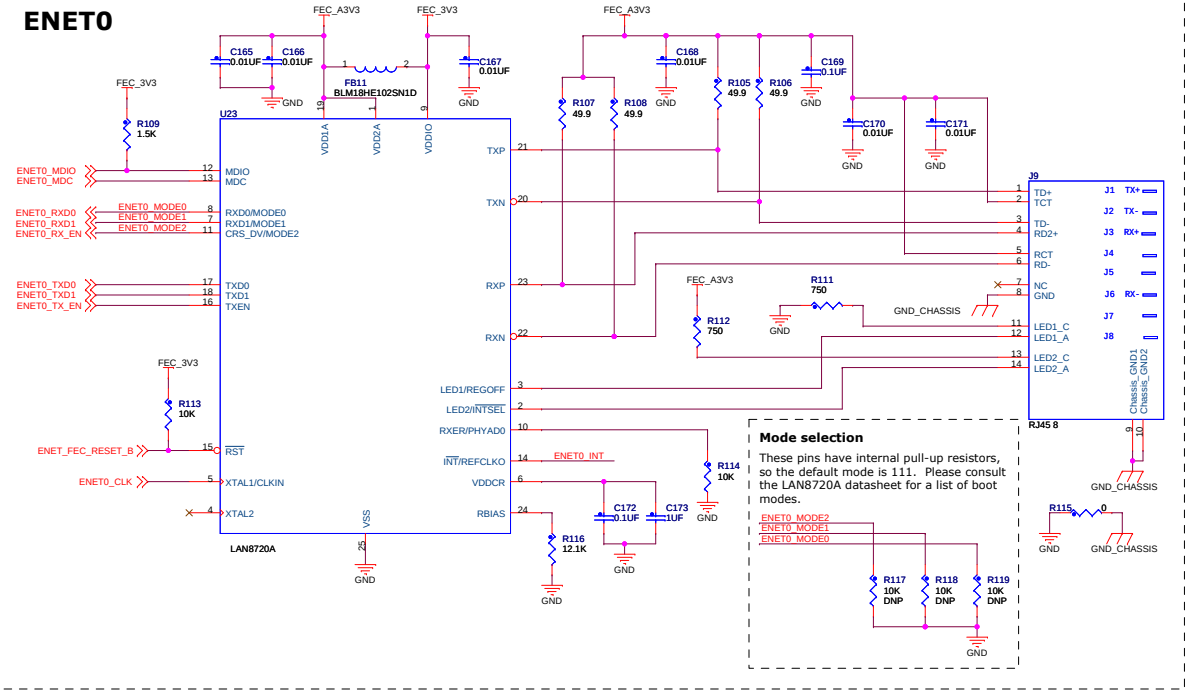
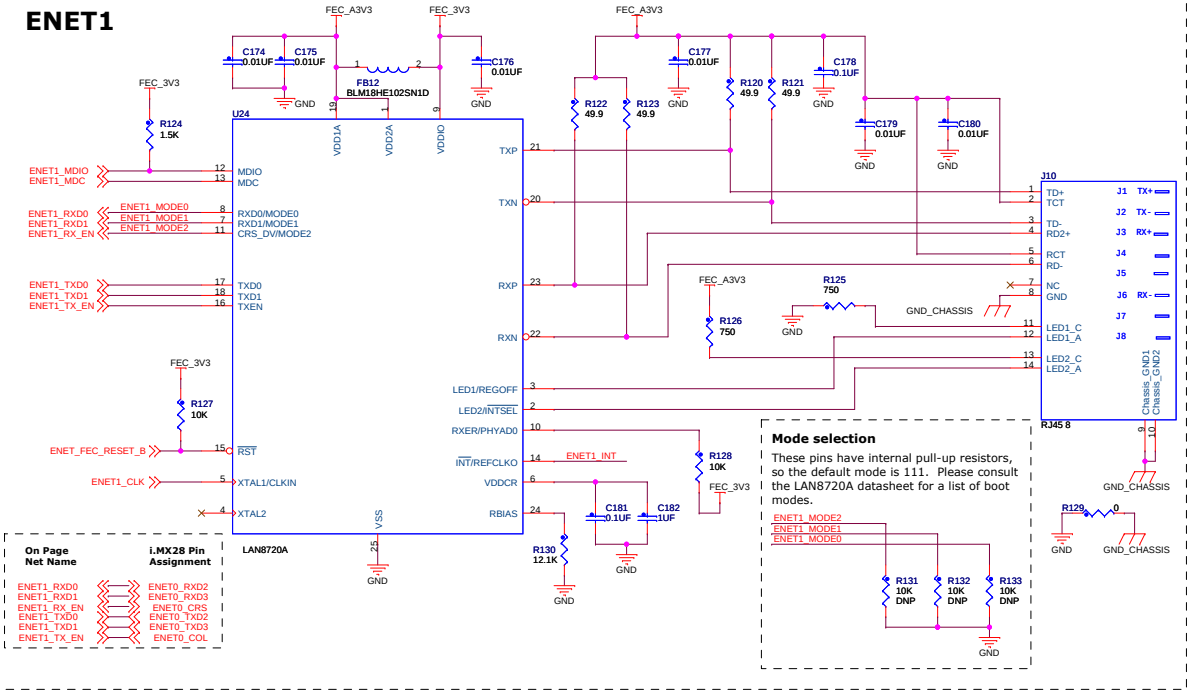
DUAL ETHERNET (RMII Mode)

ENET0

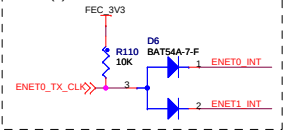


ENET1



Ethernet PHY Interrupt

Both ethernet phys share the same interrupt GPIO using this circuit below. When an interrupt event occurs, the firmware must check both phys to determine the interrupt source(s).



Ethernet PHY MDC/MDIO

Both ethernet phys share the same MDC/MDIO bus from the MX28. The etherent phys are identified by their address, which is set by pin 10 of the LAN8720A.

On Page Net Name	i.MX28 Pin Assignment
ENET0_MDC ENET1_MDC	ENET_MDC
ENET0_MDIO ENET1_MDIO	ENET_MDIO

Ethernet PHY Reset

Both ethernet phys share the same GPIO for reset in the reference scheamatics. Individual GPIOs can be assigned to each ethernet phy reset if required.

On Page Net Name	i.MX28 Pin Assignment
ENET_FEC_RESET_B	ENET0_RX_CLK

Ethernet PHY Clock

The 50MHz clock required for the ethernet phy(s) in RMII communication mode is provided to both phys by the MX28. The ENET clock trace layout should be designed to minimize stubs. For example, the ENET_CLK signal should route out of the MX28 and then split to form a T junction close to both etherent phys to minimize stubs.

On Page Net Name	i.MX28 Pin Assignment
ENET0_CLK ENET1_CLK	ENET_CLK

Ethernet PHY Power

The Ethernet PHY power can be supplied by the MX28 PMU, however caution must be taken to ensure the total VDDIO_3V3 current load does not exceed 250mA. If the total current exceeds this amount, it may be necessary to use an external regulator to supply power to the ethernet PHY or other parts of the system.

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Drawing Title: **i.MX28 REFERENCE SCHEMATICS**

Page Title: **DUAL ETHERNET**

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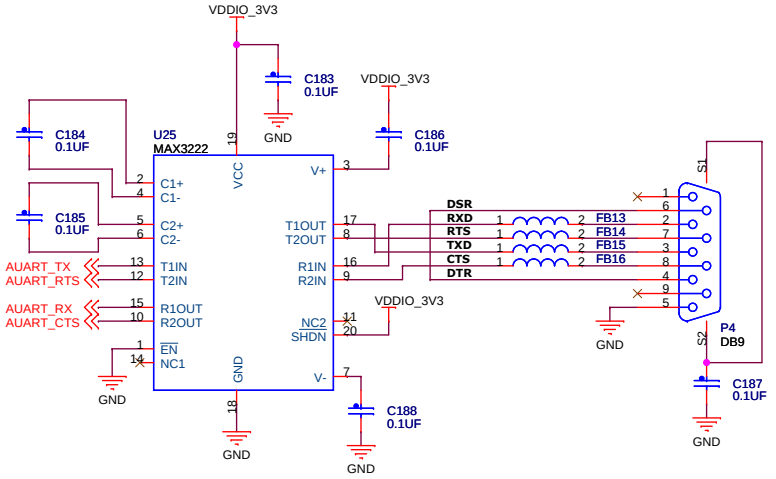
APPLICATION UART RS232 SERIAL PORT (MALE)

The circuit below shows an RS232 transceiver circuit for DTE (male connector) serial port communication. The MX28 has 5 application UART ports. One of these circuits are needed for each UART port. RS232 transcievers combining multiple RS232 interfaces can also be used for reduced cost.

For lower power consumption, the EN and/or SHUTDOWN pins of the RS232 transceiver can be connected to GPIOs so it can be turned off by software when not in use.



AUART0 Connections

On Page Net Name	i.MX28 Pin Assignment	
AUART_CTS	AUART0_CTS	BSP DEFAULT
AUART_RTS	AUART0_RTS	
AUART_RX	AUART0_RX	
AUART_TX	AUART0_TX	

AUART1 Connections

On Page Net Name	i.MX28 Pin Assignment
AUART_CTS	AUART1_CTS
AUART_RTS	AUART1_RTS
AUART_RX	AUART1_RX
AUART_TX	AUART1_TX

AUART4 Connections

On Page Net Name	i.MX28 Pin Assignment	
AUART_CTS	SSP3_SS0	AUART4_CTS
AUART_RTS	SSP3_MISO	AUART4_RTS
AUART_RX	SSP3_MOSI	AUART4_RX
AUART_TX	SSP3_SCK	AUART4_TX

OR

AUART_CTS	SAIF0_MCLK	AUART4_CTS
AUART_RTS	SAIF0_LRCLK	AUART4_RTS
AUART_RX	SAIF0_BITCLK	AUART4_RX
AUART_TX	SAIF0_SDATA0	AUART4_TX

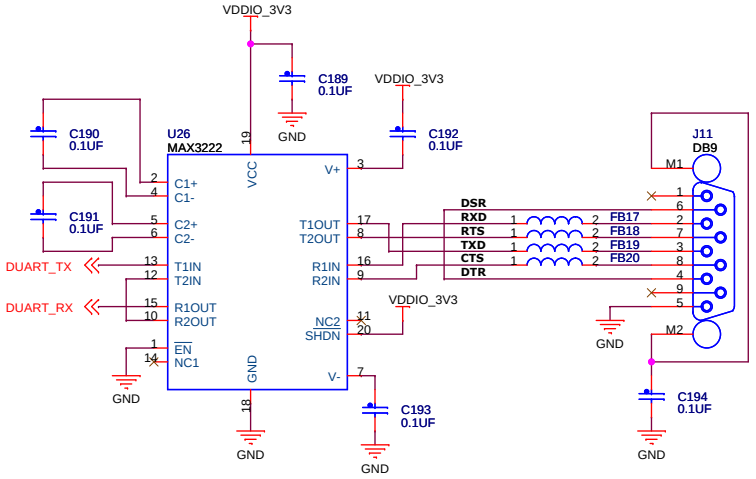
AUART3 Connections

On Page Net Name	i.MX28 Pin Assignment		
AUART_CTS	AUART3_CTS	BSP DEFAULT	
AUART_RTS	AUART3_RTS		
AUART_RX	AUART3_RX		
AUART_TX	AUART3_TX		
AUART_RX	SSP2_MISO	AUART3_RX	OPTIONAL
AUART_TX	SSP2_SS0	AUART3_TX	

AUART2 Connections

On Page Net Name	i.MX28 Pin Assignment		
AUART_CTS	AUART2_CTS		
AUART_RTS	AUART2_RTS		
AUART_RX	AUART2_RX		
AUART_TX	AUART2_TX		
AUART_RX	SSP2_SCK	AUART2_RX	OPTIONAL
AUART_TX	SSP2_MOSI	AUART2_TX	

OPTIONAL:
DEBUG UART RS232 SERIAL PORT (FEMALE)



DUART Connections

On Page Net Name	i.MX28 Pin Assignment		
DUART_RX	PWM0	DUART_RX	BSP DEFAULT
DUART_TX	PWM1	DUART_TX	
DUART_RX	AUART0_CTS	DUART_RX	OPTIONAL
DUART_TX	AUART0_RTS	DUART_TX	
DUART_RX	I2C0_SCL	DUART_RX	OPTIONAL
DUART_TX	I2C0_SDA	DUART_TX	

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Drawing Title: **i.MX28 REFERENCE SCHEMATICS**

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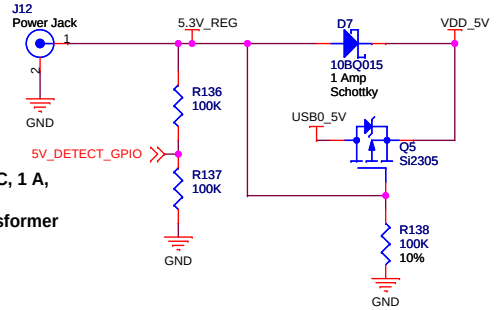
MISC. CIRCUITS

OPTIONAL: Wall Power + USB Power Switch

This circuit allows the i.MX28 to power from an external wall power supply. In the case where wall power and USB power are both connected, power will come from the wall power supply. Note that a GPIO and some firmware support may be required to help the i.MX28 differentiate between USB5V and wall power.

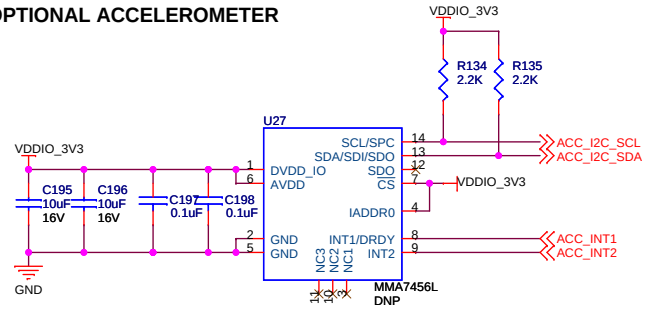
To implement this circuit, remove the direct USB_5V connection on the i.MX28 VDD5V pin, and connect the USB_5V line through a FET as shown.

Note that the 5V wall power supply may need to be slightly higher than 5.0V to ensure that it is always higher than the USB_5V supply and thus always supplying power. Use of 5.2V or 5.3V for the wall power supply is ideal.



Select an available GPIO pin for 5V_DETECT_GPIO.

OPTIONAL ACCELEROMETER



Option 1: I2C0

On Page Net Name	i.MX28 Pin Assignment
ACC_I2C_SCL	I2C0_SCL
ACC_I2C_SDA	I2C0_SDA

I2C0 Alternate Connections

ACC_I2C_SCL	AUART0_RX	I2C0_SCL
ACC_I2C_SDA	AUART0_TX	I2C0_SDA

Option 2: I2C1

On Page Net Name	i.MX28 Pin Assignment	
ACC_I2C_SCL	AUART2_CTS	I2C1_SCL
ACC_I2C_SDA	AUART2_RTS	I2C1_SDA

I2C1 Alternate Connections

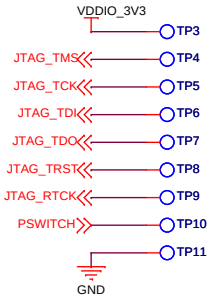
ACC_I2C_SCL	PWM0	I2C1_SCL
ACC_I2C_SDA	PWM1	I2C1_SDA

Select two free GPIO pins for ACC_INT1 and ACC_INT2

OPTIONAL PARALLEL JTAG PORT CONNECTIONS

In order to allow debugging on a i.MX28-based device, it is recommended to add JTAG testpoints as shown below. In addition, there are other changes that may be required to support debugging:

1) The C125 0.1uF capacitor on PSWITCH may need to be moved to the other side of R72, the 1K resistor.



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Drawing Title: i.MX28 REFERENCE SCHEMATICS

Page Title: OPTIONAL CIRCUITS

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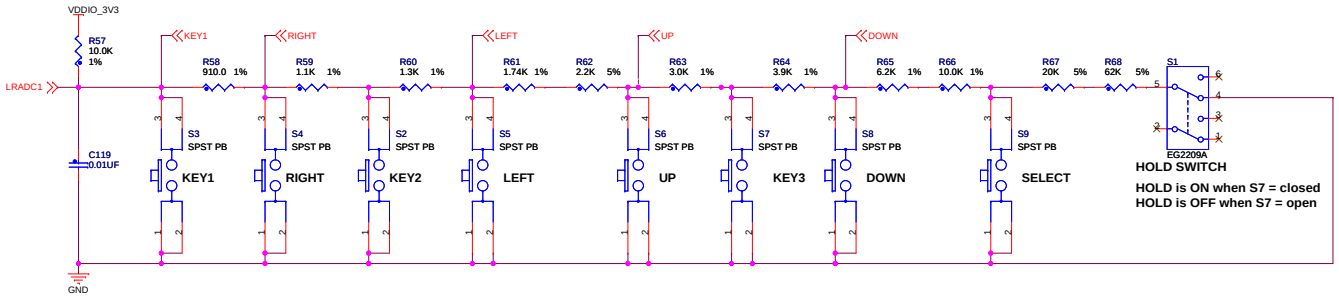
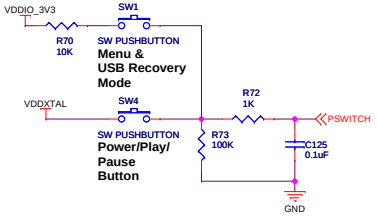
User Buttons



POWER / PLAY / PAUSE & MENU / USB RECOVERY BUTTONS



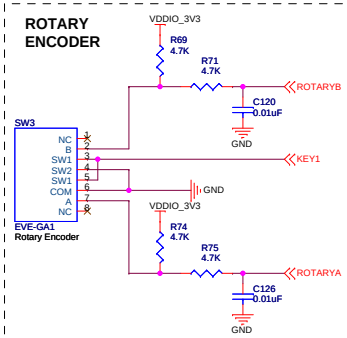
RESISTIVE TOUCHSCREEN / TOUCHPANEL

NOTES:

1. If using a device with an impedance greater than a few kOhms (such as a Touchpanel), the filter capacitors on the LRADC channels (see page 3) may be reduced to 5pF. These smaller capacitors reduce the settling time, which reduces the amount of time the processor must wait to take an accurate reading. These filter capacitors should be placed close to the i.MX28.

2. If a 5 wire resistive touch panel is being used, the 5th analog wire should be connected to LRADC6.

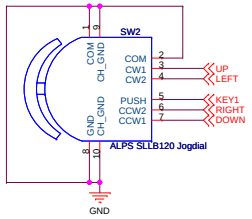
ROTARY ENCODER



Connections

On Page Net Name		i.MX28 Pin Assignment
ROTARYA	AUART1_CTS	TIMROT_ROTARYA
ROTARYB	AUART1_RTS	TIMROT_ROTARYB
OR		
ROTARYA	I2C0_SCL	TIMROT_ROTARYA
ROTARYB	I2C0_SDA	TIMROT_ROTARYB

JOG DIAL

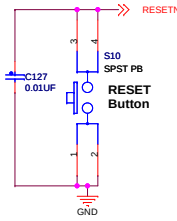


NOTE: The JogDial as shown uses the LRADC resistor network for its internal buttons.

RESET CIRCUIT OPTIONS

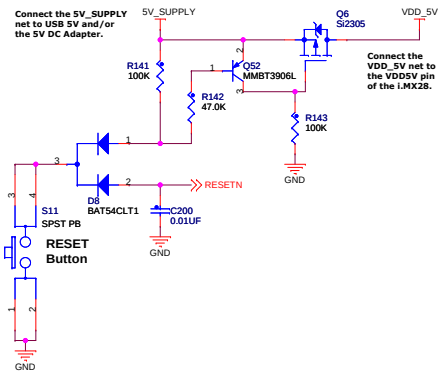
Option 1: i.MX28 chip reset

This circuit will reset the i.MX28 processor as well as shutdown the i.MX28 DCDC converter outputs when connected to the Li-ion battery with no 5V present on the VDD5V pin. However, this circuit will not shutdown the i.MX28 PMU outputs when a 5V supply is connected to the VDD5V pin. If this is desired/required, option 2 should be used.



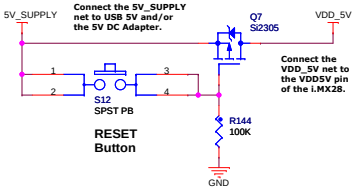
Option 2: System reset with a Li-ion Battery and 5V Supply

This circuit will reset the i.MX28 processor as well as shutdown the i.MX28 DCDC converter outputs when connected to the Li-ion battery with no 5V present on the VDD5V pin. This circuit will also disconnect the 5V supply to the i.MX28 VDD5V pin thereby turning off the i.MX28 PMU outputs when a 5V supply is present. The other components in the system should also connect to the VDD_5V net to ensure power is disconnected from those peripherals.



Option 3: System reset with a 5V Supply only (no Li-ion battery)

This circuit will also disconnect the 5V supply to the i.MX28 VDD5V pin thereby turning off the i.MX28 PMU outputs when a 5V supply is present. The other components in the system should also connect to the VDD_5V net to ensure power is disconnected from those peripherals.



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Drawing Title: **i.MX28 REFERENCE SCHEMATICS**

Page Title: **USER INTERFACE**

Size	Document Number	Rev
C	N/A	A

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