i.MX8QXP/8QM USB Test Guide

Because imx8QM and imx8QXP have same USB PHYs, the registers address are same for both chips, we just take imx8QXP board as a sample, the test method on imx8QM is same.

Prerequisites

To complete the USB test, you will need to download and install the following software:

1. Terminal Emulator such as PUTTY: https://www.putty.org/
2. MfgtoolV3 (uuu); this tool will be used for installing Linux and Android onto the boards and can be found here. Download the latest Released version.
3. Pre-released and pre-built Linux images can be found here. Look for i.MX 8QXP MEK. The latest Linux image is “Linux 5.4.47_2.2.0”

Programming the SD card with Linux

1) Download the Linux file to a subdirectory. For this instance we will assume the download file is L5.4.47_2.2.0_images_MX8QXPC0MEK.zip. You can find the unzipped file in below path, C:\Users\Desktop\i.MX8QXP\ \Linux, which is the same path with uuu.exe file.
2) Set the boot switch SW2 to Serial Download mode.

SCU_BOOT_ MODE0	SCU_BOOT _MODE1	SCU_BOOT _MODE2	SCU_BOOT_ MODE3	Boot Source
1	0	0	0	Serial Download

3) Plug a USB type C cable from your host computer to the MEK Type-C connector J10. Insert a SD card to the MEK SD card slot J12.
4) Open a command prompt window

Type:

cd C:\Users\Desktop\i.MX8QXP\ \Linux

uuu -b sd_all imx-boot-imx8qxpc0mek-sd.bin-flash_regression_linux_m4 test-internal-qt5-imx8qxpc0mek.wic

The program indicates "Wait for Known USB Device Appear"

```
uuu (Universal Update Utility) for nxp imx chips -- libuuu_1.1.81-0-ge39adc4

uuu [-d -m -v -V] <bootloader|cmdlists|cmd>

    bootloader  download bootloader to board by usb
    cmdlist     run all commands in cmdlist file
                If it is path, search uuu.auto in dir
                If it is zip, search uuu.auto in zip
    cmd         Run one command, use -H see detail
                example: SDPS: boot -f flash.bin
    -d          Deamon mode, wait for forever.
    -v -V       verbose mode, -V enable libusb error\warning info
    -m          USBPATH Only monitor these pathes.
                    -m 1:2 -m 1:3

uuu -s          Enter shell mode. uuu.inputlog record all input commands
                you can use "uuu uuu.inputlog" next time to run all commands

uuu -h -H       show help, -H means detail helps

uuu [-d -m -v] -b[run] <emmc|emmc_all|qspi|sd|sd_all|spl> arg...
        Run Built-in scripts
        emmc    burn boot loader to eMMC boot partition
                arg0: _flash.bin
        emmc_all        burn whole image to eMMC
                arg0: _flash.bin
                arg1: _rootfs.sdcard
        qspi    burn boot loader to qspi nor flash
                arg0: _flexspi.bin  bootloader
                arg1: _image[Optional]  image burn to flexspi, default is the same as bootloader
        sd      burn boot loader to sd card
                arg0: _flash.bin
        sd_all  burn whole image to sd card
                arg0: _flash.bin
                arg1: _rootfs.sdcard
        spl     boot spl and uboot
                arg0: _flash.bin

uuu -bshow <emmc|emmc_all|qspi|sd|sd_all|spl>
        Show built-in script

Wait for Known USB Device Appear
```

Note: uuu.exe is a command line program. Just double clicking on it will not work

5) Power on the board.

a. This process will take a few minutes. The status is indicated on the host PC.

```
Success 0    Failure 0

1:2    4/ 7   [=>          10%            ] FB: flash -raw2sparse all fsl-image-validation-imx-imx8mmevk.sdcard
```

b. When the programming of the memory is completed, the program will indicate "Done".

```
Success 1    Failure 0

1:2    7/ 7   [Done                        ] FB: done
```

6) Power Off the board

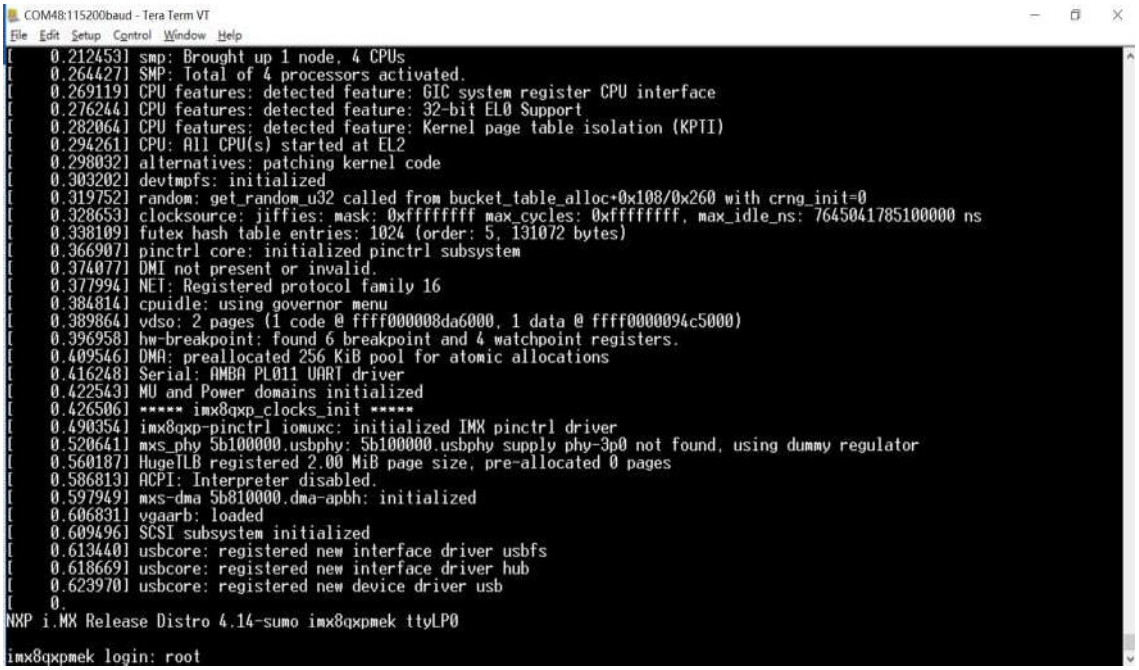
7) Reset the switches to boot from the SD card

SCU_BOOT_MODE0	SCU_BOOT_MODE1	SCU_BOOT_MODE2	SCU_BOOT_MODE3	Boot Device
1	1	0	0	SD1

8) Plug a Micro USB cable from your host computer to the MEK Micro_AB connector J11. Start your favorite terminal program and connect to the appropriate com port. Set Baud rate to 11520.

9) Power on the board.

a. You will see many messages cross the console and finally land on a prompt. The log in is "root" with no password.

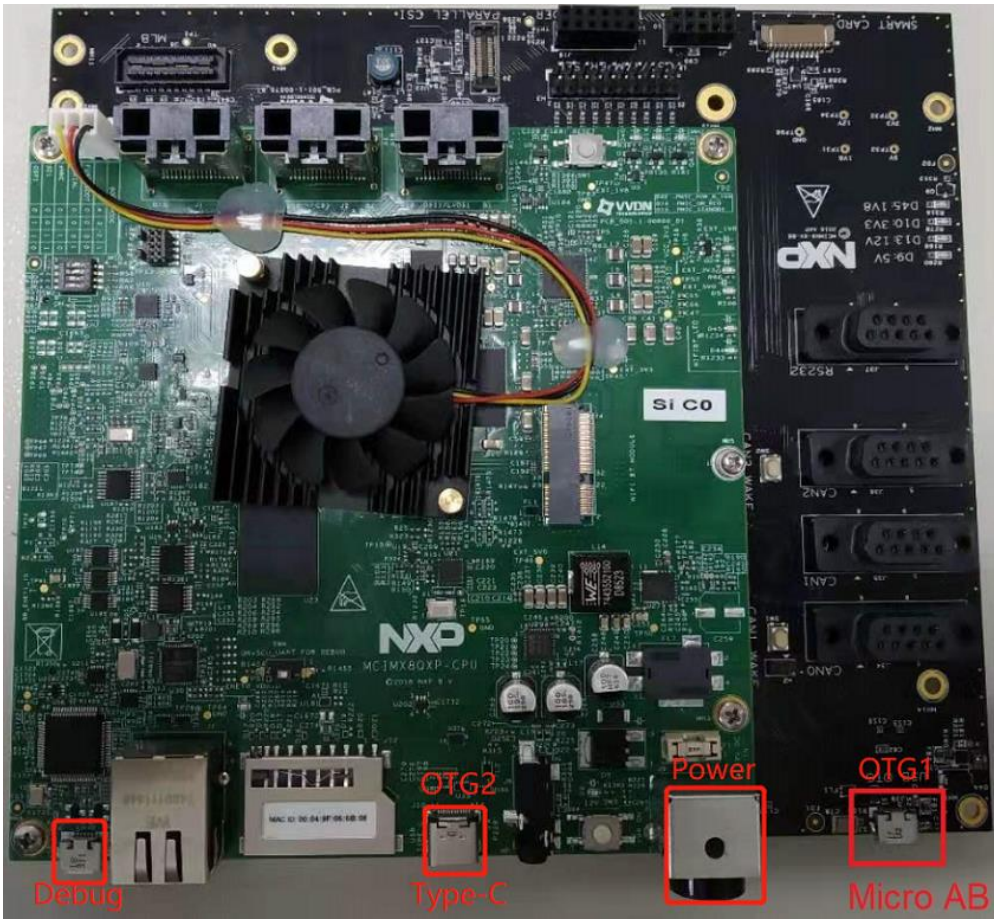


USB Test steps on imx8QXP MEK board

imx8QM/QXP has two OTG controller:

1. OTG1 is USB2.0
2. OTG2 can be either USB 2.0 or USB 3.0

So for OTG2 port, we have split the test with USB 2.0 and USB 3.0.



1. USB OTG1 port （on baseboard of MEK）

1.1 USB2.0 host mode

Enter into kernel and login on:

root

Then please see AN12409 for detail descriptions of the Certification Test requirements, equipment, procedures.

Note: if you want to trig the test pattern, please run the following command with “Blue”:

echo -1 > /sys/module/usbcore/parameters/autosuspend

for i in $(find /sys -name control | grep usb);do echo on > $i;echo "echo on > $i";done;

/unit_tests/memtool 0x5b0d0184 1 //read the register settings, address of the other USB port;

/unit_tests/memtool 0x5b0d0184=0x18441205 // Force to output Test Packet for Eye Diagram Test

/unit_tests/memtool 0x5b0d0184=0x18411205 // Force to output **J_STATE**

/unit_tests/memtool 0x5b0d0184=0x18421205 // Force to output **K_STATE**

/unit_tests/memtool 0x5b0d0184=0x18431205 // Force to output **SE0 (host) / NAK (device)**

/unit_tests/memtool 0x5b0d0184=0x18001305 // Force to output **Reset**

/unit_tests/memtool 0x5b0d0184=0x18001285 // Force to output **Suspend**

/unit_tests/memtool 0x5b0d0184=0x18001245 // Force to output **Resume**

Note:

(echo -1 > /sys/module/usbcore/parameters/autosuspend)

Disable USB bus enters suspend state

(for i in $(find /sys -name control | grep usb);do echo on > $i;echo "echo on > $i";done;)

Disable USB runtime suspend, in that case, the controller and PHY will not enter low power mode, and we can visit the register even there is no device on the port.

Registers that entry into USB2.0 test mode for USB OTG1 --USB_x_PORTSC1 (offset:184h)

Name	PORTSC1															
Description	Device Controller															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	PTS_1		STS	PTW	PSPD		PTS_2	PFSC	PHCD	WKOC	WKDC	WKCN	PTC			
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	1
Field definitions	PIC		PO	PP	LS		HSP	PR	SUSP	FPR	OCC	OCA	PEC	PE	CSC	CCS

Signal Names	Description
19–16 **PTC**	Port Test Control - Read/Write. Default = 0000b. Refer to Port Test Mode for the operational model for using these test modes and the USB Specification Revision 2.0, Chapter 7 for details on each test mode. The FORCE_ENABLE_FS and FORCE ENABLE_LS are extensions to the test mode support specified in the EHCI specification. Writing the PTC field to any of the FORCE_ENABLE_{HS/FS/LS} values will force the port into the connected and enabled state at the selected speed. Writing the PTC field back to TEST_MODE_DISABLE will allow the port state machines to progress normally from that point. NOTE: Low speed operations are not supported as a peripheral device. Any other value than zero indicates that the port is operating in test mode. Value Specific Test 0000 TEST_MODE_DISABLE 0001 J_STATE 0010 K_STATE 0011 SE0 (host) / NAK (device) 0100 Packet 0101 FORCE_ENABLE_HS 0110 FORCE_ENABLE_FS 0111 FORCE_ENABLE_LS 1000-1111 Reserved

Table3-1. USB_PORTSC1 field descriptions

1.2 USB2.0 device mode

Enter into kernel and login on:

root

./configfs.sh “” ci

Please refer to Software Configuration to complete ./configfs.sh “” ci . Then please see AN12409 for detail descriptions of the Certification Test requirements, equipment, procedures.

Note:

(./configfs.sh “” ci)

Set the device to visible.

2. USB OTG2 port （Type-C port on MEK）

2.1 USB2.0 host mode

Enter into kernel and login on:

root

Then please see AN12409 for detail descriptions of the Certification Test requirements, equipment, procedures.

Note: if you want to trig the test pattern, please run the following command with “Blue”:

```
echo -1 > /sys/module/usbcore/parameters/autosuspend
for i in $(find /sys -name control | grep usb);do echo on > $i;echo "echo on > $i";done;
#PORTSC1USB2:1_0480h
/unit_tests/memtool 0x5b130480 1
/unit_tests/memtool 0x5b130480=0xa0
#PORTSC1USB3:1_0490h
/unit_tests/memtool 0x5b130490=0xa0
#USBCMD:1_0080h
/216unit_tests/memtool 0x5b130080=0x804
#PORTPMSC1USB2：1_0484h
# enable Test mode
/unit_tests/memtool 0x5b130484=0x80000000

# Test Packet
/unit_tests/memtool 0x5b130484=0x40000000

# Test_J Mode
/unit_tests/memtool 0x5b130484=0x10000000

# Test_K Mode
/unit_tests/memtool 0x5b130484=0x20000000

# Test Nek Mode
/unit_tests/memtool 0x5b130484=0x30000000
```

Registers that entry into USB2.0 test mode for OTG2

Name	PORTSC1USB2/ PORTSC1USB3															
Description	USB2/3 Port Status and Control															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	WPR	DR	Reserved	Reserved	WOE	WOE	WOE	CAS	CEC	PLC	PRC	OCC	WRC	PEC	CSC	LWS
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	1
Field definitions	PIC		PortSpeed				PP	PLS				PR	OCA	Reserved	PED	CCS

Signal Names	Description
9 **PP**	Port Power (PP), RWS. Default = '1'. This flag reflects a port's logical, power control state. Because host controllers can implement different methods of port power switching, this flag may or may not represent whether (VBus) power is actually applied to the port. When PP equals a '0' the port is nonfunctional and shall not report attaches, detaches, or Port Link State (PLS) changes. However, the port shall report overcurrent conditions when PP = '0' if PPC = '0'. After modifying PP, software shall read PP and confirm that it has reached its target state before modifying it again, undefined behavior may occur if this procedure is not followed. '0' = This port is in the Powered-off state. '1' = This port is not in the Powered-off state. If the Port Power Control (PPC) flag in the HCCPARAMS register is '1', then xHC has port power control switches and this bit represents the current setting of the switch ('0' = off, '1'=on). If the Port Power Control (PPC) flag in the HCCPARAMS register is '0', then xHC does not have port power control switches and each port is hard wired to power, and not affected by this bit. When an over-current condition is detected on a powered port, the xHC shall transition the PP bit in each affected port from a '1' to '0' (removing power from the port).

Name	USBCMD															
Description	USB Command															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	Reserved															
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	Reserved				EU3S	EWE	CRS	CSC	LHCRST	Reserved			HSEE	INTE	HCRST	R_S

Signal Names	Description
0 **R_S**	Run/Stop (R/S), RW. Default = '0'. '1' = Run. '0' = Stop. When set to a '1', the xHC proceeds with execution of the schedule. The xHC continues execution as long as this bit is set to a '1'. When this bit is cleared to '0', the xHC completes any current or queued commands or TDs, and any USB transactions associated with them, then halts. Refer to section 5.4.1.1 of xHCI specification for more information on how R/S shall be managed. The xHC shall halt within 16 ms after software clears the Run/Stop bit if the above conditions have been met. The HCHalted (HCH) bit in the USBSTS register indicates when the xHC has finished its pending pipelined transactions and has entered the stopped state. Software shall not write a '1' to this flag unless the xHC is in the Halted state (i.e. HCH in the USBSTS register is '1'). Doing so may yield undefined results. Writing a '0' to this flag when the xHC is in the Running state (i.e. HCH = '0') and any Event Rings are in the Event Ring Full state (refer to section 4.9.4 of xHCI specification) may result in lost events. When this register is exposed by a Virtual Function (VF), this bit only controls the run state of the xHC instance presented by the selected VF. Refer to section 8 of xHCI specification for more information.

Name	PORTPMSC1USB2															
Description	USB2 Port Power Management Status and Control															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	PTC				Reserved											HLE
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	L1DS								BESL				RWE	L1S		

Signal Names	Description
9 PP	Port Test Control, RW. Default = '0'. When this field is '0', the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. A non-zero Port Test Control value is only valid to a port that is in the Powered-Off state (PLS = Disabled). If the port is not in this state, the xHC shall respond with the Port Test Control field set to Port Test Control Error. Refer to section 4.19.6 for the operational model for using these test modes. The encoding of the Test Mode bits for a USB2 protocol port are: 0: Test mode not enabled 1: Test J_STATE 2: Test K_STATE 3: Test SE0_NAK 4: Test Packet 5: Test FORCE_ENABLE 6-14: Reserved. 15: Port Test Control Error.

2.2 USB2.0 device mode

Boot up

Enter into kernel, input below commands:

root

./configfs.sh

Please refer to Software Configuration to complete ./configfs.sh . Then please see AN12409 for detail descriptions of the Certification Test requirements, equipment, procedures.

Note:

(./configfs.sh)

Set the device to visible.

2.3 USB3.0 host mode

Note: write the command and then connect the test fixture.

Enter into kernel and log in:

root

then, input below commands:

echo -1 > /sys/module/usbcore/parameters/autosuspend

for i in $(find /sys -name control | grep usb);do echo on > $i;echo "echo on > $i";done;

/unit_tests/memtool 0x5b130490=0x0a000340

Then please see AN12409 for detail descriptions of the Certification Test requirements, equipment, procedures.

Note:

(echo -1 > /sys/module/usbcore/parameters/autosuspend)

Disable USB bus enters suspend state

(for i in $(find /sys -name control | grep usb);do echo on > $i;echo "echo on > $i";done;)

Disable USB runtime suspend, in that case, the controller and PHY will not enter low power mode, and we can visit the register even there is no device on the port.
(/unit_tests/memtool 0x5b130490=0x0a000340)

Set Link is in the Compliance Mode State

Search PORTSC1USB3. PLS find the register in reference manual.

2.4 USB3.0 device mode

Note: write the command and then connect the test fixture.

1. boots up and log in:
   root
2. then, input below commands:
   ./configfs.sh

Please refer to Software Configuration to complete ./configfs.sh . Then please see AN12409 for detail descriptions of the Certification Test requirements, equipment, procedures.

3. 8QXP/8QM register

Type-C port base address：USB3_PHY3P0（5B16_0000）
USB3 (5B12_0000)
USB2PHY(5B19_8000)
Micro-AB port base address: USBOH_OTG(5B0D_0000)
Register address：base address+offset

3.1 Register to Fine tune the OTG2 eye pattern--AFE_TX_REG1 (offset: 04h）

/unit_tests/memtool 0x5b198004 1 // Read register data

/unit_tests/memtool 0x5b198004=0x3f // Write AFE_TX_REG1 register data

Register Name	Register Address (offset)	Register Bit	Description FastChar	Value
AFE_TX_REG1	0x0004	<7:6>	UNUSED	00
		<5>	HSTX DEEMP AMPLITUDE TRIM - TURN OFF	0
			HSTX DEEMP AMPLITUDE TRIM - TURN ON	1
		<4>	HSTX DEEMP AMPLITUDE TRIM - TURN OFF	0
			HSTX DEEMP AMPLITUDE TRIM - TURN ON	1
		<3>	HSTX DEEMP AMPLITUDE TRIM - TURN OFF	0
			HSTX DEEMP AMPLITUDE TRIM - TURN ON	1
		<2>	HSTX DEEMP AMPLITUDE TRIM - TURN OFF	0
			HSTX DEEMP AMPLITUDE TRIM - TURN ON	1
		<1>	HSTX DEEMP AMPLITUDE TRIM - TURN OFF	0
			HSTX DEEMP AMPLITUDE TRIM - TURN ON	1
		<0>	HSTX DEEMP AMPLITUDE TRIM - TURN OFF	0
			HSTX DEEMP AMPLITUDE TRIM - TURN ON	1

AFE_TX_REG12	0x0030	<7:2>	UNUSED	000000
		<1>	HSTX DEEMP AMPLITUDE TRIM - TURN OFF	0
			HSTX DEEMP AMPLITUDE TRIM - TURN ON	1
		<0>	HSTX DEEMP AMPLITUDE CANNOT BE CONTROLLED BY ANALOG TEST BITS IN AFE_TX_REG1	0
			HSTX DEEMP AMPLITUDE CAN BE CONTROLLED BY ANALOG TEST BITS IN AFE_TX_REG1	1

Table3-2. HS Tx Amplitude Tune bits control Register

Register Name	Register Address	Register Bit	Description FastChar	Value
AFE_TX_REG5	0x0014	<7>	Reserved	0
AFE_TX_REG5	0x0014	<6:1>	HSTX Slew Rate control code	<000000> to <111111> 64 steps
AFE_TX_REG5	0x0014	<0>	HSTX Slew control set to default code<111000>	0
			HSTX Slew control Set by control code AFE_TX_REG<6:1> value	1

Table3-3. HS Tx Slew Rate control Register

3.2 Register to Fine tune OTG1 eye pattern --USBPHY_TX (offset:10h)

/unit_tests/memtool 0x5b100010 1 // Read register data

/unit_tests/memtool 0x5b100010=0x10080803 //write USBPHY_TX

Name	USBPHYx_TXn															
Description	The USB PHY Transmitter Control Register handles the transmit controls.															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0
Field definitions	Reserved			Reserved			Reserved	Reserved	Reserved		TXENCAL45DP	Reserved	**TXCAL45DP**			
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	1
Field definitions	Reserved		TXENCAL45DN	Reserved	**TXCAL45DM**				Reserved				**D_CAL**			

Signal Names	Description
TXCAL45DP	Decode to trim the nominal 45Ω series termination resistance to the USB_DP output pin. Maximum resistance = 0000. Resistance is centered by design at 1000. Trimming this resistance will impact both the overshoot/undershoot of the Full Speed TX output and the amplitude of the High Speed TX output.

TXCAL45DM	Decode to trim the nominal 45Ω series termination resistance to the USB_DM output pin. Maximum resistance = 0000. Resistance is centered by design at 1000. Trimming this resistance will impact both the overshoot/undershoot of the Full Speed TX output and theamplitude of the High Speed TX output.
D_CAL	Decode to trim the nominal 17.78mA current source for the High Speed TX drivers on USB_DP andUSB_DM. This current is directly proportional to the amplitude of the High Speed TX eye diagram. 0000 Maximum current, approximately 19% above nominal. 0111 Nominal 1111 Minimum current, approximately 19% below nominal.

Table3-4. USBPHYx_TXn Register Settings

3.3 Adjust USB3.0 to compliance mode registers--PORTSC1USB3（offset: 1_0490h）

/unit_tests/memtool 0x5b130490=0x0a000340

Name	**PORTSC1USB3**															
Description	USB3 Port Status and Control															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	WPR	DR	Reserved	Reserved	WOE	WOE	WOE	CAS	CEC	PLC	PRC	OCC	WRC	PEC	CSC	LWS
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	1
Field definitions	PIC		PortSpeed				PP	PLS				PR	OCA	Reserved	PED	CCS

Signal Names	**Description**
8-5 PLS	Port Link State (PLS), RWS. Default = RxDetect ('5'). This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. Write Values: 0: The link shall transition to a U0 state from any of the U states. 3: The link shall transition to a U3 state from the U0 state. This action selectively suspends the device connected to this port. While the Port Link State = U3, the hub does not propagate downstream-directed traffic to this port, but the hub shall respond to resume signaling from the port. 5: If the port is in the Disabled state (PLS = Disabled, PP = '1'), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored. 1-2,4,6-15: Ignored. State Encoding: 0: Link is in the U0 State, 1: Link is in the U1 State, 2: Link is in the U2 State, 3: Link is in the U3 State (Device Suspended), 4: Link is in the Disabled State, 5: Link is in the RxDetect State, 6: Link is in the Inactive State, 7: Link is in the Polling State, 8: Link is in the Recovery State, 9: Link is in the Hot Reset State, 10: Link is in the Compliance Mode State, 11: Link is in the Test Mode State, 12-14: Reserved, 15: Link is in the Resume State. Note: The Port Link State Write Strobe (LWS) shall also be set to '1' to write this field. This field is undefined if PP = '0'. Note: Transitions between different states are not reflected until

	the transition is complete. Refer to section 4.19 of xHCI specification for PLS transition conditions. Refer to sections 4.15.2 and 4.23.5 for more information on the use of this field

Table3-5. PORTSC1USB3 field descriptions

Appendix:

1. Software Configuration

After the board boots up, input the following commands to create configfs.sh:

```
Example configfs.sh
if [ "$1" == "" ]; then
export FUNC="mass_storage"
else
export FUNC=$1
fi
#38100000.dwc3 for imx850D Synopsys USB3 IP
#5b110000.usb3 for imx8qm and imx8qxp Cadence USB3 IP
#ci_hdrc.0 for Legacy NXP USB2 IP
if [ "$2" == "" ]; then
export CONTROLLER="5b110000.usb3"
else
export CONTROLLER="ci_hdrc.0"
fi
if ! mount|grep -sq '/sys/kernel/config'; then
mount -t configfs none /sys/kernel/config
fi
cd /sys/kernel/config/usb_gadget
mkdir g1
cd g1
echo "0x1fc9" > idVendor
echo "0x0129" > idProduct
mkdir strings/0x409
echo "12345678ABCD" > strings/0x409/serialnumber
echo "NXP Semiconductors" > strings/0x409/manufacturer
echo "i.MX Reference Board" > strings/0x409/product
mkdir configs/c.1
mkdir functions/$FUNC".0"

ln -s functions/$FUNC".0" configs/c.1
if [ "$FUNC" == "mass_storage" ]; then
echo "/home/root/storage.img" > functions/mass_storage.0/lun.0/file
echo 1 > functions/mass_storage.0/lun.0/removable
echo 0xc0 > configs/c.1/bmAttributes
fi
if [ "$FUNC" == "ncm" ]; then
echo 10 > functions/ncm.0/qmult
fi
echo $CONTROLLER > /sys/kernel/config/usb_gadget/g1/UDC
```

After finishing the above edit, quit(Ctrl+X) and save(Y). Then to input the following commands:

```
chmod +x configfs.sh
```

```
dd if=/dev/zero of=/home/root/storage.img bs=1M count=256
mkfs.vfat /home/root/storage.img
```