Crystal Image through Imaging Innovation

PIXELPLUS

1 CH Multi-Standard Analog HD Video Receiver with MIPI Interface

PR2000K

Preliminary Datasheet

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1. General Description

1.1. Product Overview

The PR2000 is a HD/SD video receiver which accepts **Any Standard and Resolution of Analog HD/SD video** and guarantees high quality image for **Long-Reach Analog HD** applications. It accepts **Single-ended/Differential** analog HD/SD video signal from camera, then **Cable Equalizer** compensates cable attenuation, and HD/SD video decoder converts analog video signal to digital component data. The PR2000 supports 8bit parallel interface with BT1120/BT656 standard and MIPI-CSI2 interface compliant with MIPI-DPHY v1.0 and MIPI-CSI2 v1.0. The PR2000 also provides **Bi-Directional Coaxial/UTP PTZ** interface so that host can control PTZ camera and receive information from camera with 2-wire serial interface.

1.2. Features

- **Video Decoder**
  - ✓ Multi-standard Analog HD and SD Video with Auto-Detection
    - *All Kind of Analog HD Standard and NTSC/PAL*
  - ✓ Any Resolution of Analog HD and SD Video with Auto-Detection
    - *1080p25/30, 720p25/30/50/60, 960p25/30/50/60 and 480i60, 576i50*
  - ✓ Superior Cable Equalizer for Long-Reach Analog HD Application
  - ✓ Differential Analog Input or Two Single-ended Analog Input with MUX Switch
  - ✓ Multi-Channel Time-Multiplexed Video Output with Dual Edge of Clock
  - ✓ BT1120/BT656 Parallel Output
  - ✓ MIPI-CSI2 2/4 Data Lane Configuration
    - YUV422 8 Bit Format
    - 2/4 Data Lanes for 720p25/30, 4 Data Lanes for 720p50/60, 1080p@25/30
- **Bi-Directional PTZ Communication**
  - ✓ Flexible Protocol
- **Graphic Overlay**
  - ✓ Dynamic Parking Guide Line or OSG Overlay
- **Host Interface**
  - ✓ I2C Serial Interface
- **Low Power Consumption**
  - ✓ 340mW (Parallel Output) / 268mW (MIPI Output)
- **Package**
  - ✓ 40 eQFN (5mm x 5mm)

1.3. Block Diagram

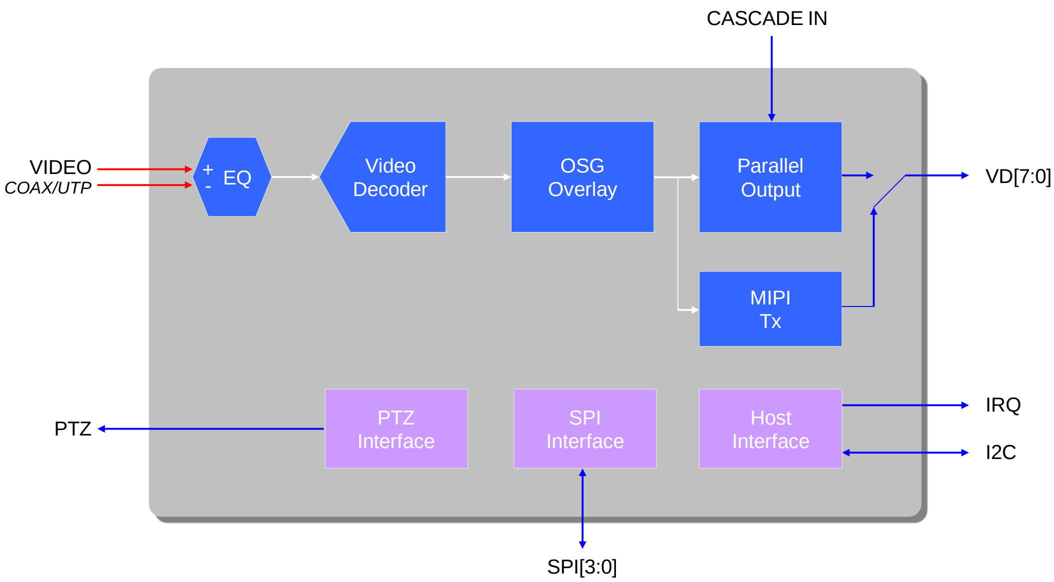

Fig 1. Functional Block Diagram

2. Pin Information

2.1. Pin Diagram

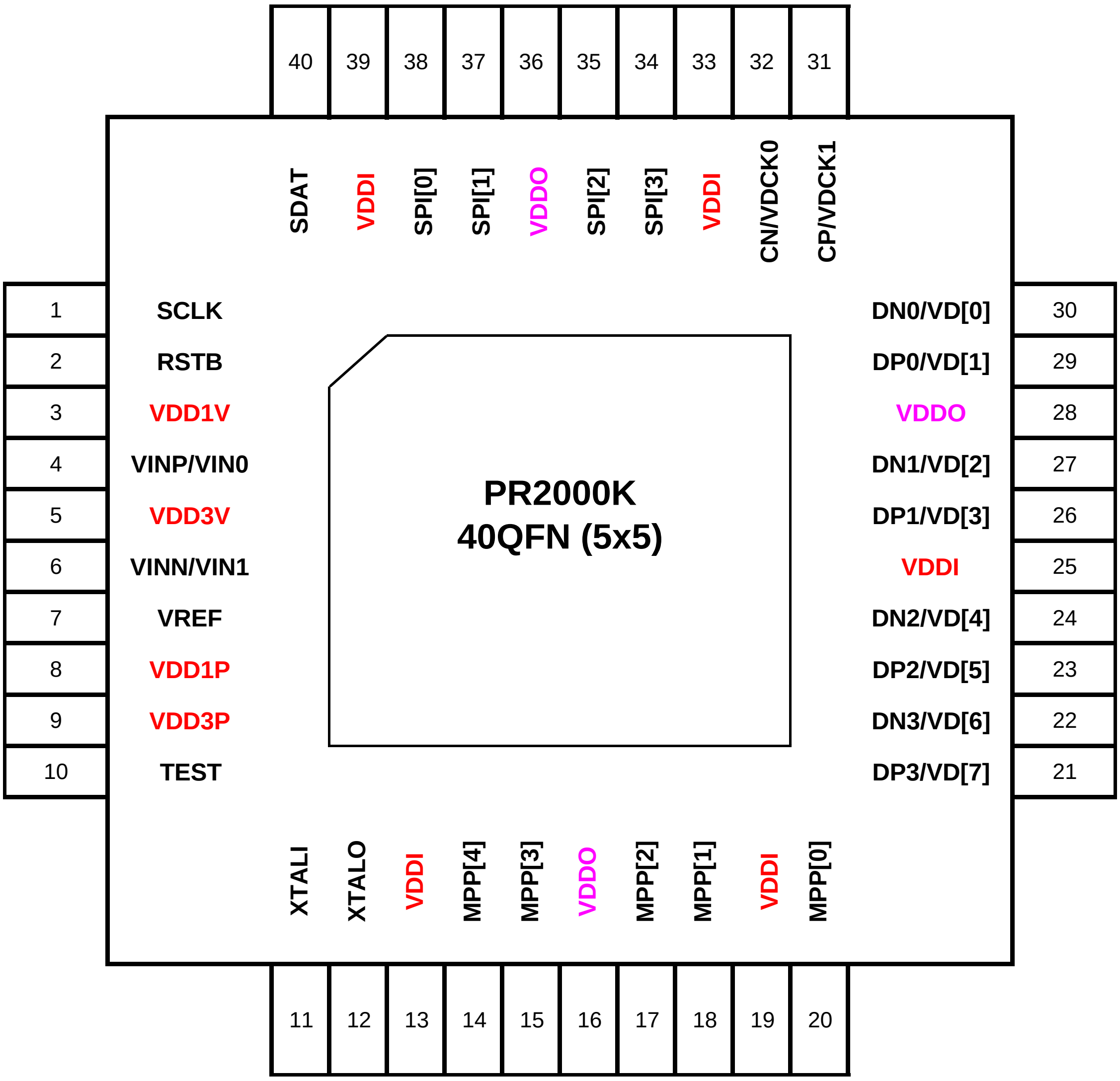

Fig 2. Pin Diagram

2.2. Pin Description

Table 1. Pin Description

Pin Name	Pin Number	Type	Pin Description
Analog Video Interface (3 Pin)			
VINP/VIN0	4	A	Analog Video Differential Positive Input or Single-ended VIN0
VINN/VIN1	6	A	Analog Video Differential Negative Input or Single-ended VIN1
VREF	7	A	Analog Voltage Reference Output
Digital Video Interface (10 Pin)			
CN/VDCK0	32	O	Clock 0 for Digital Video Output / MIPI Clock Negative Output
CP/VDCK1	31	O	Clock 1 for Digital Video Output / MIPI Clock Positive Output
DN0/VD[0]	30	O	Digital Video Output[0] / MIPI Data0 Negative Output
DP0/VD[1]	29	O	Digital Video Output[1] / MIPI Data0 Positive Output
DN1/VD[2]	27	O	Digital Video Output[2] / MIPI Data1 Negative Output
DP1/VD[3]	26	O	Digital Video Output[3] / MIPI Data1 Positive Output
DN2/VD[4]	24	O	Digital Video Output[4] / MIPI Data2 Negative Output
DP2/VD[5]	23	O	Digital Video Output[5] / MIPI Data2 Positive Output
DN3/VD[6]	22	O	Digital Video Output[6] / MIPI Data3 Negative Output
DP3/VD[7]	21	O	Digital Video Output[7] / MIPI Data3 Positive Output
Multi-Purpose Pin Interface (5 Pin)			
MPP[4:0]	14, 15, 17, 18, 20	I/O	Multi-purpose Pin Input/Output [4:0]
SPI Interface (4 Pin)			
SPI[3:0]	34, 35, 37, 38	I/O	SPI Interface Input/Output [3:0]
System Control Interface (6 Pin)			
TEST	10	I	Reserved Pin for TEST
RSTB	2	I	System Reset
XTALI	11	I	Crystal (27MHz) Input
XTALO	12	I/O	Crystal (27MHz) Input / Output
SCLK	1	I	I2C Clock Line
SDAT	40	I/O	I2C Data Line
Power and Ground (13 Pin)			
VDD3V	5	P	3.3V Power for Analog Video
VDD1V	3	P	1.2V Power for Analog Video
VDD3P	9	P	3.3V Power for PLL
VDD1P	8	P	1.2V Power for PLL
VDDI	13, 19, 25, 33, 39	P	1.2V Power for Digital Core
VDDO	16, 28, 36	P	3.3V Power for Digital I/O
VSS	Exposed Pad	G	Ground

3. Functional Description

3.1. Video Input

3.1.1. Cable Equalizer

The PR2000 includes an adaptive cable equalizer that automatically recovers loss resulted from the long transmission of analog HD/SD video signal over Coaxial (3C-2V/RG-59/RG6) or UTP (Unshielded Twisted-Pair, CAT-5/6) cables as shown in Fig 3. The recommended video input application circuits for Coaxial cable and CAT-5/6 are illustrated in the Fig 4 and Fig 5.

Without Cable EQ **With Cable EQ**

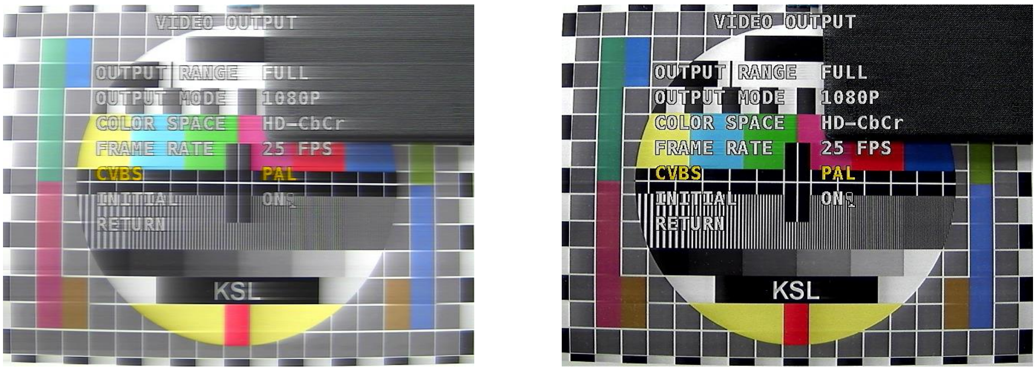

Fig 3. Cable EQ Performance Illustration

Table 2. Transmission Distance for RG6 Coaxial Cable

Cable Type	720p@25/30Hz	720p@50/60Hz	1080p@25/30Hz
RG6 Coaxial	1200m	1000m	1000m

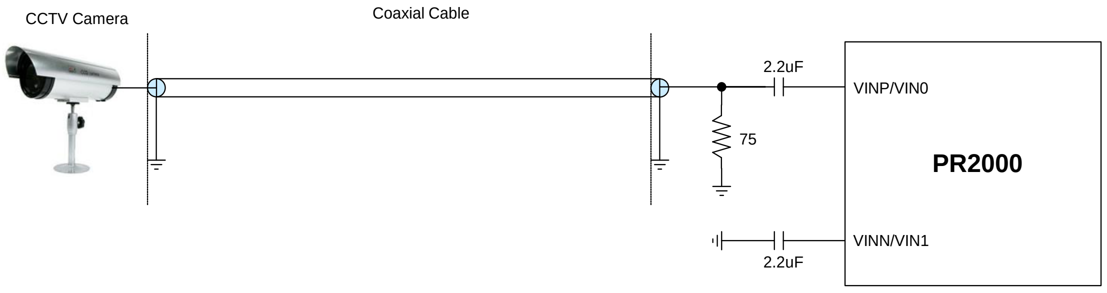

Fig 4. The Recommended Application Circuit for Coaxial Cable

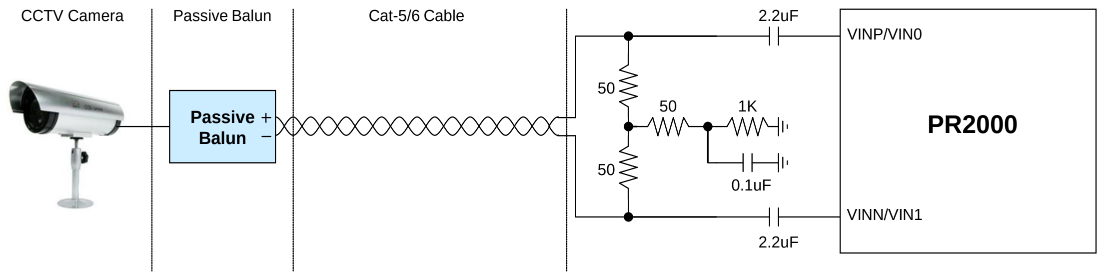

Fig 5. The Recommended Application Circuit for CAT-5/6 Cable

3.1.2. Analog Front End

The analog front end comprises the cable EQ, anti-aliasing filter and ADC to digitize the analog video signal. The analog front end can accept differential video input to improve the noise immunity or two single-ended video inputs with embedded analog MUX switch. The anti-aliasing filters are integrated to provide out-of band noise rejection on the analog video input signal.

3.1.3. Video Decoder

The PR2000 supports all existing HD/SD video standard and all video format (1080p@25/30, 720p@25/30/50/60, 960p@25/30/50/60 and 480i@60/576i@50) with automatic standard and format detection. The adaptive comb filter or band selected filter automatically adjusts its processing mode according to video standard and format with no user intervention required. The PR2000 contains a luminance peaking filter and a chrominance transient improvement (CTI) processor which increase the edge rate on video signal transitions, resulting in a sharper video image. The PR2000 also provides the video control registers such as brightness, contrast, saturation, and hue for the picture adjustment.

3.1.4. Bi-directional Coaxial/UTP PTZ

The PR2000 supports any bidirectional Coaxial/UTP PTZ protocol that transmits the data between a controller and the PTZ (Pan/Tilt/Zoom) camera. The PR2000 can define the H/V location and line width for PTZ protocol with the register PTZ_RX/TX_HST(2x02/22), PTZ_TX_HPST(2x29/2A) and PTZ_RX/TX_LINE_LEN(2x0B/2B). The bit-stream can be comprised of several lines and one line data can be defined via the PTZ_FIFO_WR_DATA (2x11) register. Each bit width can be controlled by the PTZ_RX/TX_FREQ (2x03~2x08/ 2x23~2x28) register. The PTZ_RX/TX data transfer can be programmed easily with IRQ interface in PR2000. After one channel PTZ TX data is programmed and the transfer is done, the PR2000 sends the IRQ data to host, then the host will program the other channel. Likewise, if all predefined quantity of PTZ Rx data is filled in the embedded FIFO, the IRQ data is sent to host, then the host will read the PTZ Rx data from it.

3.1.5. OSG Overlay

The PR2000 supports a graphic overlay layer with 256 Color LUT including 256 Alpha Blending to display a dynamic parking guide line or OSG. The OSG overlay data is compressed with Run-length encoding and saved to external SPI Flash memory.

The PR2000 includes SPI-Tx and Rx to transfer OSG overlay data and 256 color index LUT through two 256-bytes FIFO. In SPI-Rx operation, the PR2000 supports not only single page read transfer mode but also dual page read transfer mode.

3.2. Video Output

The PR2000 supports ITU-R BT.656/1302/1120 format according to the input video format. In case that all video input formats are SD 720H, the video output format can be ITU-R BT.656. But if at least one of SD video input formats is 960H format, the video output format should be ITU-R BT.1302. Likewise, if at least one of video input formats is HD720p or HD1080p, the video output format should be ITU-R BT1120 because multi-channel output clocks should be synchronous. In other words, all video data of multi-channel are synchronous with output clock so that two channels can be multiplexed and only one clock can be used for it. Each clock can be controlled by 16 phase via the MPLL_PHASE_SEL (0xD8) and VDCK_PHASE (0xE3/E4) register. The PR2000 also supports DDR (Dual Data Rate) format so that the maximum data rate can be raised up to 297MHz.

3.2.1. Parallel Output Format

3.2.1.1. One Channel Standard ITU-R BT.656/1302/1120 Format

The video output data is ITU-R BT.656/1302/1120 standard format with 27/36/74.25/148.5MHz. The Fig 6 and Fig 7 show the timing diagram of one channel standard ITU-R BT.656/1302/ 1120 format.

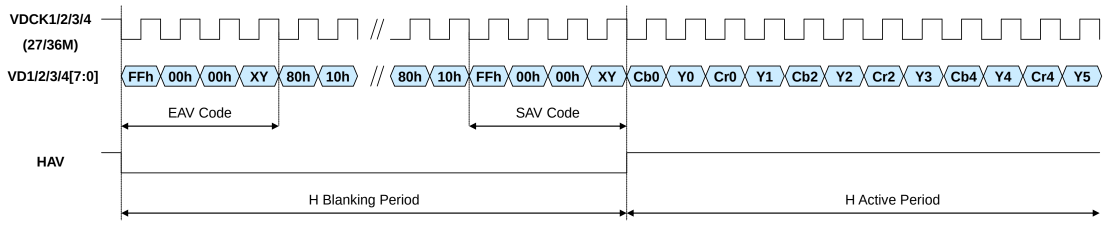

Fig 6. Timing Diagram of One Channel Standard ITU-R BT.656/1302 Format

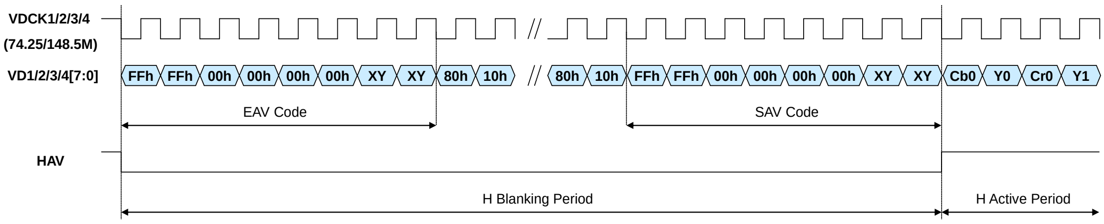

Fig 7. Timing Diagram of One Channel Standard ITU-R BT.1120 Format

3.2.1.2. Two Channel Multiplexed ITU-R BT.656/1302/1120 Format

The video output data from two video channels can be multiplexed at 54/72/74.25/148.5/297MHz. The two channel multiplexed format is available only for cascaded connection mode. (The cascaded connection will be described in the next section.) The video output data is triggered at clock rising or falling edge for SDR (Single Data Rate) mode, but it is triggered at both rising and falling edge for DDR (Dual Data Rate) mode. The video output of each channel is compatible with ITU-R BT.656/1302/1120 format. The Fig 8 and Fig 9 show the timing diagram of two channel multiplexed format for SDR and DDR mode.

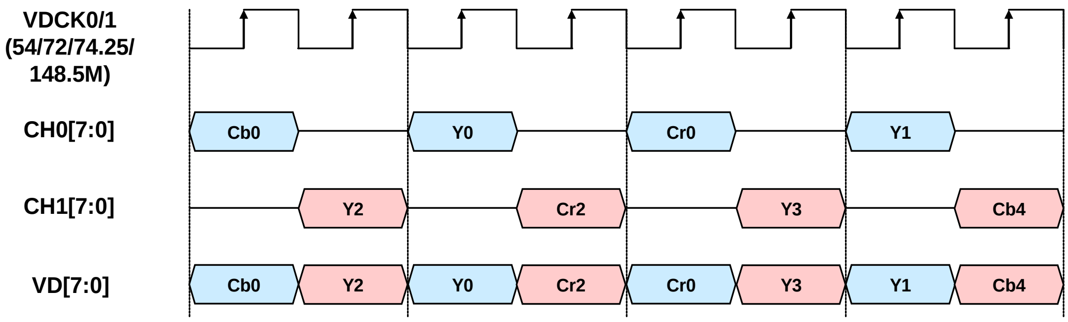

Fig 8. Timing Diagram of Two Channel Multiplexed Format for SDR Mode

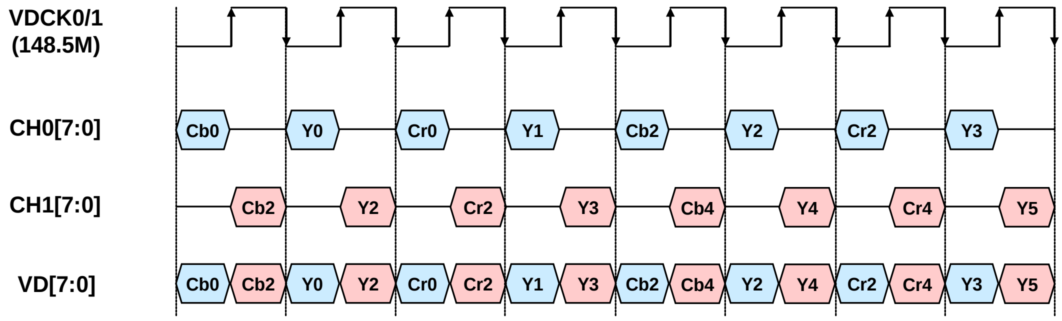

Fig 9. Timing Diagram of Two Channel Multiplexed Format for DDR Mode

3.2.1.3. Channel ID Insertion in SAV/EAV Code

In the multi-channel multiplexed mode for cascaded application, the channel ID can be inserted in 4 LSB of SAV/EAV code in ITU-R BT.656/1120 format as shown in the Table 3 and Table 4.

Table 3. Channel ID Insertion in SAV/EAV Code for 2 Channels in ITU-R BT.656 Format

Condition			FVH Value			SAV/EAV Code Sequence for Four CH Format				
Field	V time	H time	F	V	H	1st	2nd	3rd	4th	
									CH1	CH2
Even	Blank	EAV	1	1	1	FFh	00h	00h	F0h	F1h
		SAV			0				E0h	E1h
	Active	EAV		0	1				D0h	D1h
		SAV			0				C0h	C1h
Odd	Blank	EAV	0	1	1				B0h	B1h
		SAV			0				A0h	A1h
	Active	EAV		0	1				90h	91h
		SAV			0				80h	81h

Table 4. Channel ID Insertion in SAV/EAV Code for 2 Channels in ITU-R BT.1120 Format

Condition		VH Value		SAV/EAV Code Sequence for Four CH Format				
V time	H time	V	H	1st 2nd	3rd 4th	5th 6th	7th/8th	
							CH1	CH2
Blank	EAV	1	1	FFh	00h	00h	B0h	B1h
	SAV		0				A0h	A1h
Active	EAV	0	1				90h	91h
	SAV		0				80h	81h

3.2.2. MIPI Output Format

The PR2000 supports a MIPI interface compliant with MIPI CSI2 V1.00 standard and DPHY V1.00.00 standard with 1 clock lane and 4 data lane. The max data rate of MIPI data lane is up to 297Mbps in HS transmission with YUV 422-8bit format. The four data lane should be used for 1920x1080@25/30Hz format and two data lane can be used for 1280x720@25/30Hz format.

During MIPI Tx operation, there are two lane states such as Low Power (LP) state and High Speed (HS) state. The HS Tx always drives the lane differentially so that it results in two possible HS lane states such as differential-0 and differential-1. The LP Tx drives two lines of a lane independently with single-ended termination so that it results in four possible LP lane states that are used for Control Mode and Escape Mode. The HS data transmission is used to transfer data in burst mode. It starts from and ends with a stop state (LP-11) of LP Control Mode. The special Escape Mode can only be entered via a request within Control Mode. The data lane shall always exit Escape Mode and return to Control Mode with stop state. If not in HS state or Escape Mode, the data lane shall stay in Control mode.

Table 5. Lane State Description of MIPI Transmission

State Code	Line Voltage Levels		High-Speed	Low-Power	
	DP-Line	DN-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A	N/A
HS-1	HS High	HS Low	Differential-1	N/A	N/A
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A

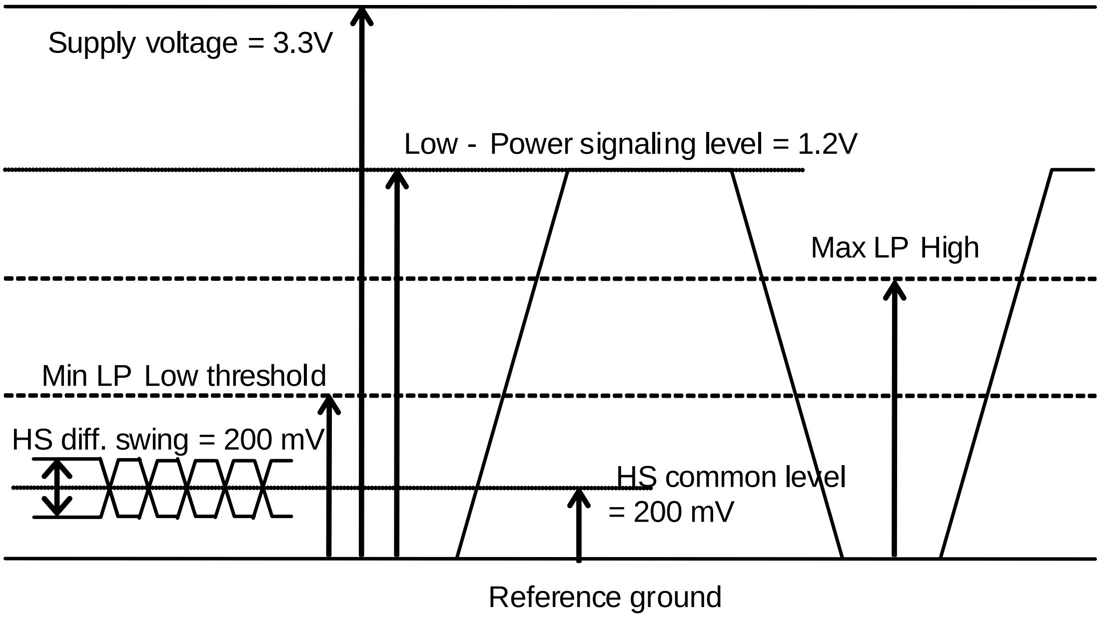

Fig 10. MIPI Signal Levels for HS and LP State

The Low Level Protocol (LLP) is a byte oriented, packet based protocol that supports the transport of image data using Short and Long packet formats. After exiting from the low power state, the Start of Transmission (ST) sequence indicates the start of the packet and the End of Transmission (ET) sequence indicates the end of the packet.

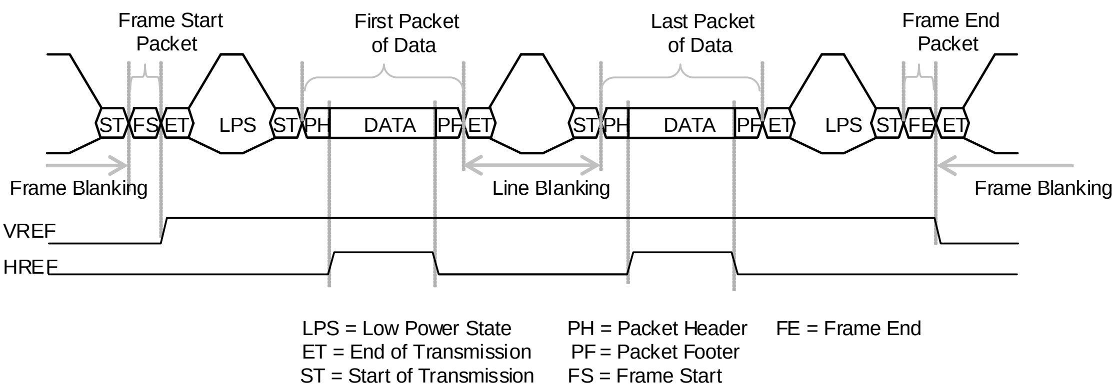

Fig 11. MIPI Low Power Protocol

The PR2000 supports two kinds of Short packet format for frame synchronization such as Frame Start (FS) packet and Frame End (FE) packet. Each image frame shall begin with a FS packet containing the Frame Start Code. The FS Packet shall be followed by one or more long packets containing image data. Each image frame shall end with the FE packet containing the Frame End Code.

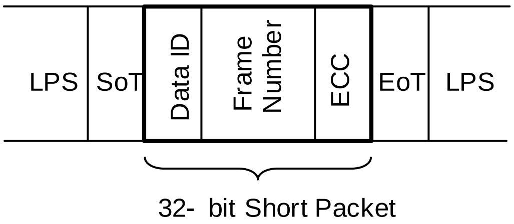

Fig 12. MIPI Short Packet Structure

A Long packet shall consist of 3 elements such as a 32-bit Packet Header (PH), an application Data Payload with a variable number of 8-bit words and a 16-bit Packet Footer (PF).

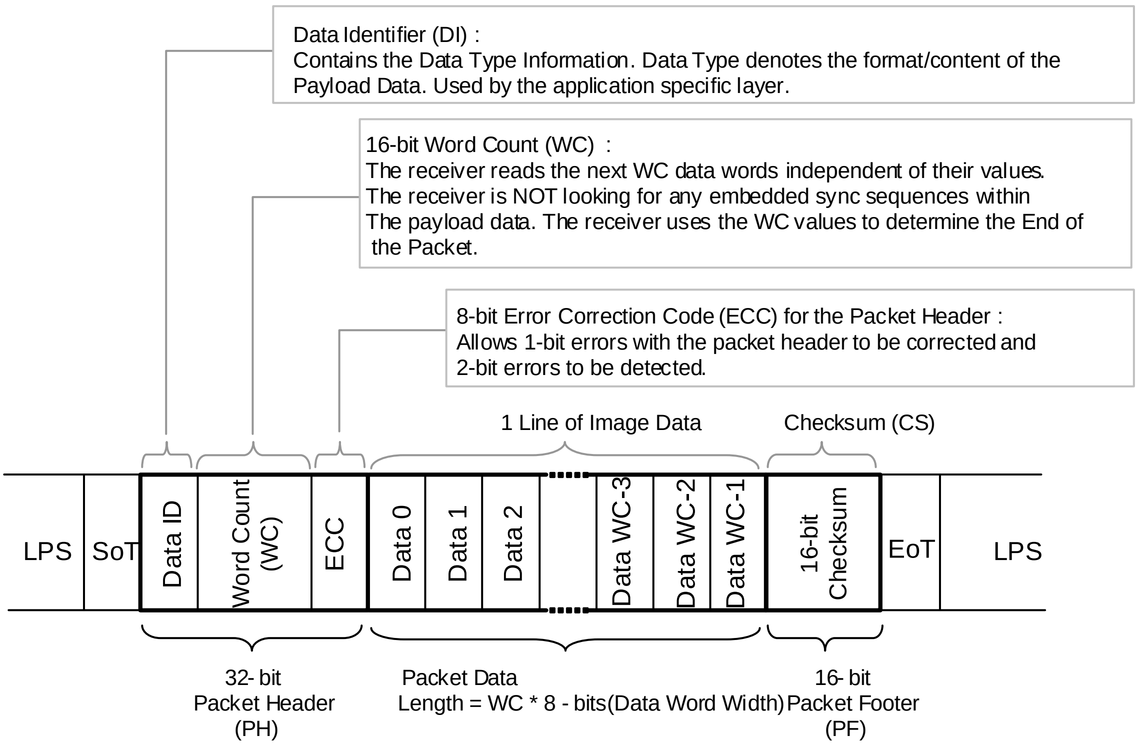

Fig 13. MIPI Long Packet Structure

The Fig 14 shows the detailed Data Payload structure of YUV422 8bit frame format in the Long packet.

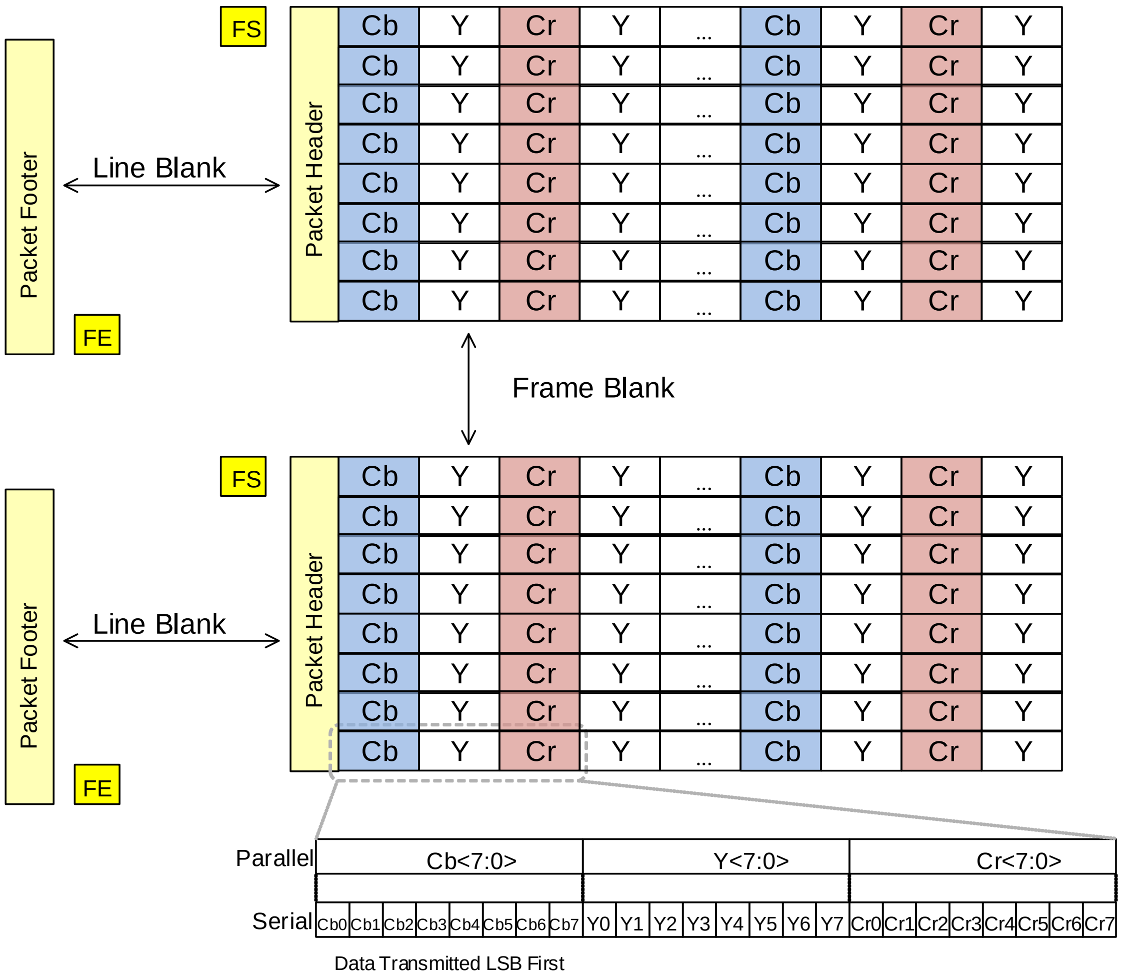

Fig 14. YUV422 8 Bit Frame Format for MIPI Transfer

The Fig 15 and Fig 16 describe the MIPI data lane transmission order for 4 lane and 2 lane mode.

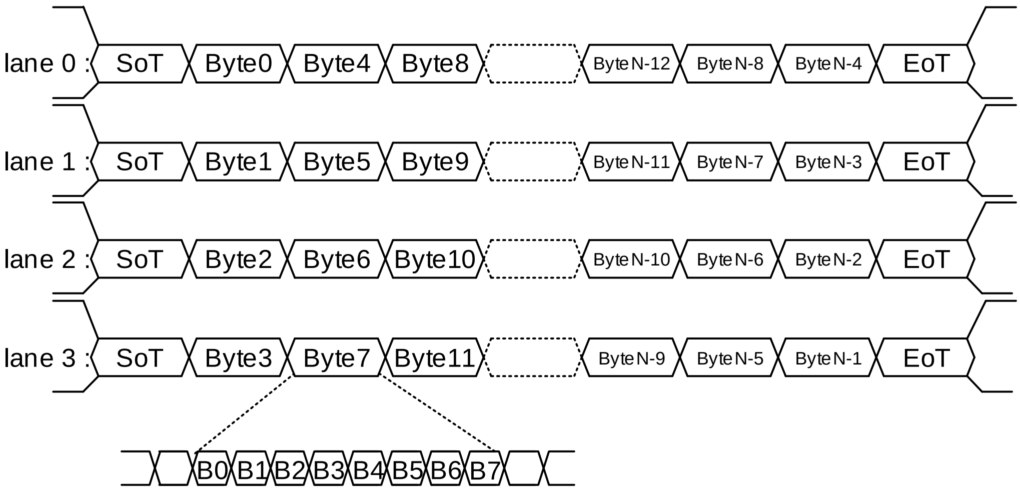

Fig 15. MIPI Data Lane Transmission Order for 4 Lane Mode

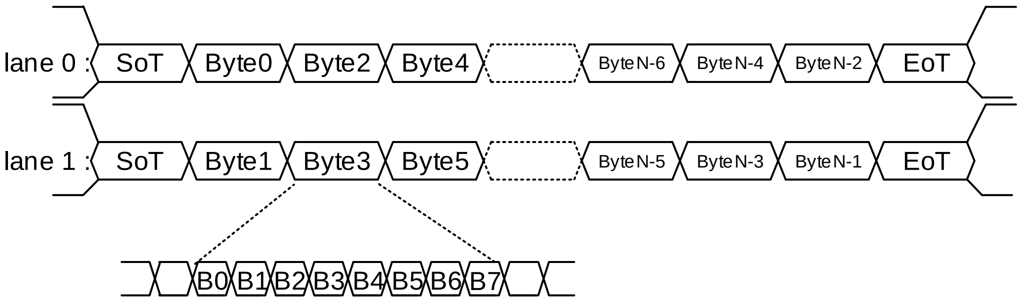

Fig 16. MIPI Data Lane Transmission Order for 2 Lane Mode

3.2.3. Chip Cascade

The PR2000 provides a multi-chip cascaded operation supporting channel multiplexed output mode to reduce the interface pin count with back-end chipset only in case of parallel output mode. The multi-chip cascaded connection is illustrated in Fig 17.

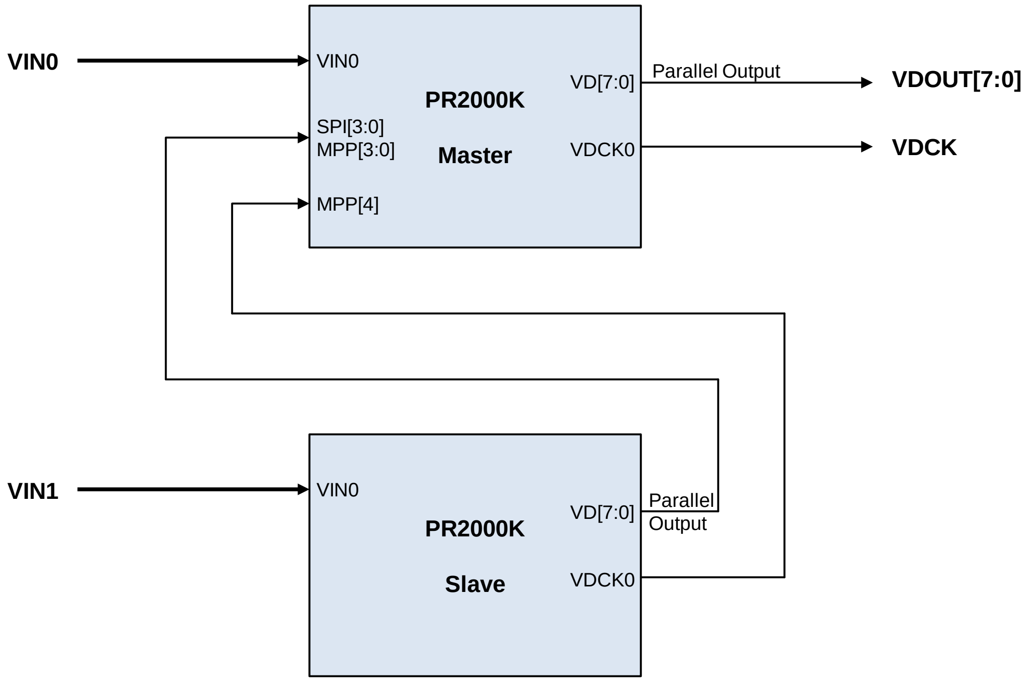

Fig 17. Cascade Connection for Multi-chip Application

3.3. Host Interface

3.3.1. I2C Interface

The PR2000 supports serial interface consisting of two signals, serial data line SDAT (Pin 40) and clock line SCLK (Pin 1) that should be connected to VDDO via pull up resistors. The PR2000 also provides auto-increment mode of sub-address for multi-byte serial read/write operation. The MPP[4:3] (Pin 14,15) are used to select the slave address which are 7'h5C for MPP[4:3] = 0, 7'h5D for MPP[4:3] = 1, 7'h5E for MPP[4:3] = 2, and 7'h5F for MPP[4:3] = 3 when SADDR_LAT_EN (0xFF bit[7]) = "1". The maximum data transfer rate on the bus is up to 400kbit/s. The detailed I2C protocol is shown in the following Fig 18.

I2C Slave Address							R/W
1	0	1	1	1	MPP[4]	MPP[3]	1/0

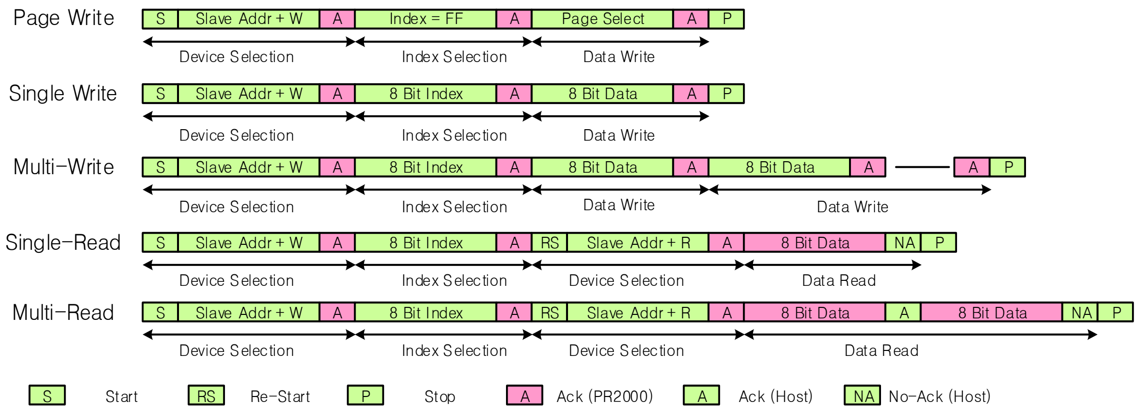

Fig 18. Protocol of I2C Interface

The PR2000 has total 3 page x 256 register map in it so that the page selection register HOST_RW_PAGE (0xFF) should be accessed before any register is programmed. The brief page descriptions are shown in the following Table 6.

Table 6. Page Selection Register Description

Index Page Number	Description
Page 0	Video Format + IRQ + PAD I/O Control
Page 1	Video Decoder Control
Page 2	PTZ / SPI / OSG Control

3.3.2. GPIO Interface

The MPP[4:0], SPI[3:0] pin can be used as GPIO pins for general purpose such as monitoring input, programming output pin and receiving interrupt source. Each GPIO pin can be enabled via the corresponding registers as the following Table 7. The data direction of GPIO can be controlled by the register GPIO_IOB (0xA0 ~ 0xA1) that is set to “1” for input and “0” for output. The output value of GPIO pin can be programmed via the GPIO_OUT (0xA2 ~ A3) register. The input value of GPIO pin can be read via the STATUS_GPIO (0x99 ~ 9A) register.

Table 7. Pins and Registers of GPIO

GPIO	Pin Name	Related Register for GPIO
GPIO[0]	MPP[0]	GPIO_EXT_MD[0] (0xA5) = “0”, GPIO_MPP0_MD (0xA6) = “1”
GPIO[1]	MPP[1]	GPIO_EXT_MD[1] (0xA5) = “0”, GPIO_MPP1_MD (0xA6) = “1”
GPIO[2]	MPP[2]	GPIO_EXT_MD[2] (0xA5) = “0”, GPIO_MPP2_MD (0xA7) = “1”
GPIO[3]	MPP[3]	GPIO_EXT_MD[3] (0xA5) = “0”, GPIO_MPP3_MD (0xA7) = “1”
GPIO[4]	MPP[4]	GPIO_EXT_MD[4] (0xA5) = “0”, GPIO_MPP4_MD (0xA8) = “1”
GPIO[5]	SPI[0]	GPIO_EXT_MD[5] (0xA5) = “0”,
GPIO[6]	SPI[1]	GPIO_EXT_MD[6] (0xA5) = “0”,
GPIO[7]	SPI[2]	GPIO_EXT_MD[7] (0xA5) = “0”,
GPIO[8]	SPI[3]	GPIO_EXT_MD[8] (0xA4) = “0”,

The MPP[4:0] and SPI[3:0] pin configuration is described as the following table.

Table 8. MPP[4:0] Pin Output Matrix

Pin Name	GPIO_ EXT_MD	GPIO_ MPP_MD	MPP_SEL	GPIO_ IRQ_MD	Type	Pin Description
MPP[0]	1	x	x	1	O	IRQ Output
	1	x	x	0	O	PTZ Output
	0	1	x	x	I/O	GPIO[0] output
	0	0	0	x	I/O	H Sync Output
	0	0	1	x	I/O	V Sync Output
	0	0	2	x	I/O	F Sync Output
MPP[1]	1	x	x		O	PTZ Output
	0	1	x		I/O	GPIO[1] output
	0	0	0		I/O	H Sync Output
	0	0	1		I/O	V Sync Output
	0	0	2		I/O	F Sync Output
MPP[2]	1	x	x		O	PTZ Output
	0	1	x		I/O	GPIO[2] output
	0	0	0		I/O	H Sync Output
	0	0	1		I/O	V Sync Output
	0	0	2		I/O	F Sync Output
MPP[3]	1	x	x		O	PTZ Output
	0	1	x		I/O	GPIO[3] output
	0	0	0		I/O	H Sync Output
	0	0	1		I/O	V Sync Output
	0	0	2		I/O	F Sync Output
MPP[4]	1	x	x		O	PTZ Output
	0	1	x		I/O	GPIO[4] output
	0	0	0		I/O	H Sync Output
	0	0	1		I/O	V Sync Output
	0	0	2		I/O	F Sync Output

Table 9. SPI[3:0] Pin Output Matrix

Pin Name	GPIO_ EXT_MD	Type	Pin Description
SPI[0]	1	I/O	SPI_IO[0] or SPI_MOSI
	0	I/O	GPIO[5] output
SPI[1]	1	I/O	SPI_IO[1] or SPI_MISO
	0	I/O	GPIO[6] output
SPI[2]	1	O	SPI_SCK Output
	0	I/O	GPIO[7] output
SPI[3]	1	O	SPI_SS Output
	0	I/O	GPIO[8] output

Table 10. SPI[3:0], MPP[4:0] Pin Input Matrix

Pin Name	Type	Pin Description
MPP[0]	I	GPIO[0]
	I	Cascade Video data Bit[0]
MPP[1]	I	GPIO[1]
	I	Cascade Video data Bit[1]
MPP[2]	I	GPIO[2]
	I	Cascade Video data Bit[2]
MPP[3]	I	GPIO[3]
	I	Cascade Video data Bit[3]
	I	I2C Slave Sub-address Bit[0]
MPP[4]	I	GPIO[4]
	I	Cascade Video Clock Input
	I	I2C Slave Sub-address Bit[1]
SPI[0]	I	GPIO[5]
	I	Cascade Video data Bit[4]
	I	SPI Data Bit[0]
SPI[1]	I	GPIO[6]
	I	Cascade Video data Bit[5]
	I	SPI Data Bit[1]
SPI[2]	I	GPIO[7]
	I	Cascade Video data Bit[6]
SPI[3]	I	GPIO[8]
	I	Cascade Video data Bit[7]

3.3.3. Interrupt Interface

The PR2000 requests the interrupt to host through the IRQ pin. The polarity of IRQ pin is determined by the IRQOUT_POL (0x80) register. The interrupt is repeated periodically via the IRQOUT_RPT (0x80) register until the host receives interrupt correctly. The PR2000 requests the interrupt to host when the event of video format change, video loss, PTZ and GPIO transition happens. Each event can be activated via the IRQENA (0x90 ~ 92) register. When host receives the interrupt from PR2000, the host should read the IRQCLR (0x94 ~ 96) register to find out which event requests interrupt service and then write “1” into corresponding bit of the IRQCLR register to clear the interrupt request because the PR2000 maintains the interrupt status until it is cleared. Additionally, the host can read the current state of each event through the STATUS (0x98 ~ 9A) register. The event list of interrupt request is described in the following Table 11.

Table 11. Event List of Interrupt Request

Event	Bit Size	Status		Interrupt Mode	
		0	1	Level	Edge
Video Loss	1	Normal	Video Loss	High/Low	Both
Video Format	1	Match	Format Error	High/Low	Both
PTZ Tx Done	1	Normal	Tx Busy	X	Falling
PTZ Tx Error	2	Normal	Tx Error	High	X
PTZ Rx Done	1	Normal	Rx Busy	X	Falling
PTZ Rx Error	4	Normal	Rx Error	High	X
GPIO	9	0	1	High/Low	Rising/Falling/Both
Timer IRQ	2	0	Timer Period	High	X

3.4. PLL

An analog clock multiplier PLL is used to generate a clock of digital video output from an external 27MHz crystal or external oscillator clock input. A crystal can be connected across terminals Pin 11(XTALI) and Pin 12(XTALO), or an external oscillator clock input can be connected to Pin 11 (XTALI). The following Fig 19 and Fig 20 show the reference clock configurations.

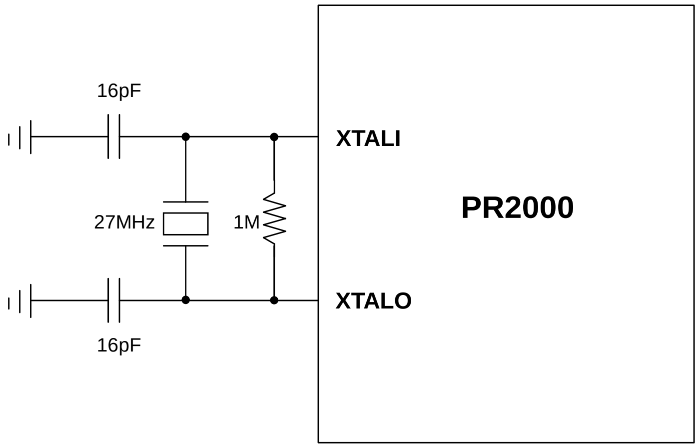

Fig 19. Recommended Crystal Oscillating Circuit

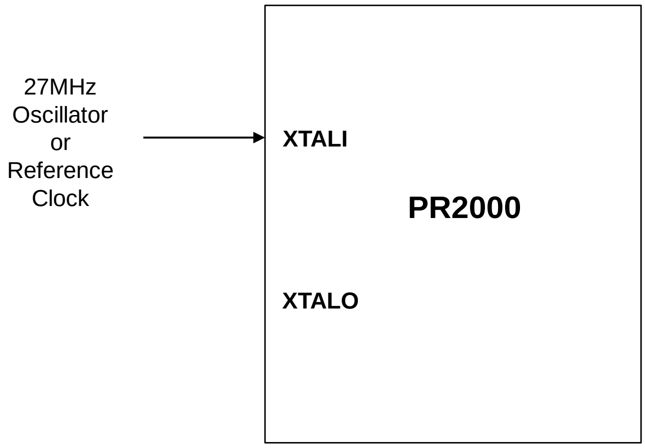

Fig 20. Recommended External Oscillator Clock Input Circuit

4. Register Information

4.1. Register Map

4.1.1. PAGE 0 (Video EQ and IRQ)

Note : * Read Only Register

<table>
<tr><th>ADD</th><th>MNEMONIC</th><th>BIT7</th><th>BIT6</th><th>BIT5</th><th>BIT4</th><th>BIT3</th><th>BIT2</th><th>BIT1</th><th>BIT0</th></tr>
<tr><td>0x00*</td><td>VID_STATUS_0</td><td colspan="2">DET_IFMT_STD</td><td colspan="2">DET_IFMT_REF</td><td>DET_VIDEO</td><td colspan="3">DET_IFMT_RES</td></tr>
<tr><td>0x01*</td><td>VID_STATUS_1</td><td>LOCK_STD</td><td>LOCK_GAIN</td><td>LOCK_CLAMP</td><td></td><td>LOCK_HPLL</td><td>LOCK_C_FINE</td><td>LOCK_CHROMA</td><td>DET_CHROMA</td></tr>
<tr><td>0x02*</td><td>VID_STATUS_2</td><td></td><td></td><td>DET_STD_HDT2</td><td>DET_STD_HDT1</td><td>DET_STD_HDT0</td><td>DET_STD_HDA</td><td>DET_STD_CVI</td><td>DET_STD_PVI</td></tr>
<tr><td>~</td><td>RESERVED</td><td colspan="8">RESERVED</td></tr>
<tr><td>0x10</td><td>MAN_IFMT</td><td colspan="2">MAN_IFMT_STD</td><td colspan="2">MAN_IFMT_REF</td><td>MAN_IFMT_
STD_HDT_N</td><td colspan="3">MAN_IFMT_RES</td></tr>
<tr><td>0x11</td><td>MAN_IFMT_EN0</td><td></td><td colspan="3">VADC_GAIN_SEL</td><td colspan="4">MAN_IFMT_EN</td></tr>
<tr><td>0x12</td><td>MAN_EQ_AC_GN</td><td>DET_SIGNAL</td><td></td><td></td><td colspan="5">MAN_EQ_GAIN_MD</td></tr>
<tr><td>0x13</td><td>VADC_EQ_BAND</td><td></td><td></td><td colspan="2">MAN_EQ_LOW_BAND</td><td></td><td colspan="3">MAN_EQ_HIGH_BAND</td></tr>
<tr><td>0x14</td><td>VADC_CTRL</td><td colspan="6">RESERVED</td><td colspan="2">VADC_IN_SEL</td></tr>
<tr><td>~</td><td>RESERVED</td><td colspan="8">RESERVED</td></tr>
<tr><td>0x40</td><td>MIPI_CTRL</td><td></td><td>MIPI_EN</td><td></td><td></td><td>MIPI_ULP_DATA</td><td>MIPI_ULP_CLK</td><td></td><td>MIPI_STM</td></tr>
<tr><td>0x41</td><td>MIPI_CLK_CTRL</td><td colspan="4">MIPI_CK_CTRL</td><td>MIPI_HSCLK_E</td><td>MIPI_HSCLK_O</td><td></td><td></td></tr>
<tr><td>0x42</td><td>MIPI_D01_CTRL</td><td colspan="4">MIPI_D0_CTRL</td><td colspan="4">MIPI_D1_CTRL</td></tr>
<tr><td>0x43</td><td>MIPI_D23_CTRL</td><td colspan="4">MIPI_D2_CTRL</td><td colspan="4">MIPI_D3_CTRL</td></tr>
</table>

ADD	MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x44	DPHY_ISEL_TRIM						DPHY_ISEL_TRIM		
0x45	DPHY_V12_TRIM		DPHY_V12_TRIM				DPHY_V04_TRIM		
0x46	DPHY_V03_TRIM		DPHY_V03_TRIM				DPHY_V01_TRIM		
0x47	MIPI_IN_MD	MIPI_IN_EN		MIPI_LANE		MIPI_FRM_MD		MIPI_IN_MD	
0x48	MIPI_PKT_SIZE_L	MIPI_PKT_SIZE[07:00]							
0x49	MIPI_PKT_SIZE_M	MIPI_PKT_SIZE[15:08]							
0x4A	MIPI_STP1_L	MIPI_STP1[07:00]							
0x4B	MIPI_STP1_M	MIPI_STP1[15:08]							
0x4C	MIPI_STP2_L	MIPI_STP2[07:00]							
0x4D	MIPI_STP2_M	MIPI_STP2[15:08]							
0x4E	MIPI_PD_CTRL	DPHY_VCTRL_INIT	DPHY_FLD	reg_mipi_pd[5:0]					
Empty		Empty							
0x50	MIPI_DATA_ID	MIPI_DATA_ID							
0x51	MIPI_T_LPX	MIPI_T_LPX							
0x52	MIPI_T_CLK_PREP	MIPI_T_CLK_PREP							
0x53	MIPI_T_HS_PREP	MIPI_T_HS_PREP							
0x54	MIPI_T_HS_ZERO	MIPI_T_HS_ZERO							
0x55	MIPI_T_HS_TRAIL	MIPI_T_HS_TRAIL							
0x56	MIPI_T_CLK_ZERO	MIPI_T_CLK_ZERO							
0x57	MIPI_T_CLK_TRAIL	MIPI_T_CLK_TRAIL							
0x58	MIPI_T_CLK_PRE	MIPI_T_CLK_PRE							

ADD	MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x59	MIPI_T_CLK_POST	MIPI_T_CLK_POST							
0x5A	MIPI_T_WAKEUP	MIPI_T_WAKEUP							
0x5B	MIPI_T_HS_EXIT	MIPI_T_HS_EXIT							
0x5C	MIPI_T_ESC_CMD	MIPI_T_ESC_CMD							
0x5D	MIPI_MON_SEL					MIPI_MON_SEL			
0x5E*	MIPI_MONITOR	mipi_monitor_data* (read only)							
Empty		Empty							
0x70	DUMMY_REG0	DUMMY_RW_REG0							
0x71	DUMMY_REG1	DUMMY_RW_REG1							
0x72	DUMMY_REG2	DUMMY_RW_REG2							
0x73	DUMMY_REG3	DUMMY_RW_REG3							
0x74	DUMMY_REG4	DUMMY_RW_REG4							
0x75	DUMMY_REG5	DUMMY_RW_REG5							
0x76	DUMMY_REG6	DUMMY_RW_REG6							
0x77	DUMMY_REG7	DUMMY_RW_REG7							
~	RESERVED	RESERVED							
0x80	IRQ_CTRL	IRQOUT_EN		IRQOUT_POL	IRQOUT_RPT		SYNC_GPIO	SYNC_FUNC	SYNC_PTZ
0x81	IRQ_SYNC_PERIOD	IRQ_SYNC_PERIOD							
0x82	IRQ_TIMER_PERIOD	IRQ_TIMER0_PERIOD							
0x83	IRQ_EVENT_STATE			STATUS_TIMER	STATUS_GPIO	STATUS_SPI	STATUS_VFD	STATUS_NOVID	STATUS_PTZ
0x84	IRQ_NOVID_MD	IRQ_VFD_PEND	IRQ_NOVID_PEND	IRQ_VFD_MD	IRQ_NOVID_MD				IRQ_GPIO_MD[8]

ADD	MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x85	IRQ_GPIO_MD	IRQ_GPIO_MD[7:0]							
0x86	IRQ_NOVID_LV			IRQ_VFD_LV	IRQ_NOVID_LV				IRQ_GPIO_LV[8]
0x87	IRQ_GPIO_LV	IRQ_GPIO_LV[7:0]							
0x88	IRQ_GPIO_BOTH								IRQ_GPIO_BOTH[8]
0x89	IRQ_GPIO_BOTH	IRQ_GPIO_BOTH[7:0]							
0x8A	IRQ_TIMER_PERIOD	IRQ_TIMER1_PERIOD							
~	RESERVED	RESERVED							
0x90	IRQENA_0	IRQENA_PTZ							
0x91	IRQENA_1	IRQENA_TIMER1	IRQENA_TIMER0	IRQENA_VFD	IRQENA_NOVID	IRQENA_SPI			IRQENA_GPIO[8]
0x92	IRQENA_2	IRQENA_GPIO[7:0]							
~	RESERVED	RESERVED							
0x94	IRQCLR_0	IRQENA_PTZ							
0x95	IRQCLR_1	IRQCLR_TIMER1	IRQCLR_TIMER0	IRQCLR_VFD	IRQCLR_NOVID	IRQCLR_SPI			IRQCLR_GPIO[8]
0x96	IRQCLR_2	IRQCLR_GPIO[7:0]							
~	RESERVED	RESERVED							
0x98	IRQ_STATUS_0	STATUS_PTZ							
0x99	IRQ_STATUS_1	STATUS_TIMER1	STATUS_TIMER0	STATUS_VFD	STATUS_NOVID	STATUS_SPI			STATUS_GPIO[8]
0x9A	IRQ_STATUS_2	STATUS_GPIO[7:0]							
~	RESERVED	RESERVED							
0xA0	GPIO_IOB0								GPIO_IOB[8]
0xA1	GPIO_IOB1	GPIO_IOB[7:0]							

ADD	MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0xA2	GPIO_OUT0								GPIO_OUT[8]
0XA3	GPIO_OUT1	GPIO_OUT[7:0]							
0xA4	GPIO_EXT_MD0	TST_MPP_MD = 0			MPP0_IRQ_MD				GPIO_EXT_MD[8]
0xA5	GPIO_EXT_MD1	GPIO_EXT_MD[7:0]							
0xA6	MPP01_SEL	GPIO_MPP1_MD	MPP1_POL	MPP1_SEL		GPIO_MPP0_MD	MPP0_POL	MPP0_SEL	
0xA7	MPP23_SEL	GPIO_MPP3_MD	MPP3_POL	MPP3_SEL		GPIO_MPP2_MD	MPP2_POL	MPP2_SEL	
0xA8	MPP4_SEL					GPIO_MPP4_MD	MPP4_POL	MPP4_SEL	
~	RESERVED	RESERVED							
0xD2	FPLL_CON			FPLL_MAIN_CNT					
~	RESERVED	RESERVED							
0xD8	MPLL_CON0					MPLL_PHASE_SEL			
0xDA	MPLL_CON1			MPLL_MAIN_CNT					
~	RESERVED	RESERVED							
0xE0	LATCHEN_CON	VDEC_CLK_PWDN	VOUT_CLK_PWDN	MIPI_CLK_PWDN	CC_CLK_PWDN	LATCH_EN_CON			
0xE1	OUT_FMT	OUTFMT_BT656	OUTFMT_YC _INV	OUTFMT_RATE			CH_MUX_MD	CH_SEL_B	CH_SEL_A
0xE2	CHID_NUM	CKOUT_2X_MD				OUTFMT_HAV_ VBLK	OUTFMT_SYNC_ BYP	CHID_NUM	
0xE3	VDCK1_PHASE			VDCK1_PHASE					
0xE4	VDCK0_PHASE			VDCK0_PHASE					
0xE5	MIPI_DCLK_PHASE					MIPI_DCLK_PHASE			
0xE6	MIPI_ICLK_PHASE					MIPI_ICLK_PHASE			
~	RESERVED	RESERVED							

ADD	MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0xE8	PAR_IN_EN_M							PAR_IN_EN[9:8]	
0xE9	PAR_IN_EN_L	PAR_IN_EN[7:0]							
0xEA	PAR_OUT_EN_M							PAR_OUT_EN[9:8]	
0xEB	PAR_OUT_EN_L	PAR_OUT_EN[7:0]							
~	RESERVED	RESERVED							
0xF0	PAD_DIG_CTL						DIG_SMT_EN	DIG_DRV_SEL	
0xF1	PAD_MPP_CTL		SPI_SMT_EN	SPI_DRV_SEL			MPP_SMT_EN	MPP_DRV_SEL	
0xF2	PAD_VD_CTL		VD_SMT_EN	VD_DRV_SEL			VDCK_SMT_EN	VDCK_DRV_SEL	
~	RESERVED	RESERVED							
0xF8	SOFT_RESET	0	MPLL_RST	FPLL_RST	MIPI_RST	SPI_RST	OSG_RST	PTZ_RST	DEC_RST
~	RESERVED	RESERVED							
0xFC	CHIP_ID_MSB	0	0	1	0	0	0	0	0
0xFD	CHIP_ID_LSB	0	0	0	0	0	0	0	0
0xFE	REV_ID	REV_ID							
?xFF *	PAGE_SEL	SADDR_LATEN	0	0	0	0	0	HOST_RW_PAGE[1:0]	

4.1.2. PAGE 1 (Video Decoder Channel)

ADD	MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1x00	VID_CON	AGCEN0	AUTO_BGND	PEAKEN		PEAKREF		BGND_MD	
1x01 ~1x10	RESERVED	RESERVED							
1x11	HDELAY_MSB0	VDELAY0[10:8]			HDELAY0[12:8]				
1x12	HACTIVE_MSB	VACTIVE0[10:8]			HACTIVE0[12:8]				
1x13	HDELAY_LSB0	HDELAY0[7:0]							
1x14	HACTIVE_LSB0	HACTIVE0[7:0]							
1x15	VDELAY0	VDELAY0[7:0]							
1x16	VACTIVE0	VACTIVE0[7:0]							
1x1D	HSCL_ACTIVE_MSB0	CBP_DELAY[9:8]			HSCL_ACTIVE[12:8]				
1x1E	RESERVED	RESERVED							
1x1F	HSCL_ACTIVE_LSB0	HSCL_ACTIVE[7:0]							
1x20	CONT	CONT							
1x21	BRGT	BRGT							
1x22	SAT	SAT							
1x23	HUE	HUE							
1x24 ~ 1x28	RESERVED	RESERVED							
1x29	DOWN_HSCL_MSB0	DOWN_HSCL0[15:8]							
1x2A	DOWN_HSCL_LSB0	DOWN_HSCL0[7:0]							
1x2B ~ 1x36	RESERVED	RESERVED							

ADD	MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1x37	HD_Y_NOTCH_MD	COMB_FLT_EN0							
1x38	RESERVED	RESERVED							
1x39	Y_DYN_PEAK_GN	MAN_NOVID[1:0]			HPEAK_MD	HPEAK_GAIN			
1x3A	HD_Y_LPF_MD	NR_EN			YLPF_MD				
1x3B ~ 1x3C	RESERVED	RESERVED							
1x3D	CORE_CON			CTI_CORE		C_CORE		HPEAK_CORE	
1x3E	MAN_CLPF_MD	MAN_CKIL				CLPF_MD			
1x3F	HD_CTI_CON				CTI_MD	CTI_GAIN			
1x40	PAL_COMP_EN	PAL_COMP_EN							
1x41 ~ 1x4C	RESERVED	RESERVED							
1x4D	YC_DELAY		C_DELAY			Y_DELAY			
1x4E	HD_HALF_MD_0	MAN_VIN_FMT						SD_720H_MD	HD_HALF_MD
1x4F	OUTFMT_CON0	BT1120_LIM		VIN_BT656_MD	OSG_DIS_EN	CHID_EN		NOVID_BT1120	
1x50	HD_CSC_MD	HD_CSC_MD							
1x50 ~ 1x54	RESERVED	RESERVED							
1x55	PTZ_SLICE_LVL	PTZ_SLICE_LEVEL							
1x56 ~ 1x7F	RESERVED	RESERVED							
1x80~1xBA	RESERVED	RESERVED							
1xBB	EXT_SYNC_CON			VS_EXT_MD	SYNC_FLD_EN	MIPI_VAV_TRG_MD		MIPI_VAV_TRG_EN	MIPI_DATA_EN
1xBC	SYNC_HDELAY_MSB				SYNC_HDELAY[12:8]				
1xBD	SYNC_HDELAY_LSB	SYNC_HDELAY[7:0]							

ADD	MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1xBE	SYNC_HACTIVE_MSB				SYNC_HACTIVE[12:8]				
1xBF	SYNC_HACTIVE_LSB	SYNC_HACTIVE[7:0]							
1xC0	SYNC_VDELAY_MSB				SYNC_VDELAY[12:8]				
1xC1	SYNC_VDELAY_LSB	SYNC_VDELAY[7:0]							
1xC2	SYNC_VACTIVE_MSB				SYNC_VACTIVE[12:8]				
1xC3	SYNC_VACTIVE_LSB	SYNC_VACTIVE[7:0]							
1xC4 ~ 1xCE	RESERVED	RESERVED							

4.1.3. PAGE 2 (PTZ/SPI/OSG)

ADD	MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
2x00	PTZ_RX_EN	PTZ_RX_PATH_EN	PTZ_RX_START	PTZ_IGNORE_LINE_EN		PTZ_IGNORE_FRM_EN	PTZ_RX_FIELD_POL	PTZ_RX_FIELD_TYPE	
2x01	PTZ_RX_LINE_CNT	PTZ_RX_LINE_CNT					PTZ_RX_HST_OS		
2x02	PTZ_RX_HST	PTZ_RX_DATA_POL	PTZ_RX_HST						
2x03	PTZ_RX_FREQ_FIRST	PTZ_RX_FREQ_FIRST[23:16]							
2x04	PTZ_RX_FREQ_FIRST	PTZ_RX_FREQ_FIRST[15:08]							
2x05	PTZ_RX_FREQ_FIRST	PTZ_RX_FREQ_FIRST[07:00]							
2x06	PTZ_RX_FREQ	PTZ_RX_FREQ [23:16]							
2x07	PTZ_RX_FREQ	PTZ_RX_FREQ [15:08]							
2x08	PTZ_RX_FREQ	PTZ_RX_FREQ[7:0]							
2x09	PTZ_RX_LPF_LEN			PTZ_RX_LPF_LEN					
2x0A	PTZ_RX_H_PIX_OFFSET	PTZ_RX_H_PIX_OFFSET							
2x0B	PTZ_RX_LINE_LEN			PTZ_RX_LINE_LEN					
2x0C	PTZ_RX_VALID_CNT	PTZ_RX_VALID_CNT							
2x0D	PTZ_RX_ADDR_HOLD_EN		PTZ_ADDR_HOLD_EN						
2x0E ~ 2x0F	RESERVED	RESERVED							
2x10	PTZ_FIFO_WR_INIT	PTZ_WR_ADR_INIT	PTZ_WR_BIT_SWAP				PTZ_FIFO_WR_MD (Def 0) 0 : Tx Data, 1 : Tx Flag, 2 : Tx Flag_data 3 : Rx Data(x), 4 : Rx Flag, 5 : Rx Start Flag 6 : Rx Start Flag Data		
2x11	PTZ_FIFO_WR_DATA	PTZ_FIFO_WR_DATA (Address Hold)							
2x12	PTZ_TX_QUEUE_SIZE*	PTZ_TX_QUEUE_SIZE							

ADD	MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
2x13	PTZ_FIFO_WR_ADDR*	PTZ_FIFO_WR_ADDR							
2x14	PTZ_FIFO_RD_INIT	PTZ_RD_ADR_INIT	PTZ_RD_BIT_SWAP		PTZ_PRE_RD_EN		PTZ_FIFO_RD_MD (Def : 3) 0 : Tx Data(x), 1 : Tx Flag, 2 : Tx Flag Data 3 : Rx Data, 4 : Rx Flag, 5 : Rx Star Flag, 6 : Rx Start Flag Data		
2x15	PTZ_RX_QUEUE_SIZE*	PTZ_RX_QUEUE_SIZE* or PTZ_FIFO READ ADDR							
2x16	PTZ_RX_DATA_DET*	PTZ_RX_DATA_DET* (Address Hold) or PTZ_FIFO READ DATA							
2x17	PTZ_FIFO_RD_ADDR*	PTZ_FIFO_RD_ADDR							
2x18	PTZ_RX_HSTRT_OS	PTZ_RX_HSYNC_POL							
2x19	RESERVED	RESERVED							
2x1A	PTZ_RX_VSTRT_OS	PTZ_RX_VSYNC_POL							
2x1B	RESERVED	RESERVED							
2x1C	PTZ_TX_HSTRT_OS	PTZ_TX_HSYNC_POL							
2x1D	RESERVED	RESERVED							
2x1E	PTZ_TX_VSTRT_OS	PTZ_TX_VSYNC_POL							
2x1F	RESERVED	RESERVED							
2x20	PTZ_TX_EN	PTZ_TX_PATH_EN	PTZ_TX_START				PTZ_TX_FIELD_POL	PTZ_TX_FIELD_TYPE	
2x21	PTZ_TX_LINE_CNT	PTZ_TX_LINE_CNT					PTZ_TX_HST_OS		
2x22	PTZ_TX_HST	PTZ_TX_DATA_POL	PTZ_TX_HST						
2x23	PTZ_TX_FREQ_FIRST_MSB	PTZ_TX_FREQ_FIRST[23:16]							
2x24	PTZ_TX_FREQ_FIRST_MLSB	PTZ_TX_FREQ_FIRST[15:08]							
2x25	PTZ_TX_FREQ_FIRST_LSB	PTZ_TX_FREQ_FIRST[07:00]							

ADD	MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
2x26	PTZ_TX_FREQ_MSB	PTZ_TX_FREQ[23:16]							
2x27	PTZ_TX_FREQ_MLSB	PTZ_TX_FREQ[15:08]							
2x28	PTZ_TX_FREQ_LSB	PTZ_TX_FREQ[07:0]							
2x29	PTZ_TX_HPST_MSB				PTZ_TX_HPST[12:8]				
2x2A	PTZ_TX_HPST_LSB	PTZ_TX_HPST[07:0]							
2x2B	PTZ_TX_LINE_LEN			PTZ_TX_LINE_LEN					
2x2C	PTZ_TX_ALL_DATA_LEN	PTZ_TX_ALL_DATA_LEN							
2x2D ~ 2x3F	RESERVED	RESERVED							
2x40	SPI_CTL	SPI_PATH_EN		SPI_TX_EDGE	SPI_RX_EDGE	SPI_DIVIDER			
2x41	SPI_CMD0	SPI_CMD0 = Command							
2x42	SPI_CMD1	SPI_CMD1 = Addr[23:16]							
2x43	SPI_CMD2	SPI_CMD2 = Addr[15:08]							
2x44	SPI_CMD3	SPI_CMD3 = Addr[07:00]							
2x45	SPI_CMD4	SPI_CMD4 = Dummy Data							
2x46	SPI_DATA_SIZE0	SPI_SINGLE							SPI_DATA_SIZE[8]
2x47	SPI_DATA_SIZE1	SPI_DATA_SIZE[7:0]							
2x48	SPI_CMD_SIZE	SPI_RX_MD	SPI_CMD_SKIP	SPI_DUAL_A	SPI_DUAL_D		SPI_CMD_SIZE		
2x49	SPI_REQ	SPI_REQ	SPI_RX_DLY						SPI_BUF_PAGE
2x4A	spi_rx_data	spi_rx_data (read only)							
2x4B ~ 2x4F	RESERVED	RESERVED							
2x50	SPI_FIFO_WR_MD	ADDR_LAT	WR_ADDR_HOLD	ADDR_WR_MD					FIFO_WR_PAGE

ADD	MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
2x51	SPI_FIFO_WR_ADDR	SPI_FIFO_WR_ADDR[7:0]							
2x52	SPI_FIFO_WR_DATA	SPI_FIFO_WR_DATA[7:0] with **Address Hold**							
2x53 ~ 2x57	RESERVED	RESERVED							
2x58	SPI_FIFO_RD_MD		RD_ADDR_HOLD	ADDR_RD_MD					FIFO_RD_PAGE
2x59	SPI_FIFO_RD_ADDR	SPI_FIFO_RD_ADDR[7:0]							
2x5A	SPI_FIFO_RD_DATA	SPI_FIFO_RD_DATA[7:0] with **Address Hold**							
2x5B ~ 2x7F	RESERVED	RESERVED							
2x80	OSG_PATH_EN	OSG_PATH_EN	OSG_INT_MD	OSG_TP_EN	OSG_TP_SEL	OSG_VAV_DLY	OSG_HSTRT_OS[10:8]		
2x81	OSG_HSTRT_OS	OSG_HSTRT_OS[7:0]							
2x82	OSG_VSTRT_OS	OSG_TP_MODE					OSG_VSTRT_OS[10:8]		
2x83	OSG_VSTRT_OS	OSG_VSTRT_OS[7:0]							
2x84	OSG_HACT_SIZE	LUT_AUTO_EN	LUT_AUTO_MD				OSG_HACT_SIZE[10:8]		
2x85	OSG_HACT_SIZE	OSG_HACT_SIZE[7:0]							
2x86	OSG_VACT_SIZE	ALPHA_MODE	OSG_BLINK_EN [2] : Window, [1] : Blink Index, [0] : Blink[7]				OSG_VACT_SIZE[10:8]		
2x87	OSG_VACT_SIZE	OSG_VACT_SIZE[7:0]							
2x88	OSG_ODD_LOC2	OSG_ODD_LOC[23:16]							
2x89	OSG_ODD_LOC1	OSG_ODD_LOC[15:8]							
2x8A	OSG_EVEN_LOC2	OSG_EVEN_LOC[23:16]							
2x8B	OSG_EVEN_LOC1	OSG_EVEN_LOC[15:8]							
2x8C	OSG_LUT_LOC2	OSG_LUT_LOC[23:16]							
2x8D	OSG_LUT_LOC1	OSG_LUT_LOC[15:8]							

ADD	MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
2x8E	OSG_BLK_INDEX	OSG_BLINK_INDEX							
2x8F	OSG_BLK_PER	OSG_BLINK_PERIOD							
2x90	OSG_CMD		OSG_CMD_SKIP	OSG_DUAL_A	OSG_DUAL_D		OSG_CMD_SIZE		
2x91	OSG_CMD0	OSG_CMD0							
2x92	OSG_CMD4	OSG_CMD4							
2x93	OSG_BUG_SIZE	OSG_UP_EN							OSG_BUF_SIZE
2x94 ~ 2x9F	RESERVED	RESERVED							
2xA0	LUT_WR_DATA0	OSG_LUT_WR_DATA0 : Cr Data							
2xA1	LUT_WR_DATA1	OSG_LUT_WR_DATA1 : Cb Data							
2xA2	LUT_WR_DATA2	OSG_LUT_WR_DATA2 : Y Data							
2xA3	LUT_WR_DATA3	OSG_LUT_WR_DATA3 : {BLINK, ALPHA[6:0]} or ALPHA[7:0]							
2xA4	LUT_WR_ADDR	OSG_LUT_WR_ADDR							
2xA5 ~ 2xA7	RESERVED	RESERVED							
2xA8	LUT_RD_ADDR	OSG_LUT_RD_ADDR							
2xA9	LUT_RD_DATA0	OSG_LUT_RD_DATA0 : Cr Data							
2xAA	LUT_RD_DATA1	OSG_LUT_RD_DATA1 : Cb Data							
2xAB	LUT_RD_DATA2	OSG_LUT_RD_DATA2 : Y Data							
2xAC	LUT_RD_DATA3	OSG_LUT_RD_DATA3 : {BLINK, ALPHA[6:0]} or ALPHA[7:0]							
2xAD ~ 2xFE	RESERVED	RESERVED							

4.2. Register Description

4.2.1. Page 0 Register

Addr	Name	R/W	Bit	Descriptions	Default
0x00	DET_IFMT_STD	R	[7:6]	Status Information of Detected Video Input Standard 0 : HD-PVI 1 : HD-CVI 2 : HDA 3 : HDT	2'h0
	DET_IFMT_REF	R	[5:4]	Status Information of Detected Video Input Refresh Rate 0 : 25Hz 1 : 30Hz 2 : 50Hz 3 : 60Hz	2'h0
	DET_VIDEO	R	[3]	Status Information of Video Detection 0 : Not Detected 1 : Detected	1'h0
	DET_IFMT_RES0	R	[2:0]	Status Information of Detected Video Input Resolution 0 : SD 480i 1 : SD 576i 2 : HD720p 3 : HD1080p 4 : HD960p or HD800p	3'h0
0x01	LOCK_STD	R	[7]	Lock Status of Video Standard Detection 0 : Not Detected 1 : Detected	1'h0
	LOCK_GAIN	R	[6]	Lock Status of Gain Loop 0 : Not Locked 1 : Locked	1'h0
	LOCK_CLAMP	R	[5]	Lock Status of Clamp Loop 0 : Not Locked 1 : Locked	1'h0
	RESERVED	R	[4]	Reserved	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
	LOCK_HPLL	R	[3]	Lock Status of Horizontal PLL Loop 0 : Not Locked 1 : Locked	1'h0
	LOCK_C_FINE	R	[2]	Fine Lock Status of Chroma Phase Tracking Loop 0 : Not Locked 1 : Locked	1'h0
	LOCK_CHROMA	R	[1]	Coarse Lock Status of Chroma Phase Tracking Loop 0 : Not Locked 1 : Locked	1'h0
	DET_CHROMA	R	[0]	Status of Chroma Detection 0 : Not Detected 1 : Detected	1'h0
0x10	MAN_IFMT_STD	R/W	[7:6]	Set the Video Input Standard 0 : HD-PVI 1 : HD-CVI 2 : HDA 3 : HDT	2'h0
	MAN_IFMT_REF	R/W	[5:4]	Set the Video Input Refresh Rate 0 : 25Hz 1 : 30Hz 2 : 50Hz 3 : 60Hz	2'h0
	MAN_IFMT_STD_HDT_N	R/W	[3]	Set the Video Input Standard of HDT 0 : Old HDT 1 : New HDT	1'h0
	MAN_IFMT_RES	R/W	[2:0]	Set the Video Input Resolution 0 : SD 480i 1 : SD 576i 2 : HD720p 3 : HD1080p	2'h0
0x11	RESERVED	R/W	[7]	Reserved	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
	VADC_GAIN_SEL	R/W	[6:4]	Set the Video ADC Input Gain 0 : x 1 1 : x 1.28 2 : x 1.57 3 : x 1.85 4 : x 2.15 5 : x 2.42 6 : x 2.71 7 : x 3	3'h0
	MAN_IFMT_EN	R/W	[3:0]	Set the Video Input Format Manually with MAN_IFMT_STD, MAN_IFMT_REF and MAN_IFMT_RES [2] : Force the Video Input Standard with MAN_IFMT_STD [1] : Force the Video Input Refresh Rate with MAN_IFMT_REF [0] : Force the Video Input Resolution with MAN_IFMT_RES	4'h0
0x12	MAIN_EQ_ GAIN_MD	R/W	[4:0]	Select the EQ Global Gain 0 : No Gain ~ 16 : Middle Gain ~ 31 : High Gain	5'h0
0x13	VADC_EQ_LOW_ BAND	R/W	[5:4]	Select the EQ Low Bandwidth Gain 0 : No Gain 1 : Low Gain 2 : Middle Gain 3 : High Gain	2'h0
	VADC_EQ_HIGH_ BAND	R/W	[2:0]	Select the EQ High Bandwidth Gain 0 : No Gain 1 : Low Gain 2 : Middle Gain 3 : High Gain	2'h0
0x14	RESERVED	R/W	[7:2]	Reserved	6'h0

Addr	Name	R/W	Bit	Descriptions	Default
	VADC_IN_SEL	R/W	[1:0]	Select the Video Input 0 : Differential Input Mode 1 : Single Input Mode with VINP 2 : Single Input Mode with VINP 3 : Single Input Mode with VINN	
0x40	MIPI_EN	R/W	[6]	Enable the MIPI Controller 0 : Disable 1 : Enable	1'h0
	MIPI_PD	R/W	[5]	Enable the Power Down Mode of MIPI Controller 0 : Disable 1 : Enable	1'h0
	MIPI_ULP_DATA	R/W	[3]	Enable the ULP Mode for MIPI Data Lane 0 : Disable 1 : Enable	1'h0
	MIPI_ULP_CLK	R/W	[2]	Enable the ULP Mode for MIPI Clock Lane 0 : Disable 1 : Enable	1'h0
	MIPI_STM	R/W	[0]	Select the Test Mode for MIPI Data/Clock Lane	1'h0
0x41	MIPI_CK_CTRL	R/W	[7:4]	Control the MIPI CP/CN Lane State 4'b0000 : Normal Operation Mode 4'b0001 : CP/CN = LP-00 state 4'b0010 : CP/CN = LP-01 state 4'b0011 : CP/CN = LP-10 state 4'b0100 : CP/CN = LP-11 state 4'b0101 : CP/CN = HS-0 state 4'b0110 : CP/CN = HS-1 state 4'b0111 : CP/CN = Hi-z state 4'b1000 : CP/CN = ULP state 4'b1001 : CP/CN = Serialize Test mode	4'h8
	MIPI_HDCLK_E	R/W	[3]	Select the Level of Even Phase for MIPI Clock Lane 0 : Low 1 : High	1'h1
	MIPI_HDCLK_O	R/W	[2]	Select the Level of Odd Phase for MIPI Clock Lane 0 : Low 1 : High	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
0x42	MIPI_D0_CTRL	R/W	[7:4]	Control the MIPI DP0/DN0 Lane State 4'b0000 : Normal Operation Mode 4'b0001 : DP0/DN0 = LP-00 state 4'b0010 : DP0/DN0 = LP-01 state 4'b0011 : DP0/DN0 = LP-10 state 4'b0100 : DP0/DN0 = LP-11 state 4'b0101 : DP0/DN0 = HS-0 state 4'b0110 : DP0/DN0 = HS-1 state 4'b0111 : DP0/DN0 = Hi-z state 4'b1000 : DP0/DN0 = ULP state 4'b1001 : DP0/DN0 = Serialize Test mode	4'h8
	MIPI_D1_CTRL	R/W	[3:0]	Control the MIPI DP1/DN1 Lane State 4'b0000 : Normal Operation Mode 4'b0001 : DP1/DN1 = LP-00 state 4'b0010 : DP1/DN1 = LP-01 state 4'b0011 : DP1/DN1 = LP-10 state 4'b0100 : DP1/DN1 = LP-11 state 4'b0101 : DP1/DN1 = HS-0 state 4'b0110 : DP1/DN1 = HS-1 state 4'b0111 : DP1/DN1 = Hi-z state 4'b1000 : DP1/DN1 = ULP state 4'b1001 : DP1/DN1 = Serialize Test mode	4'h8
0x43	MIPI_D2_CTRL	R/W	[7:4]	Control the MIPI DP2/DN2 Lane State 4'b0000 : Normal Operation Mode 4'b0001 : DP2/DN2 = LP-00 state 4'b0010 : DP2/DN2 = LP-01 state 4'b0011 : DP2/DN2 = LP-10 state 4'b0100 : DP2/DN2 = LP-11 state 4'b0101 : DP2/DN2 = HS-0 state 4'b0110 : DP2/DN2 = HS-1 state 4'b0111 : DP2/DN2 = Hi-z state 4'b1000 : DP2/DN2 = ULP state 4'b1001 : DP2/DN2 = Serialize Test mode	4'h8

Addr	Name	R/W	Bit	Descriptions	Default
	MIPI_D3_CTRL	R/W	[3:0]	Control the MIPI DP3/DN3 Lane State 4'b0000 : Normal Operation Mode 4'b0001 : DP3/DN3 = LP-00 state 4'b0010 : DP3/DN3 = LP-01 state 4'b0011 : DP3/DN3 = LP-10 state 4'b0100 : DP3/DN3 = LP-11 state 4'b0101 : DP3/DN3 = HS-0 state 4'b0110 : DP3/DN3 = HS-1 state 4'b0111 : DP3/DN3 = Hi-z state 4'b1000 : DP3/DN3 = ULP state 4'b1001 : DP3/DN3 = Serialize Test mode	4'h8
0x44	DPHY_ISEL_TRIM	R/W	[2:0]	Select the Current of MIPI Output Driver Current = 17uA + 1uA step/code 3'b000 : Low Current (17uA) ~ 6 : High Current (26uA)	3'h3
0x45	DPHY_V12_TRIM	R/W	[6:4]	Select the LP Mode Output Voltage of MIPI output Driver Voltage = 1.14V + 0.02 V step/code 0 : Low ~ 6 : High (1.26V)	3'h3
	DPHY_V04_TRIM	R/W	[2:0]	Select the HS Mode High Output Voltage of MIPI output Driver Voltage = 0.34V + 0.02 V step/code 0 : Low (0.34V) ~ 6 : High (0.46V)	3'h3
0x46	DPHY_V03_TRIM	R/W	[6:4]	Select the HS Mode Reference Output Voltage of MIPI Output Driver Voltage = 0.27V + 0.01 V step/code 0 : Low (0.27V) ~ 6 : High (0.33V)	3'h3

Addr	Name	R/W	Bit	Descriptions	Default
	DPHY_V01_TRIM	R/W	[2:0]	Select the HS Mode Low Output Voltage of MIPI Output Driver Voltage = 0.07V + 0.01 V step/code 0 : Low (0.07V) ~ 6 : High (0.13V)	3'h3
0x47	MIPI_IN_EN	R/W	[7]	Enable the Video Input for MIPI 0 : Disable 1 : Enable	1'h0
	MIPI_LANE	R/W	[5:4]	Select the Data Lane Number for MIPI 0 : N/A 1 : 2 Lane Mode 2 : N/A 3 : 4 Lane Mode	2'h3
	MIPI_FRM_MD	R/W	[3:2]	Select the Frame Count ID Mode for MIPI 0 : Fix to "0" 1 : Fix to "1" for Odd Field, "2" for Even Field 2 : Free-running for Progressive 3 : Free-running for Interlace	2'h0
	MIPI_IN_MD	R/W	[1:0]	Select the Synchronization Mode for MIPI [1] : Select the Synchronization Mode for MIPI HS Start/stop 0 : Bypass 1 : Synchronize with V Sync [0] : Select the H Sync during V Blank Period 0 : Enable H Sync 1 : Disable H sync	2'h0
0x48 /0x49	MIPI_PKT_SIZE	R/W	[7:0]	Select the Packet size of MIPI Active Line 16'h5A0 : 720H 16'hA00 : 1280H 16'hF00 : 1920H	16'h0A00
0x4A ~ 0x4D	MIPI_STP	R/W	[7:0]	Reserved for Test Mode	32'h00
0x4E	DPHY_VCTRL_INIT	R/W	[7]	Select the initial condition of MIPI DLL 0 : 0V 1 : 3.3V	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
	DPHY_FLD	R/W	[6]	Select the MIPI DLL Control Mode Reserved to "0"	1'h0
	MIPI_PD	R/W	[5:0]	Enable the Power Down of the MIPI Output Lane and DLL [5] : For MIPI DLL [4] : For MIPI Clock Lane & MIPI BGR [3] : For MIPI Data3 Lane [2] : For MIPI Data2 Lane [1] : For MIPI Data1 Lane [0] : For MIPI Data0 Lane	6'h3F
0x50	MIPI_DATA_ID	R/W	[7:0]	Select the MIPI Data ID for MIPI HS Mode 8'h1E : For YUV 8Bits Interface	8'h1E
0x51	MIPI_T_LPX	R/W	[7:0]	Select the Transition Time for LP Data transfer	8'h09
0x52	MIPI_T_CLK_PREP	R/W	[7:0]	Select the Time of LP00 State for Clock Lane	8'h0B
0x53	MIPI_T_HS_PREP	R/W	[7:0]	Select the Time of LP00 State for Data Lane	8'h0B
0x54	MIPI_T_HS_ZERO	R/W	[7:0]	Select the Time of HS Zero State at Start for Data Lane	8'h14
0x55	MIPI_T_HS_TRAIL	R/W	[7:0]	Select the Time of HS Zero State at End for Data Lane	8'h0F
0x56	MIPI_T_CLK_ZERO	R/W	[7:0]	Select the Time of HS Zero State at Start for Clock Lane	8'h23
0x57	MIPI_T_CLK_TRAIL	R/W	[7:0]	Select the Time of HS Zero State at End for Clock Lane	8'h0F
0x58	MIPI_T_CLK_PRE	R/W	[7:0]	Select the Time of Data Transfer Start from Clock Lane	8'h0F
0x59	MIPI_T_CLK_POST	R/W	[7:0]	Select the Time of Clock Transfer End from Data Transfer End	8'h42
0x5A	MIPI_T_WAKEUP	R/W	[7:0]	Select the Time of Exit Time from ULP State	8'h40
0x5B	MIPI_T_HS_EXIT	R/W	[7:0]	Select the Time of LP11 to HS Burst State for Clock Lane	8'h11
0x5C	MIPI_T_ESC_CMD	R/W	[7:0]	Select the Data of LP Data Transfer	8'h00
0x5D	MIPI_MON_SEL	R/W	[3:0]	Reserved for Test	4'h0
0x5E*	MIPI_MONITOR	R/W	[7:0]	Reserved for Test	8'h00
0x70	DUMMY_RW_REG0	R/W	[7:0]	Dummy R/W Register for User Programming Purpose	8'h00
0x71	DUMMY_RW_REG1	R/W	[7:0]	Dummy R/W Register for User Programming Purpose	8'h00
0x72	DUMMY_RW_REG2	R/W	[7:0]	Dummy R/W Register for User Programming Purpose	8'h00
0x73	DUMMY_RW_REG3	R/W	[7:0]	Dummy R/W Register for User Programming Purpose	8'h00
0x74	DUMMY_RW_REG4	R/W	[7:0]	Dummy R/W Register for User Programming Purpose	8'h00
0x75	DUMMY_RW_REG5	R/W	[7:0]	Dummy R/W Register for User Programming Purpose	8'h00
0x76	DUMMY_RW_REG6	R/W	[7:0]	Dummy R/W Register for User Programming Purpose	8'h00
0x77	DUMMY_RW_REG7	R/W	[7:0]	Dummy R/W Register for User Programming Purpose	8'h00

Addr	Name	R/W	Bit	Descriptions	Default
0x80	IRQOUT_EN	R/W	[7:6]	Select the Interrupt Output Mode 0 : Disable 1 : Output Mode 2/3 : Pull-up / Pull Down Mode	1'h0
	IRQOUT_POL	R/W	[5]	Select the Output Polarity for interrupt 0 : Bypass / Pull-Up Mode 1 : Inversion / Pull-Down Mode	1'h0
	IRQOUT_RPT	R/W	[4]	Enable the Repeat Mode of IRQ 0 : Bypass 1 : Enable the Repeat Mode of IRQ	1'h0
	SYNC_GPIO	R/W	[2]	Enable the Synchronized Interrupt with Synchronization Period SYNC_GPIO : For GPIO[8:0] Interrupt SYNC_FUNC : For SPI/VFD/NOVID Interrupt SYNC_PTZ : For PTZ Detection Interrupt	1'h0
	SYNC_FUNC	R/W	[1]		1'h0
	SYNC_PTZ	R/W	[0]		1'h0
0x81	IRQ_SYNC_PERIOD	R/W	[7:0]	Select the Interrupt Synchronization Reference Period Synchronization Period = (IRQ_SYNC_PERIOD + 1) * 20msec Period	8'h00
0x82	IRQ_TIMER_PERIOD	R/W	[7:0]	Select the Interrupt Timer Reference Period Timer Period = (IRQ_TIMER_PERIOD + 1) * Synchronization Period	8'h00
0x83	STATE_TIMER	R	[5]	Pending Status for Interrupt IRQSTATE_TIMER : For Timer0/1 Interrupt IRQSTATE_GPIO : For GPIO[8:0] interrupt IRQSTATE_VFD : For Video Format detection interrupt IRQSTATE_NOVID : For Novideo detection interrupt IRQSTATE_PTZ : For PTZ detection interrupt 0 : No Pending 1 : Pending	1'b0
	STATE_GPIO	R	[4]		1'b0
	STATE_SPI	R	[3]		1'b0
	STATE_VFD	R	[2]		1'b0
	STATE_NOVID	R	[1]		1'b0
	STATE_PTZ	R	[0]		1'b0
0x84	SYNC_VFD_PEND	R/W	[7]	Select the Interrupt Mode for Video Format Detection 0 : Maintain New Event at Synchronized Mode 1 : Clear New Event by Interrupt Clear at Synchronized Mode	1'b0
	SYNC_NOVID_PEND	R/W	[6]	Select the Interrupt Mode for No Video Detection 0 : Maintain New Event at Synchronized Mode 1 : Clear New Event by Interrupt Clear at Synchronized Mode	1'b0

Addr	Name	R/W	Bit	Descriptions	Default
	IRQ_VFD_MD	R/W	[5]	Select the Interrupt Mode for Video Format Detection 0 : Edge Interrupt (Interrupt when Video format status is changed) 1 : Level Interrupt (Interrupt when Video format status is different from IRQ_VFD_LV	1'h0
	IRQ_NOVID_MD	R/W	[4]	Select the Interrupt Mode for Novideo Detection 0 : Edge Interrupt (Interrupt when Novideo status changed) 1 : Level Interrupt (Interrupt when Novideo status different with IRQ_NOVID_LV	1'h0
0x84	IRQ_GPIO_MD	R/W	[0]	Select the Interrupt Mode for GPIO[8:0] GPIO[8:5] for P_SPI[3:0] GPIO[4:0] for P_MPP[4:0] 0 : Edge Interrupt 1 : Level Interrupt	9'h00
0x85		R/W	[7:0]		
0x86	IRQ_VFD_LV	R/W	[5]	Select the Interrupt Mode of Video Format Detection 0 : Low Level Interrupt 1 : High Level Interrupt	1'h0
	IRQ_NOVID_LV	R/W	[4]	Select the Interrupt Mode of No-video Detection 0 : Low Level Interrupt (Normal) 1 : High Level Interrupt (Video Loss)	1'h0
	IRQ_GPIO_LV	R/W	[0]	Select the Interrupt Mode for GPIO [8:0] GPIO[8:5] for P_SPI[3:0] GPIO[4:0] for P_MPP[4:0] @ IRQ_GPIO_MD = 0 & GPIO_BOTH = 0 0 : Falling Edge Interrupt 1 : Rising Edge Interrupt @ IRQ_GPIO_MD = 1 0 : Low Level Interrupt 1 : High Level Interrupt	9'h0
0x87		R/W	[7:0]		
0x88	IRQ_GPIO_BOTH	R/W	[0]	Select the Interrupt Mode for GPIO[8:0] @IRQ_GPIO_MD = 0 GPIO[8:5] for P_SPI[3:0] GPIO[4:0] for P_MPP[4:0] 0 : Interrupt by IRQ_GPIO_LV 1 : Interrupt by Rising or Falling Edge	9'h0
0x89		R/W	[7:0]		
0x8A	IRQ_TIMER_PERIOD	R/W	[7:0]	Select the Interrupt Timer1 Reference Period Timer Period = (IRQ_TIMER_PERIOD + 1) * Synchronization Period	8'h0

Addr	Name	R/W	Bit	Descriptions	Default
0x90	IRQENA_PTZ	R/W	[7:0]	Enable the Interrupt of PTZ Detection PTZ[7] for PTZ Rx Data Error Detection PTZ[6] for PTZ Rx Sync Error Detection PTZ[5] for PTZ Rx Data Buffer Overflow Error Detection PTZ[4] for PTZ Rx Data Buffer Underflow Error Detection PTZ[3] for PTZ Rx Done Detection PTZ[2] for PTZ Tx Data Buffer Overflow Error Detection PTZ[1] for PTZ Tx Data Buffer Underflow Error Detection PTZ[0] for Tx Data Done Detection 0 : Disable 1 : Enable	8'h0
0x91	IRQENA_TIMER1	R/W	[7]	Enable the interrupt of Timer 1 0 : Disable 1 : Enable	1'h0
	IRQENA_TIMER0	R/W	[6]	Enable the interrupt of Timer 0 0 : Disable 1 : Enable	1'h0
	IRQENA_VFD	R/W	[5]	Enable the Interrupt of Video Format Detection 0 : Disable 1 : Enable	1'h0
	IRQENA_NOVID	R/W	[4]	Enable the Interrupt of No-video Detection 0 : Disable 1 : Enable	1'h0
	IRQENA_SPI	R/W	[3]	Enable the Interrupt of SPI Transfer 0 : Disable 1 : Enable	1'h0
	IRQENA_GPIO	R/W	[0]	Enable the Interrupt of GPIO[8:0] GPIO[8:5] for P_SPI[3:0] GPIO[4:0] for P_MPP[4:0] 0 : Disable 1 : Enable	9'h0
0x92		R/W	[7:0]		

Addr	Name	R/W	Bit	Descriptions	Default
0x94	IRQCLR_PTZ	R/W	[7:0]	Clear the Interrupt of PTZ Detection PTZ[7] for PTZ Rx Data Error Detection PTZ[6] for PTZ Rx Sync Error Detection PTZ[5] for PTZ Rx Data Buffer Overflow Error Detection PTZ[4] for PTZ Rx Data Buffer Underflow Error Detection PTZ[3] for PTZ Rx Done Detection PTZ[2] for PTZ Tx Data Buffer Overflow Error Detection PTZ[1] for PTZ Tx Data Buffer Underflow Error Detection PTZ[0] for Tx Data Done Detection 0 : Done 1 : Clear (After Writing “1”, the interrupt will be cleared)	8’h0
0x95	IRQCLR_TIMER1	R/W	[7]	Clear the interrupt of Timer 1 0 : Done 1 : Clear (After Writing “1”, the interrupt will be cleared)	1’h0
	IRQCLR_TIMER0	R/W	[6]	Clear the interrupt of Timer 0 0 : Done 1 : Clear (After Writing “1”, the interrupt will be cleared)	1’h0
	IRQCLR_VFD	R/W	[5]	Clear the Interrupt of Video Format Detection 0 : Done 1 : Clear (After Writing “1”, the interrupt will be cleared)	1’h0
	IRQCLR_NOVID	R/W	[4]	Clear the Interrupt of No-video Detection 0 : Done 1 : Clear (After Writing “1”, the interrupt will be cleared)	1’h0
	IRQCLR_SPI	R/W	[3]	Clear the Interrupt of SPI Transfer 0 : Done 1 : Clear (After Writing “1”, the interrupt will be cleared)	1’h0
	IRQCLR_GPIO	R/W	[0]	Clear the Interrupt of GPIO[8:0] GPIO[8:5] for P_SPI[3:0] GPIO[4:0] for P_MPP[4:0] 0 : Done 1 : Clear (After Writing “1”, the interrupt will be cleared)	9’h0
0x96		R/W	[7:0]		

Addr	Name	R/W	Bit	Descriptions	Default
0x98	STATUS_PTZ			Status of the Interrupt for PTZ Detection PTZ[7] for PTZ Rx Data Error Detection 0 : No Error 1 : Error PTZ[6] for PTZ Rx Sync Error Detection 0 : No Error 1 : Error PTZ[5] for PTZ Rx Data Buffer Overflow Error Detection 0 : No Error 1 : Error PTZ[4] for PTZ Rx Data Buffer Underflow Error Detection 0 : No Error 1 : Error PTZ[3] for PTZ Rx Done Detection 0 : Idle 1 : Busy PTZ[2] for PTZ Tx Data Buffer Overflow Error Detection 0 : No Error 1 : Error PTZ[1] for PTZ Tx Data Buffer Underflow Error Detection 0 : No Error 1 : Error PTZ[0] for Tx Data Done Detection 0 : Idle 1 : Busy	8'h0
0x99	STATUS_TIMER1	R/W	[7]	Status of the Interrupt for Timer 1 0 : Low 1 : High	1'b0
	STATUS_TIMER0	R/W	[6]	Status of the Interrupt for Timer 0 0 : Low 1 : High	1'b0
	STATUS_VFD	R	[5]	Status of the Interrupt for Video Format Detection 0 : No Video Format Change 1 : Detection of the Video Format Change	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
	STATUS_NOVID	R	[4]	Status of the Interrupt for No-video Detection 0 : Video 1 : No-video Detect	1'h0
	STATUS_GPIO	R	[0]	Status of the Interrupt for GPIO[8:0]	9'h0
0x9A		R/W	[7:0]	GPIO[8:5] for P_SPI[3:0] GPIO[4:0] for P_MPP[4:0] 0 : Low 1 : High	
0xA0	GPIO_IOB	R/W	[0]	Select the In/Output Mode of GPIO[8:0]	9'h1FF
0xA1		R/W	[7:0]	GPIO[8:5] for P_SPI[3:0] GPIO[4:0] for P_MPP[4:0] 0 : Output Mode 1 : Input Mode	
0xA2	GPIO_OUT	R/W	[0]	Select the Output Value of GPIO[8:0]	9'h0
0xA3		R/W	[7:0]	GPIO[8:5] for P_SPI[3:0] GPIO[4:0] for P_MPP[4:0]	
0xA4	GPIO_MPP_MD	R/W	[7:6]	Select the Output Mode for P_SPI[3:0] 0 : GPIO/SPI Output 1 : Reserved	4'd0
	GPIO_IRQ_MD	R/W	[4]	Select the Output Mode for P_MPP[0] 0 : GPIO/MPP Output 1 : IRQ Output	4'h0
	GPIO_EXT_MD	R/W	[0]	Select the Output Mode for GPIO[8:0]	9'h0
0xA5		R/W	[7:0]	GPIO[8:5] for P_SPI[3:0] 0 : GPIO Output 1 : SPI Interface Output GPIO[4:0] for P_MPP[4:0] 0 : GPIO/MPP Output 1 : PTZ Output	
0xA6	GPIO_MPP1_SEL	R/W	[7]	Select the Output Mode for P_MPP[1] 0 : H/V/F Sync Output 1 : GPIO Output	1'h0
	MPP1_POL	R/W	[6]	Select the Output Polarity of P_MPP[1] for H/V/F Sync Output 0 : Bypass 1 : Polarity Inversion	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
	MPP1_SEL	R/W	[5:4]	Select the P_MPP[1] Output Data for H/V/F Sync Output 0 : HAV Output 1 : VAV Output 2 : FLD Output 3 : Reserved	2'h0
	GPIO_MPP0_SEL	R/W	[3]	Select the Output Mode for P_MPP[0] 0 : H/V/F Sync Output 1 : GPIO Output	1'h0
	MPP0_POL	R/W	[2]	Select the Output Polarity of P_MPP[0] for H/V/F Sync Output 0 : Bypass 1 : Polarity Inversion	1'h0
	MPP0_SEL	R/W	[1:0]	Select the P_MPP[0] Output Data for H/V/F Sync Output 0 : HAV Output 1 : VAV Output 2 : FLD Output 3 : Reserved	2'h0
0xA7	GPIO_MPP3_SEL	R/W	[7]	Select the Output Mode for P_MPP[3] 0 : H/V/F Sync Output 1 : GPIO Output	1'h0
	MPP3_POL	R/W	[6]	Select the Output Polarity of P_MPP[3] for H/V/F Sync Output 0 : Bypass 1 : Polarity Inversion	1'h0
	MPP3_SEL	R/W	[5:4]	Select the P_MPP[3] Output Data for H/V/F Sync Output 0 : HAV Output 1 : VAV Output 2 : FLD Output 3 : Reserved	2'h0
	GPIO_MPP2_SEL	R/W	[3]	Select the Output Mode for P_MPP[2] 0 : H/V/F Sync Output 1 : GPIO Output	1'h0
	MPP2_POL	R/W	[2]	Select the Output Polarity of P_MPP[2] for H/V/F Sync Output 0 : Bypass 1 : Polarity Inversion	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
	MPP2_SEL	R/W	[1:0]	Select the P_MPP[2] Output Data for H/V/F Sync Output 0 : HAV Output 1 : VAV Output 2 : FLD Output 3 : Reserved	2'h0
0xA8	GPIO_MPP4_SEL	R/W	[3]	Select the Output Mode for P_MPP[4] 0 : H/V/F Sync Output 1 : GPIO Output	1'h0
	MPP4_POL	R/W	[2]	Select the Output Polarity of P_MPP[4] for H/V/F Sync Output 0 : Bypass 1 : Polarity Inversion	1'h0
	MPP4_SEL	R/W	[1:0]	Select the P_MPP[4] Output Data for H/V/F Output 0 : HAV Output 1 : VAV Output 2 : FLD Output 3 : Reserved	2'h0
0xD2	FPLL_MAIN_CNT	R/W	[5:0]	PLL Divider N for FPLL Output Frequency = Input Frequency * FPLL_MAIN_CNT / 3 6'h21 : 297MHz (Reserved)	6'h21
0xD3	BGR_PD	R/W	[7]	Select the Power Down for PLL BGR 0 : Normal Operation 1 : Power Down Mode	1'b1
0xD8	MPLL_PHASE_SEL	R/W	[2:0]	Control the Phase Delay of VDCK Pin 0 : 0/8 Phase 1 : 1/8 Phase 2 : 2/8 Phase 3 : 3/8 Phase 4 : 4/8 Phase 5 : 5/8 Phase 6 : 6/8 Phase 7 : 7/8 Phase	3'h0

Addr	Name	R/W	Bit	Descriptions	Default
0xDA	MPLL_MAIN_CNT	R/W	[5:0]	PLL Divider N for MPLL Output Frequency = Input Frequency * MPLL_MAIN_CNT / 3 6'h18 : 216MHz 6'h20 : 288MHz 6'h21 : 297MHz	6'h21
0xE0	VDEC_CLK_PWDN	R/W	[7]	Select the Power Down for Decoder Operation Clock 0 : Normal Operation 1 : Power Down Mode	1'h0
	VOUT_CLK_PWDN	R/W	[6]	Select the Power Down for Video Output Operation Clock 0 : Normal Operation 1 : Power Down Mode	1'h0
	MIPI_CLK_PWDN	R/W	[5]	Select the Power Down for MIPI Operation Clock 0 : Normal Operation 1 : Power Down Mode	1'h0
	CC_CLK_PWDN	R/W	[4]	Select the Power Down for Cascade Operation Clock 0 : Normal Operation 1 : Power Down Mode	1'h0
	RESERVED	R/W	[3:0]	Reserved	4'hC
0xE1	OUTFMT_BT656	R/W	[7]	Select the VD Data Output Standard 0 : BT1120 (FF-FF-00-00-00-00-XY-XY-Cb-Y-Cr-Y Sequence) 1 : BT656 (FF-00-00-XY-Cb-Y-Cr-Y Sequence)	1'h0
	OUTFMT_YC_INV	R/W	[6]	Select the VD Data Output Sequence 0 : Cb-Y-Cr-Y 1 : Y-Cb-Y-Cr	1'h0
	OUTFMT_RATE	R/W	[5:4]	Select the Video Data Output Rate for One Channel 0 : 148.5MHz Data Rate for 8bit Data Interface 1 : 74.25MHz Data Rate for 8bit Data Interface 2 : 36MHz Data Rate for 8bit Data Interface 3 : 27MHz Data Rate for 8bit Data Interface	2'h0
	RESERVED	R/W	[3]	Reserved	1'h0
	CH_MUX_MD	R/W	[2]	Select the Channel Multiplexing Mode 0 : 1CH Output Mode 1 : 2CH Multiplexing Output Mode	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
	CH_SEL_B	R/W	[1]	Select the Channel on 2nd Data 0 : Internal Proceeded Channel 1 : Transferred Channel with Cascaded Connection	1'h0
	CH_SEL_A	R/W	[0]	Select the Channel on 1st Data 0 : Internal Proceeded Channel 1 : Transferred Channel with Cascaded Connection	1'h0
0xE2	CKOUT_2X_MD	R/W	[7]	Select the VD Data Output Mode 0 : SDR (Single Data Rate) Output Mode 1 : DDR (Dual Data Rate) Output Mode	1'h0
	OUTFMT_HAV_VBLK	R/W	[3]	Select the H Sync during V Blank 0 : Enable H Sync during V Blank 1 : Disable H Sync during V Blank	1'h0
	OUTFMT_SYNC_BYP	R/W	[2]	Disable the Embedded Sync Code in BT656/BT1120 0 : Enable 1 : Disable	1'h0
	CHID_NUM	R/W	[1:0]	Select the CHID Number	2'h0
0xE3	VDCK1_PHASE	R/W	[5:0]	Select the Frequency and Phase Mode for P_CP/VDCK1	6'h0
0xE4	VDCK0_PHASE	R/W	[5:0]	Select the Frequency and Phase Mode for P_CN/VDCK0	6'h0
0xE5	MIPI_DCLK_PHASE	R/W	[3:0]	Select the Frequency of MIPI DCLK 4'hC : MCLK / 2 * 1/4 = 37.125MHz (FHD) 4'hE : MCLK / 2 * 1/8 = 18.5625MHz (HD)	4'h0
0xE6	MIPI_ICLK_PHASE	R/W	[3:0]	Select the Frequency of MIPI ICLK 4'h0 : MCLK / 2 * 1/1 = 148.5MHz (FHD) 4'h8 : MCLK / 2 * 1/2 = 74.25MHz (HD)	4'h0
0xE8	PAR_IN_EN	R/W	[1:0]	Enable the Input for VD[7:0] and VDCK0/1 pin	10'h0

Addr	Name	R/W	Bit	Descriptions	Default
0xE9		R/W	[7:0]	[9] : For CN/VDCK0 Pin [8] : For CP/VDCK1 Pin [7] : For DP3/VD[7] Pin [6] : For DN3/VD[6] Pin [5] : For DP2/VD[5] Pin [4] : For DN2/VD[4] Pin [3] : For DP1/VD[3] Pin [2] : For DN1/VD[2] Pin [1] : For DP0/VD[1] Pin [0] : For DN0/VD[0] Pin 0 : Disable the Input 1 : Enable the Input	
0xEA	PAR_OUT_EN	R/W	[1:0]	Enable the Output for VD[7:0] and VDCK0/1 Pin	10'h0
0xEB		R/W	[7:0]	[9] : For CN/VDCK0 Pin [8] : For CP/VDCK1 Pin [7] : For DP3/VD[7] Pin [6] : For DN3/VD[6] Pin [5] : For DP2/VD[5] Pin [4] : For DN2/VD[4] Pin [3] : For DP1/VD[3] Pin [2] : For DN1/VD[2] Pin [1] : For DP0/VD[1] Pin [0] : For DN0/VD[0] Pin 0 : Disable the Output 1 : Enable the Output (In this case, MIPI Output is not allowed)	
0xF0	DIG_SMT_EN	R/W	[2]	Select the Schmitt-trigger Input for P_TEST/P_RSTB/P_SCLK/ P_SDAT Pin 0 : Normal Input 1 : Schmitt-trigger input	1'h0
	DIG_DRV_SEL	R/W	[1:0]	Select the Drive Strength for P_TEST/P_RSTB/P_SCLK /P_SDAT Pin 2'b00 : 5mA ~ 2'b11 : 20mA	2'h0

Addr	Name	R/W	Bit	Descriptions	Default
0xF1	SPI_SMT_EN	R/W	[2]	Select the Schmitt-trigger Input for P_SPI[3:0] Pin 0 : Normal Input 1 : Schmitt-trigger Input	1'h0
	SPI_DRV_SEL	R/W	[1:0]	Select the Drive Strength for P_SPI[3:0] Pin 2'b00 : 5mA ~ 2'b11 : 20mA	2'h0
	MPP_SMT_EN	R/W	[2]	Select the Schmitt-trigger Input for P_MPP[4:0] Pin 0 : Normal Input 1 : Schmitt-trigger Input	1'h0
	MPP_DRV_SEL	R/W	[1:0]	Select the Drive Strength for P_MPP[4:0] Pin 2'b00 : 5mA ~ 2'b11 : 20mA	2'h0
0xF2	VD_SMT_EN	R/W	[2]	Select the Schmitt-trigger Input for P_VD[7:0] Pin 0 : Normal Input 1 : Schmitt-trigger Input	1'h0
	VD_DRV_SEL	R/W	[1:0]	Select the Drive Strength for P_VD[7:0] Pin 2'b00 : 5mA ~ 2'b11 : 20mA	2'h0
	VDCK_SMT_EN	R/W	[2]	Select the Schmitt-trigger Input for P_VDCK0/1 Pin 0 : Normal Input 1 : Schmitt-trigger Input	1'h0
	VDCK_DRV_SEL	R/W	[1:0]	Select the Drive Strength for P_VDCK0/1 Pin 2'b00 : 5mA ~ 2'b11 : 20mA	2'h0

Addr	Name	R/W	Bit	Descriptions	Default
0xF8	RESET_EN	R/W	[6:0]	Enable the Soft Reset for Each Function [6] : For MPLL [5] : For FPLL [4] : For MIPI Controller [3] : For SPI Controller [2] : For OSG Overlay Controller [1] : For PTZ Controller [0] : For Video Controller 0 : Normal 1 : Enable the Soft Reset	7'h0
0xFC	CHIP_ID[15:8]	R	[7:0]	MSB of CHIP ID Data (CHIP_ID[15:0] = 16'h2000)	8'h20
0xFD	CHIP_ID[7:0]	R	[7:0]	LSB of CHIP ID Data	8'h00
0xFE	REV_ID	R	[7:0]	Revision ID	8'h20
0xFF	ADDR_LATCH_EN	R/W	[7]	Enable the Latch of I2C Slave Address 0 : Done 1 : Enable the Latch of I2C Slave Address (Auto-cleared After Latch of I2C Slave Address)	1'h0
	HOST_RW_PAGE	R/W	[1:0]	Select the Page of Host Register Map 0 : Page 0 (Video EQ and MIPI and IRQ) 1 : Page 1 (Video Decoder) 2 : Page 2 (PTZ Tx/Rx, SPI, OSG)	2'h0

4.2.2. Page 1 Register

Addr	Name	R/W	Bit	Descriptions	Default
1x00	AGCEN	R/W	[7]	Enable the Automatic Gain Control (AGC) 0 : Disable 1 : Enable	1'h0
	AUTO_BGND	R/W	[6]	Enable the Automatic Background when No video is detected. Background Color is determined with BGND_MD[0] register. 0 : Disable 1 : Enable	1'h0
	PEAKEN	R/W	[5]	Enable the Automatic Peak Control 0 : Disable 1 : Enable	1'h0
	PEAKREF	R/W	[3:2]	Select the Automatic Peak Reference 0 : 100% White 1 : 110% White 2 : 120% White 3 : 130% White	2'h0
	BGND_MD	R/W	[1]	Control the Background Mode 0 : Normal Video Output 1 : Manual Background Mode	1'h0
			[0]	Control the Background Color 0 : Black Background 1 : Blue Background	1'h0
1x11	VDELAY[10:8]	R/W	[7:5]	MSB of the Vertical Starting Line (VDELAY[10:0])	3'h0
	HDELAY[12:8]	R/W	[4:0]	MSB of the Horizontal Starting Pixels (HDELAY[12:0])	5'h00
1x12	VACTIVE[10:8]	R/W	[7:5]	MSB of the Vertical Starting Line (VACTIVE[10:0])	3'h0
	HACTIVE[12:8]	R/W	[4:0]	MSB of the Horizontal Active Pixels (HACTIVE[12:0])	5'h00
1x13	HDELAY[7:0]	R/W	[7:0]	LSB of the Horizontal Starting Pixels (HDELAY[12:0]) : Unit 1 Pixel	8'h00
1x14	HACTIVE[7:0]	R/W	[7:0]	LSB of the Horizontal Active Pixels (HACTIVE[12:0]) : Unit 1 Pixel	8'h00
1x15	VDELAY[7:0]	R/W	[7:0]	LSB of the Vertical Starting Line (VDELAY[10:0]) : Unit 1 Line	8'h00
1x16	VACTIVE[7:0]	R/W	[7:0]	LSB of the Vertical Active Lines (VACTIVE[10:0]) : Unit 1 Line	8'h00

Addr	Name	R/W	Bit	Descriptions	Default
1x1D	RESERVED	R/W	[7:5]	Reserved	3'h0
	HSCL_HACTIVE [12:8]	R/W	[4:0]	MSB of the Horizontal Active Pixels for Down Scaled Video Output (HSCL_HACTIVE[12:0])	5'h00
1x1F	HSCL_HACTIVE [7:0]	R/W	[7:0]	LSB of the Horizontal Active Pixels for Down Scaled Video Output (HSCL_HACTIVE[12:0])	8'h00
1x20	CONT	R/W	[7:0]	Control the Contrast for Luminance 0 : Gain 0 ~ 128 : Gain 1 ~ 255 : Gain 2	8'h00
1x21	BRGT	R/W	[7:0]	Control the Brightness for Luminance 0 : -100% ~ 128 : 0 ~ 255 : +100%	8'h00
1x22	SAT	R/W	[7:0]	Control the Saturation for Chrominance 0 : Gain 0 ~ 128 : Gain 1 ~ 255 : Gain 2	8'h00
1x23	HUE	R/W	[7:0]	Control the Hue for Chrominance 0 : -180° ~ 128 : 0 ~ 255 : 180°	8'h00
1x29	DOWN_HSCL [15:8]	R/W	[7:0]	MSB of the Horizontal Down Scaling Ratio (DOWN_HSCL[15:0]	8'h00
1x2A	DOWN_HSCL [7:0]	R/W	[7:0]	LSB of the Horizontal Down Scaling Ratio (DOWN_HSCL[15:0]	8'h00

<table>
<tr><th>Addr</th><th>Name</th><th>R/W</th><th>Bit</th><th>Descriptions</th><th>Default</th></tr>
<tr><td rowspan="2">1x37</td><td>COMB_FLT_EN</td><td>R/W</td><td>[7]</td><td>Enable the Comb Filter
0 : Disable
1 : Enable</td><td>1’h0</td></tr>
<tr><td>RESERVED</td><td>R/W</td><td>[6:0]</td><td>Reserved</td><td>7’h0</td></tr>
<tr><td rowspan="5">1x39</td><td rowspan="2">MAN_NOVID</td><td rowspan="2">R/W</td><td>[7]</td><td>Control the No-Video Mode
0 : Auto No-Video Mode
1 : Manual No-Video Mode</td><td>1’h0</td></tr>
<tr><td>[6]</td><td>Select the Manual No-Video Status
0 : No-video Status
1 : Video Status</td><td>1’h0</td></tr>
<tr><td>RESERVED</td><td>R/W</td><td>[5]</td><td>Reserved</td><td>1’h0</td></tr>
<tr><td>HPEAK_MD</td><td>R/W</td><td>[4]</td><td>Control the Horizontal Peaking Frequency Band
0 : 10 ~ 20MHz
1 : 20 ~ 30MHz</td><td>1’h0</td></tr>
<tr><td>HPEAK_GAIN</td><td>R/W</td><td>[3:0]</td><td>Control the Horizontal Peaking Gain for Luminance
<table>
<tr><th>Value</th><th>Gain</th><th>Value</th><th>Gain</th></tr>
<tr><td>0</td><td>Off</td><td>8</td><td>50%</td></tr>
<tr><td>1</td><td>6.25%</td><td>9</td><td>56.25%</td></tr>
<tr><td>2</td><td>12.5%</td><td>10</td><td>62.5%</td></tr>
<tr><td>3</td><td>18.75%</td><td>11</td><td>68.75%</td></tr>
<tr><td>4</td><td>25%</td><td>12</td><td>75%</td></tr>
<tr><td>5</td><td>31.25%</td><td>13</td><td>81.25%</td></tr>
<tr><td>6</td><td>37.5%</td><td>14</td><td>87.5%</td></tr>
<tr><td>7</td><td>43.75%</td><td>15</td><td>93.75%</td></tr>
</table></td><td>4’h0</td></tr>
<tr><td rowspan="2">1x3A</td><td>NR_EN</td><td>R/W</td><td>[7]</td><td>Enable the Noise Reduction
0 : Disable
1 : Enable</td><td>1’h0</td></tr>
<tr><td>RESERVED</td><td>R/W</td><td>[6:5]</td><td>Reserved</td><td>2’h0</td></tr>
</table>

Addr	Name	R/W	Bit	Descriptions	Default
	YLPF_MD	R/W	[4:0]	Control the Cut-off Frequency of Luminance LPF 0 : Bypass 1 : 37.125MHz 2 : 35MHz 3 : 32MHz 4 : 31MHz 5 : 28MHz 6 : 18MHz 7 : 15MHz 8 : 13MHz 9 : 12MHz 10 : 11MHz 11 : 9MHz 12 : 7MHz	5'h0
1x3D	RESERVED	R/W	[7:6]	Reserved	2'h0
	CTI_CORE	R/W	[5:4]	Control the Coring Range for CTI 0 : No Coring 1 : +/- 2 2 : +/- 4 3 : +/- 8	2'h0
	C_CORE	R/W	[3:2]	Control the Coring Range for Chroma Output 0 : No Coring 1 : +/- 2 2 : +/- 4 3 : +/- 8	2'h0
	HPEAK_CORE	R/W	[1:0]	Control the Coring Range for Luminance Horizontal Peaking 0 : No Coring 1 : +/- 2 2 : +/- 4 3 : +/- 8	2'h0
1x3E	MAN_CKIL	R/W	[7:6]	Control the Color Killing Mode Manually 0 ~ 1 : Auto Color Killing Mode 2 : Always Color Alive 3 : Always Color Killed	2'h0
	RESERVED	R/W	[5:4]	Reserved	2'h0

<table>
<tr><th>Addr</th><th>Name</th><th>R/W</th><th>Bit</th><th>Descriptions</th><th>Default</th></tr>
<tr><td></td><td>CLPF_MD</td><td>R/W</td><td>[3:0]</td><td>Control the Cut-off Frequency of Chrominance LPF
0 : Bypass
1 : 9MHz
2 : 8MHz
3 : 6MHz
4 : 5MHz
5 : 4MHz
6 : 3MHz
7 : 2.5MHz
8 : 2MHz</td><td>4'h0</td></tr>
<tr><td rowspan="2">1x3F</td><td>CTI_MD</td><td>R/W</td><td>[4]</td><td>Control the CTI (Chroma Transient Improvement) Frequency Band
0 : 3 ~ 4MHz
1 : 1 ~ 2MHz</td><td>1'h0</td></tr>
<tr><td>CTI_GAIN</td><td>R/W</td><td>[3:0]</td><td>Control the CTI (Chroma Transient Improvement) Gain
<table>
<tr><th>Value</th><th>Gain</th><th>Value</th><th>Gain</th></tr>
<tr><td>0</td><td>Off</td><td>8</td><td>50%</td></tr>
<tr><td>1</td><td>6.25%</td><td>9</td><td>56.25%</td></tr>
<tr><td>2</td><td>12.5%</td><td>10</td><td>62.5%</td></tr>
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<tr><td>6</td><td>37.5%</td><td>14</td><td>87.5%</td></tr>
<tr><td>7</td><td>43.75%</td><td>15</td><td>93.75%</td></tr>
</table></td><td>4'h0</td></tr>
<tr><td rowspan="2">1x40</td><td>PAL_COMP_EN</td><td>R/W</td><td>[7]</td><td>Enable the PAL Chroma Phase Alternating Compensation Mode
0 : Bypass
1 : PAL Phase Alternating Compensation Mode</td><td>1'h0</td></tr>
<tr><td>RESERVED</td><td>R/W</td><td>[6:0]</td><td>Reserved</td><td>7'h0</td></tr>
</table>

Addr	Name	R/W	Bit	Descriptions	Default
1x4D	C_DELAY	R/W	[6:4]	Control the Chrominance Delay Compared to Luminance (2 Pixel Unit) 0 : No Delay ~ 3 : 6 CK Delay ~ 7 : 14CK Delay	3'h0
	Y_DELAY	R/W	[3:0]	Control the Luminance Delay Compared to Chrominance (1 Pixel Unit) 0 : No Delay ~ 8 : 8 CK Delay ~ 15 : 15CK Delay	4'h0
1x4E	MAN_VIN_FMT	R/W	[7:4]	Select the Cascaded Input Pixel Number 0 ~ 7 : Auto Detection Mode 8 : 720 Pixel during H Active Period 9 : 960 Pixel during H Active Period 10 : 1280 Pixel during H Active Period 11 : 1920 Pixel during H Active Period	4'h0
	RESERVED	R/W	[3:2]	Reserved	2'h0
	SD_720H_MD	R/W	[1]	Select the Down Scaler Mode to Convert SD960H to SD 720H 0 : SD960H Mode for SD Video Input 1 : Convert SD960H to SD720H Mode	1'h0
	HD_HALF_MD	R/W	[0]	Select the Down Scaler Mode to Convert HD to HD CIF 0 : HD Full 1 : HD CIF	1'h0
1x4F	BT1120_LIM	R/W	[7]	Select the Data Range of BT1120 Output 0 : 1 ~ 254 Data Range 1 : 16 ~ 240 Data Range	1'h0
	RESERVED	R/W	[6]	Reserved	1'h0
	VIN_BT656_MD	R/W	[5]	Select the Digital Interface Standard for Cascade Input 0 : BT1120 Mode 1 : BT656 Mode	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
	OSG_DIS_EN	R/W	[4]	Select the OSG Overlaid Output Mode 0 : Normal Video Output 1 : OSG Overlaid Video Output	1'h0
	CHID_EN	R/W	[3:2]	Enable the CHID Insertion for Time Multiplexed Video Output [3] : Enable the CHID Insertion in H Blanking Region [2] : Enable the CHID Insertion in BT656/BT1120 Sync Code	2'h0
	NOVID_BT1120	R/W	[1:0]	Control the No-video Flag Mode in BT656/BT1120 Sync Code 0 ~ 1 : No No-video Flag in BT656/BT1120 Sync Code 2 : No-video Flag = 1 in MSB of BT656/BT1120 Sync Code 3 : No-video Flag = 0 in MSB of BT656/BT1120 Sync Code	2'h0
1x50	HD_CSC_MD	R/W	[7:6]	Control the Color Space Converter Mode for HD Video Input 0, 1 : Bypass 2 : BT601 to BT709 3 : BT709 to BT601	2'h0
1x55	PTZ_SLICE_LEVEL	R/W	[7:0]	Control the Threshold Value for PTZ Slicing	8'h0
1xBB	RESERVED	R/W	[7:1]	Reserved	7'h0
	MIPI_DATA_EN	R/W	[0]	Select the Path for Data Output 0 : Parallel Output 1 : MIPI Output	1'h0
1xBC	RESERVED	R/W	[7:5]	Reserved	3'h0
	SYNC_HDELAY	R/W	[4:0]	Select the Active Starting Pixel Delay of H Sync 13'h000 : No Delay 13'h004 : 4 Pixel Delay	13'h0
1xBD		R/W	[7:0]		
1xBE	SYNC_HACTIVE	R/W	[4:0]	Select the Active Pixel Number of H Sync 13'h2D0 : 720 Pixel 13'h500 : 1280 Pixel 13'h780 : 1920 Pixel	13'h0
1xBF		R/W	[7:0]		
1xC0	SYNC_VDELAY	R/W	[4:0]	Select the Active Starting Line Delay of V Sync 13'h000 : No Delay 13'h002 : 2 Line Delay	13'h0
1xC1		R/W	[7:0]		
1xC2	SYNC_VACTIVE	R/W	[4:0]	Select the Active Line Number of V Sync	13'h0

Addr	Name	R/W	Bit	Descriptions	Default
1xC3		R/W	[7:0]	13'h2D0 : 720 Line 13'h320 : 800 Line 13'h3C0 : 960 Line 13'h438 : 1080 Line	

4.2.3. Page 2 Register

Addr	Name	R/W	Bit	Descriptions	Default
2x00	PTZ_RX_PATH_EN	R/W	[7]	Enable the PTZ Receiver Path 0 : Disable or Initialize for PTZ Rx 1 : Enable the PTZ Path	1'b0
	PTZ_RX_START	R/W	[6]	Start the PTZ Rx 0 : Null Operation 1 : Start the PTZ Rx	1'b0
	PTZ_IGNORE_LINE_EN	R/W	[5:4]	Enable the PTZ Receiver Ignore Mode 0 : Disable 1 : Enable	2'd0
	PTZ_IGNORE_FRM_EN	R/W	[3]	Ignore PTZ Receiver Frame 0 : Normal 1 : continuous PTZ Frame Ignore	1'b0
	PTZ_RX_FIELD_POL	R/W	[2]	Select the Field Polarity for PTZ Rx 0 : Even Field High 1 : Odd Field High	1'b0
	PTZ_RX_FIELD_TYPE	R/W	[1:0]	Select the PTZ Rx Field Mode 0 : All 1 : Even Field 2 : Odd Field 3 : Reserved	2'd0
2x01	PTZ_RX_LINE_CNT	R/W	[7:3]	Select the PTZ Receive Line Size / Frame	5'd0
	PTZ_RX_HST_OS	R/W	[2:0]	Select the PTZ Receive Line Starting Offset for Even FLD 0 : + 0 Line Offset 1 : + 1 Line Offset 2 : + 2 Line Offset 3 : + 3 Line Offset 4 : - 0 Line Offset 5 : - 1 Line Offset 6 : - 2 Line Offset 7 : - 3 Line Offset	3'd0
2x02`	PTZ_RX_DATA_POL	R/W	[7]	PTZ Receive Data Inversion 0 :Normal 1 : Inversion	1'b0

Addr	Name	R/W	Bit	Descriptions	Default
	PTZ_RX_HST	R/W	[6:0]	LSB of PTZ_RX_HST PTZ Rx Valid Line Starting Position	7'd0
2x03	PTZ_RX_FREQ_FIRST [23:16]	R/W	[7:0]	MSB of PTZ_RX_FREQ_FIRST[23:0]	8'd0
2x04	PTZ_RX_FREQ_FIRST [15:8]	R/W	[7:0]	Middle Bits of PTZ_RX_FREQ_FIRST[23:0]	8'd0
2x05	PTZ_RX_FREQ_FIRST [7:0]	R/W	[7:0]	LSB of PTZ_RX_FREQ_FIRST[23:0] PTZ Bit-width for 1st Bit Bit-width = 2^24 / (RX_FREQ_FIRST * 148.5M)	8'd0
2x06	PTZ_RX_FREQ	R/W	[7:0]	PTZ_RX_FREQ [23:16]	8'd0
2x07	PTZ_RX_FREQ	R/W	[7:0]	PTZ_RX_FREQ [15:08]	8'd0
2x08	PTZ_RX_FREQ	R/W	[7:0]	PTZ_RX_FREQ [07:00] PTZ Bit-width for All bit's except 1st Bit Bit-width = 2^24 / (RX_FREQ * 148.5M)	8'd0
2x09	RESERVED	R/W	[7:6]	Reserved	2'd0
	PTZ_RX_LPF_LEN	R/W	[5:0]	Select the RX LPF Taps 0 : No Filtering ~ 63 : 63 Taps	6'd0
2x0A	PTZ_RX_H_PIX_OFFSET	R/W	[7:0]	RX H Starting Offset for PTZ Start Bit	8'd0
2x0B	RESERVED	R/W	[7:6]	Reserved	2'd0
	PTZ_RX_LINE_LEN	R/W	[5:0]	Bit Length / Line for PTZ Data	6'd0
2x0C	PTZ_RX_VALID_CNT	R/W	[7:0]	All Byte Length per Command of PTZ Data	8'd0
2x0D	RESERVED	R/W	[7]	Reserved	1'b0
	PTZ_ADDR_HOLD_EN	R/W	[6]	Stop the Auto Increment of Host Register Address and Hold the Address	1'b0
	RESERVED	R/W	[5:0]	Reserved	6'd0
2x0E	RESERVED	R/W	[7:0]	Reserved	8'd0
2x0F	RESERVED	R/W	[7:0]	Reserved	8'd0
2x10	PTZ_WR_ADR_INIT	R/W	[7]	Initialize the FIFO Write Address 0 : Normal Write 1 : Initialize the Write FIFO Address (Auto Cleared)	1'b0
	PTZ_WR_BIT_SWAP	R/W	[6]	Swap the FIFO Write Data Bit 0 : FIFO write with host_wr_data[7:0] 1 : FIFO write with host_wr_data[0:7]	1'b0

Addr	Name	R/W	Bit	Descriptions	Default
	RESERVED	R/W	[5:3]	Reserved	3'd0
	PTZ_FIFO_WR_MD	R/W	[2:0]	Select the Write FIFO Path 0 : Tx Data 1 : Tx Flag Pattern 2 : Tx Flag Data 3 : Reserved (Rx Data) 4 : Rx Flag Pattern 5 : Rx Start Flag Pattern 6 : Rx Start Flag Data	3'd0
2x11	PTZ_FIFO_WR_DATA	R/W	[7:0]	FIFO Write Data	8'd0
2x12	PTZ_TX_QUEUE_SIZE	R	[7:0]	The Status of Remained FIFO Size for PTZ Tx Data	8'h0
2x13	PTZ_FIFO_WR_ADDR	R	[7:0]	Current FIFO Write Address	8'hff
2x14	PTZ_RD_ADR_INIT	R/W	[7]	Initialize the FIFO Read Address 0 : Normal Read 1 : Initialize Read FIFO Address (Auto Cleared)	1'b0
	PTZ_RD_BIT_ SWAP	R/W	[6]	Swap the FIFO Read Data Bit 0 : FIFO read with host_rd_data[7:0] 1 : FIFO read with host_rd_data[0:7]	1'b0
	RESERVED	R/W	[5]	Reserved	
	PTZ_PRE_RD_EN	R/W	[4]	Enable the FIFO Pre-Read 0 : No Pre-read 1 : Enable the Pre-read (Auto Cleared)	1'b0
	RESERVED	R/W	[3]	Reserved	1'b0
	PTZ_FIFO_RD_MD	R/W	[2:0]	Select the Read FIFO Path 0 : Tx Data 1 : Tx Flag Pattern 2 : Tx Flag Data 3 : Rx Data 4 : Rx Flag Pattern 5 : Rx Start Flag Pattern 6 : Rx Start Flag Data	3'd0
2x15	PTZ_RX_QUEUE_SIZE	R/W	[7:0]	The Status of Remained FIFO size for PTZ Rx Data	8'd0
2x16	PTZ_RX_DATA	R	[7:0]	The Read FIFO Data	8'd0
2x17	PTZ_FIFO_RD_ADDR	R/W	[7:0]	Current FIFO Read Address	8'hff
2x18	PTZ_RX_HSYNC_POL	R/W	[7]	Select the Rx HSYNC Polarity	1'b0
2x1A	PTZ_RX_VSYNC_POL	R/W	[7]	Select the Rx VSYNC Polarity	1'b0

Addr	Name	R/W	Bit	Descriptions	Default
2x1C	PTZ_TX_HSYNC_POL	R/W	[7]	Select the PTZ Tx HSYNC Polarity	1'b0
2x1E	PTZ_TX_VSYNC_POL	R/W	[7]	Select the PTZ Tx VSYNC Polarity	1'b0
2x20	PTZ_TX_PATH_EN	R/W	[7]	Enable the PTZ Tx Path 0 : Disable the PTZ Tx Path 1 : Enable the PTZ Tx Path	1'b0
	PTZ_TX_START	R/W	[6]	Start the PTZ Tx 0 : No Start 1 : Start PTZ Tx (Auto cleared when PTZ Tx Started)	1'b0
	RESERVED	R/W	[5:3]	Reserved	
	PTZ_TX_FIELD_POL	R/W	[2]	Select the Field Polarity for PTZ Tx 0 : Even Field is High 1 : Odd Field is High	1'b0
	PTZ_TX_FIELD_TYPE	R/W	[1:0]	Select the PTZ Tx Field Mode 0 : All 1 : Odd Field 2 : Even Field 3 : Reserved	2'd0
2x21	PTZ_TX_LINE_CNT	R/W	[7:3]	PTZ TX Line size per frame	5'd0
	PTZ_TX_HST_OS	R/W	[2:0]	Select the PTZ Transmitter Line Starting Offset for Even FLD 0 : + 0 Line Offset 1 : + 1 Line Offset 2 : + 2 Line Offset 3 : + 3 Line Offset 4 : - 0 Line Offset 5 : - 1 Line Offset 6 : - 2 Line Offset 7 : - 3 Line Offset	3'd0
2x22	PTZ_TX_DATA_POL	R/W	[7]	Select the Data Polarity 0 : Normal 1 : Data Polarity Inversion	1'b0
	PTZ_TX_HST	R/W	[6:0]	Select the PTZ Starting Line Number	8'd0
2x23	PTZ_TX_FREQ_FIRST [23:16]	R/W	[7:0]	MSB of PTZ_TX_FREQ_FIRST[23:0]	8'd0
2x24	PTZ_TX_FREQ_FIRST [15:8]	R/W	[7:0]	Middle Bits of PTZ_TX_FREQ_FIRST[23:0]	8'd0

Addr	Name	R/W	Bit	Descriptions	Default
2x25	PTZ_TX_FREQ_FIRST [7:0]	R/W	[7:0]	LSB of PTZ_TX_FREQ_FIRST[23:0] Tx Bit width for 1st PTZ Tx Bit = 1/148.5M x 2^24 / TX_FREQ_FIRST	8'd0
2x26	PTZ_TX_FREQ [23:16]	R/W	[7:0]	MSB of PTZ_TX_FREQ [23:0]	8'd0
2x27	PTZ_TX_FREQ [15:08]	R/W	[7:0]	Middle Bits of PTZ_TX_FREQ [23:0]	8'd0
2x28	PTZ_TX_FREQ [7:0]	R/W	[7:0]	LSB of PTZ_TX_FREQ [23:0] Tx Bit width except 1st PTZ Tx Bit = 1/148.5M x 2^24 / TX_FREQ	8'd0
2x29	RESERVED	R/W	[7:5]	Reserved	3'd0
	PTZ_TX_HPST[12:8]	R/W	[4:0]	MSB of PTZ_TX_HPST[12:0]	5'd0
2x2A	PTZ_TX_HPST[7:0]	R/W	[7:0]	LSB of PTZ_TX_HPST[12:0] PTZ Tx Starting Location	8'd0
2x2B	RESERVED	R/W	[7:6]	Reserved	2'd0
	PTZ_TX_LINE_LEN	R/W	[5:0]	PTZ Tx Line Length per frame	6'd0
2x2C	PTZ_TX_ALL_DATA_LEN	R/W	[7:0]	All Byte Length per Command of PTZ Tx Data	8'd0
2x40	SPI_PATH_EN	R/W	[7]	Enable the SPI Controller 0 : Disable 1 : Enable	1'h0
	SPI_TX_EDGE	R/W	[5]	Select the Transition Edge for SPI Tx Transfer 0 : Falling Edge 1 : Rising Edge	1'h0
	SPI_RX_EDGE	R/W	[4]	Select the Transition Edge for SPI Rx Transfer 0 : Falling Edge 1 : Rising Edge	1'h0
	SPI_DIVIDER	R/W	[3:0]	Select the Divider Value for SPI Clock 0 : 1/2 of 148.5MHz (74.25MHz) 1 : 1/3 of 148.5MHz (49.5MHz, Recommended) ~ 15 : 1/17 of 148.5MHz (8.7353 MHz)	4'h0
2x41	SPI_CMD0	R/W	[7:0]	Select the 1st Command Data for SPI Control 8'h03 : Normal Single Read 8'h0B : Fast Single Read 8'hBB : Fast Dual I/O Read 8'h02 : Page Program 8'hD7 : Sector Erase	8'h0

Addr	Name	R/W	Bit	Descriptions	Default
2x42	SPI_CMD1	R/W	[7:0]	Select the 2nd Command Data for SPI Control (SPI Address [23:16])	8'h0
2x43	SPI_CMD2	R/W	[7:0]	Select the 3rd Command Data for SPI Control (SPI Address [15:16])	8'h0
2x44	SPI_CMD3	R/W	[7:0]	Select the 4th Command Data for SPI Control (SPI Address [7:0])	8'h0
2x45	SPI_CMD4	R/W	[7:0]	Select the 5th Command Data for SPI Control (Dummy Data) 8'h0F : Recommended to Dual I/O Read	8'h0
2x46	SPI_SINGLE	R/W	[7]	Select the SPI Transfer Mode 0 : SPI Transfer with FIFO 1 : SPI Transfer without FIFO	1'h0
2x46	SPI_DATA_SIZE	R/W	[0]	Select the Byte Size for SPI Transfer 9'h0 : Status Read or Function Write Control 9'h1 : 1 Bytes Data Transfer Mode (RDSR/WRSR) 9'h2 ~ 9'h0FF : 2 ~ 255 Bytes Data Transfer Mode 9'h100 : 256 Bytes Data Transfer Mode ~ : Not support	9'h0
2x47		R/W	[7:0]		
2x48	SPI_RX_MD	R/W	[7]	Select the SPI Transfer Mode 0 : Tx Transfer 1 : Rx Transfer	1'h0
	SPI_CMD_SKIP	R/W	[6]	Select the CMD Skip Mode for SPI Rx Transfer 0 : Normal Transfer 1 : Command Skip for SPI Rx Transfer	1'h0
	SPI_DUAL_A	R/W	[5]	Select the Dual Transfer Mode for Address 0 : Single Transfer Mode 1 : Dual I/O Transfer Mode	1'h0
	SPI_DUAL_D	R/W	[4]	Select the Dual Transfer Mode for Data 0 : Single Transfer Mode 1 : Dual I/O Transfer Mode	1'h0
	SPI_CMD_SIZE	R/W	[2:0]	Select the Command Size for SPI Transfer 3'd0 : Reserved 3'd1 : Single Command (WREN / Chip Erase) 3'd4 : 4 Byte Command (Sector Erase / PP / NORD) 3'd5 : 5 Byte Command (FRD / FRDIO)	3'h0

Addr	Name	R/W	Bit	Descriptions	Default
2x49	SPI_REQ	R/W	[7]	Start the SPI Transfer 0 : Done 1 : Start the SPI Transfer (Automatically cleared after transfer is finished)	1'h0
	SPI_RX_DLY	R/W	[6:4]	Select the Delay of SPI RX Transfer Reserved to "0"	3'h0
	SPI_BUF_PAGE	R/W	[0]	Select the Transfer FIFO Phase for Data Transfer 0 : 0 ~ 255 FIFO Address 1 : 256 ~ 511 FIFO Address	1'h0
2x50	SPI_WR_ADDR_LAT	R/W	[7]	Select the Write FIFO Address Mode 0 : Fixed Write Address (Not Allowed for Burst FIFO Write Mode) 1 : Auto Increment of Write Address	1'h0
	SPI_WR_ADDR_HOLD	R/W	[6]	Select Write I2C Address Hold Mode 0 : Auto increment (Not allowed burst FIFO Write) 1 : Stop Auto increment if I2C Address is 2x52	1'h0
	SPI_ADDR_WR_MD	R/W	[5]	Select the Dual Page Mode for FIFO Write 0 : Single Page Mode (Max Burst Write Size = 256) 1 : Dual Page Mode (Max Burst Write Size = 256x2)	1'h0
	SPI_FIFO_WR_PAGE	R/W	[0]	Select the Write FIFO Address 0 : 0 ~ 255 Address 1 : 256 ~ 511 Address	1'h0
2x51	SPI_FIFO_WR_ADDR	R/W	[7:0]	Select the FIFO Write Starting Address	8'h0
2x52	SPI_FIFO_WR_DATA	R/W	[7:0]	Select the FIFO Write Data	8'h0
2x58	SPI_RD_ADDR_HOLD	R/W	[6]	Select the Write I2C Address Hold Mode 0 : Auto increment (Not Allowed for Burst FIFO Read) 1 : Stop Auto Increment if I2C Address is 2x5A	1'h0
	SPI_ADDR_RD_MD	R/W	[5]	Select the Dual Page Mode for FIFO Read 0 : Single Page Mode (Max Burst Read Size = 256) 1 : Dual Page Mode (Max Burst Read Size = 256x2)	1'h0
	SPI_FIFO_RD_PAGE	R/W	[0]	Select the Read FIFO Address 0 : 0 ~ 255 Address 1 : 256 ~ 511 Address	1'h0
2x59	SPI_FIFO_RD_ADDR	R/W	[7:0]	Select the FIFO Read Starting Address	8'h0
2x5A	SPI_FIFO_RD_DATA	R	[7:0]	Select the FIFO Read Data	8'h0

Addr	Name	R/W	Bit	Descriptions	Default
2x80	OSG_PATH_EN	R/W	[7]	Enable the OSG Controller 0 : Disable 1 : Enable	1'h0
	OSG_INT_MD	R/W	[6]	Select the Field Mode for OSG Overlay 0 : Progressive Mode 1 : Interlace Mode	1'h0
	OSG_TP_EN	R/W	[5]	Enable the Test Patten for OSG Overlay 0 : Normal Video 1 : Enable the Test Pattern	1'h0
	OSG_TP_SEL	R/W	[4]	Select the Type of Test Pattern 0 : Black Test Pattern 1 : Color Bar Test Pattern	1'h0
	RESERVED	R/W	[3]	Reserved to "1"	1'h1
	OSG_HSTRT_OS	R/W	[2:0]	Select the OSG Starting Pixel Offset for OSG Overlay Window 11'h0 : No Offset	11'h0
2x81		R/W	[7:0]		
2x82	OSG_TP_MODE	R/W	[7:4]	Select the Resolution for OSG Test Pattern 4'h0 : 1280x720p@60Hz 4'h1 : 1280x720p@50Hz 4'h2 : 1280x720p@30Hz 4'h3 : 1280x720p@25Hz 4'hA : 1920x1080p@30Hz 4'hB : 1920x1080p@25Hz	4'h0
	OSG_VSTRT_OS	R/W	[2:0]	Select the OSG Starting Line Offset for OSG Overlay Window 11'h0 : No Offset	11'h0
2x83		R/W	[7:0]		
2x84	LUT_AUTO_EN	R/W	[7]	Select the LUT Loading Mode 0 : No Update from SPI Memory 1 : Auto Update from SPI Memory	1'h0
	LUT_AUTO_MD	R/W	[6]	Select the Auto LUT Loading Location 0 : OSG_LUT_LOC 1 : OSG_EVEN/ODD_LOC (LUT 1Kbytes + RLE Structure)	1'h0
	OSG_HACT_SIZE	R/W	[2:0]	Select the OSG Pixel Size for OSG Overlay Window	11'h0

Addr	Name	R/W	Bit	Descriptions	Default
2x85		R/W	[7:0]	11'h2D0 : 720 Pixels 11'h500 : 1280 Pixels 11'h780 : 1920 Pixels	
2x86	ALPHA_MODE	R/W	[7]	Select the OSG Attribute Mode 1'h0 : 8 Bit Alpha Blending Mode 1'h1 : 1 Bit Blink + 7 Bit Alpha Blending Mode	
	OSG_BLINK_EN	R/W	[6:4]	Enable the OSG Blink Mode [6] : OSG Window Blink Mode [5] : OSG Index Blink Mode (Matched with BLINK_INDEX) [4] :OSG Index Bit[7]	3'h0
2x86 2x87	OSG_VSTRT_SIZE	R/W R/W	[2:0] [7:0]	Select the OSG Line Size for OSG Overlay Window 11'h0F0 : NTSC SD 11'h120 : PAL SD 11'h2D0 : 1280x720 HD 11'h438 : 1920x1080 FHD	11'h0
2x88 2x89	OSG_ODD_LOC	R/W R/W	[7:0] [7:0]	Select the OSG Odd Starting Location for SPI Memory Unit = 256 Bytes Address Offset OSG_LOC[15:0] = SPI_ADDR[23:8]	16'h0
2x8A 2x8B	OSG_EVEN_LOC	R/W R/W	[7:0] [7:0]	Select the OSG Even Starting Location for SPI Memory Unit = 256 Bytes Address Offset	16'h0
2x8C 2x8D	OSG_LUT_LOC	R/W R/W	[7:0] [7:0]	Select the OSG LUT Starting Location for SPI Memory Unit = 256 Bytes Address Offset OSG_LOC[15:0] = SPI_ADDR[23:8]	16'h0
2x8E	OSG_BLINK_INDEX	R/W	[7:0]	Define the Blink Index	8'h0
2x8F	OSG_BLINK_PERIOD	R/W	[7:0]	Select the Blink Period 0 : 256 Frame Period (8 or 16 sec) ~ 255 : 2 Frame Period	8'h0
2x90	OSG_CMD_SKIP	R/W	[6]	Select the CMD Skip Mode for SPI Rx Transfer 0 : Normal Transfer 1 : Command Skip for SPI Rx Transfer	1'h0
	OSG_DUAL_A	R/W	[5]	Select the Dual Transfer Mode for Address 0 : Single Transfer Mode 1 : Dual I/O Transfer Mode	1'h0

Addr	Name	R/W	Bit	Descriptions	Default
	OSG_DUAL_D	R/W	[4]	Select the Dual Transfer Mode for Data 0 : Single Transfer Mode 1 : Dual I/O Transfer Mode	1'h0
	OSG_CMD_SIZE	R/W	[2:0]	Select the Command Size for SPI Transfer 3'd0 ~ 3'd3 : Reserved 3'd4 : 4 Bytes Command (NORD) 3'd5 : 5 Bytes Command (FRD / FRDIO)	3'd0
2x91	OSG_CMD0	R/W	[7:0]	Select the 1st Command Data for SPI Control 8'h03 : Normal Single Read 8'h0B : Fast Single Read 8'h3B : Dual I/O Read 8'hBB : Fast Dual I/O Read	8'h0
2x92	OSG_CMD4	R/W	[7:0]	Select the 5th Command Data for SPI Control (Dummy Data) 8'h0F : Recommended to Dual I/O Read	8'h0
2x93	OSG_UP_EN	R/W	[7]	Control the Update Operation for OSG Overlay 0 : Update is Done 1 : Enable the Update (Auto-cleared after update)	1'h0
	OSG_BUF_SIZE	R/W	[0]	Select the Buffer Size for OSG Operation 0 : 256 Bytes Buffer (256 Bytes Buffer can share with Host) 1 : 512 Bytes Buffer (Normal Mode) (SPI FIFO Access by Host is inhibited)	1'h0
2xA0	LUT_WR_DATA0	R/W	[7:0]	Select the Write Data for OSG LUT Cr Information	8'h0
2xA1	LUT_WR_DATA1	R/W	[7:0]	Select the Write Data for OSG LUT Cb Information	8'h0
2xA2	LUT_WR_DATA2	R/W	[7:0]	Select the Write Data for OSG LUT Y Information	8'h0
2xA3	LUT_WR_DATA3	R/W	[7:0]	Select the Write Data for OSG LUT Attribute Information	8'h0
2xA4	LUT_WR_ADDR	R/W	[7:0]	Select the Write Address for OSG LUT	8'h0
2xA8	LUT_RD_ADDR	R/W	[7:0]	Select the Read Address for OSG LUT	8'h0
2xA9	LUT_RD_DATA0	R	[7:0]	Read the Data for OSG LUT Cr Information	8'h0
2xAA	LUT_RD_DATA1	R	[7:0]	Read the Data for OSG LUT Cb Information	8'h0
2xAB	LUT_RD_DATA2	R	[7:0]	Read the Data for OSG LUT Y Information	8'h0
2xAC	LUT_RD_DATA3	R	[7:0]	Read the Data for OSG LUT Attribute Information	8'h0

5. Electrical Characteristics

5.1. DC Electrical Characteristics

Table 12. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit	Condition
Voltage for VDD3V, VDD3P, VDDO Pin	-0.5		4.6	V	
Voltage for VDD1V, VDD1P, VDDI Pin	-0.5		1.8	V	
Voltage for Digital Input Pin	-0.5		3.8	V	
Storage Temperature	-40		125	°C	
Junction Temperature	-40		125	°C	
Peak Temperature on Reflow Soldering			260	°C	15 Sec

NOTE: Long-term exposure to absolute maximum ratings may affect device reliability, and permanent damage may occur if operate exceeding the rating. The device should be operated under recommended operating condition

Table 13. Recommended Operating Conditions for Power and Temperature

Parameter	Min	Typ	Max	Unit	Condition
Voltage for VDD3V, VDD3P	3.0	3.3	3.6	V	
Voltage for VDDO	3.0/1.62	3.3/1.8	3.6/1.98	V	
Voltage for VDD1V, VDD1P, VDDI	1.18	1.25	1.32	V	
Ambient Operation Temperature	-40		105	°C	

Note : Power On/Off sequence should keep the following rule

- Apply power to VDD3V, VDD3P, VDDO and VDD1V, VDD1P, VDDI at the same time
- If it is difficult to apply the power to these pins at the same time, apply the power to VDD3V, VDD3P, VDDO first and to VDD1V, VDD1P, VDDI later
- Cut the power of VDD3V, VDD3P, VDDO and VDD1V, VDD1P, VDDI at the same time
- If it is difficult to cut the power of these pins at the same time, cut the power of VDD1V, VDD1P, VDDI first and of VDD3V, VDD3P, VDDO later

Table 14. Recommended Operating Conditions for Digital I/O

Parameter	Min	Typ	Max	Unit	Condition
Digital Inputs					
Input High Voltage	2.0		3.6	V	
Input Low Voltage	-0.3		0.8	V	
Input Capacitance		6		pF	
Input Leakage Current			±10	uA	
Digital Output					
Output High Voltage	2.4			V	
Output Low Voltage			0.4	V	
High Level Output Current	9.2	19.6	30.8	mA	Voh = 2.4V
Low Level Output Current	8.0	12.4	15.6	mA	Vol = 0.4V
Tri-state Output Current			±10	uA	
Output Capacitance		6		pF	

Table 15. Supply Current and Power Dissipation

Parameter	Parallel			MIPI			Unit
	Min	Typ	Max	Min	Typ	Max	
Supply Current at VDD3V (3.3V)	6	7	8	6	7	8	mA
Supply Current at VDD1V (1.25V)	29	31	33	29	31	33	mA
Supply Current at VDD3P (3.3V)	1	1	1	1	1	1	mA
Supply Current at VDD1P (1.25V)	3	3	3	3	3	3	mA
Supply Current at VDDO (3.3V / 1.8V)	40 / 12	45 / 16	50 / 20	21 / 21	23 / 23	25 / 25	mA
Supply Current at VDDI (1.25V)	93	98	102	93	98	102	mA
Power Dissipation for 3.3V VDDO	289	340	395	232	267	305	mW
Power Dissipation for 1.8V VDDO	188	220	254	232	267	305	mW

5.2. AC Electrical Characteristics

Table 16. Analog Input and Output Parameter

Parameter	Symbol	Min	Typ	Max	Unit
Video ADCs					
Differential Non-Linearity	DLE		± 0.5	± 1	
Integral Non-Linearity	ILE		± 1	± 3	
Signal-to-Noise Ratio	SNR	50	55		dB
Analog Clock PLL					
RMS Jitter	rms_{pll}		8		ps
Duty Cycle	dt_{pll}	45		55	%
Lock Time	t_{lock}		50		us
Crystal Input					
Nominal Frequency	$f_{x\text{-}tal}$		27		MHz
Frequency Deviation	$\Delta f_{x\text{-}tal}$	-50		50	ppm
Duty Cycle	$dt_{x\text{-}tal}$			55	%

Table 17. Serial Host Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
Bus free time between STOP and START	t1	1.3			us
Data Hold time	t2	0		0.9	us
Data Setup time	t3	0.1			us
Setup time for a(repeated) START condition	t4	0.6			us
Setup time for a STOP condition	t5	0.6			us
Hold time (repeated) START	t6	0.6			us
Rise time SDA and SCL signal	t7			250	ns
Fall time SDA and SCL signal	t8			250	ns
Capacitive load for each bus line	C_b			400	pF
I^2C Clock frequency	f_{I2C}			400	KHz

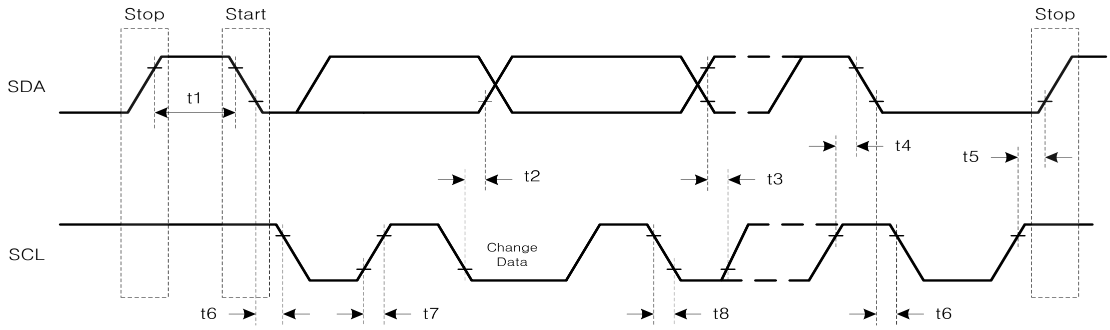


Fig 21. Serial Host Interface Timing Diagram

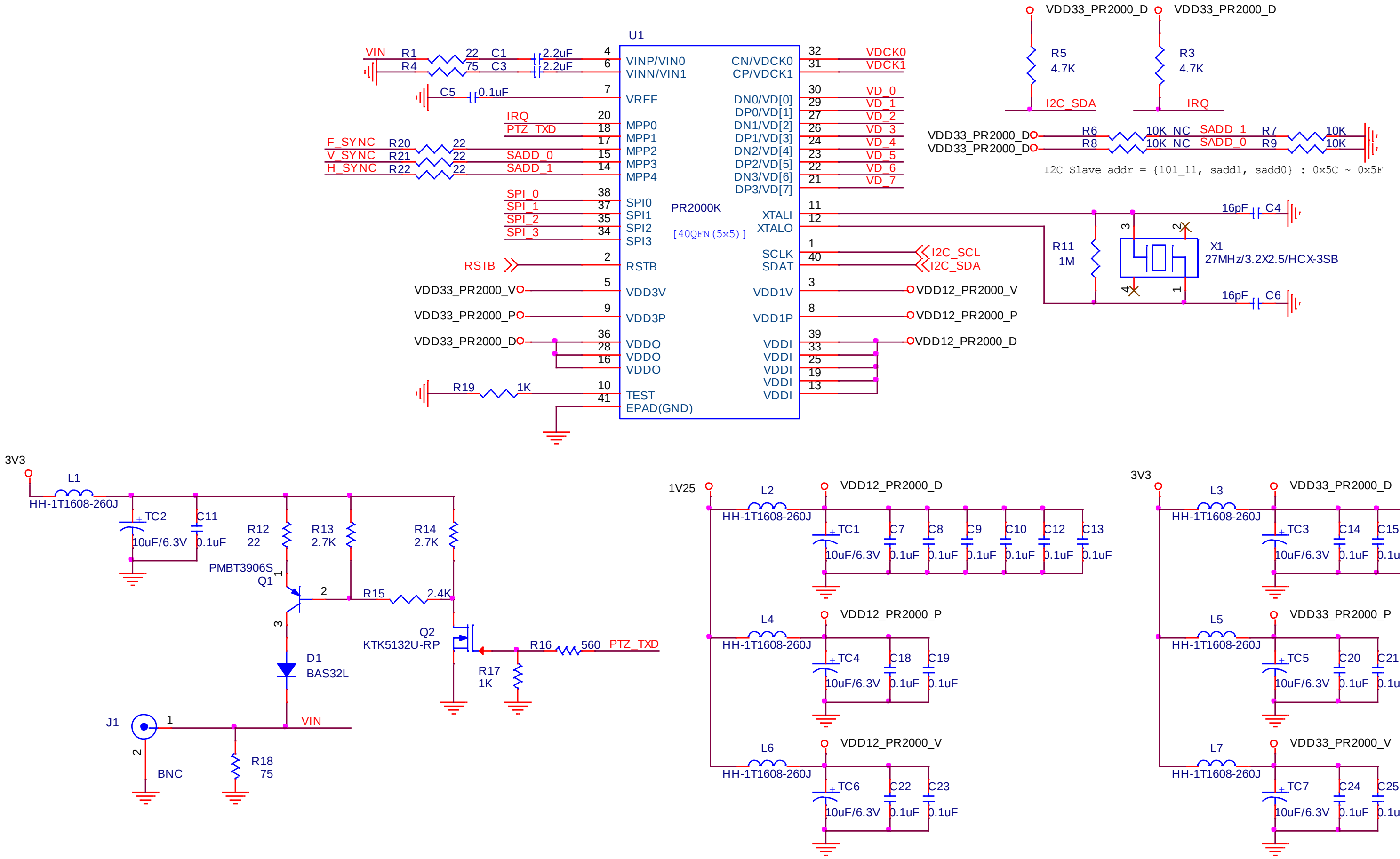
Table 18. MIPI LP Transmitter Timing

Parameter	Symbol	Min	Typ	Max	Unit
15% ~ 85% rise/fall time	t_{RLP}/t_{FLP}			25	ns
30% ~ 85% rise time in EOT state	t_{REOT}			35	ns
Slew rate	dV/dt_{SR}			120	mV/ns
Load capacitance	C_{LOAD}	0		70	pF
Thevenin output low level	V_{OL}	-50		50	mV
Thevenin output High level	V_{OH}	1.1	1.2	1.3	V
Output Impedance	Z_{OLP}	110			Ohm

Table 19. MIPI HS Transmitter Timing

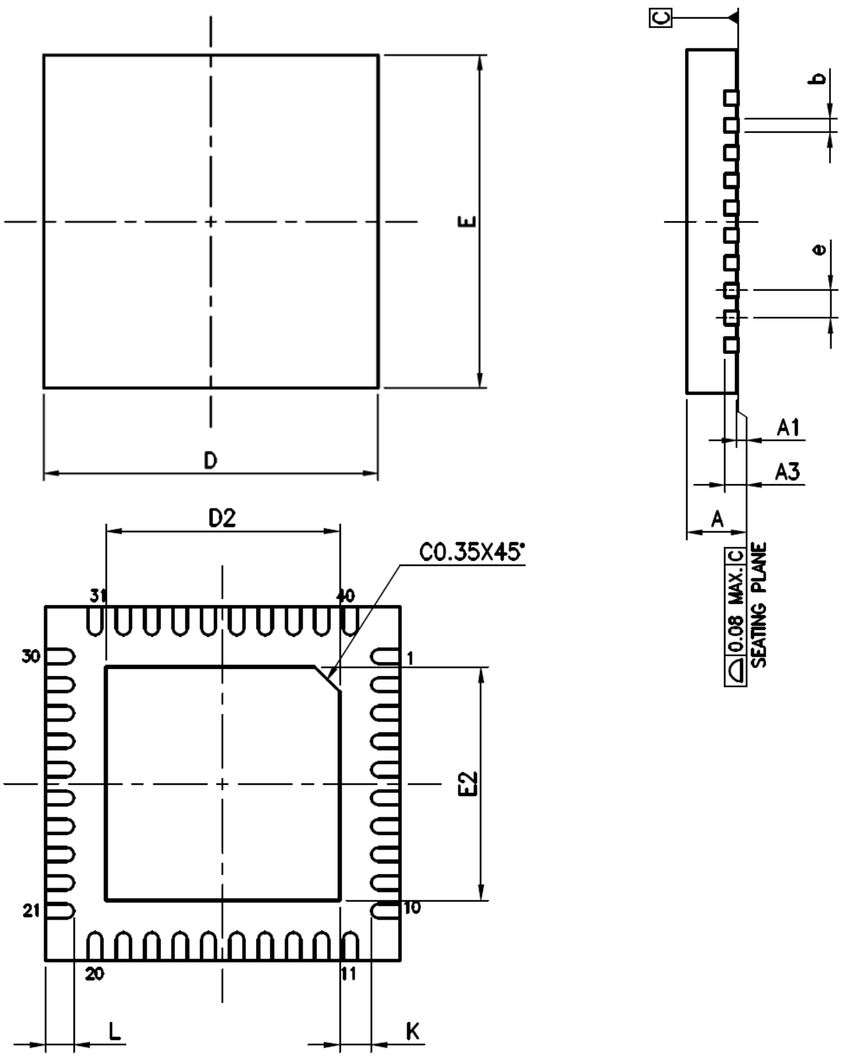
Parameter	Symbol	Min	Typ	Max	Unit
20% ~ 80% rise/fall time	t_R/t_F	150		0.3UI	ps
HS transmit differential voltage	V_{OD}	140	200	270	mV
HS transmit static common mode voltage	V_{CMTX}	150	200	250	mV
V_{OD} mismatch when output is Differntial-1 or Differntial-0	ΔV_{OD}			10	mV
V_{CMTX} mismatch when output is Differntial-1 or Differntial-0	ΔV_{CMTX}			5	mV
HS output high voltage	V_{OHHS}			360	mV
Single ended output impedance	Z_{OS}	40	50	62.5	Ohm
Single ended output impedance mismatch	ΔZ_{OS}			10	%
Common-level variation for 50~450MHz	ΔV_{CMTX}			25	mV

6. Application Schematic



7. Package Specification

40Pin QFN Package Mechanical Drawing



SYMBOLS	DIMENSION		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	5.00 BSC		
E	5.00 BSC		
e	0.40 BSC		
K	0.20	-	-
D2	3.25	3.30	3.35
E2	3.25	3.30	3.35
L	0.35	0.40	0.45

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

8. Revision History

Version	Date	Description
V0.0	2016.12.26	Preliminary datasheet is released
V0.1	2017.01.20	1. Pin Name is Revised (P.8 ~ 9) 2. Power Dissipation is Updated (P.82)
V0.2	2017.04.12	1. Update the Chip Cascaded Connection (P.21) 2. Voltage for VDD1V, VDD1P, VDDI is changed from 1.2V to 1.25V (P.82, P.87) 3. Change the Storage Temperature (P.82) 4. Add the Power Up/Down Sequence (P.82) 5. Update the Power Dissipation (P.83)
V0.3	2017.04.25	1. Update the Application Schematic (P.87)
V0.31	2017.05.02	1. Add the VIN_IN_SEL Register Description (P.46)
V0.32	2017.06.14	1. Recommended Operating Condition for 1.8V is Updated (P.82) 2. Power Dissipation for 1.8V IO Voltage is Updated (P.83)