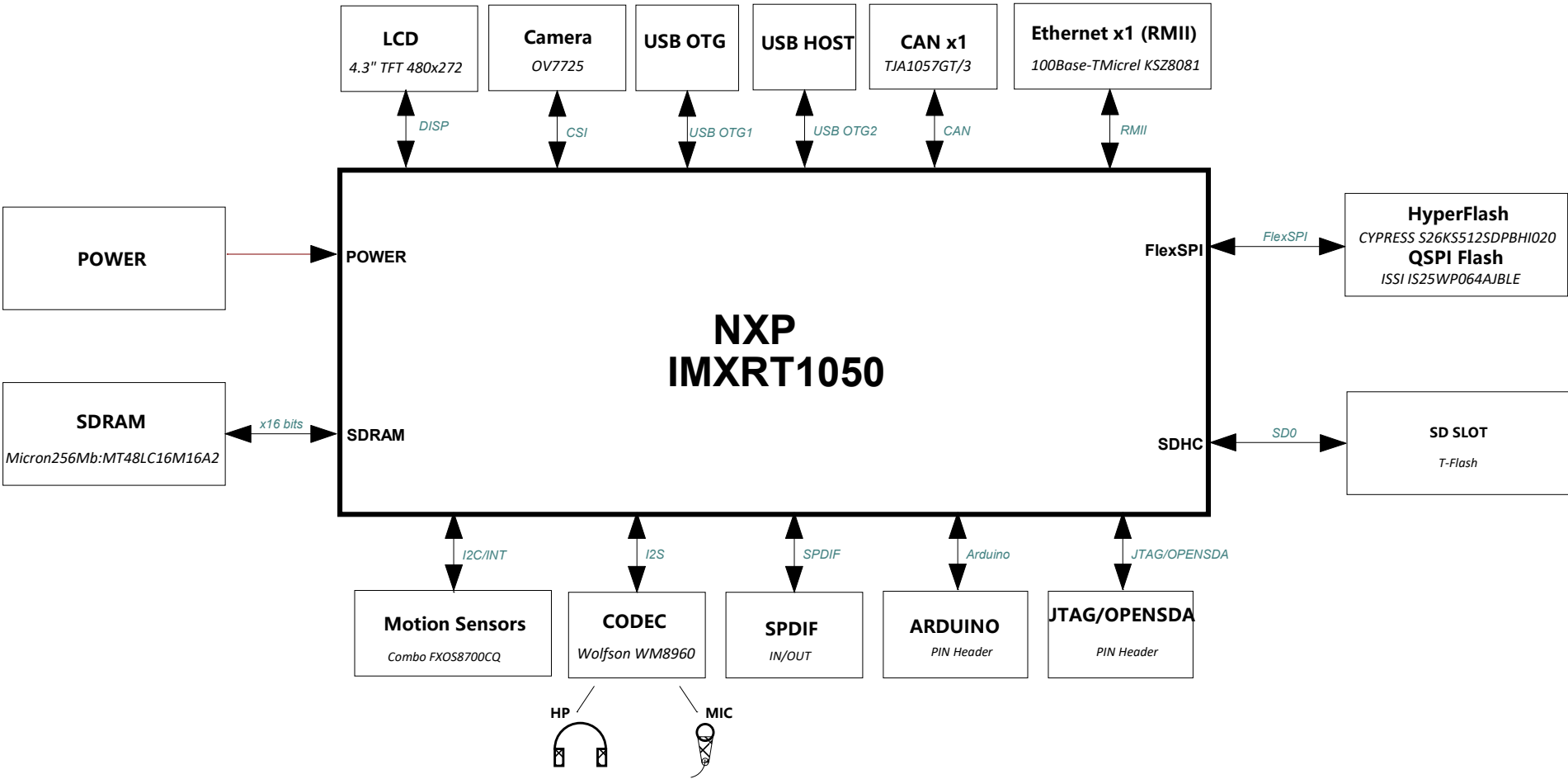
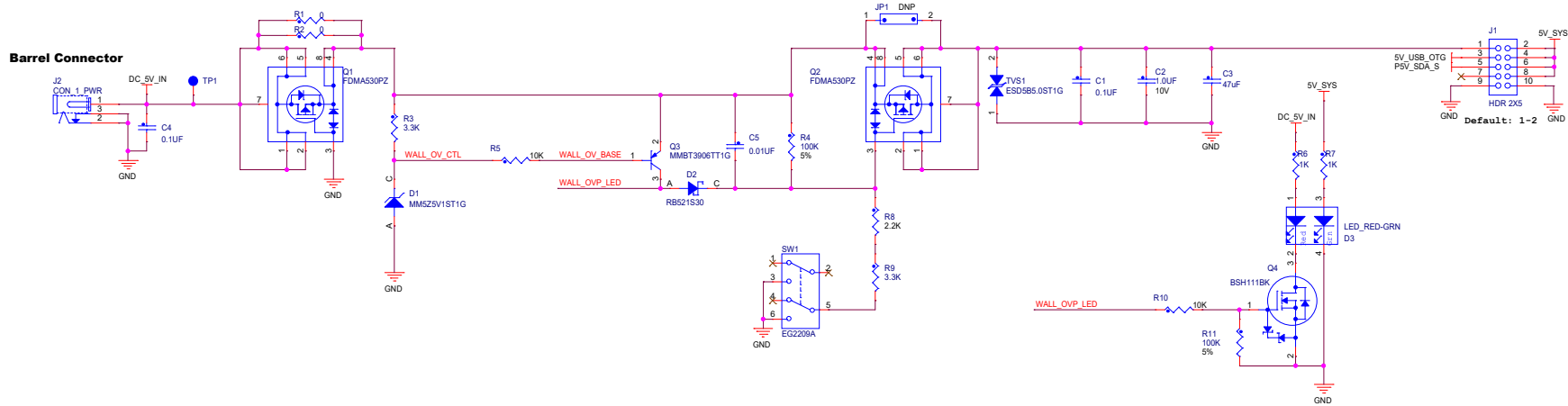




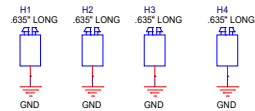
**IMXRT1050-EVKB**



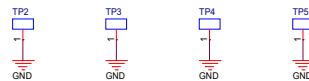
# Main Power



# Board Mounting Holes



# Ground TPs



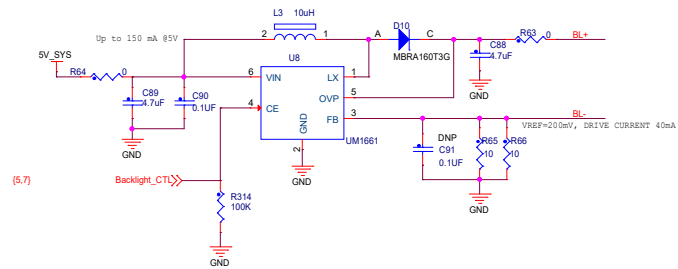
Layout Note: Place Ground TPs to assist signal measurement.

ICAP Classification: CP: IUC: X PUBI:			
Drawing Title: <b>IMXRT1050-EVKB</b>			
Page Title: <b>MAIN POWER</b>			
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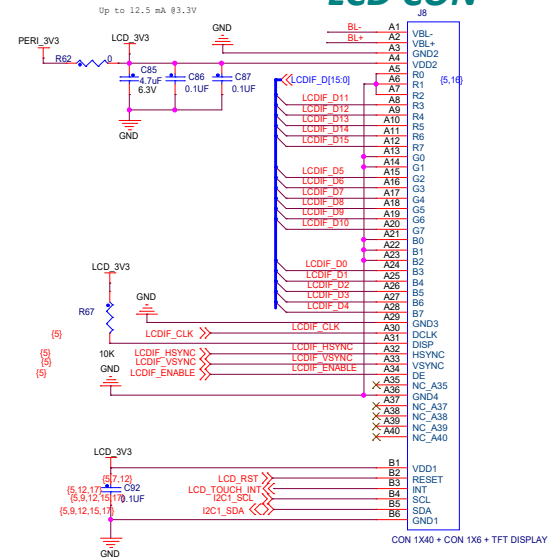




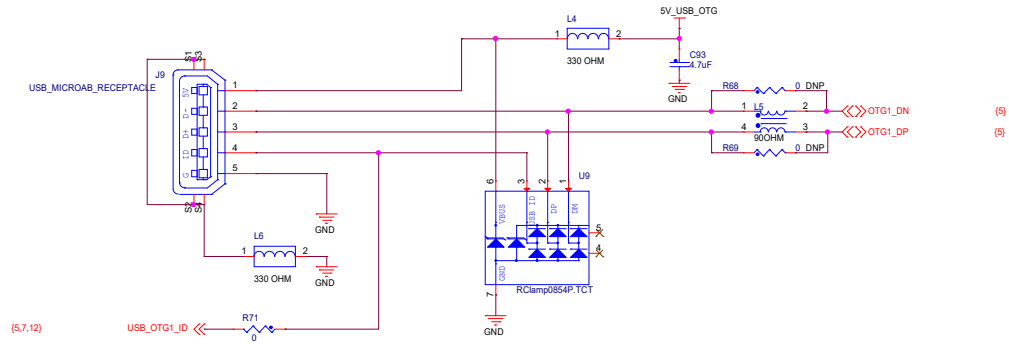
## Backlight Control



## LCD CON

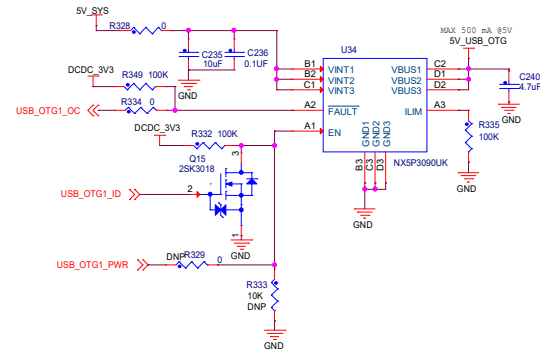


## USB OTG



(5.7.12)

## USB POWER

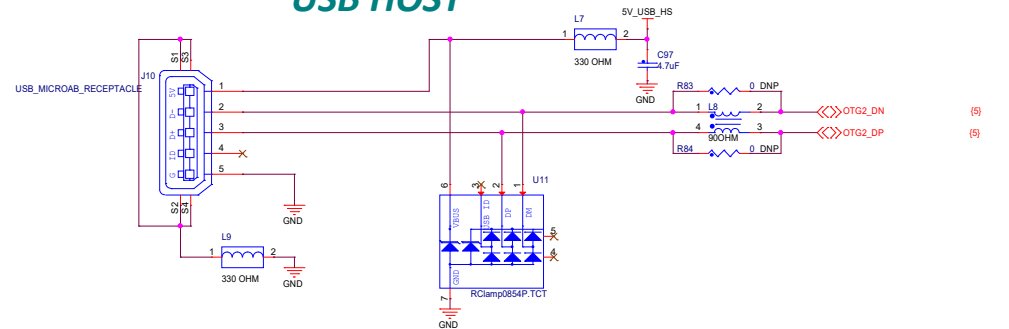


(5.12)

(5.7.12)

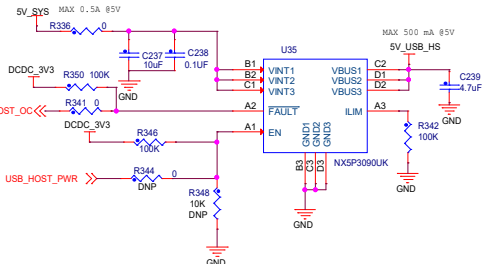
(5.6.12)

## USB HOST



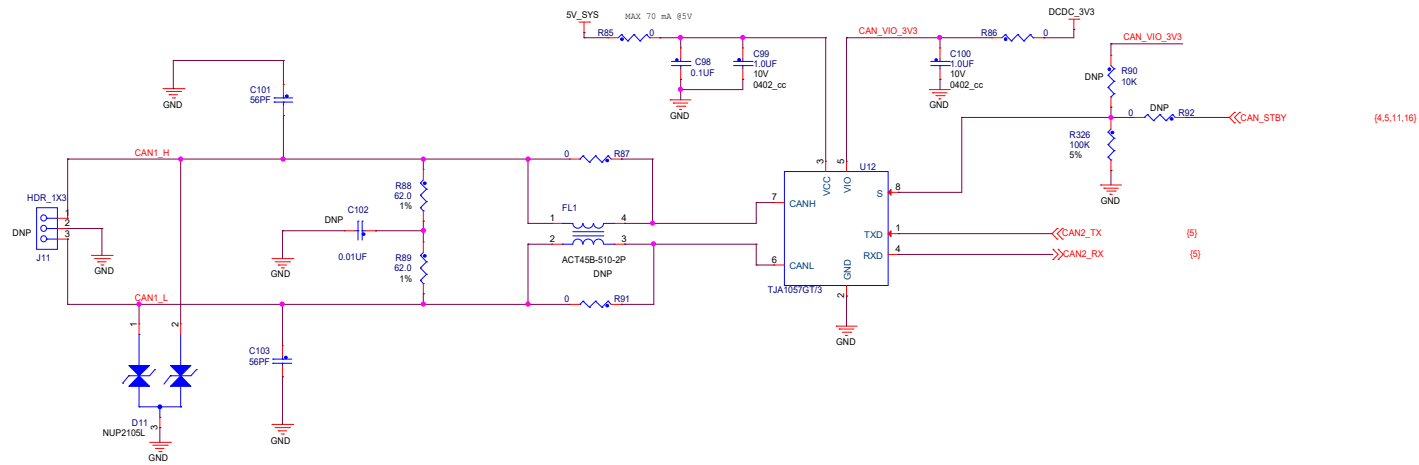
(5.12)

(5.6)



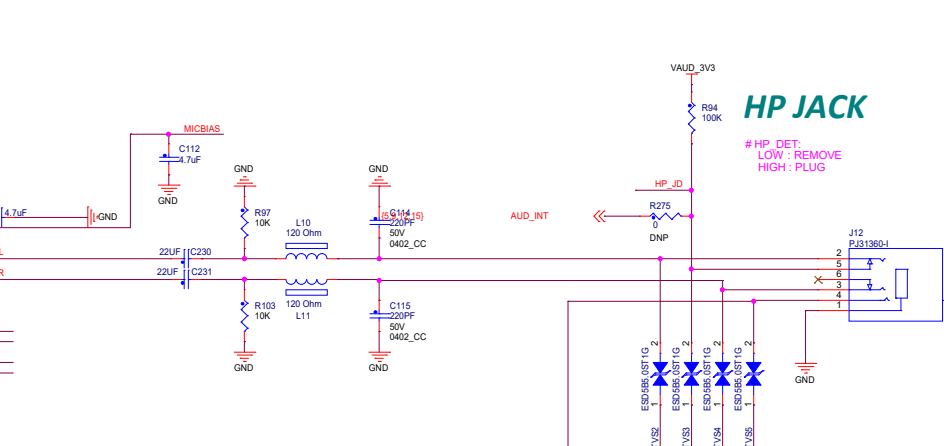
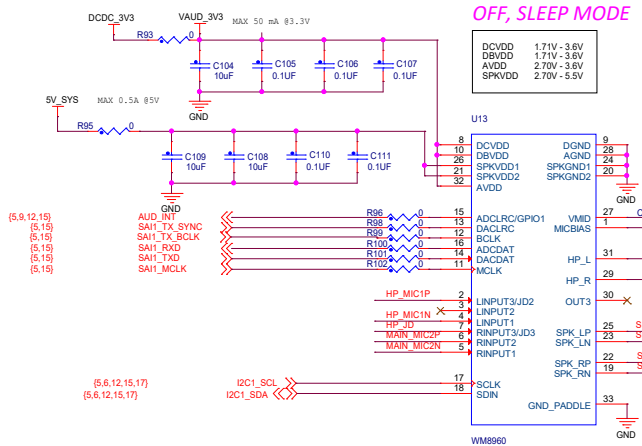
ICAP Classification: CP: IUC: X PUBL:			
<b>IMXRT1050-EVKB</b>			
Page Title: <b>USB</b>			
Size C	Document Number	SCH-30168, PDF: SPF-30168	Rev A1
Date:	Wednesday, February 28, 2018	Sheet 7 of 17	

# CAN BUS

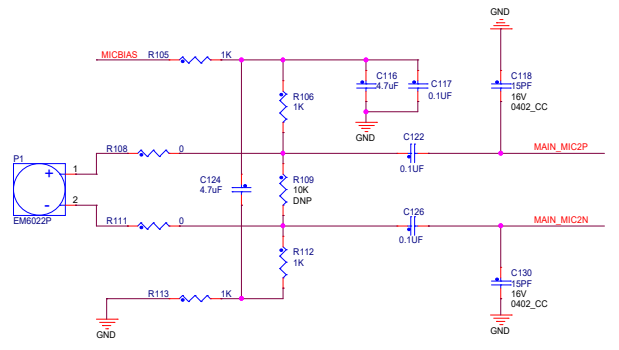


ICAP Classification: CP: IUC: X PUB:			
Drawing Title: <b>IMXRT1050-EVKB</b>			
Page Title: <b>CAN</b>			
Size C	Document Number SCH-30168, PDF: SPF-30168	Rev A1	
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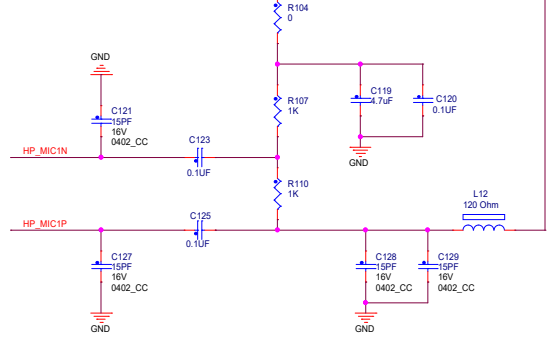




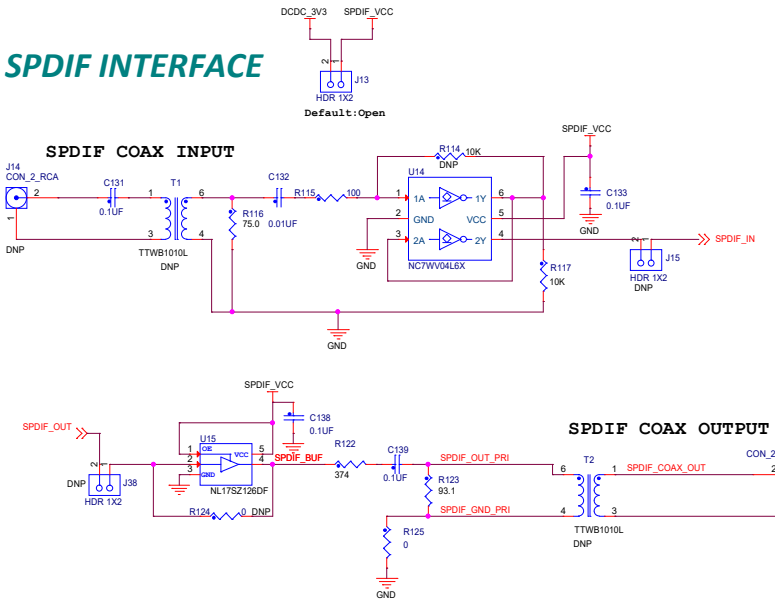
**Main Board MIC**



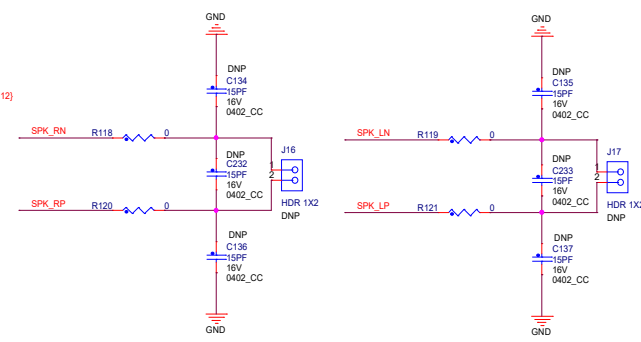
**HP MIC**



**SPDIF INTERFACE**



**Speaker**

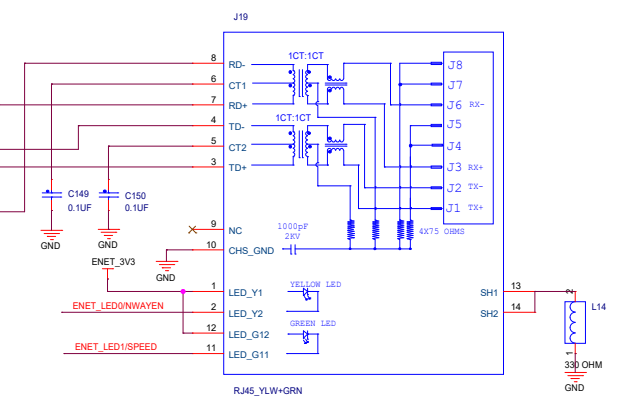
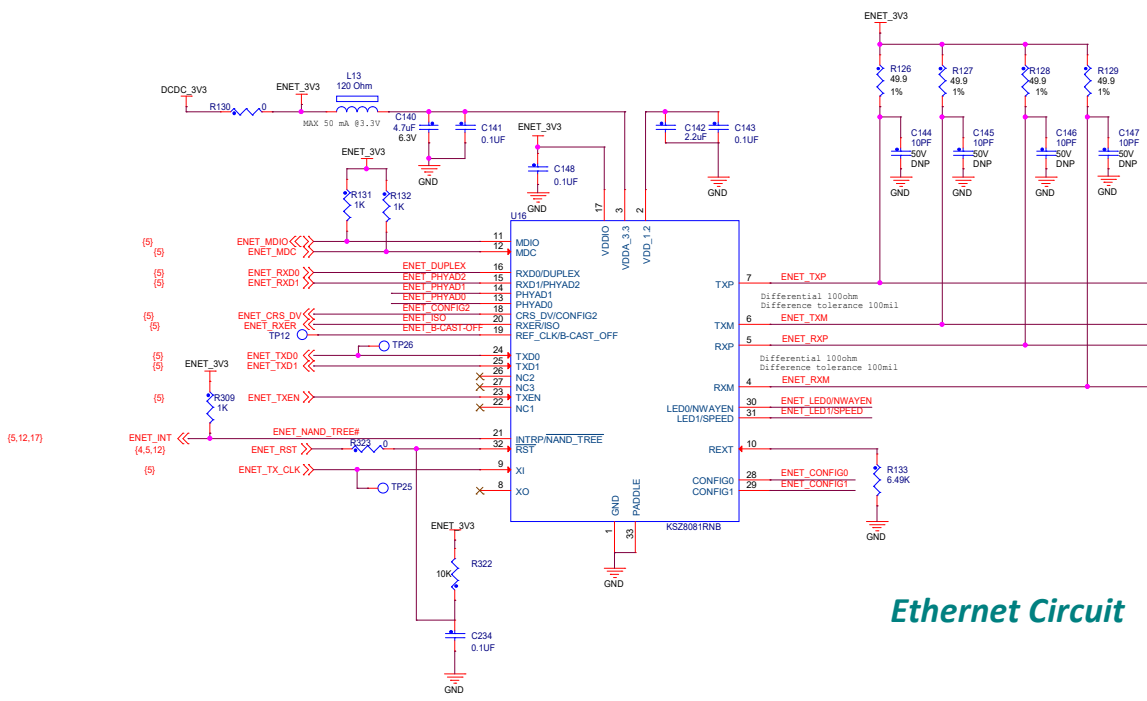


ICAP Classification: CP, IUC, X, PUBI

Drawing Title: **IMXRT1050-EVKB**

Page Title: **AUDIO**

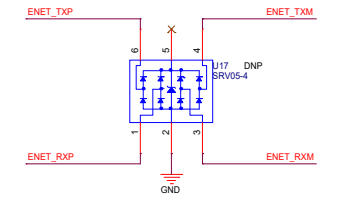
Size C	Document Number SCH-30168, PDF-SPF-30168	Rev A1
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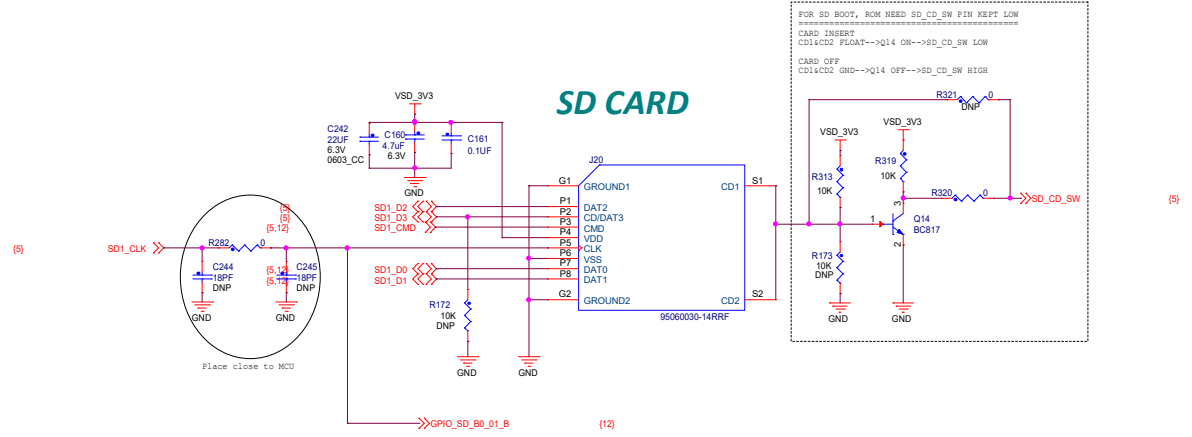


### Ethernet Circuit

# CFG	Description	# CFG	Description
PHYAD[2:0]	PHY ADDR 00-XXX (00010 DEFAULT)	DUPLEX	DUPLEX mode Pull-up (default) = Half Duplex Pull-down = Full Duplex
CONFIG[2:0]	IF MODE 001 RMII 101 RMII Back-to-Back xxx Reserved-not used	NWAYEN	Nway Auto-Negotiation Pull-up (default) = Enable Pull-down = Disable
ISO	ISOLATE mode Pull-up = Enable Pull-down (default) = Disable	B_CAST_OFF	Broadcast Off - for PHY Address 0 Pull-up = PHY Address 0 set as unique PHY addr Pull-down (default) = PHY Address 0 set as broadcast PHY addr
SPEED	SPEED mode Pull-up (default) = 100Mbps Pull-down = 10Mbps	NAND_TREE#	NAND Tree Mode Pull-up (default) = Disable Pull-down = Enable

### ESD PROTECTION

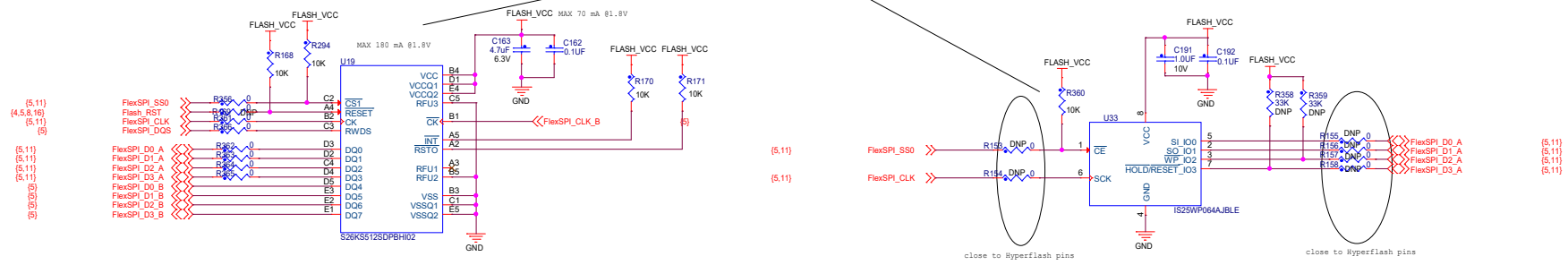




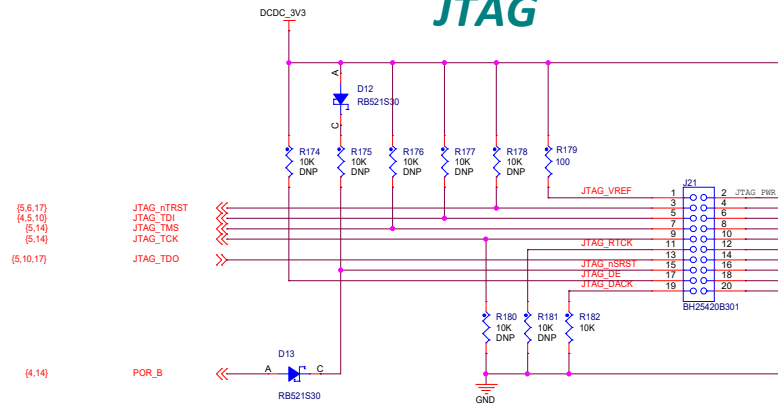
OPTION1: USE Hyperflash (by default)  
OPTION2: USE QSPI FLASH (Mount R153~R158, DNP R356, R361~R366)

## 1V8 HyperFlash

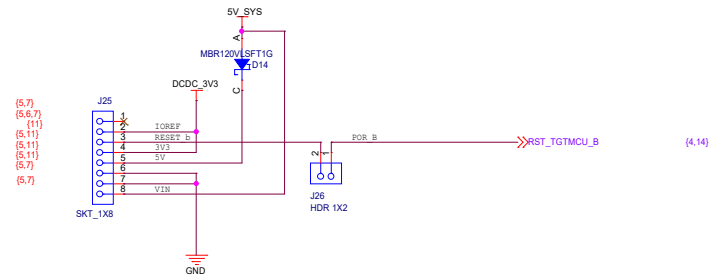
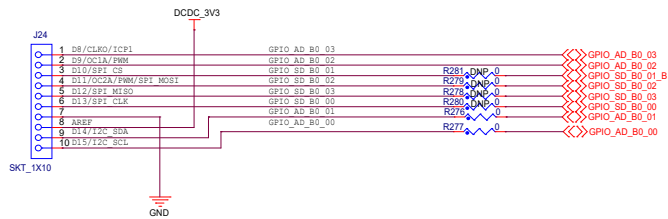
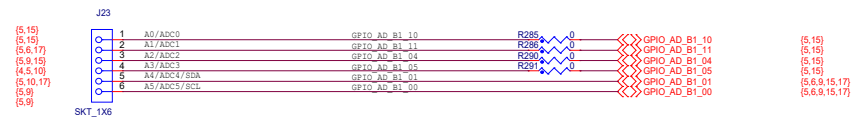
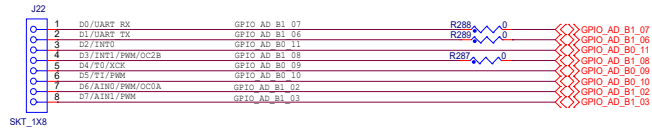
## 1V8 QSPI Flash



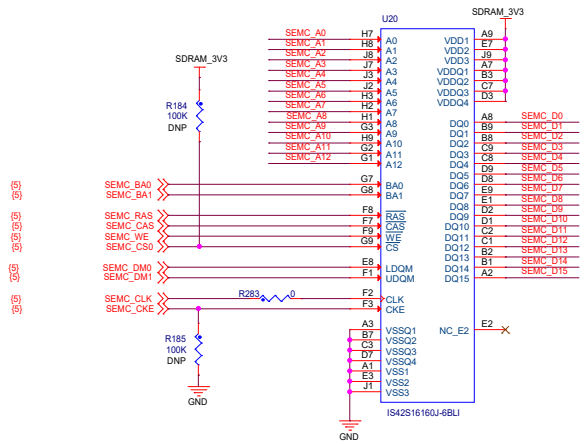
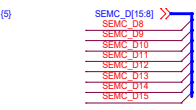
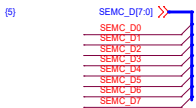
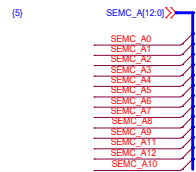
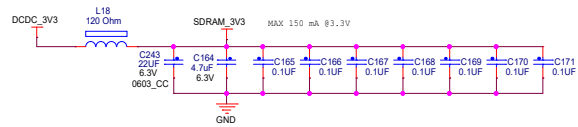
# JTAG



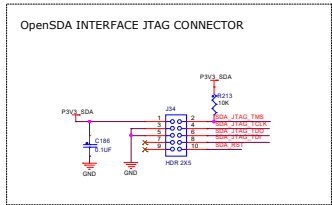
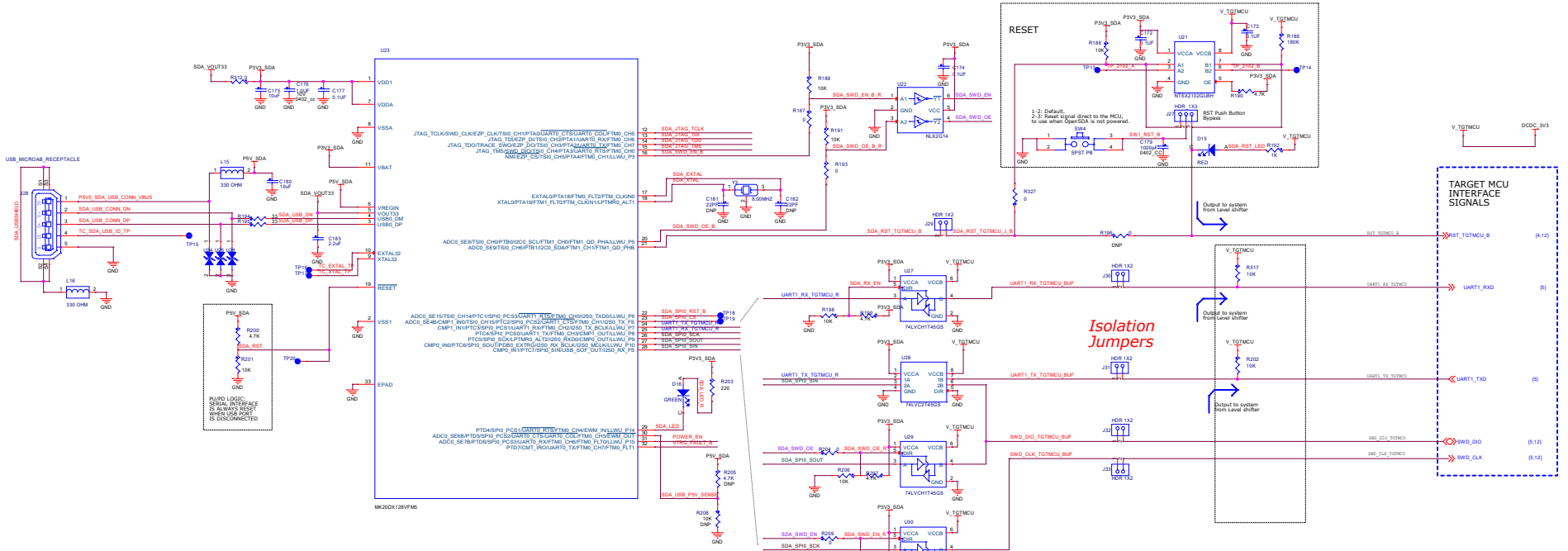
# Arduino Interface



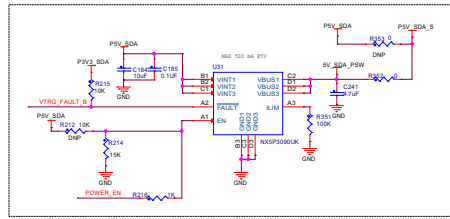
# SDRAM



# OpenSDA Interface



**PWR SWITCH**  
(To enable 5v from USB connector)

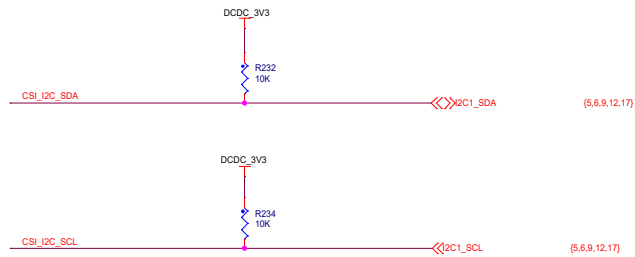
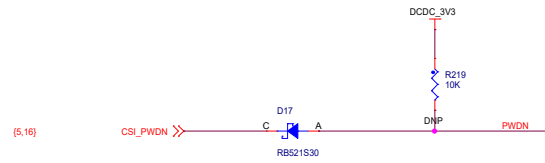


**Isolation and level shift stage**  
(for 1.8 to 3V compatibility)

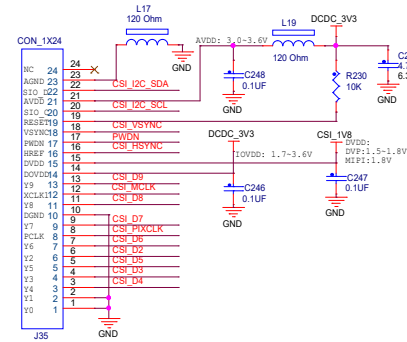
**PWR\_SWITCH\_USB**  
(To enable 5v from USB connector)


## Camera Signals

CSI_PIXCLK	R217	0	GPIO_AD_B1_04	(5,12)
CSI_MCLK	R218	0	GPIO_AD_B1_05	(5,12)
CSI_VSYNC	R220	0	GPIO_AD_B1_06	(5,12)
CSI_PSYNC	R221	0	GPIO_AD_B1_07	(5,12)
CSI_D9	R222	0	GPIO_AD_B1_08	(5,9,12)
CSI_D8	R223	0	GPIO_AD_B1_08	(5,9)
CSI_D7	R224	0	GPIO_AD_B1_10	(5,12)
CSI_D6	R225	0	GPIO_AD_B1_11	(5,12)
CSI_D5	R226	0	GPIO_AD_B1_12	(5,9)
CSI_D4	R227	0	GPIO_AD_B1_13	(5,9)
CSI_D3	R228	0	GPIO_AD_B1_14	(5,9)
CSI_D2	R229	0	GPIO_AD_B1_15	(5,9)



## FPC FOR MT9M114/OV7725 MODULE

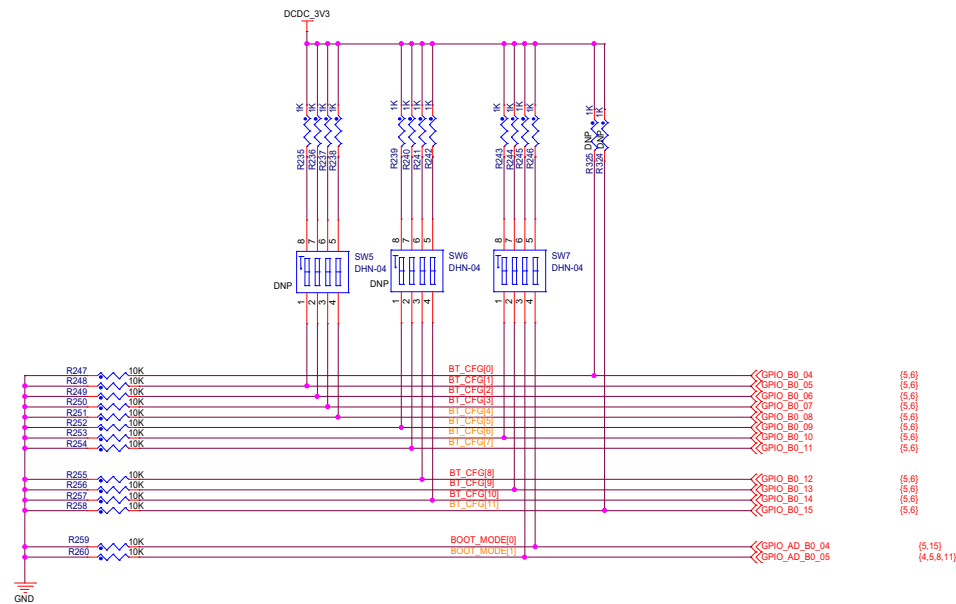





ICAP Classification: CP: _____ IUC: X PUI: _____			
Drawing Title: <b>IMXRT1050-EVKB</b>			
Page Title: <b>CSI</b>			
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# FUSE MAP

TYPE	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]	BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]
<b>FlexSPI - Serial NOR</b>	Infinit-Loop: (Debug USE only) 0 - Disable 1 - Enable	FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR			0	0	0	0	HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		EncryptedXIP 0 - Disabled 1 - Enabled	Reserved
<b>SD</b>	Infinit-Loop: (Debug USE only) 0 - Disable 1 - Enable	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	SD1 VOLTAGE SELECTION: 0 - 3.3V 1 - 1.8V	0	1		SD/SDXC Speed: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104	SD Power Cycle Enable: '0' - No power cycle '1' - Enabled via USDHC_RST pad	SD Loopback Clock Source Sel: (for SDR50 and SDR104 only) '0' - through SD '1' - direct	Port Select: 0 - eSDHC1 1 - eSDHC2	Fast Boot: 0 - Regular 1 - Fast Boot

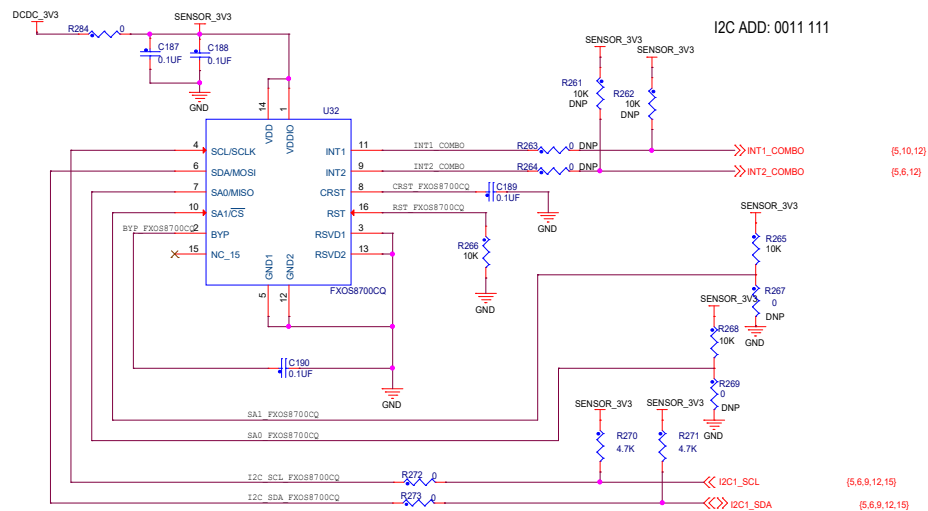




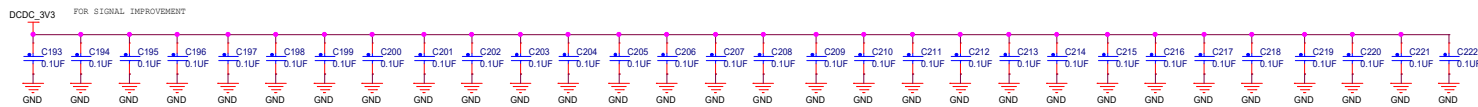
ICAP Classification: CP: _____ IUC: X PUI: _____			
Drawing Title: <b>IMXRT1050-EVKB</b>			
Page Title: <b>BOOT</b>			
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# COMBO SENSOR



## FXOS8700CQ COMBO SENSOR



ICAP Classification: CP: IUC: X PUB:	
Drawing Title: <b>IMXRT1050-EVKB</b>	
Page Title: <b>MISC</b>	
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