

MAD Modular Platform : Rita SMD Board

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Revision History

Rev. Code	Date	By	Description
1	2010/11/05	Song	Rev A Release
2	2010/12/03	Song	Change BOOT MODE CFG Volt DNP R559 Change HDMI PIN for MiniHDMI (TYPE C) Leave Open on U80.3 Change BT_HOST_WAKE to GPIO19 Change R57 to 499K ohm Change R944 to 0ohm Add R130 for ZigBee SATA power on default RM SW33 Change J35 to TH Add power LED Add OSC for PMIC DA9053 Add U44 for SATA Boot power control Add R436,R434 for PMIC LD01 input Add PMIC_STBY to PMIC Add U81 for ZigBee debug Change I2C2 to LVDS0 Add RC circuit for U50
3	2010/12/31	Song	Rev B Release

1. Unless Otherwise Specified:


All resistors are in ohms, 10%, 1/8 Watt, 0603
All capacitors are in uF, 20%, 50V, 0603
All voltages are DC
All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

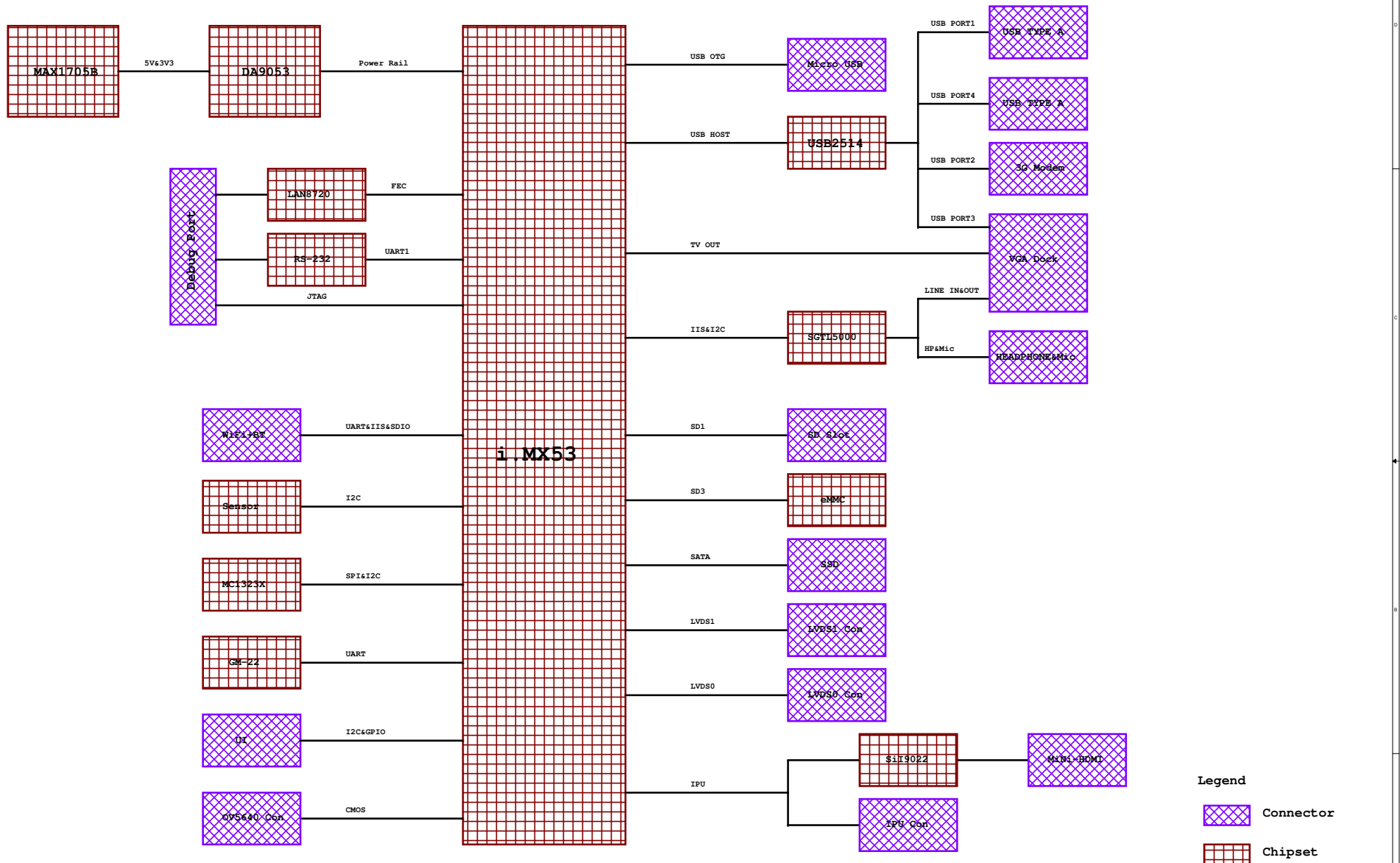
3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
_B Denotes - Active-Low Signal
<> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.


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Drawn by: <DrawnBy>	Page Title: COVER		
Approved: <Approve>	Size C	Document Number SOURCE: SCH-26876 PDF: SPF-26876	Rev B
Date: Monday, January 10, 2011		Sheet 1 of 25	

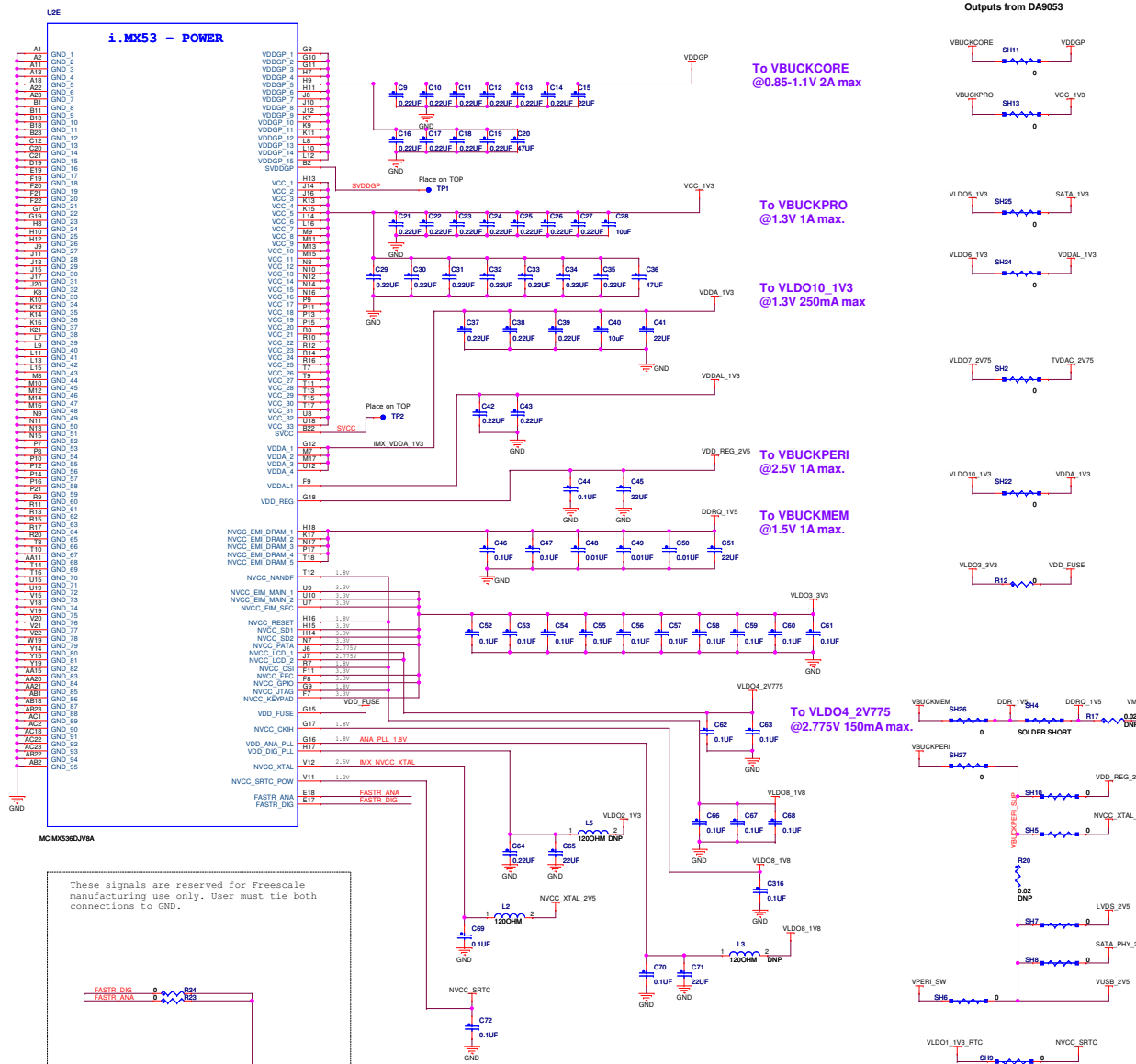
MCIMX535-SMD



Legend

 Connector

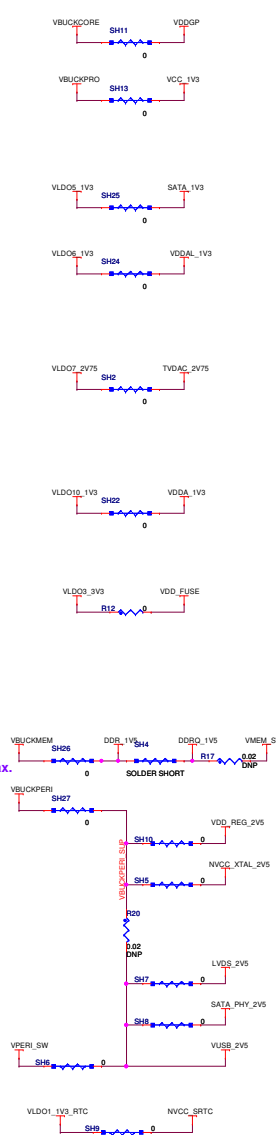
 Chipset



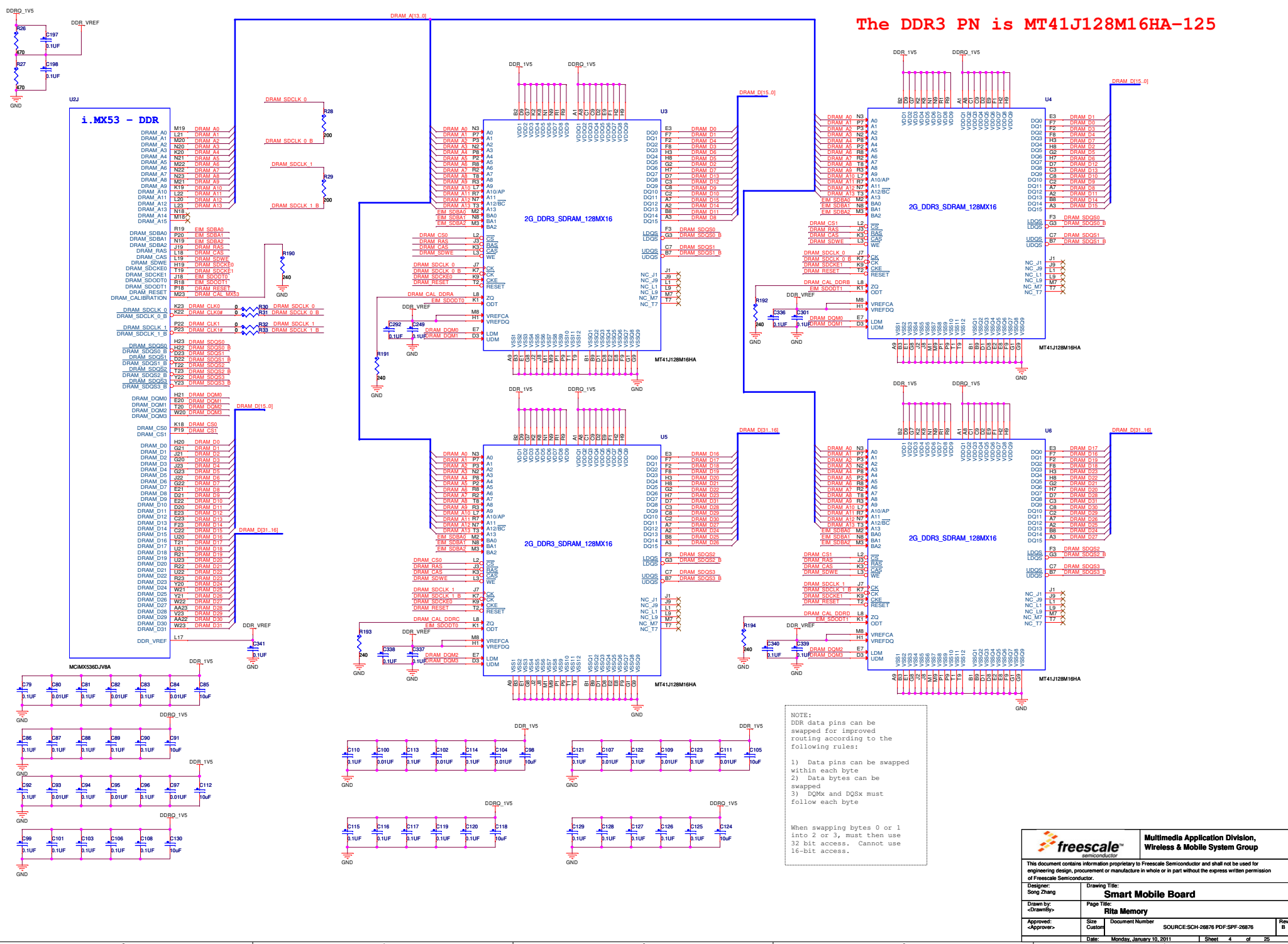
Power Sequence on current board

Power Table				
DOMAIN	VOLTAGE	MODULE	SUBSYSTEM	BOOT TIMING
DCDC_5V	5V		PMIC DCDC_3V3 DISPLAY_LEDS USB_HOST_PWR VGA_OUTPUT	ALWAYS ON
VLDO1	1V3	NVCC_SRTC		ALWAYS ON
VBUCKPRO	1V3	VCC		19 mSEC
VBUCKPERI	2V5	VDD_REG NVCC_XTAL		23 mSEC
VLDO5	1V3		SATA_1V3	23 mSEC
VLDO6	1V3	VDDAL		23 mSEC
VLDO8	1V8	NVCC_RESET NVCC_JTAG NVCC_CKIH NVCC_NANF NVCC_CSI VDD_DIG_PLL	BOOT_SEL	23 mSEC
VLDO10	1V3	VDDA		23 mSEC
VBUCKCORE	1V15	VDDGP		27 mSEC
VBUCKMEM	1V5	NVCC_EMI_DRAM	DDR3	31 mSEC
VLDO2	1V3	VDD_ANA_PLL		31 mSEC
VBUCKPERI /SW	2V5		LVDS_2V5 SATA_PHY_2V5 USB_2V5	35 mSEC
VLDO4	2V775	NVCC_LCD1&2 VIOHI		35 mSEC
VLDO7	2V75	TVDAC	VGA	35 mSEC
VLDO3	3V3	NVCC_EIM_MAIN NVCC_EIM_SEC NVCC_SD1&2 NVCC_PATA NVCC_FEC NVCC_GPIO NVCC_KEYPAD VDD_FUSE	SD1 I2C1&2 BOOT_SEL	64 mSEC
VLDO9	1V5		EXP_HDR	64 mSEC

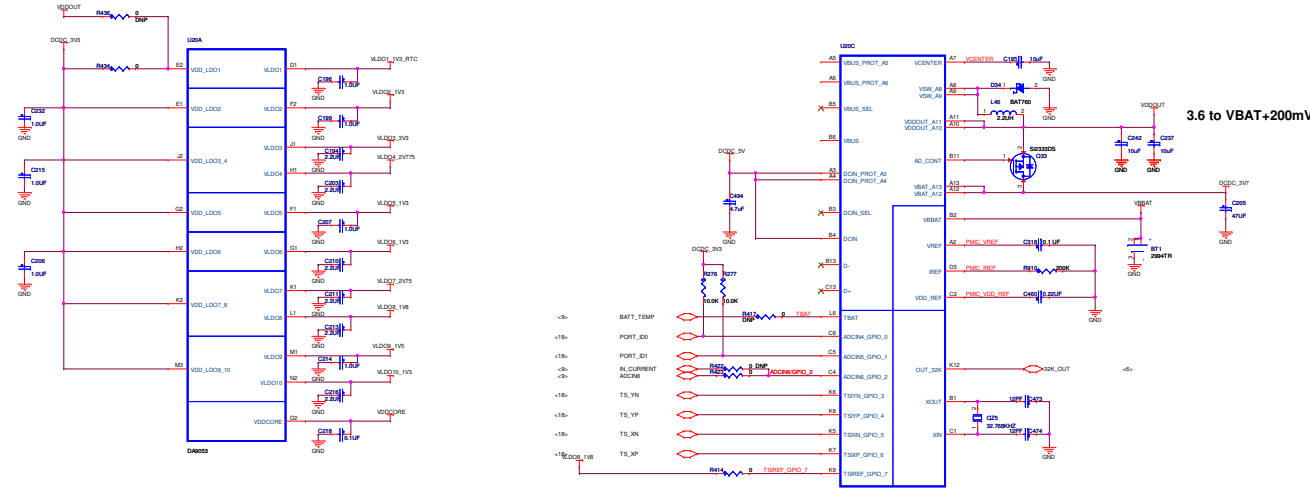
Outputs from DA9053



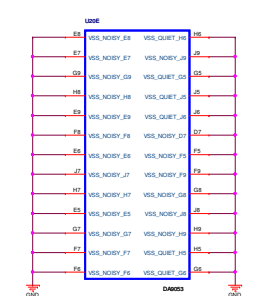
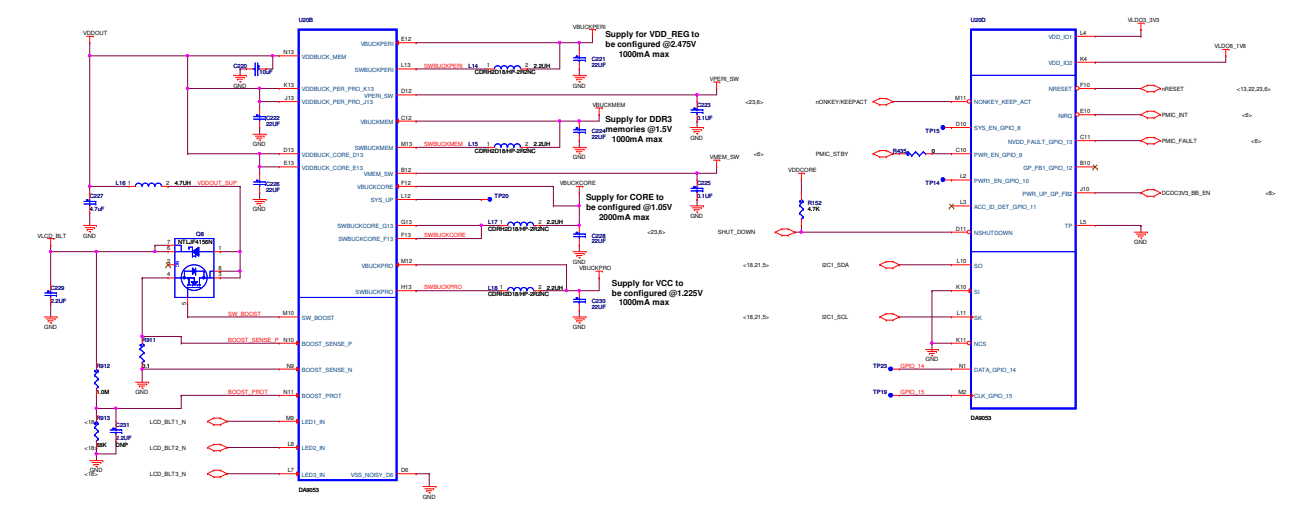
The DDR3 PN is MT41J128M16HA-125



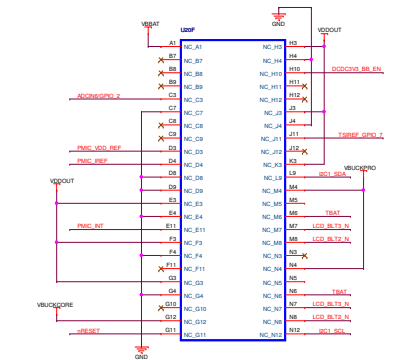
NOTE:
 DDR data pins can be swapped for improved routing according to the following rules:
 1) Data pins can be swapped within each byte
 2) Data bytes can be swapped
 3) DQSx and DQStx must follow each byte
 When swapping bytes 0 or 1 into 2 or 3, must then use 32 bit access. cannot use 16-bit access.



Regulator	Supplied pins	Supplied voltage	Supplied max. current	External Component	Notes
BUCKCORE	VBUCKCORE	0.5 - 2.075V ±3% accuracy default 1.8V	2000mA	2.2/1.0uH	DVC, 2MHz, 25mV steps, DVC ramp with controlled slow rate; pull-down resistor switch off
BUCKPRO	VBUCKPRO	0.5 - 2.075V ±3% accuracy default 1.2V	1000mA	2.2/1.0uH	DVC, 2MHz, 25mV steps, DVC ramp with controlled slow rate, pull-down resistor switch off
BUCKMEM	VBUCKMEM, VMEM_SW	0.925 - 2.5V ±3% accuracy default 2.0V	1000mA	2.2/1.0uH	DVC, 2MHz, 25mV steps, DVC ramp with controlled slow rate, 2nd output with sequencer controllable switch, pull-down resistor switch off
BUCKPERI	VBUCKPERI, VPERI_SW	0.925-2.475V ±3% accuracy default 1.2V	1000mA	2.2/1.0uH	2MHz, 25mV steps 2nd output with sequencer controllable switch
BOOST	Ext. FET	5 to 25V, regulated via current feedback	50mA	4.7uH	Current controlled boost converter for 3 strings of up to 6 serial white LEDs. Over voltage protection via a voltage feedback pin
LDO1	VLD01	0.6 - 1.8V ±3% accuracy default 1.2V	40mA	1.0uF	High PSRR, low noise LDO, 50mV steps, pull-down resistor switch off
LDO2	VLD02	0.6 - 1.8V ±3% accuracy default 1.2V	100mA	1.0uF	DVC, digital LDO, 25mV steps, DVC ramp with controlled slow rate, pull-down resistor switch off
LDO3	VLD03	1.725 - 3.0V ±3% accuracy default 2.85V	200mA	2.2uF	DVC, digital LDO, 25mV steps, DVC with controlled slow rate, common supply with LDO4
LDO4	VLD04	1.725 - 3.0V ±3% accuracy default 2.85V	150mA	2.2uF	Digital LDO, 25mV steps, optional HW control from GP11, common supply with LDO3
LDO5	VLD05	1.2 - 3.6V ±3% accuracy default 3.1V	100mA	1.0uF	Digital LDO, 50mV steps, pull-down resistor switch off, optional HW control from GP12
LDO6	VLD06	1.2 - 3.6V ±3% accuracy default 1.2V	150mA	2.2uF	High PSRR, low noise, 50mV steps
LDO7	VLD07	1.2 - 3.6V ±3% accuracy default 3.1V	200mA	2.2uF	High PSRR, low noise, 50mV steps, common supply with LDO7
LDO8	VLD08	1.2 - 3.6V ±3% accuracy default 2.85V	200mA	2.2uF	High PSRR, low noise, 50mV steps, common supply with LDO7
LDO9	VLD09	1.2 - 3.6V ±1% accuracy default 2.5V	100mA	1.0uF	High PSRR, low noise, 50mV steps, OTP trimmed, optional HW control from GP12, common supply with LDO10
LDO10	VLD010	1.2 - 3.6V ±3% accuracy default 1.8V	250mA	2.2uF	High PSRR, low noise, 50mV steps, common supply with LDO9
BACKUP	VBBAT	1.1 - 3.1V default 3.0V	6mA	470nF	100/200mV steps, configurable current limit between 100 and 6000uA, reverse current protection
LDOCORE	Internal PMIC supply	2.5V ±2% accuracy	4mA	100nF	Not for external use

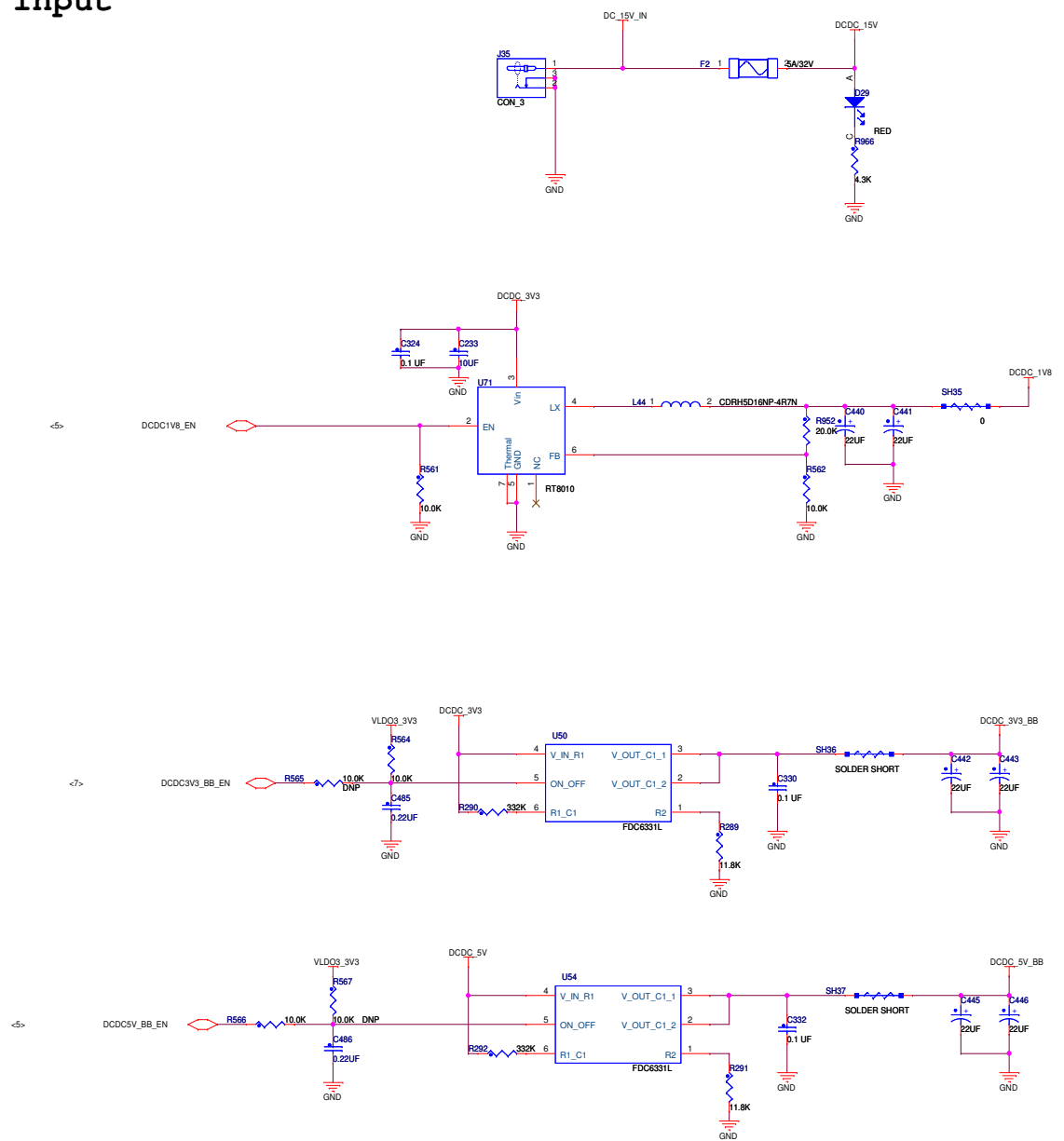


Pins D7 and F5 can be left open as they are "NC" pins.

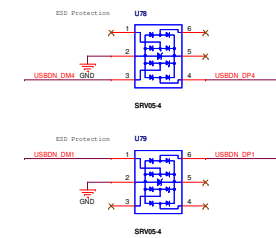
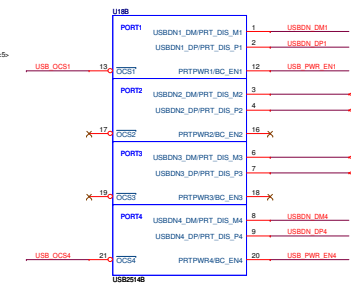
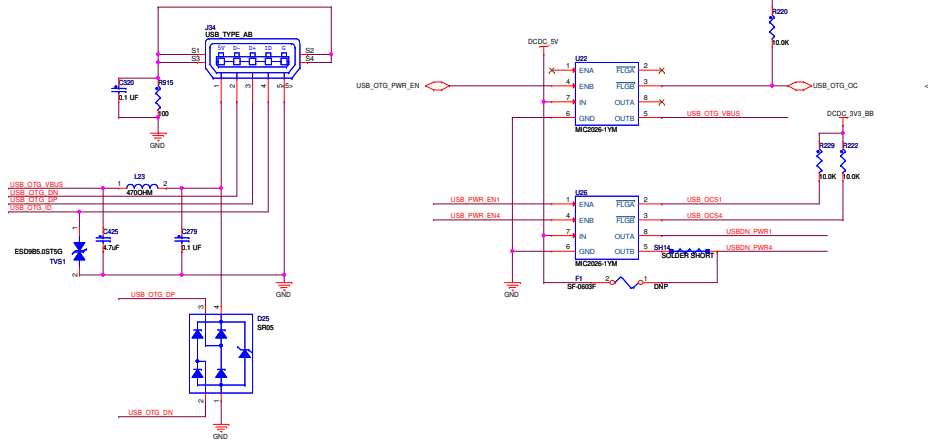
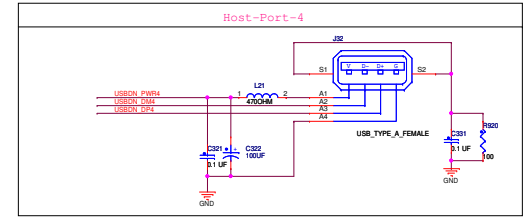
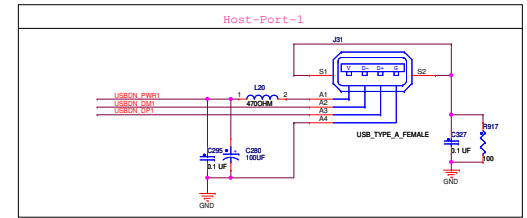
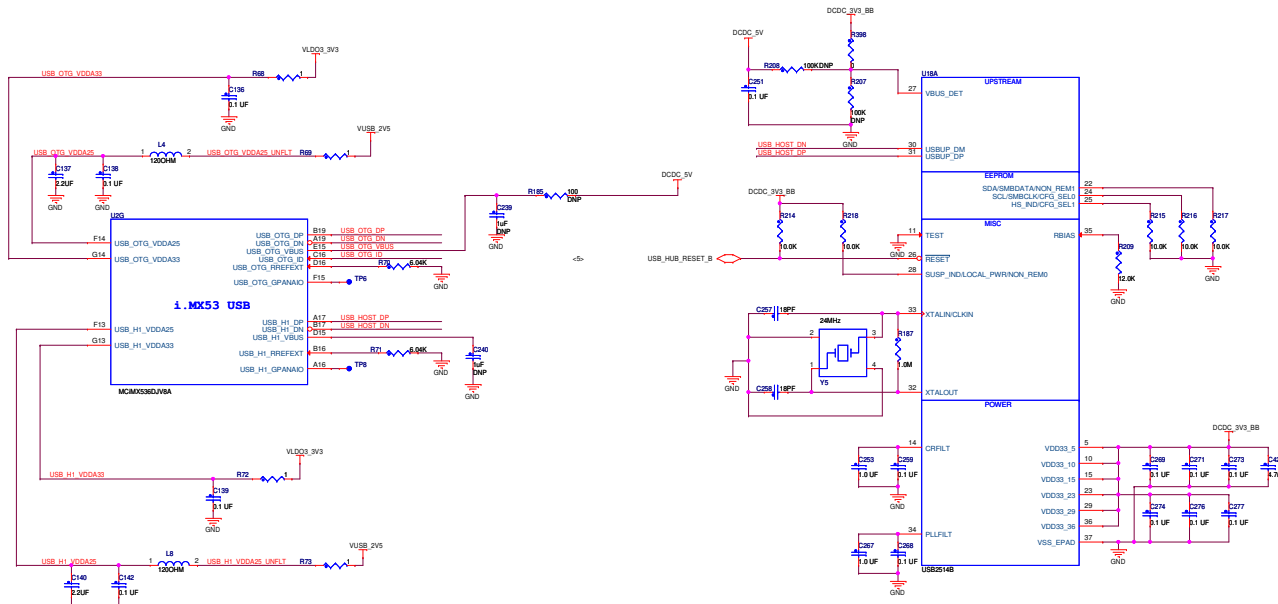


For easy layout and assembly

+15V@3A Input



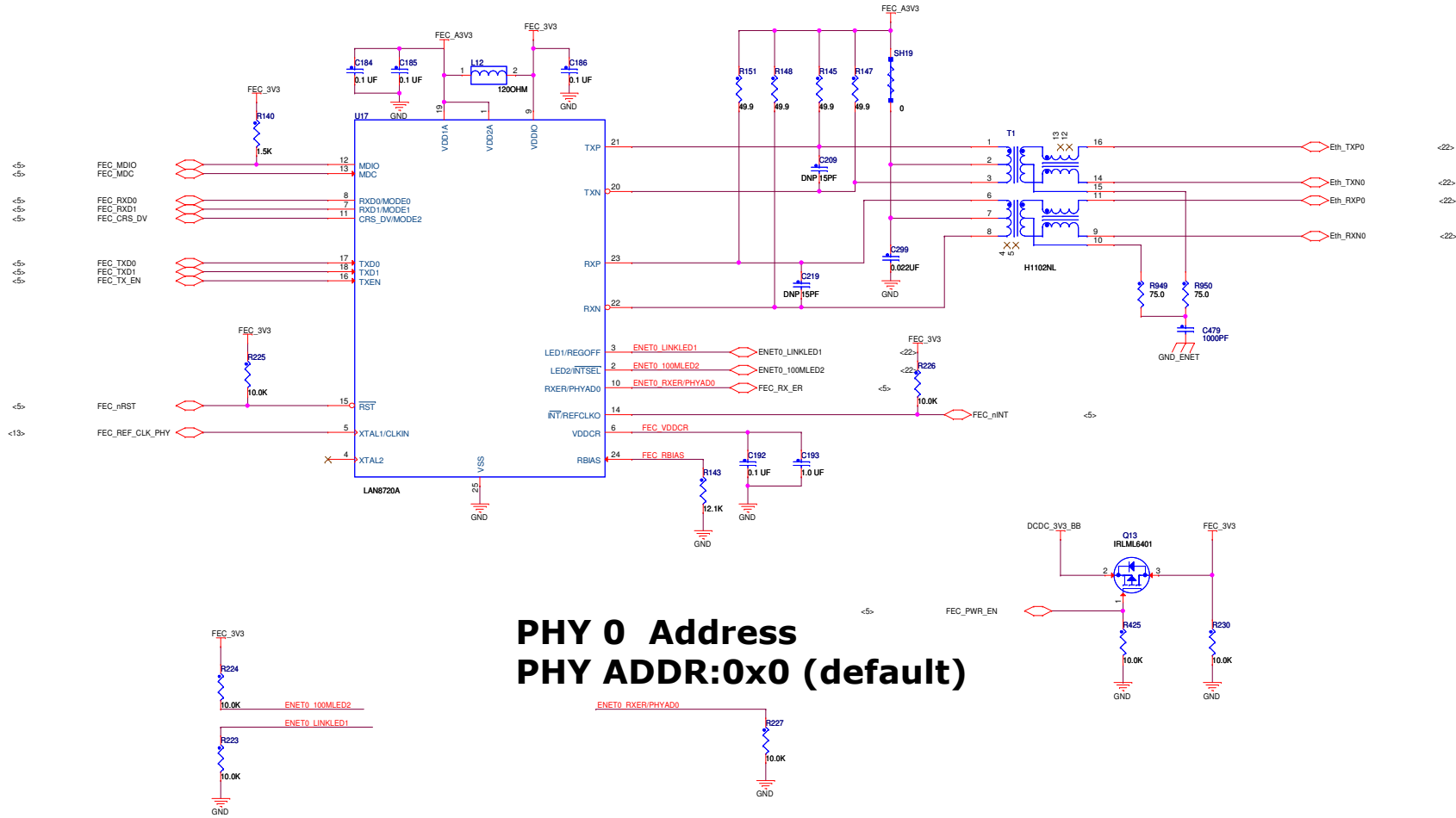
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Drawn by: <DrawnBy>	Page Title: Discrete Power		
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USB1: Host_Port_1
USB2: Mini-PCIE
USB3: VGA Dock
USB4: Host_Port_4

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Created By: Song Zhang	Page No: USB HOST&OTG		
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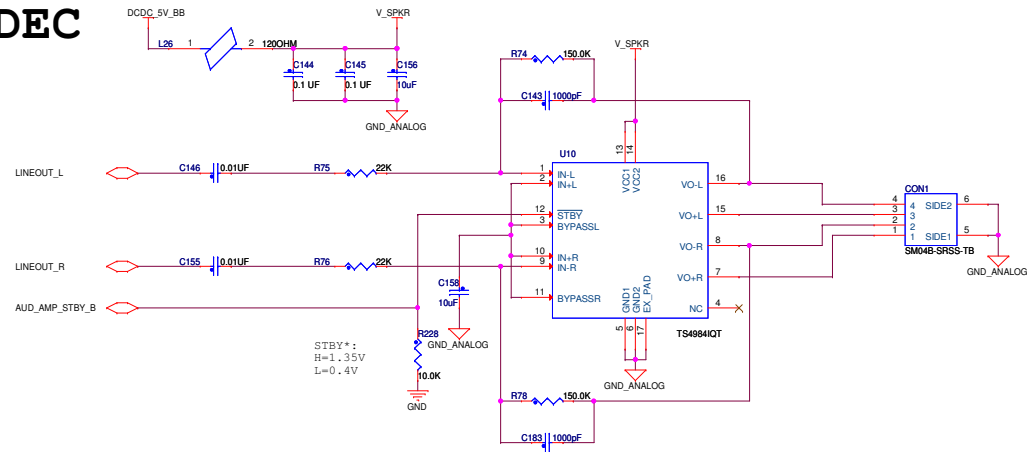
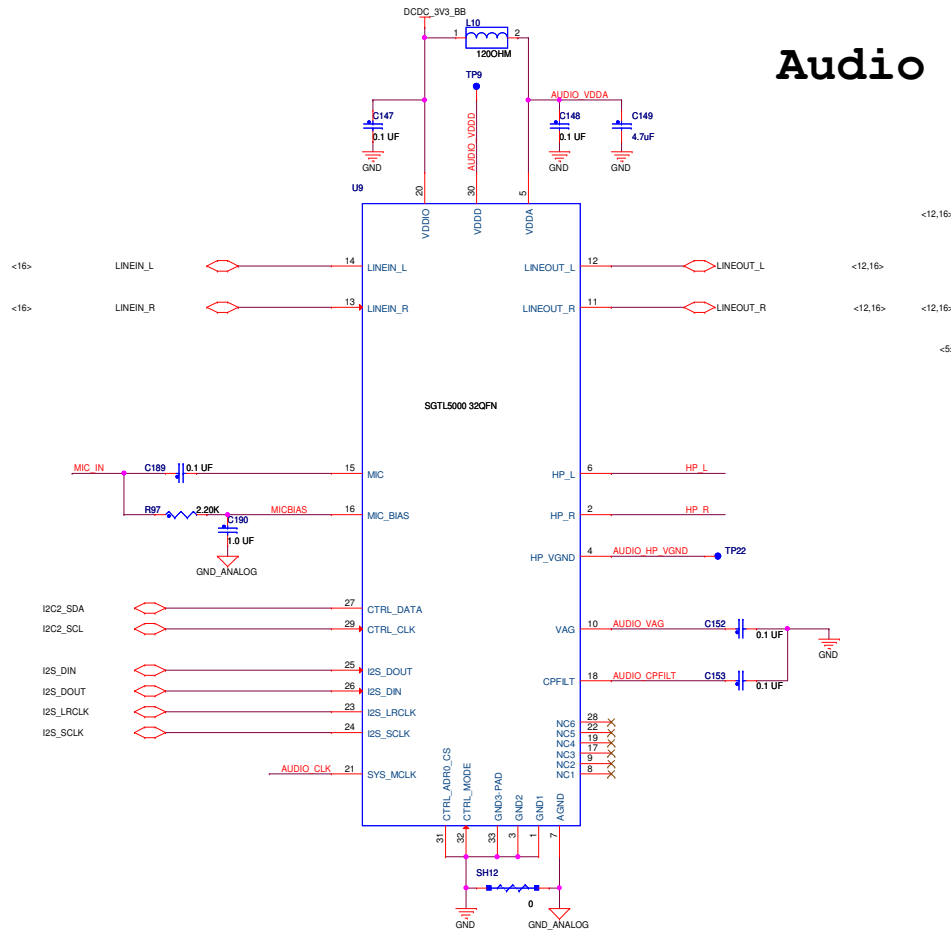
FAST ETHERNET PHY



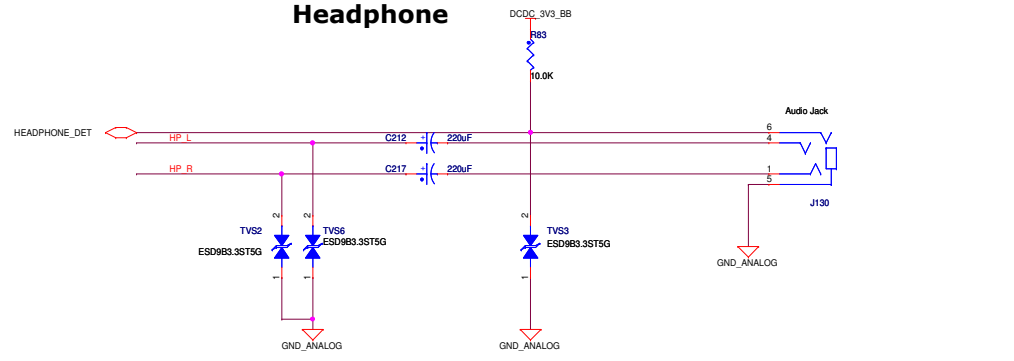
PHY 0 Address
PHY ADDR:0x0 (default)

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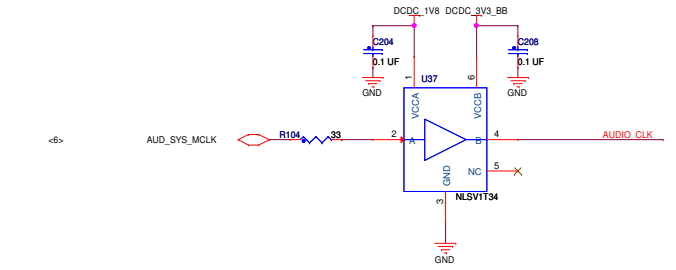
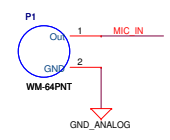
Audio CODEC



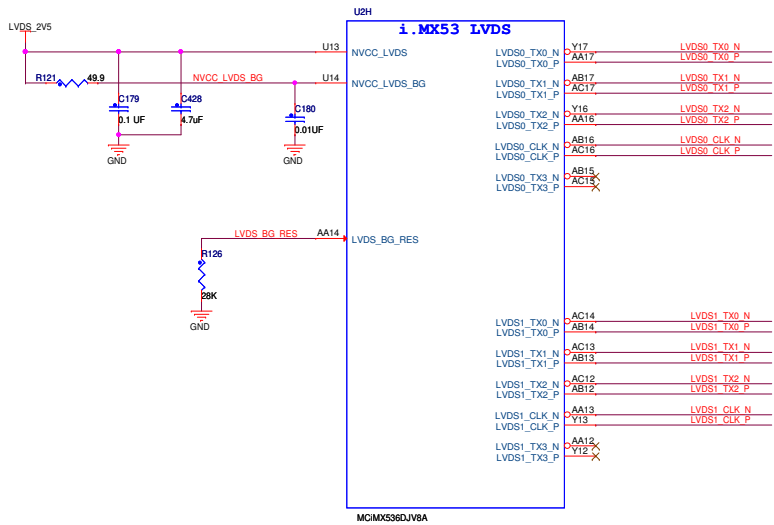
Headphone



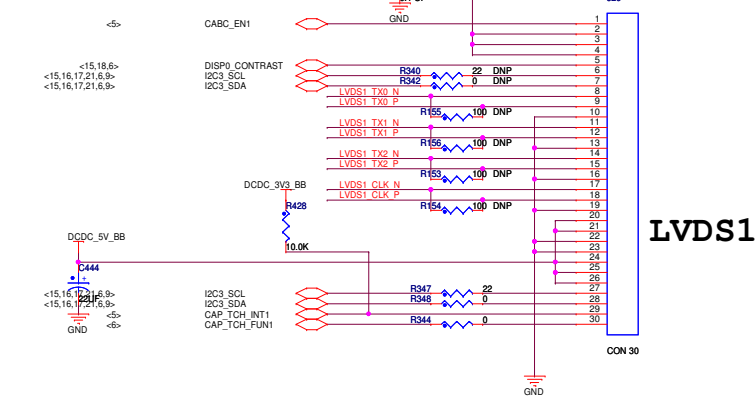
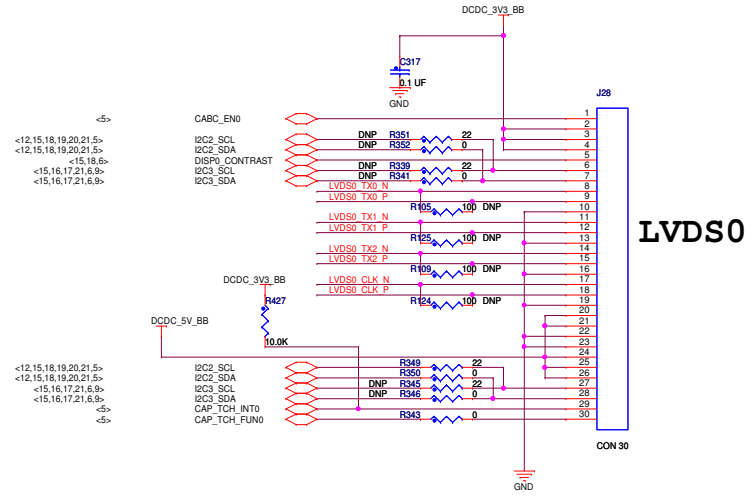
SET MIC_BIAS POWER OFF TO DETECT HEADPHONE MIC



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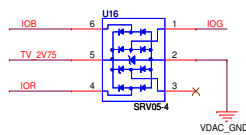
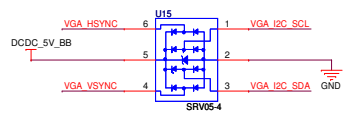
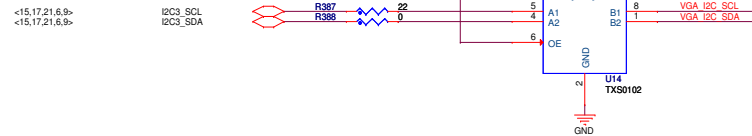
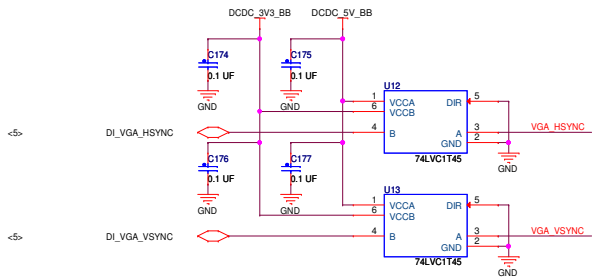
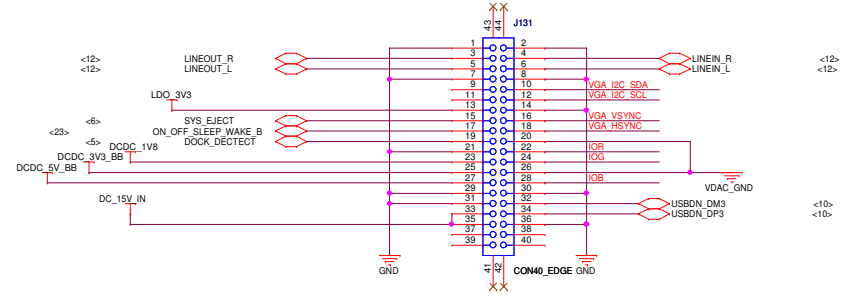
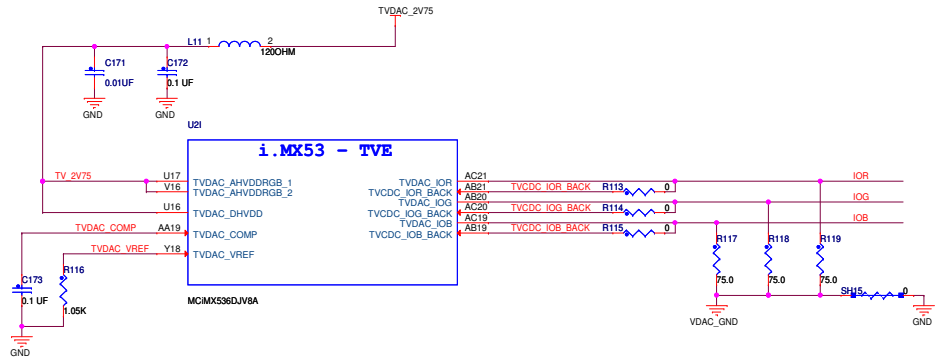
HSD100PXN1-A00-C00
Default Port is LVDS1



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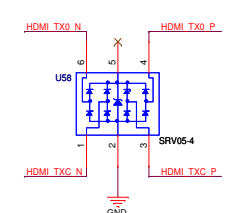
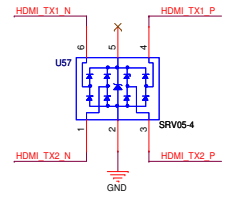
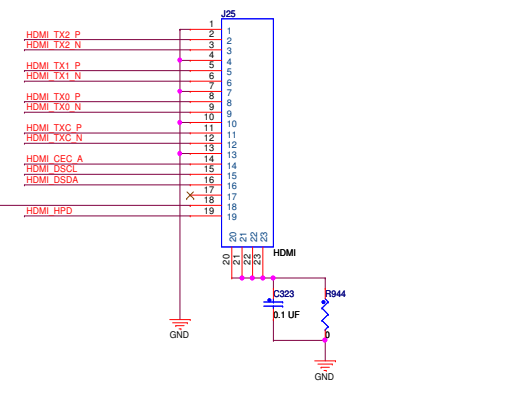
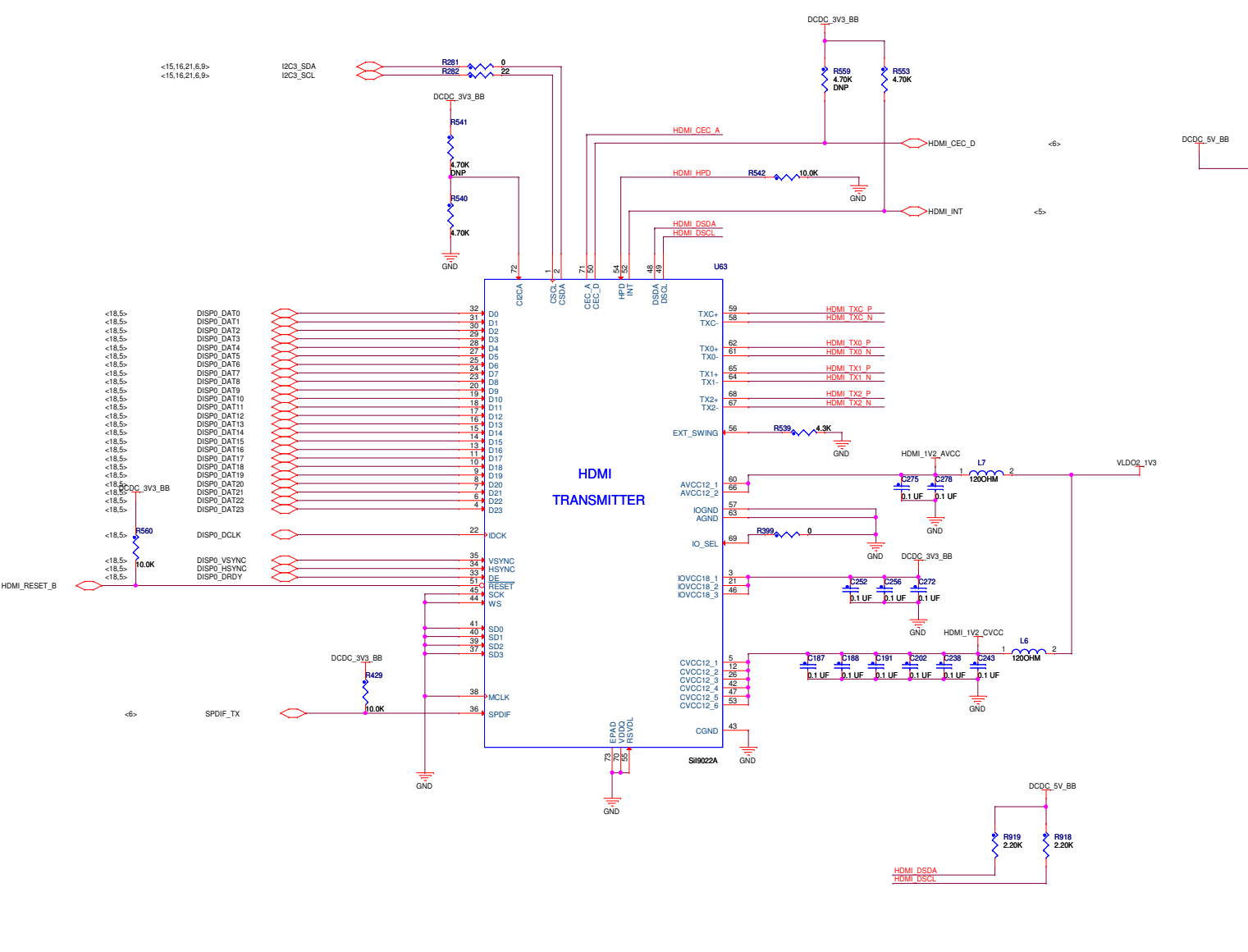
VGA

VGA VIDEO CONNECTOR



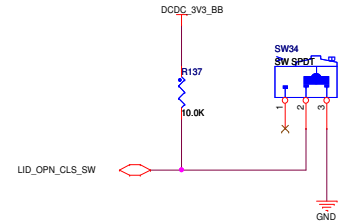
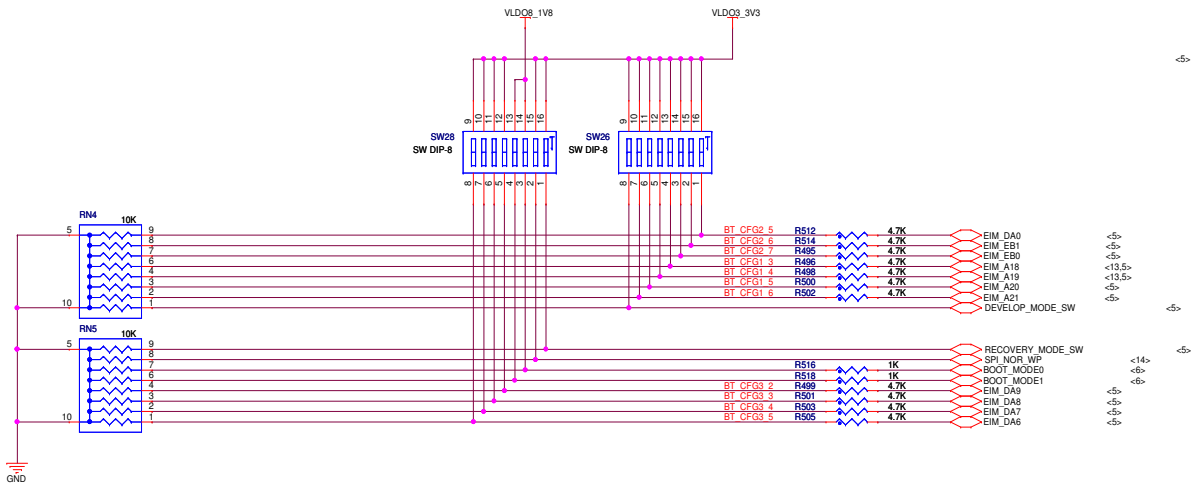
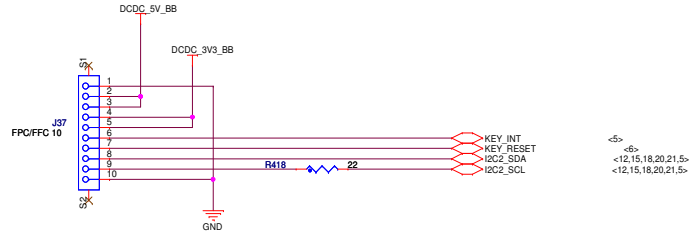
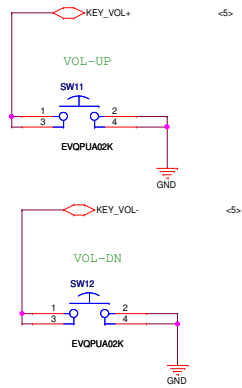
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Drawn by: <DrawnBy>		Page Title: VGA	
Approved: <Approve>		Size C Document Number SOURCE: SCH-26876 PDF: SPF-26876 Rev B	
Date: Monday, January 10, 2011		Sheet 16 of 25	

Mini HDMI (TYPE C)



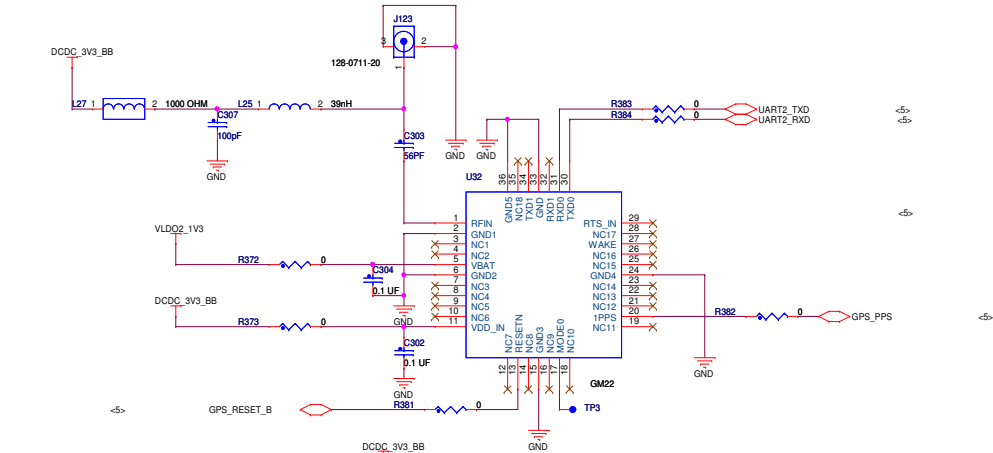
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U/I KEY

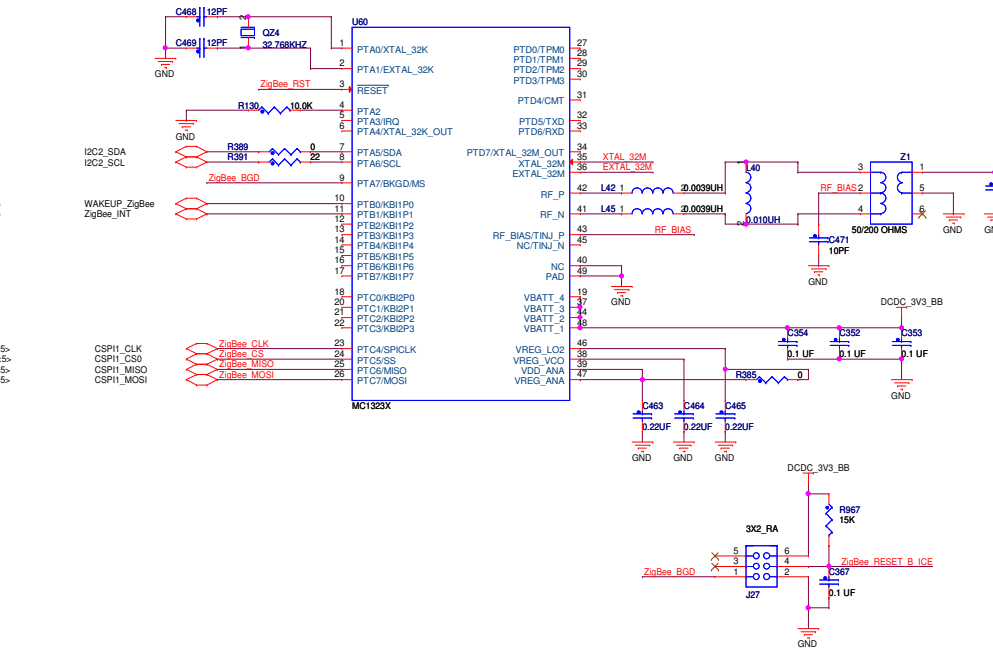


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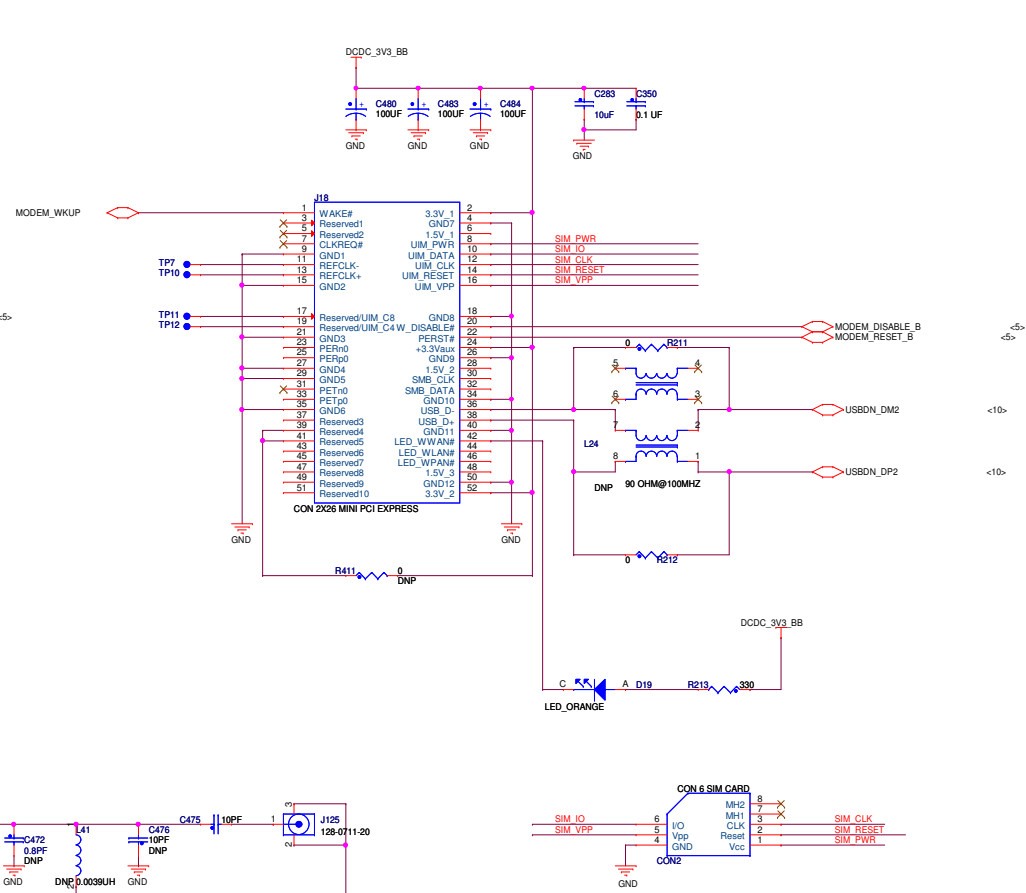
GPS Receiver



ZigBee

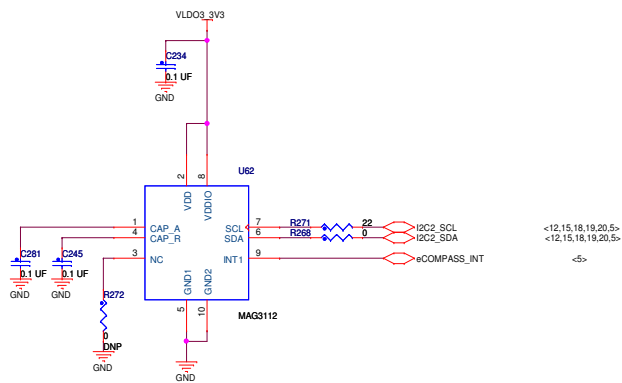


3G Modem (Mini-PCIE)

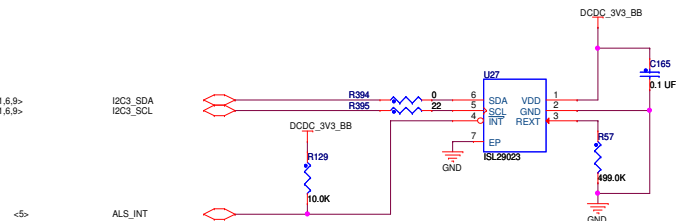


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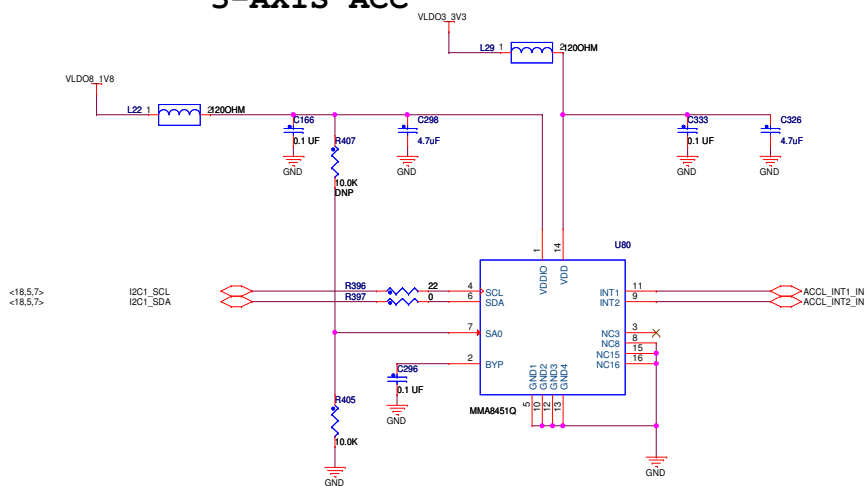
Digital eCompass (MAG3112 as default)



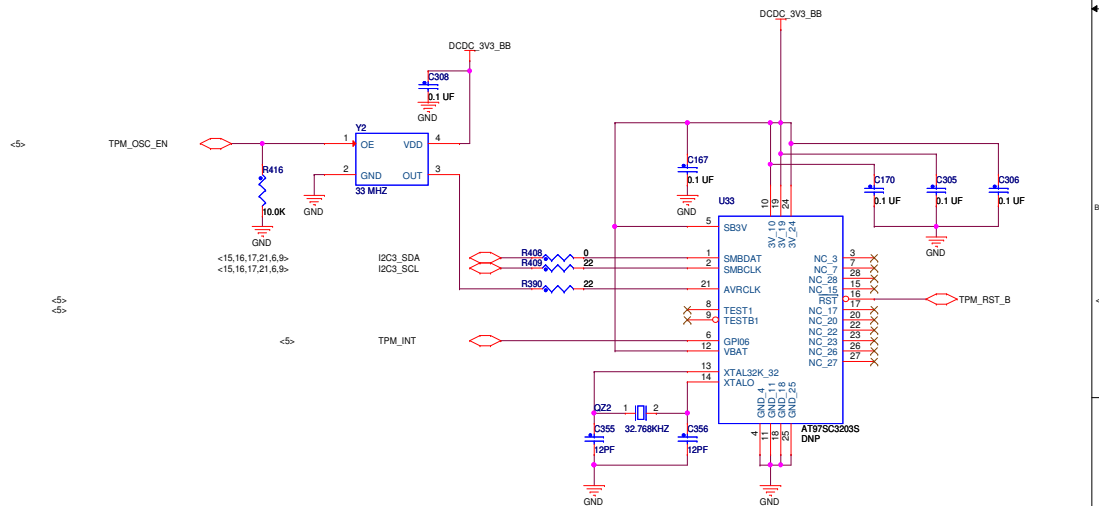
Ambient Light Sensor



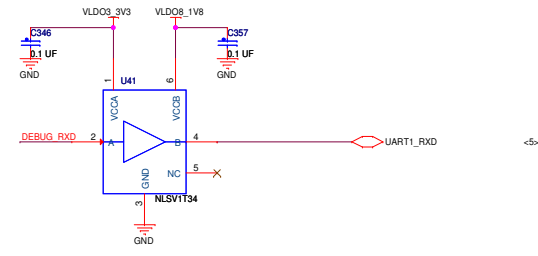
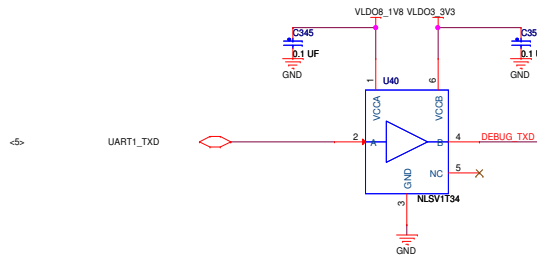
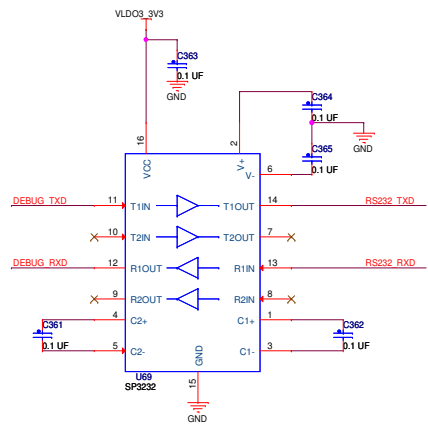
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TPM

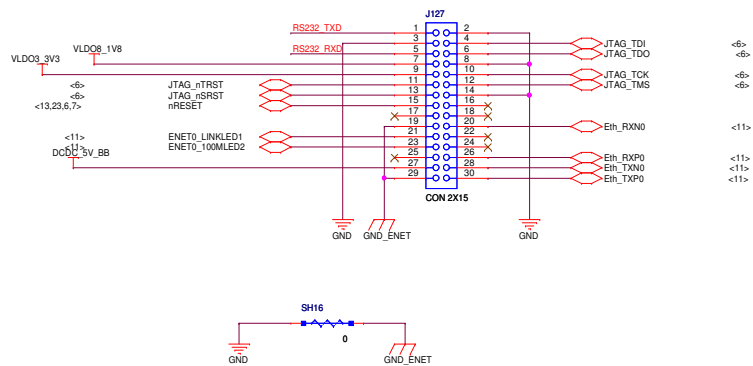


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DEBUG SMT CONNECTOR

LS2-115-01-L-D-RA1-TR



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Designer: Song Zhang	Drawing Title: Smart Mobile Board		
Drawn by: <DrawnBy>	Page Title: Debug		
Approved: <Approve>	Size C	Document Number SOURCE: SCH-26876 PDF-SPF-26876	Rev B
Date: Monday, January 10, 2011	Sheet	22	of 25

5V_ON is Always Present when Battery or External DC is present.

ON/OFF KEY

Remote switch hook-up option

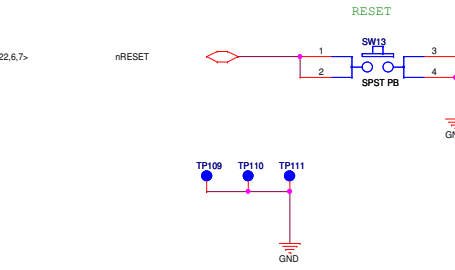
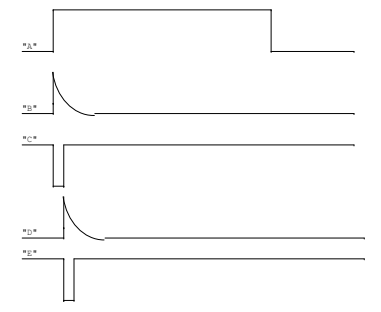
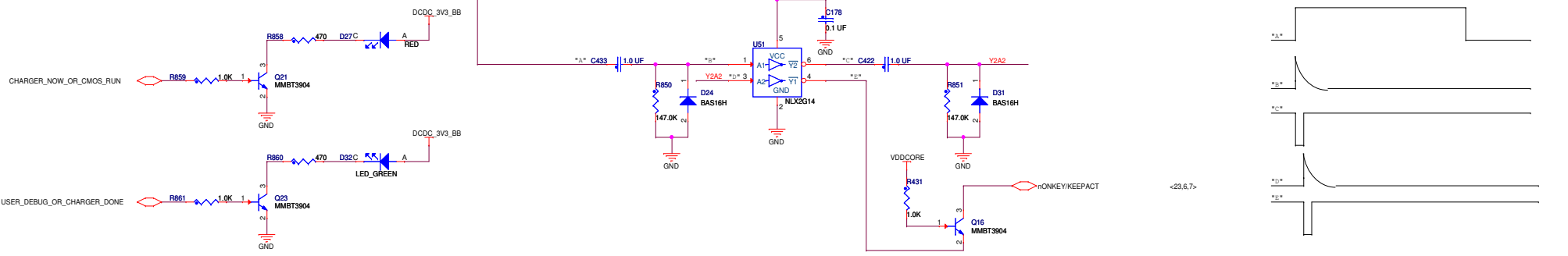
If system is OFF, press momentary contact switch to turn system ON.

If system is ON, press momentary contact switch to start s/w based shutdown_entry or resume operation.

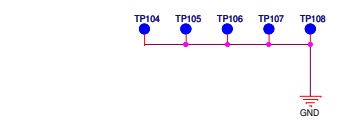
If system is hung, press contact switch for at least 10 seconds.

This switch to be used for Boot Mode Configuration.

NOTE:
SYS_ON_OFF_CTL (GPIO7) must be set to HIGH as the first action in the BOOT sequence.
Clear this GPIO to LOW to turn the system OFF.

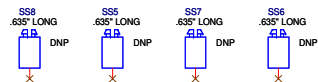


GND Testpoint on Bottom



GND Testpoint on Top

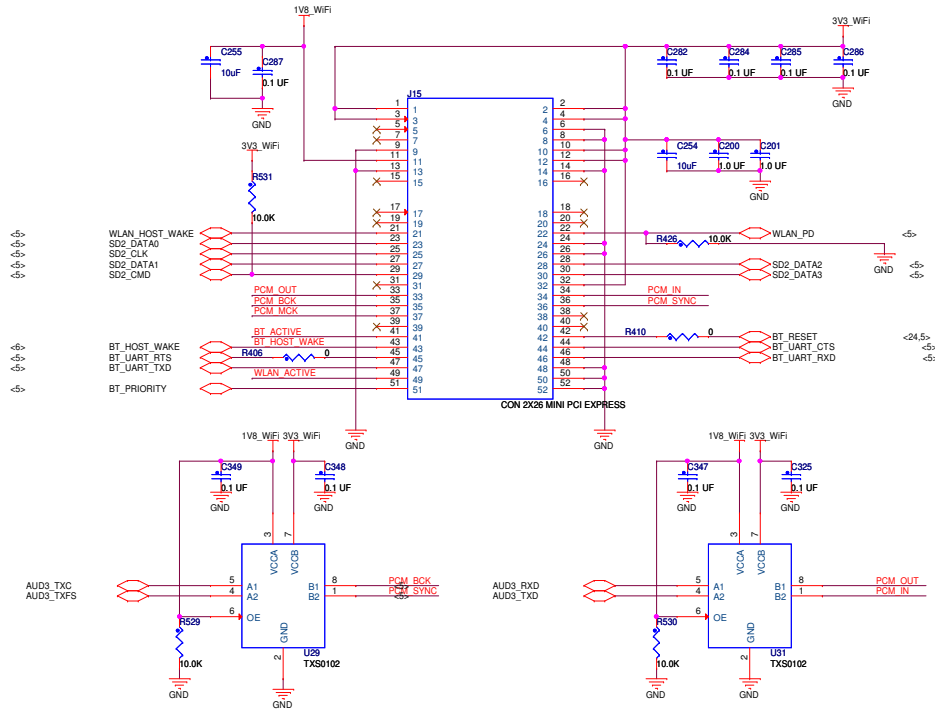
ANT Standoff



Placement of these components is not sensitive to proximity to the power block. This group can be placed anywhere on the board, as space permits.

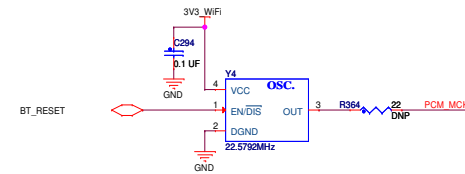
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Designer: Song Zhang	Drawing Title: Smart Mobile Board		
Drawn by: <DrawnBy>	Page Title: Misc		
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WiFi + BT Module Connector

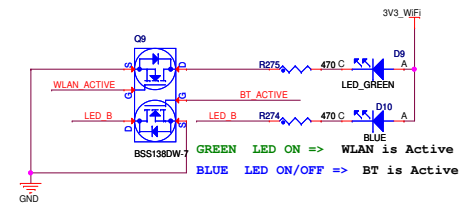


WiFi+BT

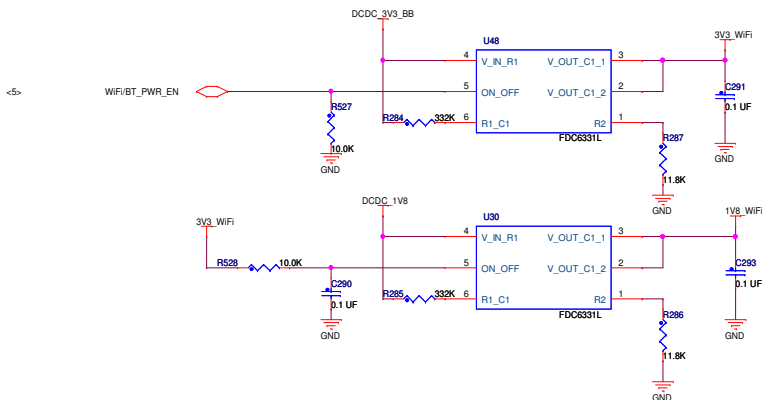
WiFi+BT module Clock Generation Block



WiFi + BT activity Indication Block



WiFi+BT Power Sequencer Block



WARNING:

This connector (J15) is mapped to Atheros WiFi+BT module which uses a non standard mini-PCIE pin map. No other mini PCIe card should be connected to this slot!!!

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