X-815LPD4-CPUCY

(i.MX8M Nano Reference Board)

Table of Content

Revision History

Rev. Code	Date	By	Description
A	*2019-09-03*	*Mac*	*Initial version release*
A1	*2019-11-05*	*Mac*	*Add notes for JTAG_TMS and WDOG_B.*

1. Interrupted lines coded with the same letter or letter combinations are electrically connected.

2. Device type number is for reference only. The number varies with the manufacturer.

3. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

4. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Preliminary - Subject to Change without Notice!

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.

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Austin, TX 78735-8598

ICAP Classification: CP: IUO: X PUBI:

Designer: Mac Zhang	Drawing Title: X-815LPD4-CPUCY		
Drawn by: Mac Zhang	Page Title: Title and Rev History		
Approved: <Approver>	Size C	Document Number SCH-46441 PDF: SPF-46441	Rev A1
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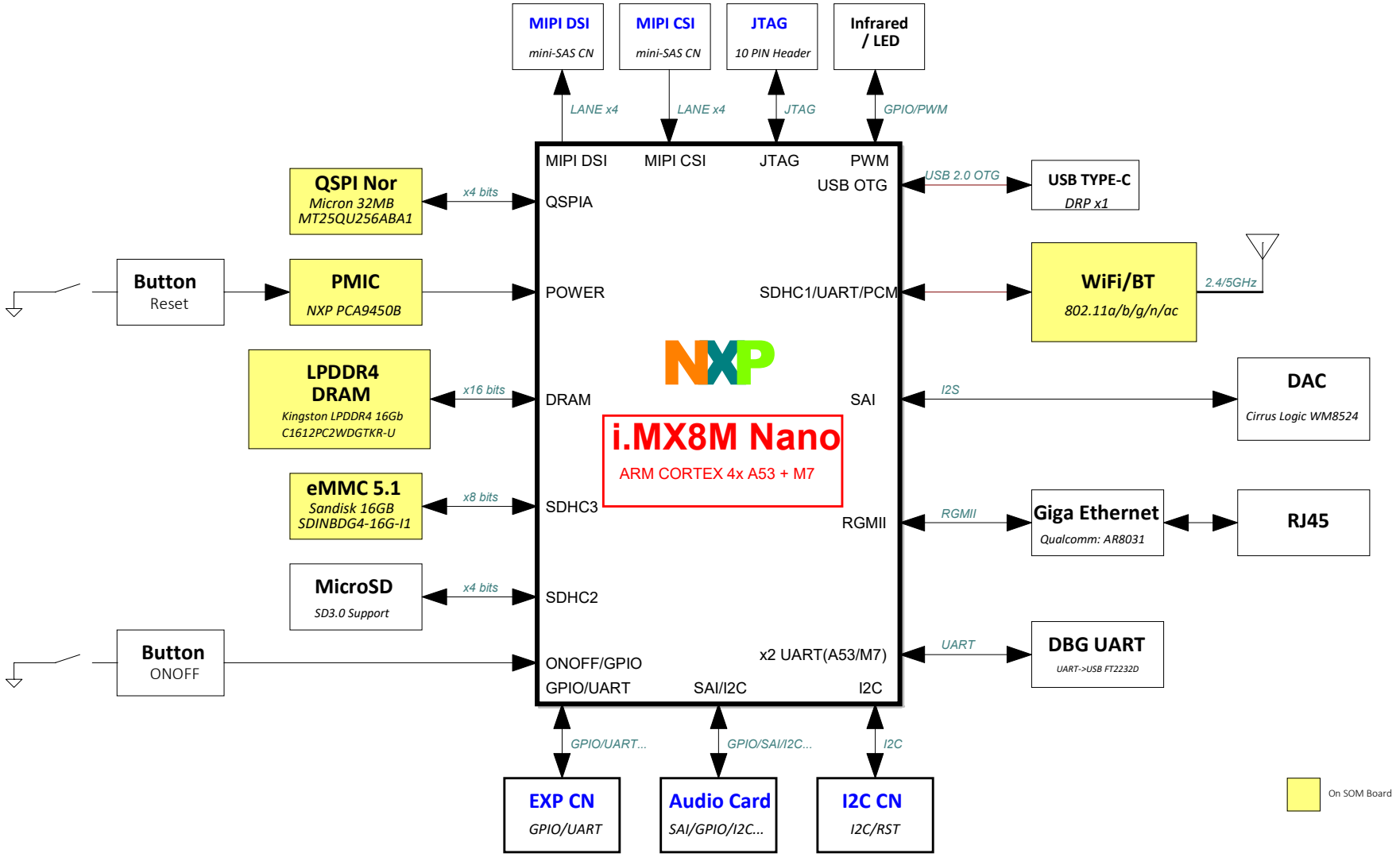
X-815LPD4-EVKCY Block Diagram



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Drawn by: Mac Zhang	Page Title: Block Diagram
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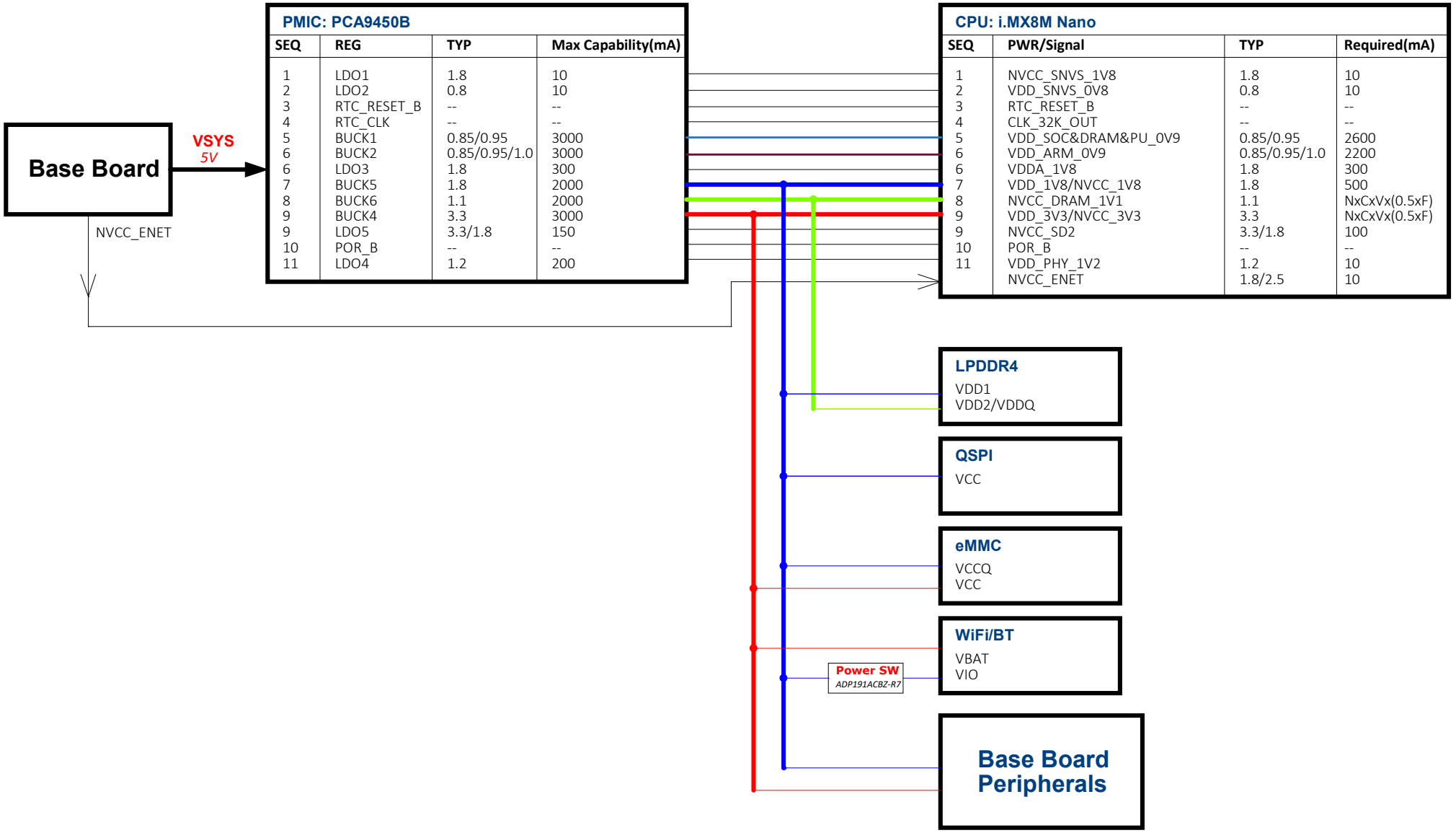
815LPD4-EVKCY PWR TREE



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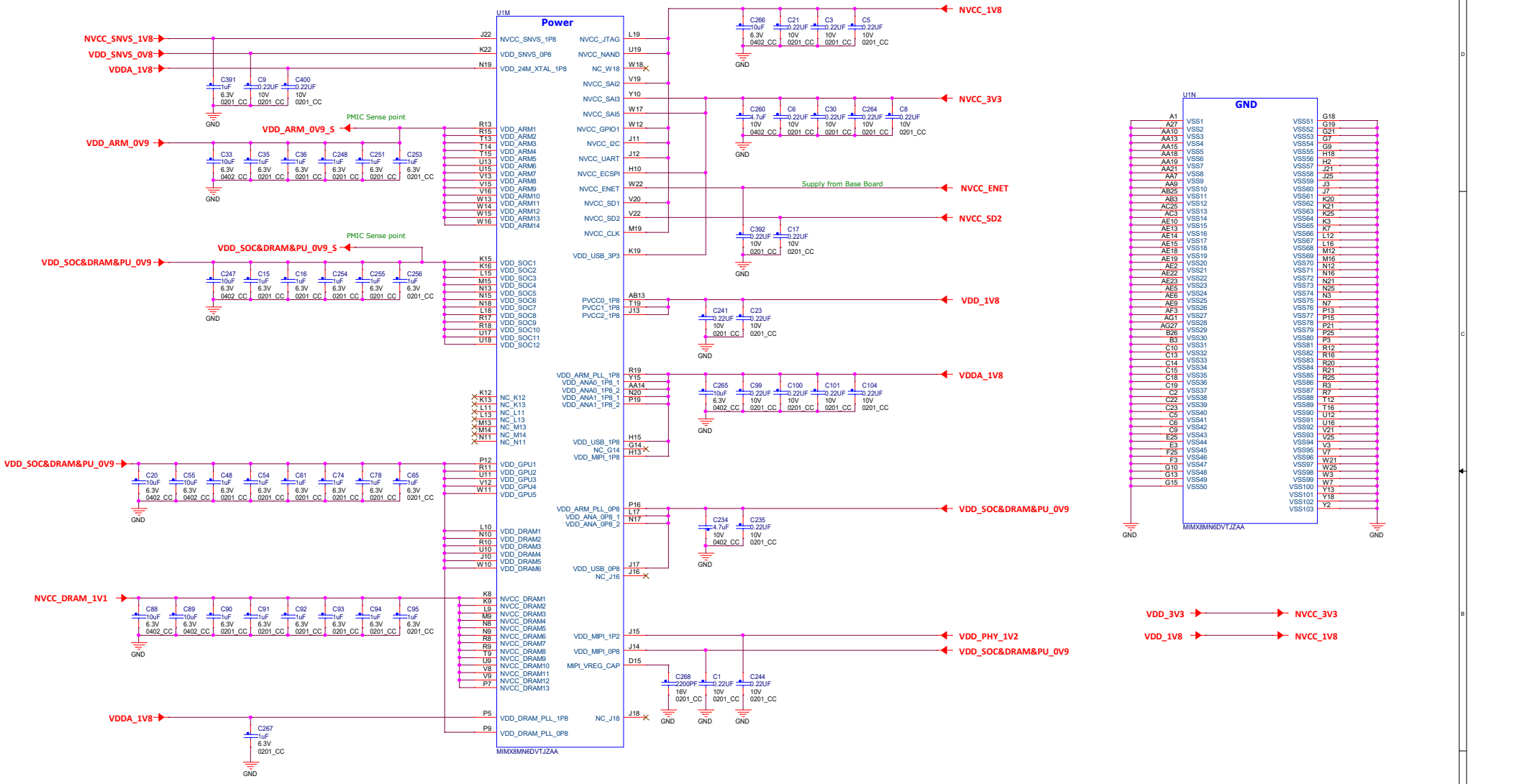
	Date: Tuesday, November 05, 2019; Sheet 3 of 13

i.MX8M Nano PWR



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Drawn by: Mac Zhang	Page Title: CPU PWR	
Approved: <Approver>	Size C	Document Number SCH-46441 PDF: SPF-46441 Rev A1
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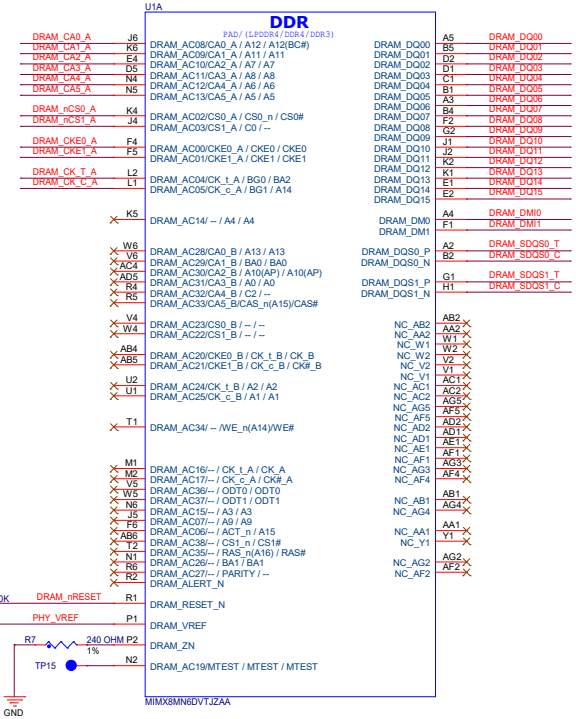
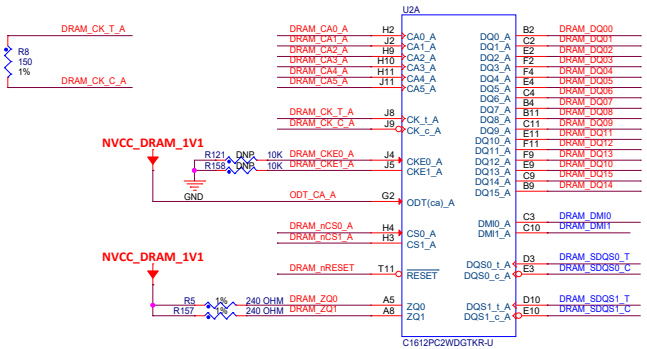
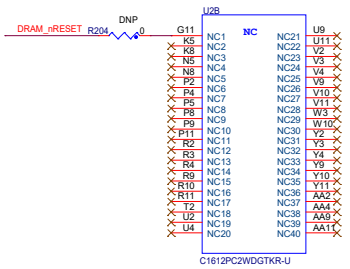
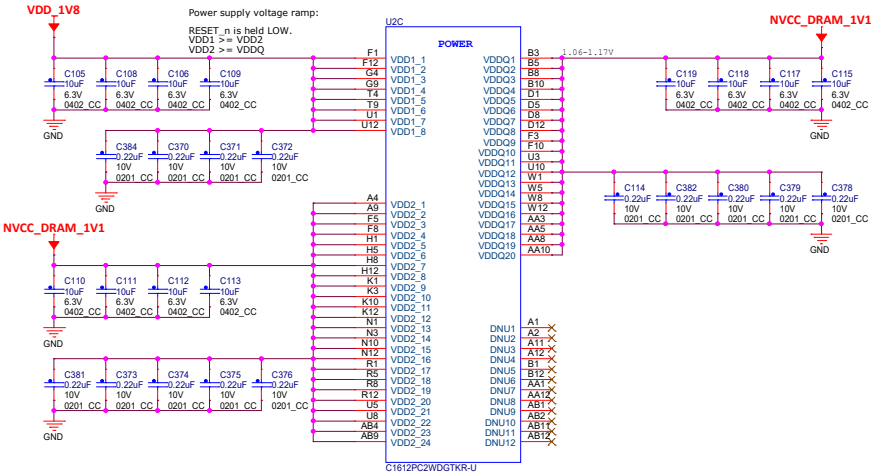
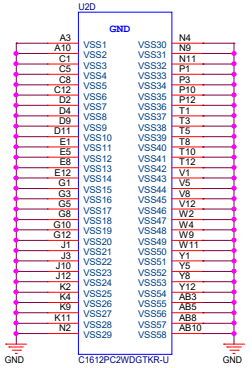
LPDDR4 2GB











Data Bus

Pin Name	LPDDR4	DDR4
DRAM_DQS0_P	DQS0_t_A	DQSL_t_A
DRAM_DQS0_N	DQS0_c_A	DQSL_c_A
DRAM_DM0	DMI0_A	DML_n_A / DBIL_n_A
DRAM_DQ00	DQ0_A	DQL0_A
DRAM_DQ01	DQ1_A	DQL1_A
DRAM_DQ02	DQ2_A	DQL2_A
DRAM_DQ03	DQ3_A	DQL3_A
DRAM_DQ04	DQ4_A	DQL4_A
DRAM_DQ05	DQ5_A	DQL5_A
DRAM_DQ06	DQ6_A	DQL6_A
DRAM_DQ07	DQ7_A	DQL7_A
DRAM_DQS1_P	DQS1_t_A	DQSU_t_A
DRAM_DQS1_N	DQS1_c_A	DQSU_c_A
DRAM_DM1	DMI1_A	DMU_n_A / DBIU_n_A
DRAM_DQ08	DQ08_A	DQU0_A
DRAM_DQ09	DQ09_A	DQU1_A
DRAM_DQ10	DQ10_A	DQU2_A
DRAM_DQ11	DQ11_A	DQU3_A
DRAM_DQ12	DQ12_A	DQU4_A
DRAM_DQ13	DQ13_A	DQU5_A
DRAM_DQ14	DQ14_A	DQU6_A
DRAM_DQ15	DQ15_A	DQU7_A
DRAM_DQS2_P	DQS0_t_B	DQSL_t_B
DRAM_DQS2_N	DQS0_c_B	DQSL_c_B
DRAM_DM2	DMI0_B	DML_n_B / DBIL_n_B
DRAM_DQ16	DQ0_B	DQL0_B
DRAM_DQ17	DQ1_B	DQL1_B
DRAM_DQ18	DQ2_B	DQL2_B
DRAM_DQ19	DQ3_B	DQL3_B
DRAM_DQ20	DQ4_B	DQL4_B
DRAM_DQ21	DQ5_B	DQL5_B
DRAM_DQ22	DQ6_B	DQL6_B
DRAM_DQ23	DQ7_B	DQL7_B
DRAM_DQS3_P	DQS1_t_B	DQSU_t_B
DRAM_DQS3_N	DQS1_c_B	DQSU_c_B
DRAM_DM3	DMI1_B	DMU_n_B / DBIU_n_B
DRAM_DQ24	DQ08_B	DQU0_B
DRAM_DQ25	DQ09_B	DQU1_B
DRAM_DQ26	DQ10_B	DQU2_B
DRAM_DQ27	DQ11_B	DQU3_B
DRAM_DQ28	DQ12_B	DQU4_B
DRAM_DQ29	DQ13_B	DQU5_B
DRAM_DQ30	DQ14_B	DQU6_B
DRAM_DQ31	DQ15_B	DQU7_B

Command/Address

Pin Name	LPDDR4	DDR4
DRAM_RESET_N	RESET_N	RESET_n
DRAM_ALERT_N	MTEST1	ALERT_n / MTEST1
DRAM_AC00	CKE0_A	CKE0
DRAM_AC01	CKE1_A	CKE1
DRAM_AC02	CS0_A	CS0_n
DRAM_AC03	CS1_A	C0
DRAM_AC04	CK_t_A	BG0
DRAM_AC05	CK_c_A	BG1
DRAM_AC06	/	ACT_n
DRAM_AC07	/	A9
DRAM_AC08	CA0_A	A12
DRAM_AC09	CA1_A	A11
DRAM_AC10	CA2_A	A7
DRAM_AC11	CA3_A	A8
DRAM_AC12	CA4_A	A6
DRAM_AC13	CA5_A	A5
DRAM_AC14		A4
DRAM_AC15	/	A3
DRAM_AC16	/	CK_t_A
DRAM_AC17	/	CK_c_A
DRAM_AC19	MTEST	MTEST
DRAM_AC20	CKE0_B	CK_t_B
DRAM_AC21	CKE1_B	CK_c_B
DRAM_AC22	CS1_B	/
DRAM_AC23	CS0_B	/
DRAM_AC24	CK_t_B	A2
DRAM_AC25	CK_c_B	A1
DRAM_AC26	/	BA1
DRAM_AC27	/	PARITY
DRAM_AC28	CA0_B	A13
DRAM_AC29	CA1_B	BA0
DRAM_AC30	CA2_B	A10 / AP
DRAM_AC31	CA3_B	A0
DRAM_AC32	CA4_B	C2
DRAM_AC33	CA5_B	CAS_n / A15
DRAM_AC34		WE_n / A14
DRAM_AC35	/	RAS_n / A16
DRAM_AC36	/	ODT0
DRAM_AC37	/	ODT1
DRAM_AC38	/	CS1_n
DRAM_ZN	ZQ	ZQ
DRAM_VREF	VREF	VREF

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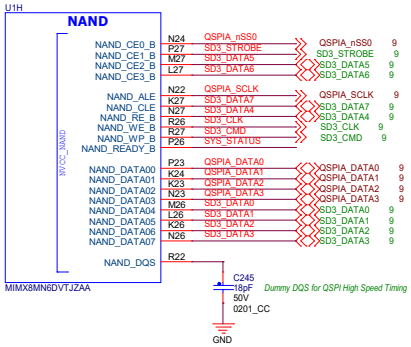
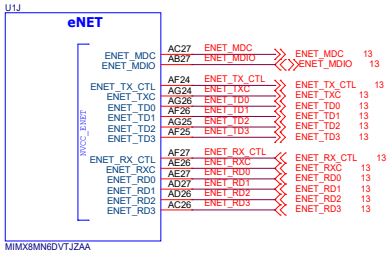
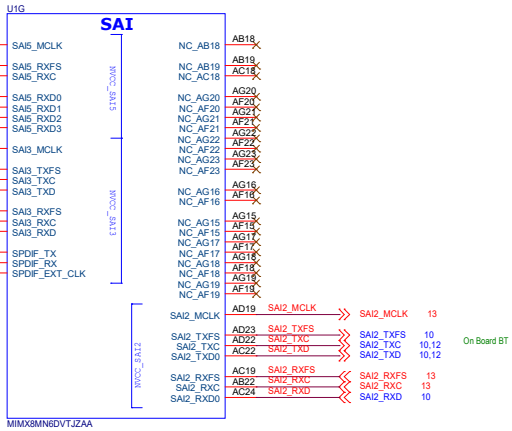
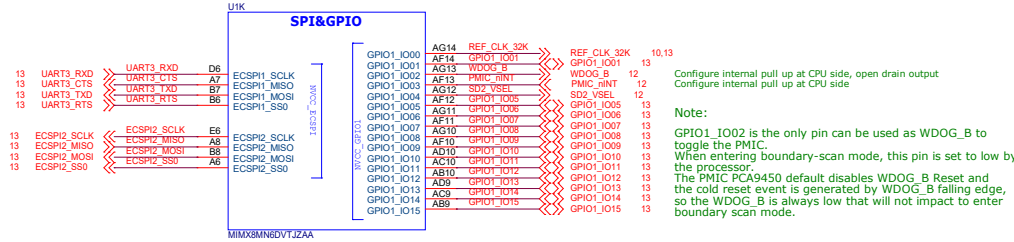
i.MX8M Nano IO Interface





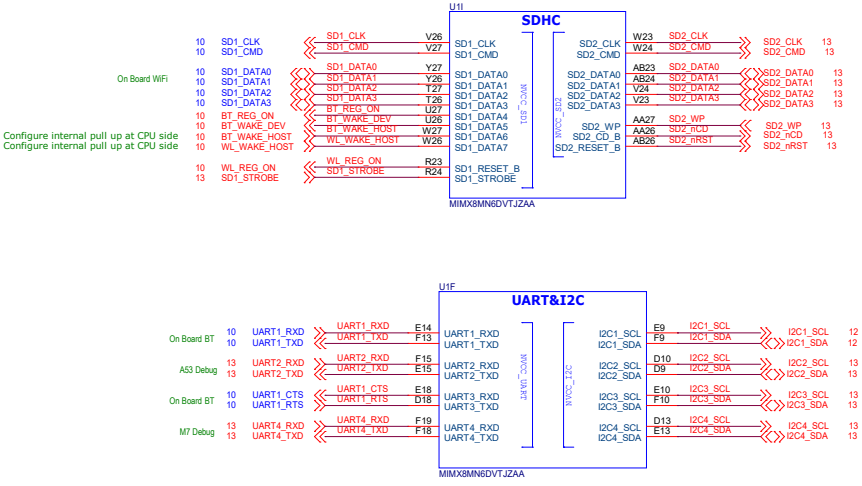


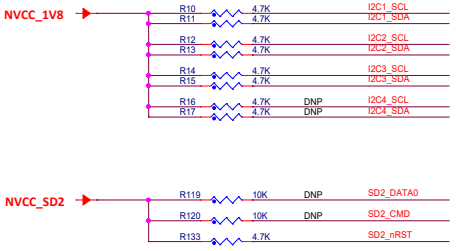


Configure internal pull up at CPU side, open drain output
Configure internal pull up at CPU side

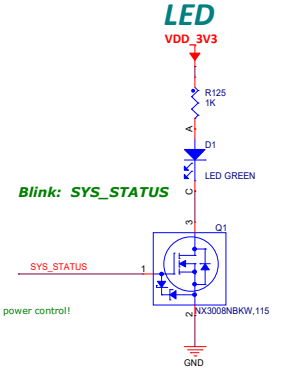
Note:

GPIO1_IO02 is the only pin can be used as WDOG_B to toggle the PMIC.
When entering boundary-scan mode, this pin is set to low by the processor.
The PMIC PCA9450 default disables WDOG_B Reset and the cold reset event is generated by WDOG_B falling edge, so the WDOG_B is always low that will not impact to enter boundary scan mode.





External PU R133 is necessary for SD2 power control!



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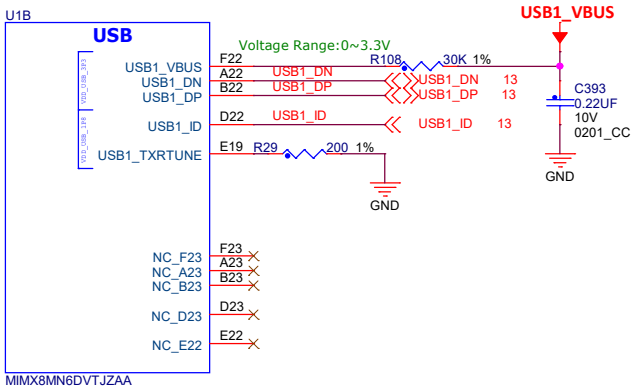
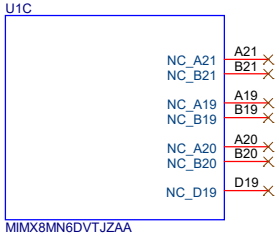
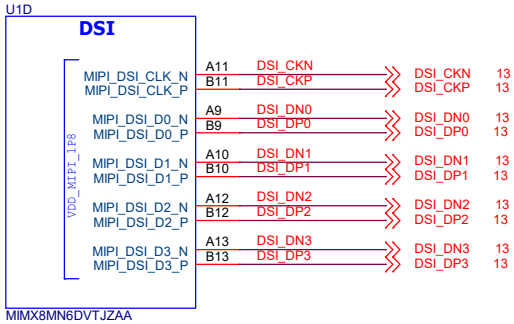
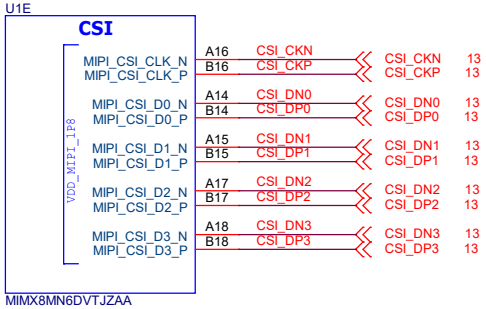
i.MX8M Nano PHYs









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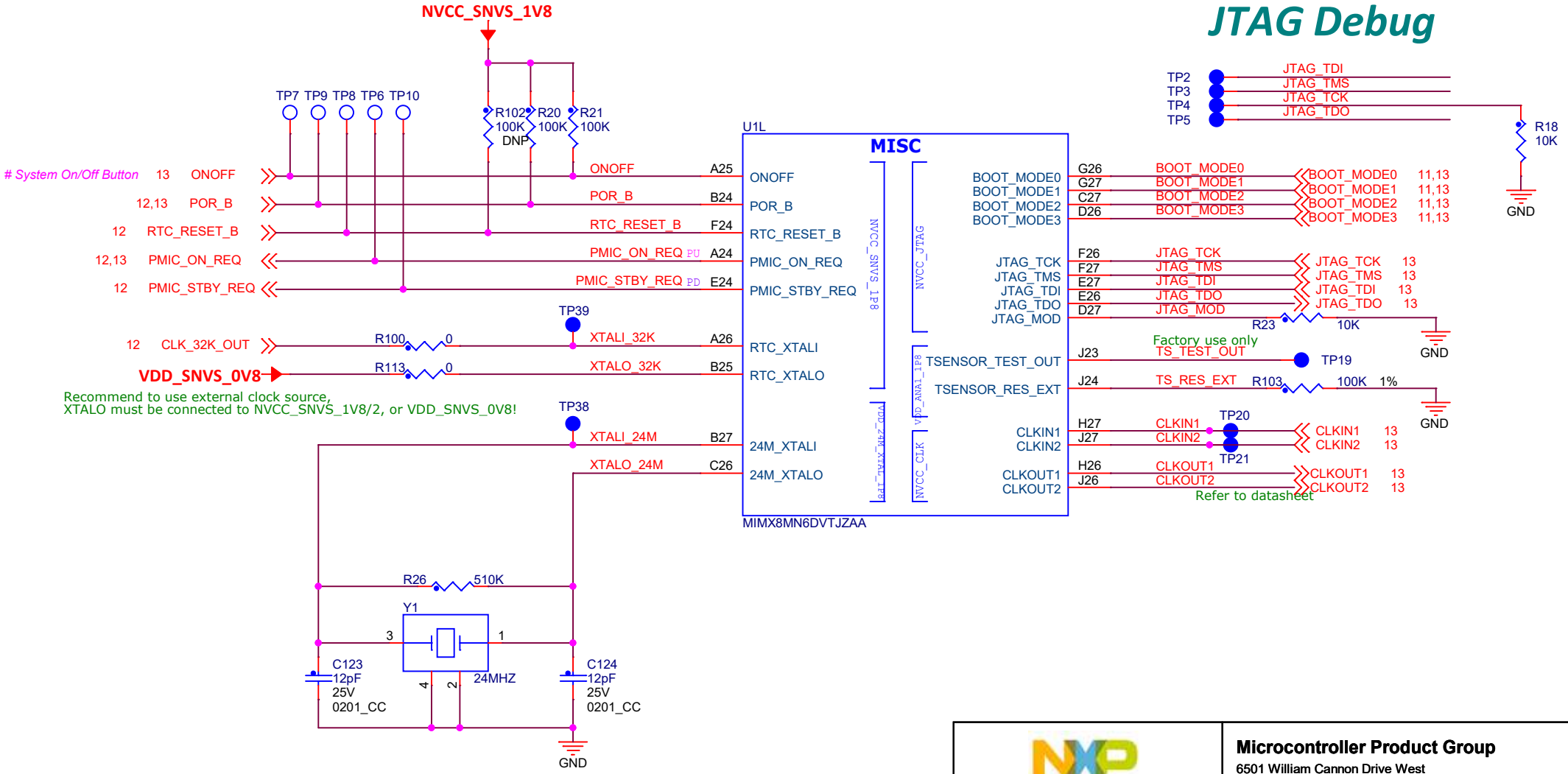
i.MX8M Nano MISC

Caution:
JTAG_TMS pin must be connected with a 50ohm serial resistor near the component if used or fanout. Otherwise, floating if not fanout.



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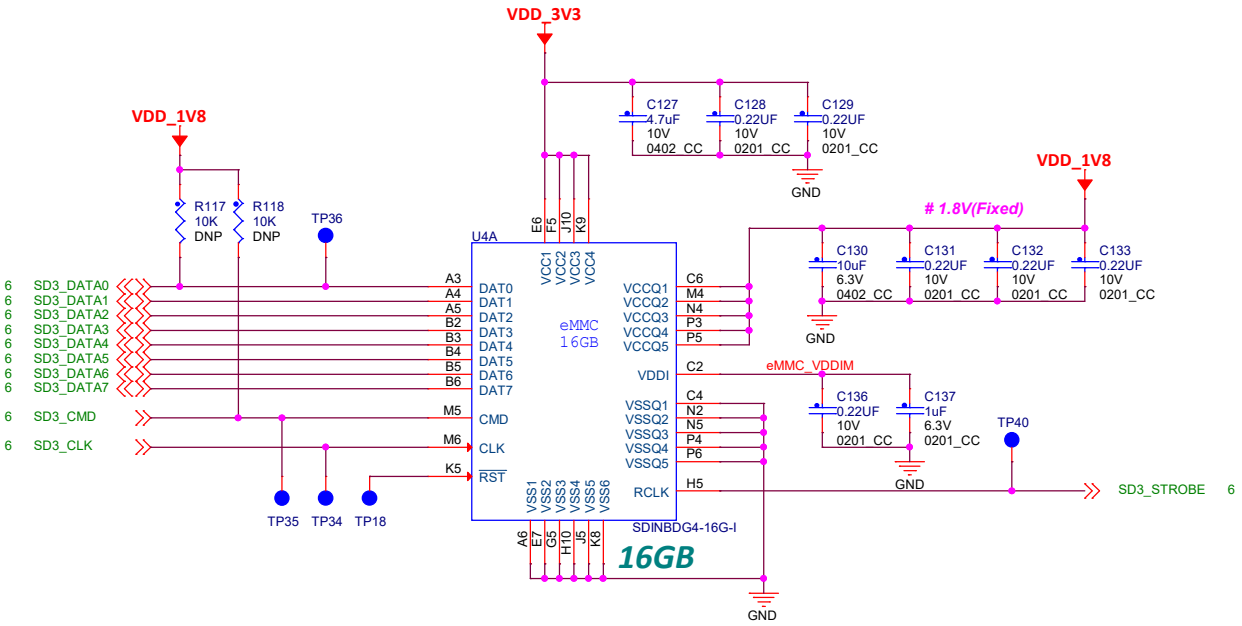
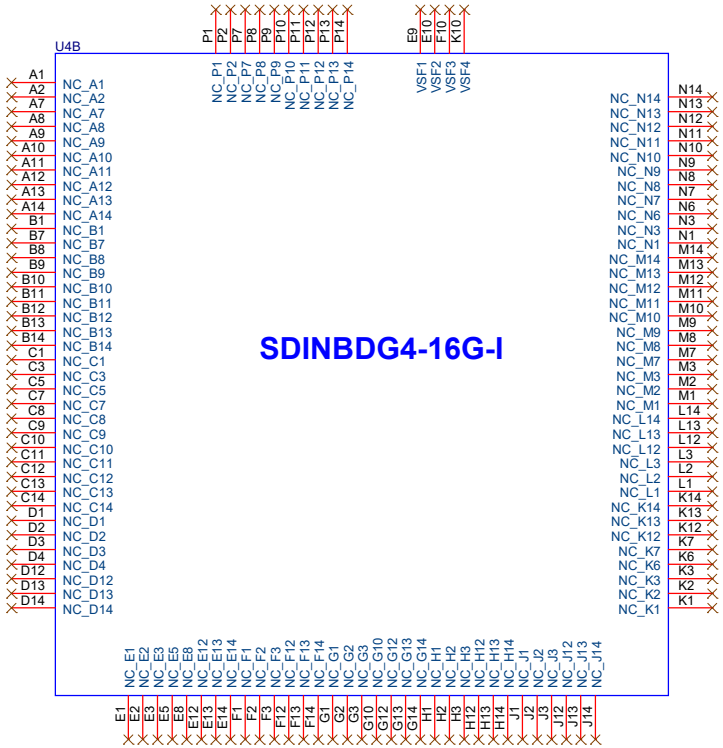
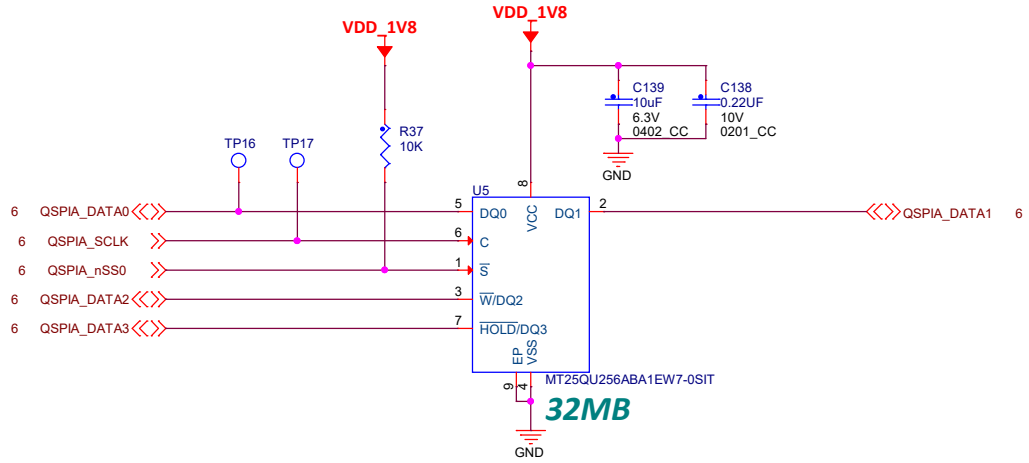
Storage

eMMC





QSPI Flash



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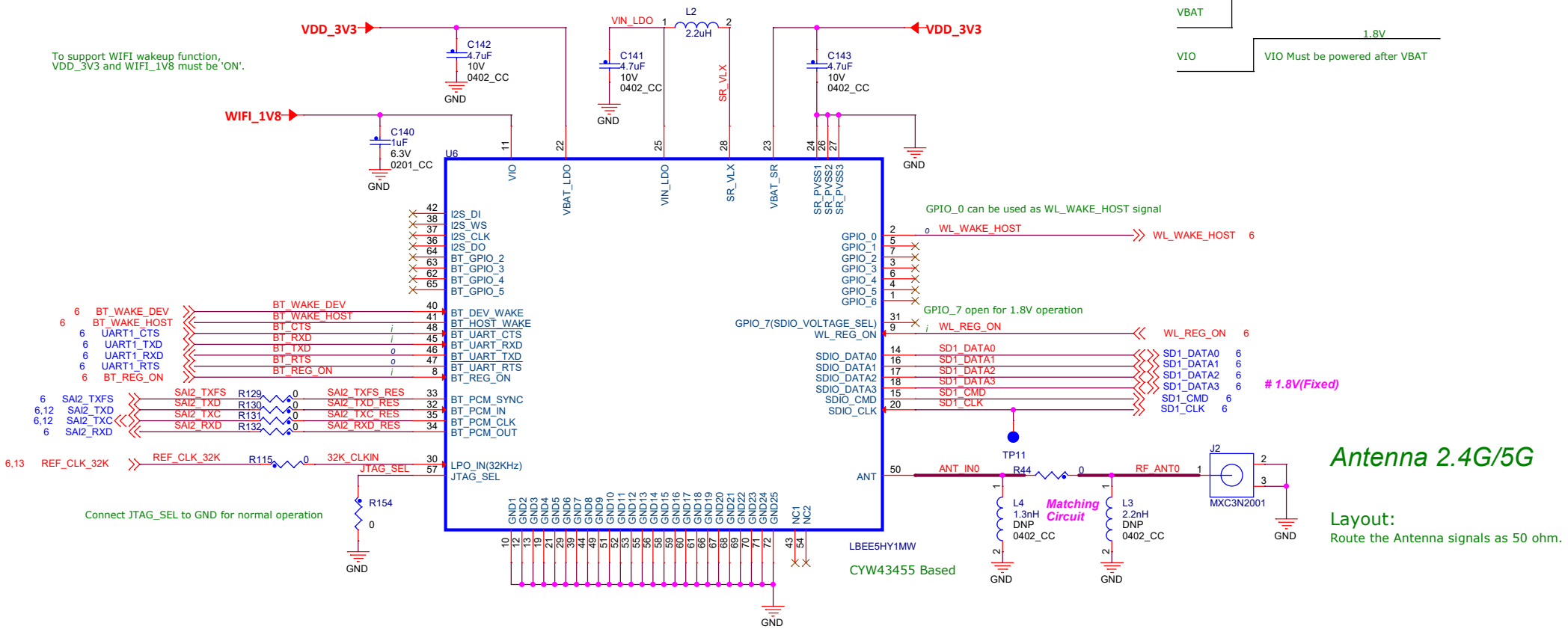
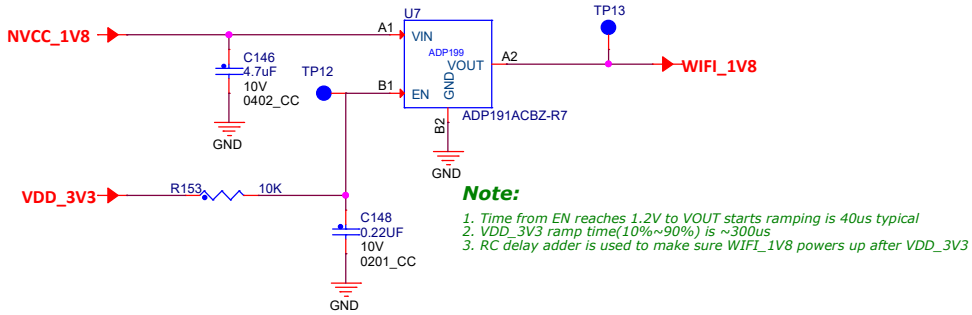
2.4G/5G WIFI/BT Module



Power Sequence

Antenna 2.4G/5G

Layout:
Route the Antenna signals as 50 ohm.



Note:

1. Time from EN reaches 1.2V to VOUT starts ramping is 40us typical
2. VDD_3V3 ramp time(10%~90%) is ~300us
3. RC delay adder is used to make sure WIFI_1V8 powers up after VDD_3V3

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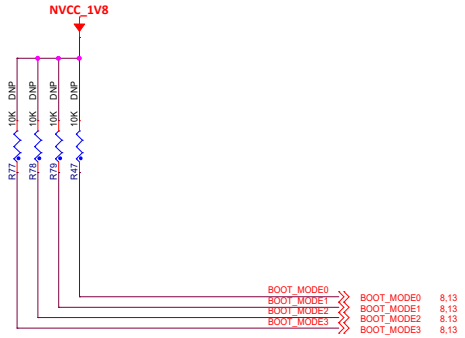
Boot Mode

i.MX8M Nano Boot Mode

BOOT_PIN[3]	BOOT_PIN[2]	BOOT_PIN[1]	BOOT_PIN[0]	Boot Modes
BOOT_MODE3 (TEST_MODE)	BOOT_MODE2 (JTAG_TRST_B)	BOOT_MODE1	BOOT_MODE0	Function
0	0	0	0	Boot From Internal Fuses
0	0	0	1	USB Serial Download
0	0	1	0	USDHC3 (eMMC boot only, SD3 8-bit)
0	0	1	1	USDHC2 (SD boot only, SD2)
0	1	0	0	NAND 8-bit single device 256 page
0	1	0	1	NAND 8-bit single device 512 page
0	1	1	0	QSPI 3B Read
0	1	1	1	QSPI Hyperflash 3.3V
1	0	0	0	ecSPI Boot
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved (Boot on I2C connected to BOOT PIN[3:2])
1	1	0	1	Reserved
1	1	1	0	Infinite Loop Mode
1	1	1	1	Test Mode



Note:

1. BOOT_MODE0-3 singals are used for boot selections

2. BOOT_MODE singals have internal PD before and after POR_B reset is deasserted!

3. When using Base Board for Multi boot selection, you must keep the resistors DNP on SOM board!

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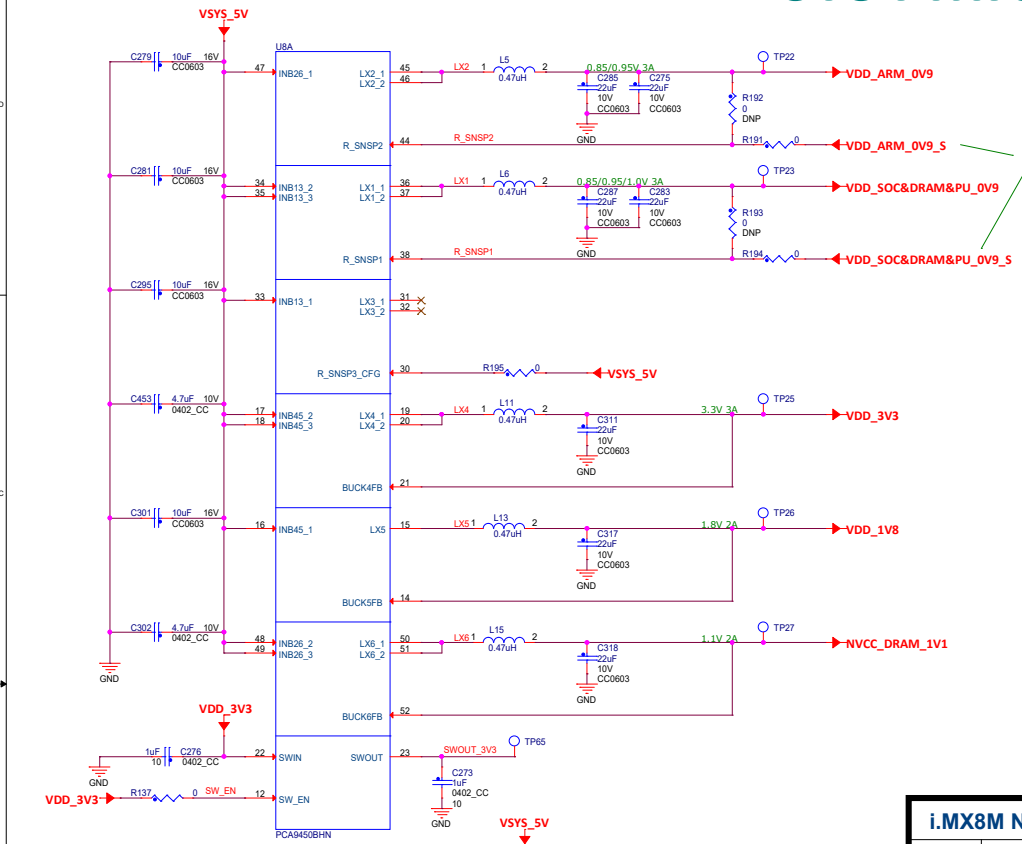
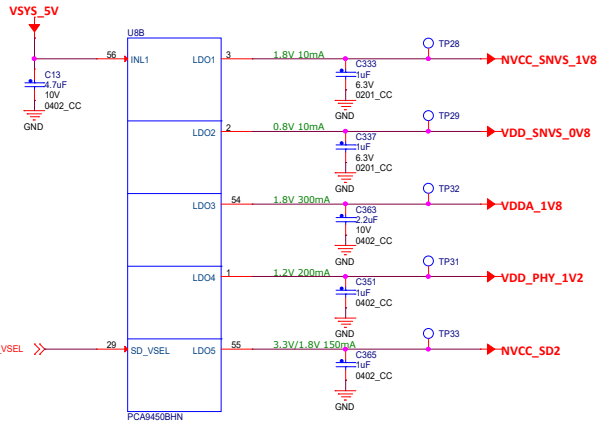
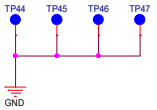
SYS PMIC

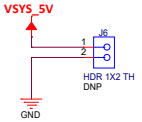


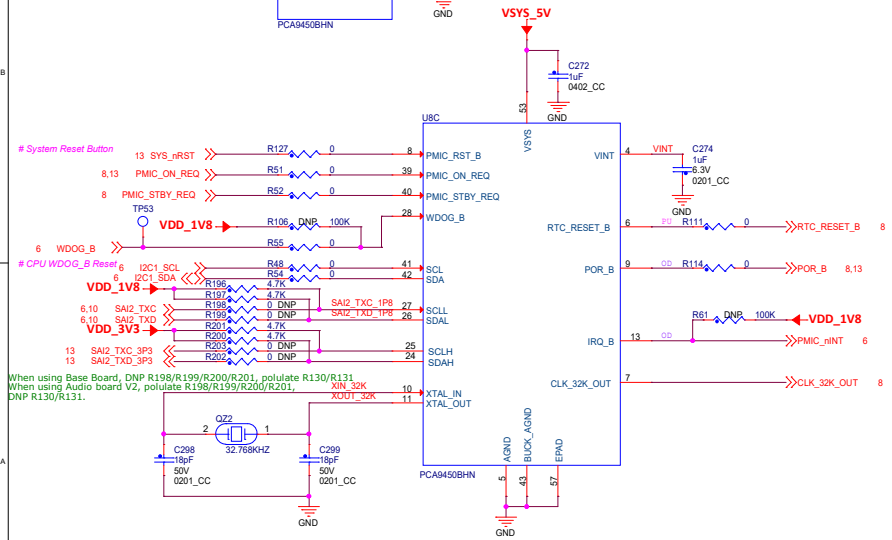


GND Testpoints



Backup PWR Supply





i.MX8M Nano LPDDR4 EVK Power Sequence

SEQ	PWR/Signal	REG	MIN	TYP	MAX	Max Current(mA)
1	NVCC_SNVS_1V8	LDO1	1.62	1.8	1.98	10
2	VDD_SNVS_0V8	LDO2	0.76	0.8	0.9	10
3	RTC_RESET_B	RTC_RESET_B	--	--	--	--
4	CLK_32K_OUT	RTC_CLK	--	--	--	--
5	VDD_SOC&DRAM&PU_0V9	BUCK1	0.78/0.805	0.82/0.85	0.9	3000
6	VDD_ARM_0V9	BUCK2	0.805/0.9/0.95	0.85/0.95/1.0	0.95/1.0/1.05	3000
6	VDDA_1V8	LDO3	1.71	1.8	1.89	300
7	VDD_1V8/NVCC_1V8	BUCK5	1.65	1.8	1.95	2000
8	NVCC_DRAM_1V1	BUCK6	1.06	1.1	1.14	2000
9	VDD_3V3/NVCC_3V3	BUCK4	3	3.3	3.6	3000
9	NVCC_SD2	LDO5	3.0/1.65	3.3/1.8	3.6/1.95	150
10	POR_B	POR_B	--	--	--	--
11	VDD_PHY_1V2	LDO4	1.14	1.2	1.26	150

Note:

1. WDOG_B is used as Cold Reset, external pull up is needed. On EVK, R106 is not necessary, since WDOG_B/GPIO1_IO02 of CPU has internal pull up.
2. PMIC_nINT is ppen drain output, external pull up is needed. On EVK, R61 is not necessary, since PMIC_nINT/GPIO1_IO03 of CPU has internal pull up.
3. AGND/BUCK_AGND should be connected to ground plane through Via. Do not short to EP directly on top layer

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: X PUBI:

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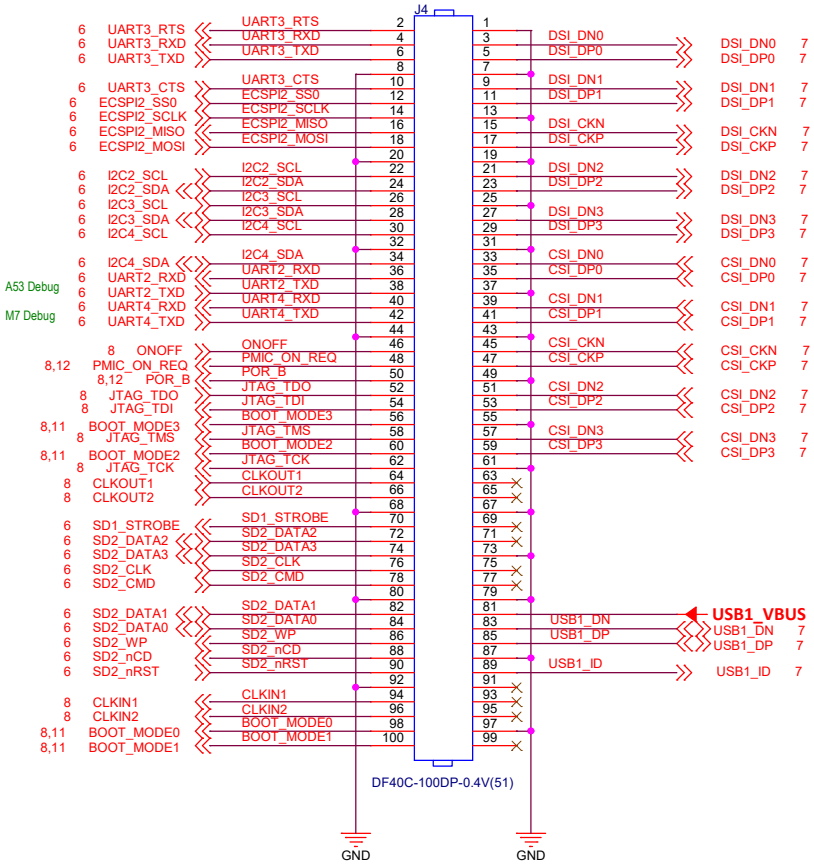
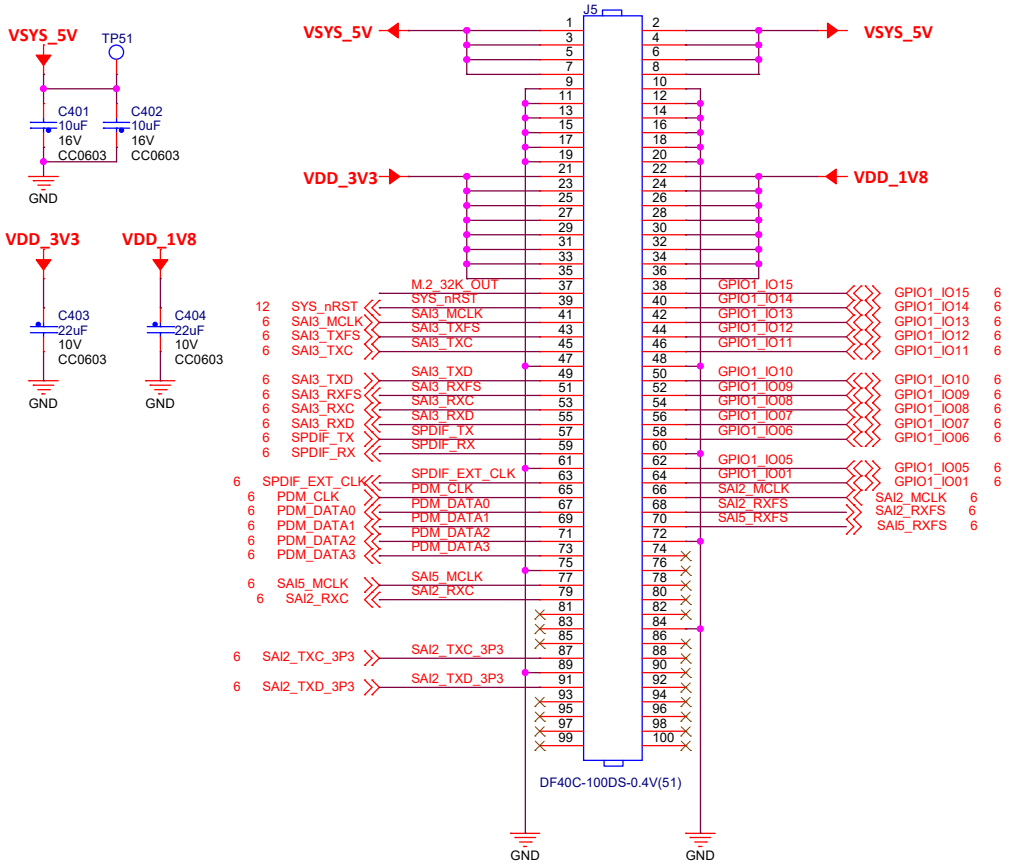
Drawn by: Mac Zhang	Page Title: PMIC PCA9450B		
Approved: <Approver>	Size C	Document Number SCH-46441 PDF: SPF-46441	Rev A1
	Date: Tuesday, November 05, 2019	Sheet 12 of 13	

B2B Connector for CPU Board

Header



Receptacle



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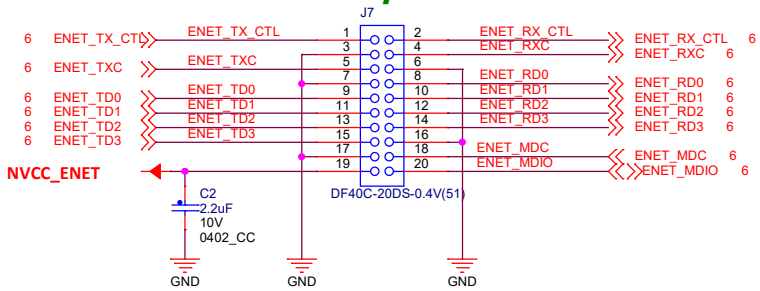

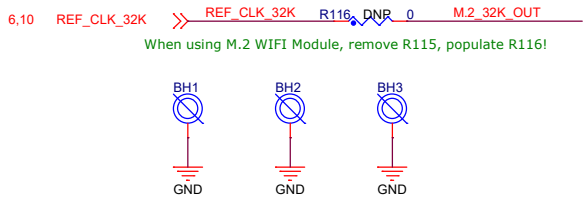

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Designer: Mac Zhang	Drawing Title: **X-815LPD4-CPUCY**		
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