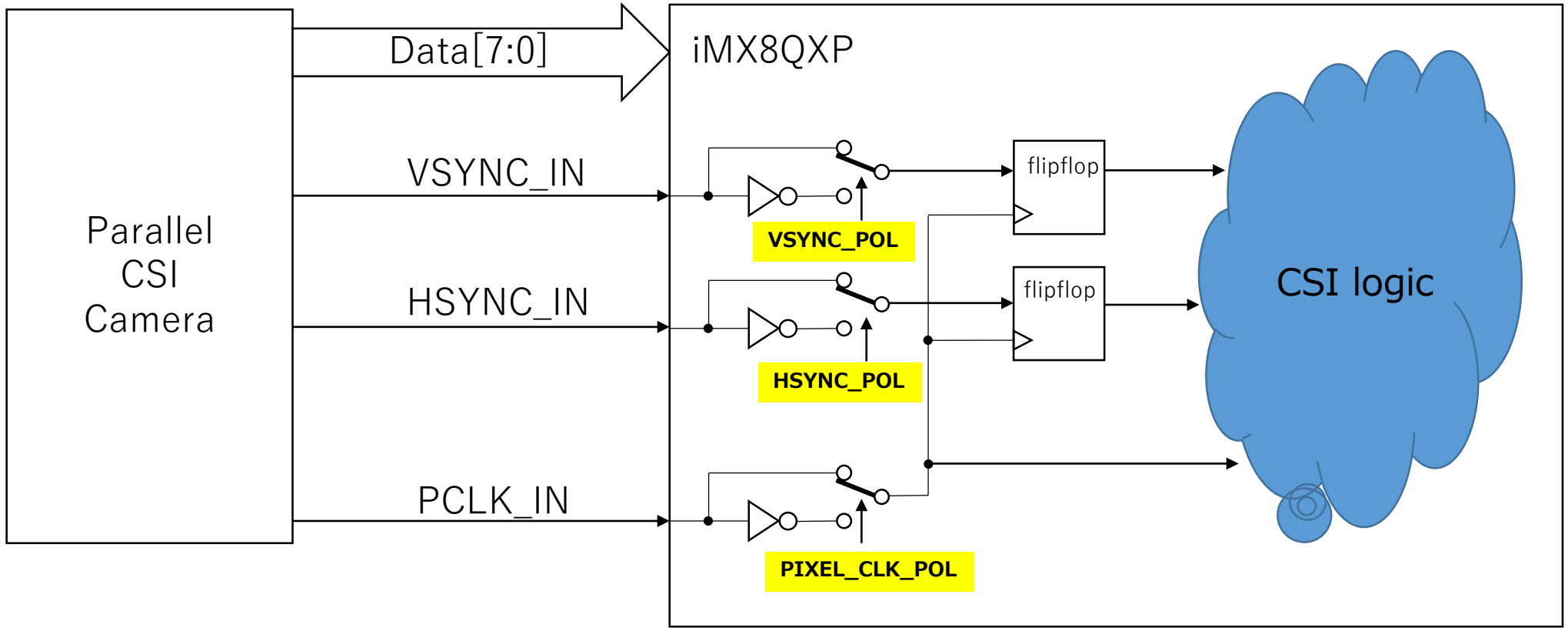
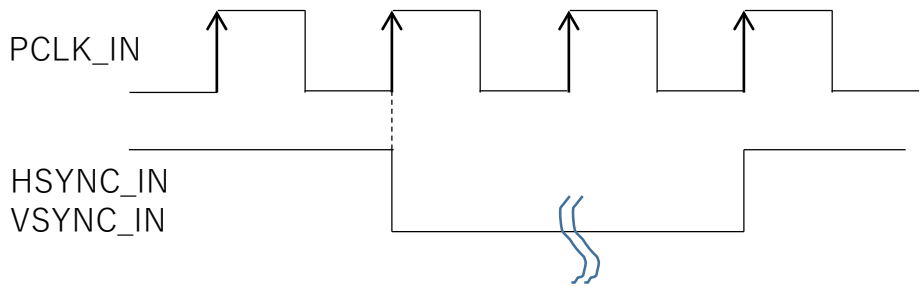


15.8.2.1.8 CSI Interface Control Register (CSI_CTRL_REG_CLR)

Field	Function
3 VSYNC_POL	VSYNC polarity control
2 HSYNC_POL	HSYNC polarity control
1 PIXEL_CLK_POL	Pixel Clock polarity control



Q) Does VSYNC_POL, HSYNC_POL, PIXEL_CLK_POL of CSI_CTRL_REG_CLR look like the circuit diagram above?

(If the camera signal has the timing shown in the figure above, is it better to reverse the PCLK polarity.)