



**FTF 2016**  
TECHNOLOGY FORUM

# ENABLING ULTIMATE MINIATURIZATION AND CUSTOMIZATION WITH THE LATEST SINGLE CHIP SYSTEM MODULE TECHNOLOGY

## SCM-i.MX 6SX and 6SX V-link

NAVJOT CHHABRA  
PRODUCT DEVELOPMENT MANAGER  
SYSTEM SOLUTIONS ORGANIZATION  
FTF-MHW-N1990  
MAY 18<sup>TH</sup>, 2016



# AGENDA

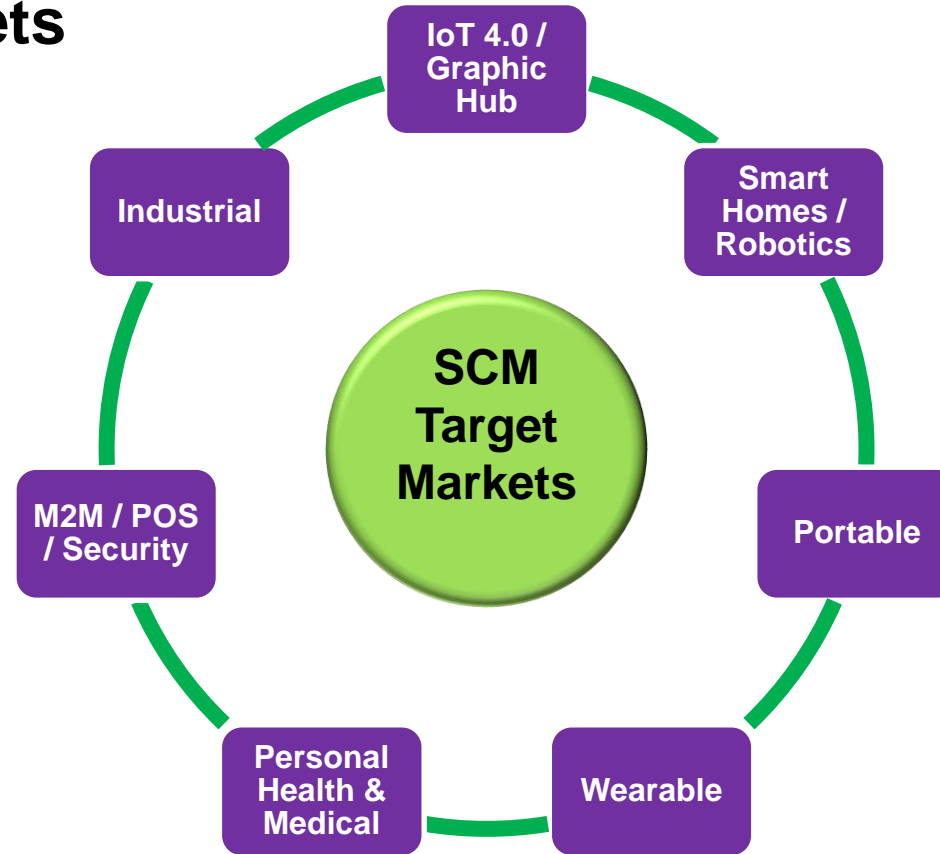
- Introduction
- **Single Chip System Module and 1<sup>st</sup> Product Launch**
- **Single Chip Module Roadmap**
- **Introduction to the Two New SCM Products**
- **Partner Demos**
  - Boundry Devices
  - Code
  - FirstView
- **Summary**
- **Q & A**

# INTRODUCTION



# New solutions for today's markets.

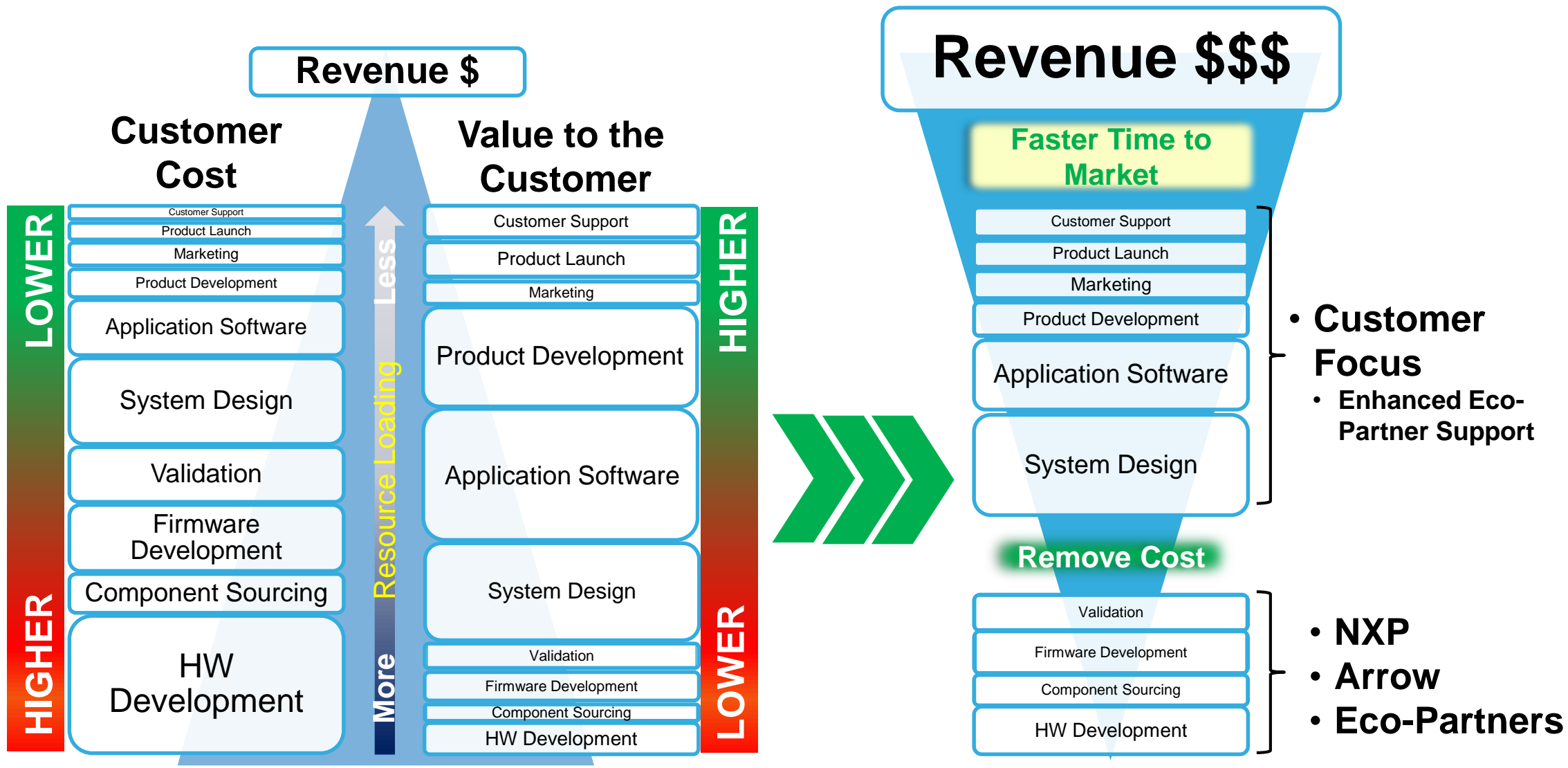
## Targeted Growth Markets



## What emerging products need.

- More integration
- More communications
- More sensing
- More features
- More access
- Faster time to Market

# Customer Value Based Costing



# INTRODUCTION TO THE SINGLE CHIP SYSTEM MODULE



# Why Choose a Single Chip System Module (SCM)?

- **>50% reduction** over current discrete solutions for your application board
- Reduces average **development time by up to 25%**
- **Reduces design complexity** of integrating and validating DDR memory and power management into customer design
- **Eliminates extensive testing** and validation for your application
- **Higher level of customer enablement** (hardware integration and software enablement)
- **Reduces our customer's supply chain complexity**
- **Provide customizable option** for unique customer solutions

**PRODUCTION  
LAUNCHED: SCM-  
I.MX 6DUAL / 6 QUAD**



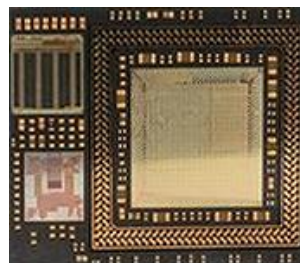


# The World's Smallest Single Chip System



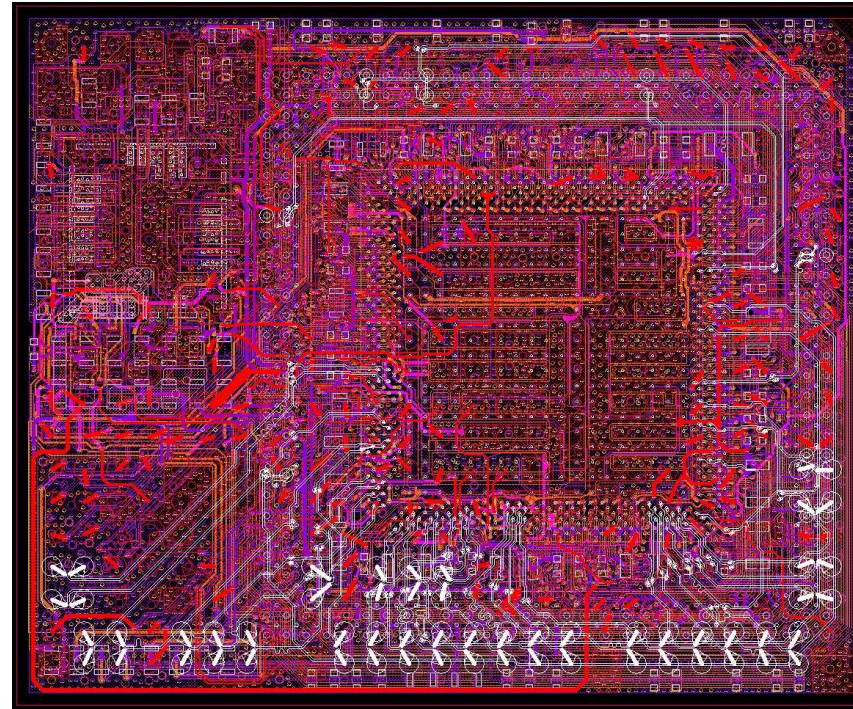
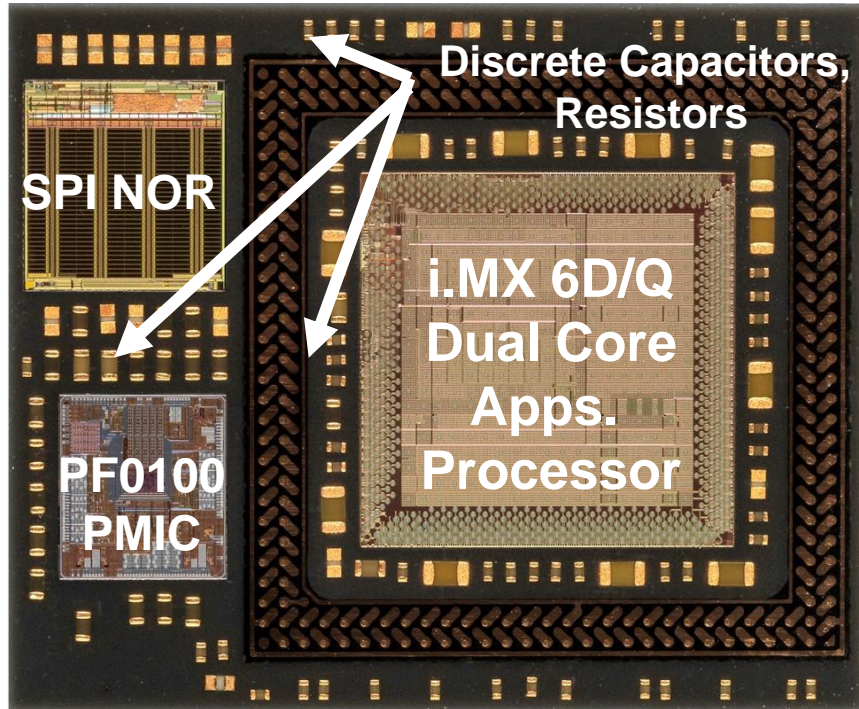
## SCM-i.MX 6D / Q

*Smaller than a 2-cent Euro or U.S. Dime*

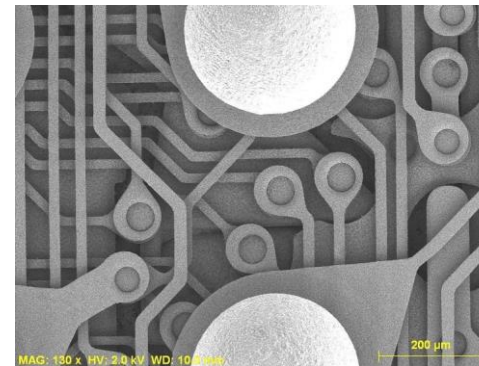
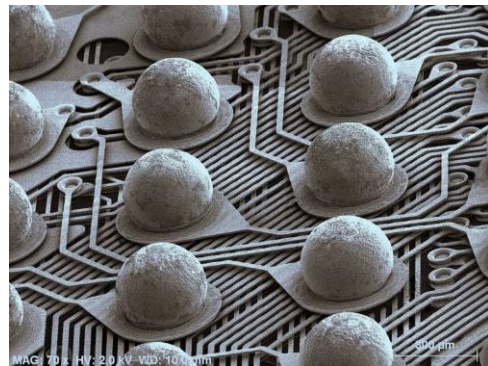
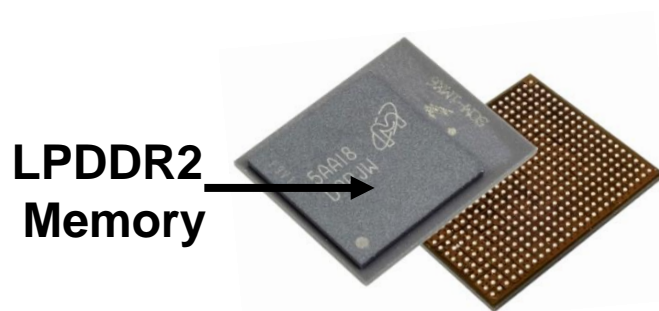


**Production Launched February 2016**

# Family 1 SCM-i.MX 6D/6Q



- 14mm x 17mm x 1.7mm
- i.MX6Dual or i.MX6Quad
- PF0100 PMIC
- 16MB SPI NOR
- Enabled for 1GB or 2GB LPDDR2
- 109 discrete components
- 500 BGA balls P0.65mm

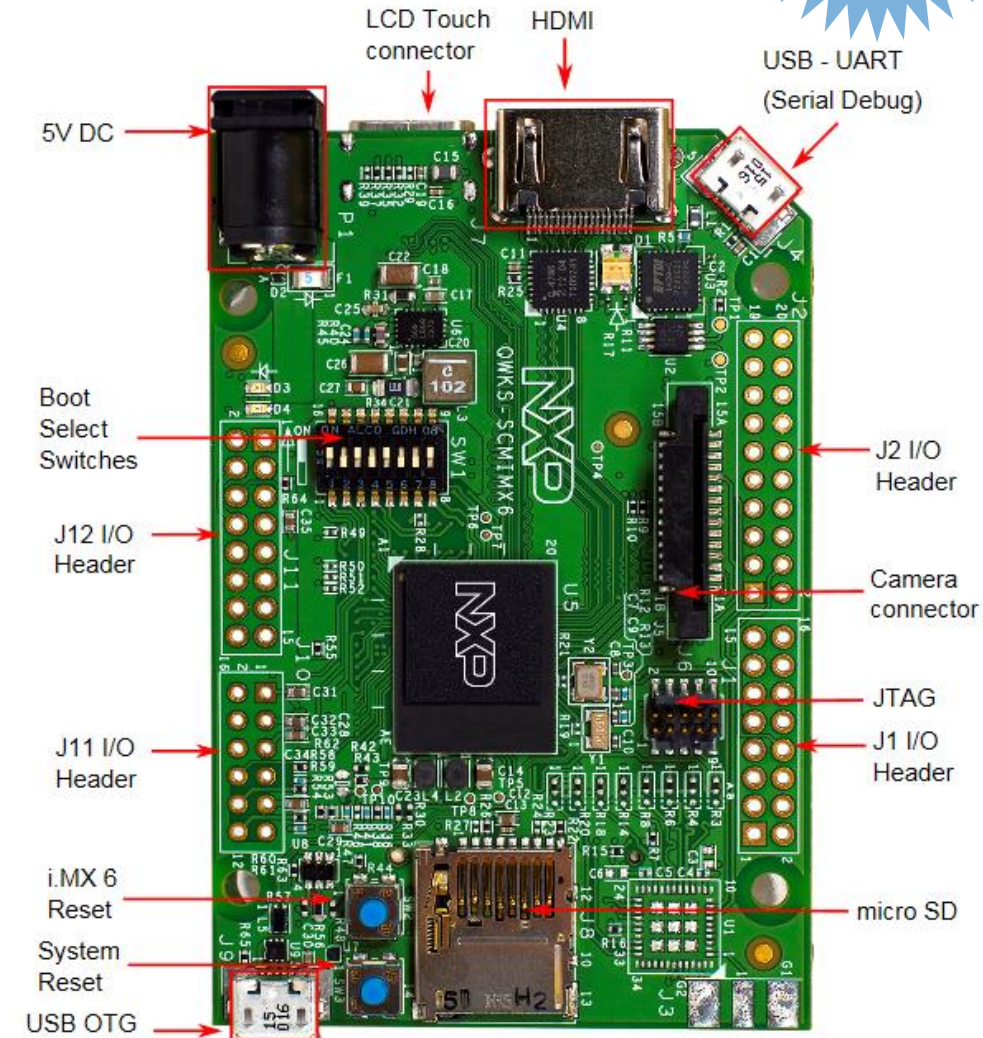


# SCM-i.MX 6Dual/6Quad Collateral

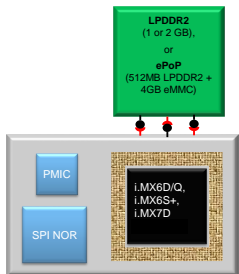
- Orderable part #'s in place (NXP p/n, Arrow p/n)

Assembly Part Number	SCM Revision	SCM Family	DRAM	DRAM Part Number	Qualification Tier
MSCMMX6DZDK08AB	Rev1.0	SCM-i.MX6D	-	-	Commercial
MSCMMX6QZDK08AB	Rev1.0	SCM-i.MX6Q	-	-	Commercial
MSCMMX6DZDK08AB1G0A	Rev1.0	SCM-i.MX6D	1 GB LPDDR2	MT42L128M64D2LL-25AT:A	Commercial
MSCMMX6DZDK08AB2G0A	Rev1.0	SCM-i.MX6D	2 GB LPDDR2	MT42L256M64D4LM-18 WT:A	Commercial
MSCMMX6QZDK08AB1G0A	Rev1.0	SCM-i.MX6Q	1 GB LPDDR2	MT42L128M64D2LL-25AT:A	Commercial
MSCMMX6QZDK08AB2G0A	Rev1.0	SCM-i.MX6Q	2 GB LPDDR2	MT42L256M64D4LM-18 WT:A	Commercial

- Development boards in place along with support HW (LVDS display, MIPI camera, WLAN +BT modules, etc).
- NXP web site live ([www.nxp.com/scm](http://www.nxp.com/scm))
  - Datasheet, factsheets, users guide HW developers guide, App notes, Linux SW patch releases, etc
- Software Enablement
  - Linux.
  - Android (July)
- Longevity program (10yr, Feb 2026) on SCM.



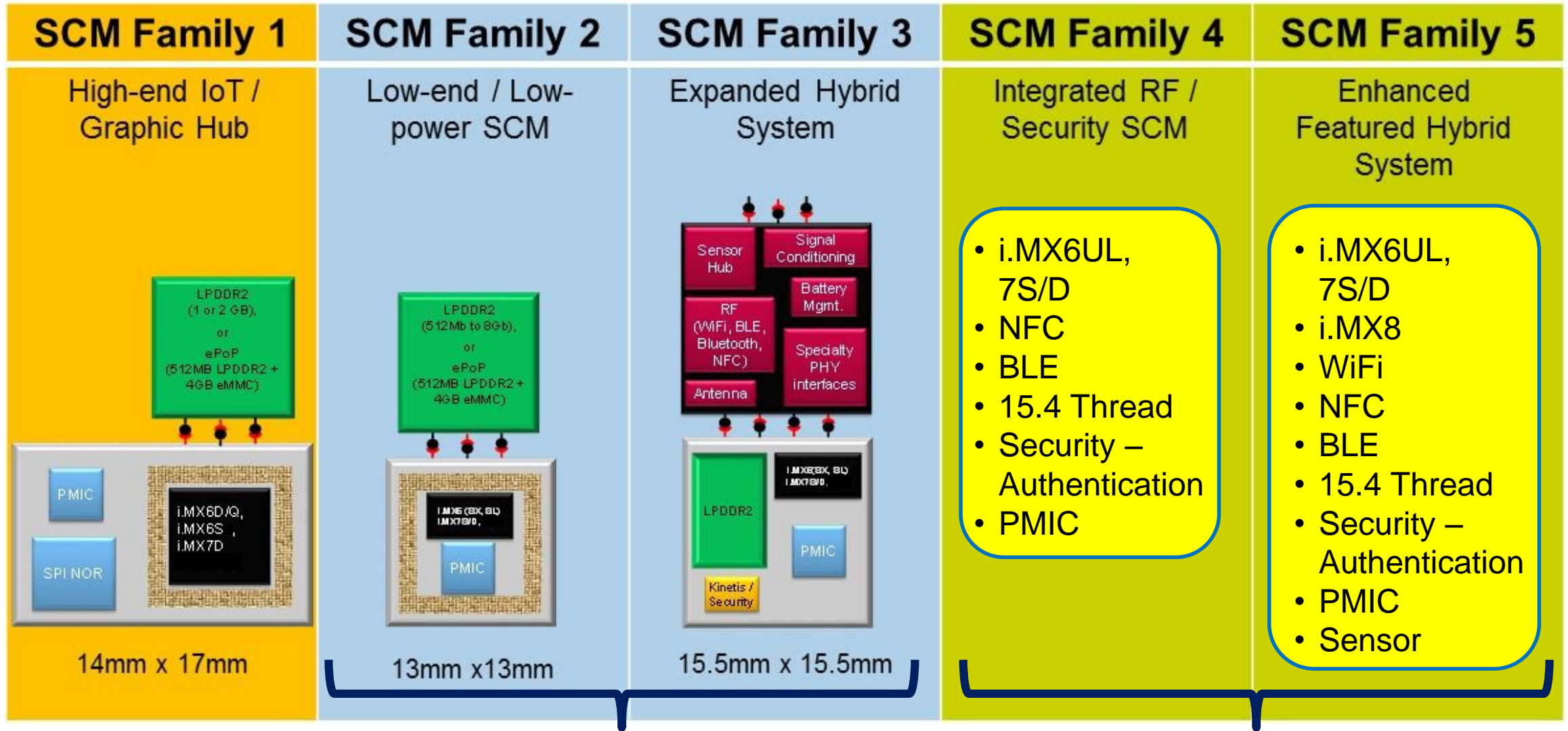
# Derivative Products For Family 1

SCM	SCM Family	SCM Family	Configuration	Availability	
				Beta Samples	Production
SCM-i.MX6D (Commercial)	1	 <p>The diagram shows a central i.MX6D/Q chip. To its left are two blue boxes labeled 'PMIC' and 'SPI NOR'. Above the chip is a green box labeled 'LPDDR2 (1 or 2 GB) or ePoP (512MB LPDDR2 + 4GB eMMC)'. Red lines indicate connections between the chip and these components.</p>	i.MX6D, PMIC, SPI-NOR, PoP LPDDR2 Memory (1 or 2 GB)		In Production
SCM-i.MX6Q (Commercial)	1		i.MX6D, PMIC, SPI-NOR, PoP LPDDR2 Memory (1 or 2 GB)		In Production
SCM-i.MX6D ePoP (Commercial)	1		i.MX6D, PMIC, SPI-NOR, ePoP (512MB LPDDR2 + 4GB eMMC) Memory	Available	Jun-16
SCM-i.MX6S (Commercial)	1		i.MX6S*, PMIC, ePoP or LPDDR2	Jun-16	Jul-16
SCM-i.MX6D/Q (Industrial)	1		i.MX6D/Q, PMIC, SPI-NOR, PoP LPDDR2 Memory		In Production

# SINGLE CHIP MODULE ROADMAP



# System Solutions Family of Products



Launching this week

In definition

# INTRODUCTION TO THE TWO NEW FAMILIES IN THE SCM FAMILY



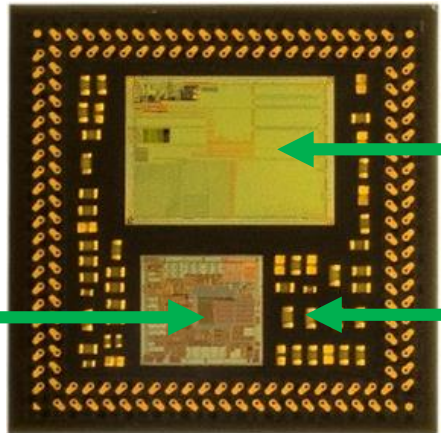
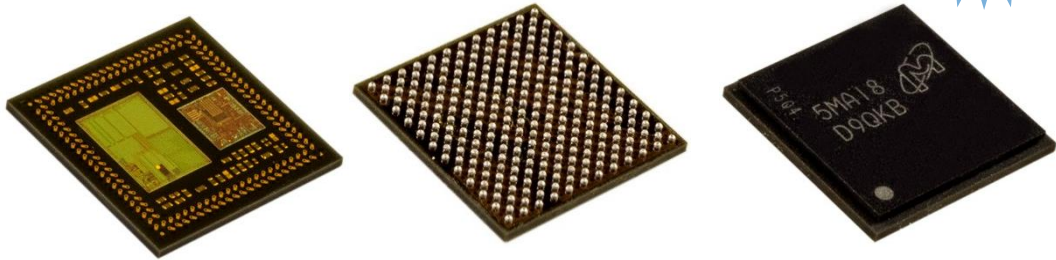
# SCM-i.MX 6SX





# Family 2 SCM-i.MX 6SX (13mm x 13mm)

Available  
BETA



i.MX6SX Apps Processor

47 Discrete components

PD0100 PMIC

PoP Memory options:

- 512MB, 1GB LPDDR2
- ePoP (512MB LPDDR@ + 4GB eMMC)

0.75mm Ball pitch (diagonal array)

BSP released

Enabled for Linux

LPDDR2 - 168 FBGA
512 MB LPDDR2/ 1 GB LPDDR2 / ePoP - 0.5GB LPDDR2 + 4GB eMMC

## SCM-i.MX6 SoloX

<table border="1"> <tr><th>System Control</th></tr> <tr><td>Secure JTAG</td></tr> <tr><td>PLL, Osc</td></tr> <tr><td>Clock &amp; Reset</td></tr> <tr><td>Smart DMA</td></tr> <tr><td>IOMUX</td></tr> <tr><td>Timer x3</td></tr> <tr><td>PWM x8</td></tr> <tr><td>Watch Dog x3</td></tr> <tr><td>RDC</td></tr> </table>	System Control	Secure JTAG	PLL, Osc	Clock & Reset	Smart DMA	IOMUX	Timer x3	PWM x8	Watch Dog x3	RDC	<table border="1"> <tr><th>CPU1 Platform</th></tr> <tr><td colspan="2">Cortex-A9</td></tr> <tr><td>32KB I-cache</td><td>32KB D-cache</td></tr> <tr><td>NEON</td><td>PTM</td></tr> <tr><td colspan="2">256KB L2-cache</td></tr> </table>	CPU1 Platform	Cortex-A9		32KB I-cache	32KB D-cache	NEON	PTM	256KB L2-cache		<table border="1"> <tr><th>Connectivity</th></tr> <tr><td>MMC 4.4 / SD 3.0 x3</td></tr> <tr><td>UART x6</td></tr> <tr><td>I<sup>2</sup>C x 4, SPI x5</td></tr> <tr><td>USB2 OTG &amp; PHY</td></tr> <tr><td>USB2 Host &amp; PHY</td></tr> <tr><td>1Gb Ethernet</td></tr> <tr><td>ESAI, I<sup>2</sup>S/SSI x5</td></tr> <tr><td>S/PDIF Tx/Rx</td></tr> <tr><td>2 x FlexCAN</td></tr> <tr><td>GPIO, Keypad</td></tr> <tr><td>MLB25/50*</td></tr> <tr><td>1x PCIe 2.0 (x1 lane)*</td></tr> </table>	Connectivity	MMC 4.4 / SD 3.0 x3	UART x6	I <sup>2</sup> C x 4, SPI x5	USB2 OTG & PHY	USB2 Host & PHY	1Gb Ethernet	ESAI, I <sup>2</sup> S/SSI x5	S/PDIF Tx/Rx	2 x FlexCAN	GPIO, Keypad	MLB25/50*	1x PCIe 2.0 (x1 lane)*
System Control																																		
Secure JTAG																																		
PLL, Osc																																		
Clock & Reset																																		
Smart DMA																																		
IOMUX																																		
Timer x3																																		
PWM x8																																		
Watch Dog x3																																		
RDC																																		
CPU1 Platform																																		
Cortex-A9																																		
32KB I-cache	32KB D-cache																																	
NEON	PTM																																	
256KB L2-cache																																		
Connectivity																																		
MMC 4.4 / SD 3.0 x3																																		
UART x6																																		
I <sup>2</sup> C x 4, SPI x5																																		
USB2 OTG & PHY																																		
USB2 Host & PHY																																		
1Gb Ethernet																																		
ESAI, I <sup>2</sup> S/SSI x5																																		
S/PDIF Tx/Rx																																		
2 x FlexCAN																																		
GPIO, Keypad																																		
MLB25/50*																																		
1x PCIe 2.0 (x1 lane)*																																		
<table border="1"> <tr><th>Security</th></tr> <tr><td>RNG</td></tr> <tr><td>TrustZone</td></tr> <tr><td>Ciphers</td></tr> <tr><td>Security Ctrl</td></tr> <tr><td>Secure RTC</td></tr> <tr><td>eFuses</td></tr> </table>	Security	RNG	TrustZone	Ciphers	Security Ctrl	Secure RTC	eFuses	<table border="1"> <tr><th>CPU2 Platform</th></tr> <tr><td colspan="2">Cortex-M4, MPU, FPU</td></tr> <tr><td>16KB I-cache</td><td>16KB D-cache</td></tr> <tr><td colspan="2">64KB TCM</td></tr> </table>	CPU2 Platform	Cortex-M4, MPU, FPU		16KB I-cache	16KB D-cache	64KB TCM		<table border="1"> <tr><th>External Memory</th></tr> <tr><td>NAND (BCH62)</td></tr> <tr><td>16-bit NOR</td></tr> <tr><td>2x DDR Quad SPI</td></tr> <tr><td>LPDDR2 x32</td></tr> </table>	External Memory	NAND (BCH62)	16-bit NOR	2x DDR Quad SPI	LPDDR2 x32													
Security																																		
RNG																																		
TrustZone																																		
Ciphers																																		
Security Ctrl																																		
Secure RTC																																		
eFuses																																		
CPU2 Platform																																		
Cortex-M4, MPU, FPU																																		
16KB I-cache	16KB D-cache																																	
64KB TCM																																		
External Memory																																		
NAND (BCH62)																																		
16-bit NOR																																		
2x DDR Quad SPI																																		
LPDDR2 x32																																		
<table border="1"> <tr><th>Display and Camera Interface</th></tr> <tr><td>24-bit RGB</td></tr> <tr><td>1ch LVDS</td></tr> <tr><td>2x 20-bit CSI*</td></tr> </table>	Display and Camera Interface	24-bit RGB	1ch LVDS	2x 20-bit CSI*	<table border="1"> <tr><th>Multimedia</th></tr> <tr><td colspan="2">Hardware Graphics Accelerators</td></tr> <tr><td>3D</td><td>2D</td></tr> <tr><th colspan="2">PXP</th></tr> <tr><td>CSC</td><td>Rotate</td></tr> <tr><td>Combine</td><td>Gamma Mapping</td></tr> <tr><th>Audio</th></tr> <tr><td>ASRC</td></tr> </table>	Multimedia	Hardware Graphics Accelerators		3D	2D	PXP		CSC	Rotate	Combine	Gamma Mapping	Audio	ASRC	<table border="1"> <tr><th>ADC</th></tr> <tr><td>8ch 12-bit ADC*</td></tr> </table>	ADC	8ch 12-bit ADC*													
Display and Camera Interface																																		
24-bit RGB																																		
1ch LVDS																																		
2x 20-bit CSI*																																		
Multimedia																																		
Hardware Graphics Accelerators																																		
3D	2D																																	
PXP																																		
CSC	Rotate																																	
Combine	Gamma Mapping																																	
Audio																																		
ASRC																																		
ADC																																		
8ch 12-bit ADC*																																		

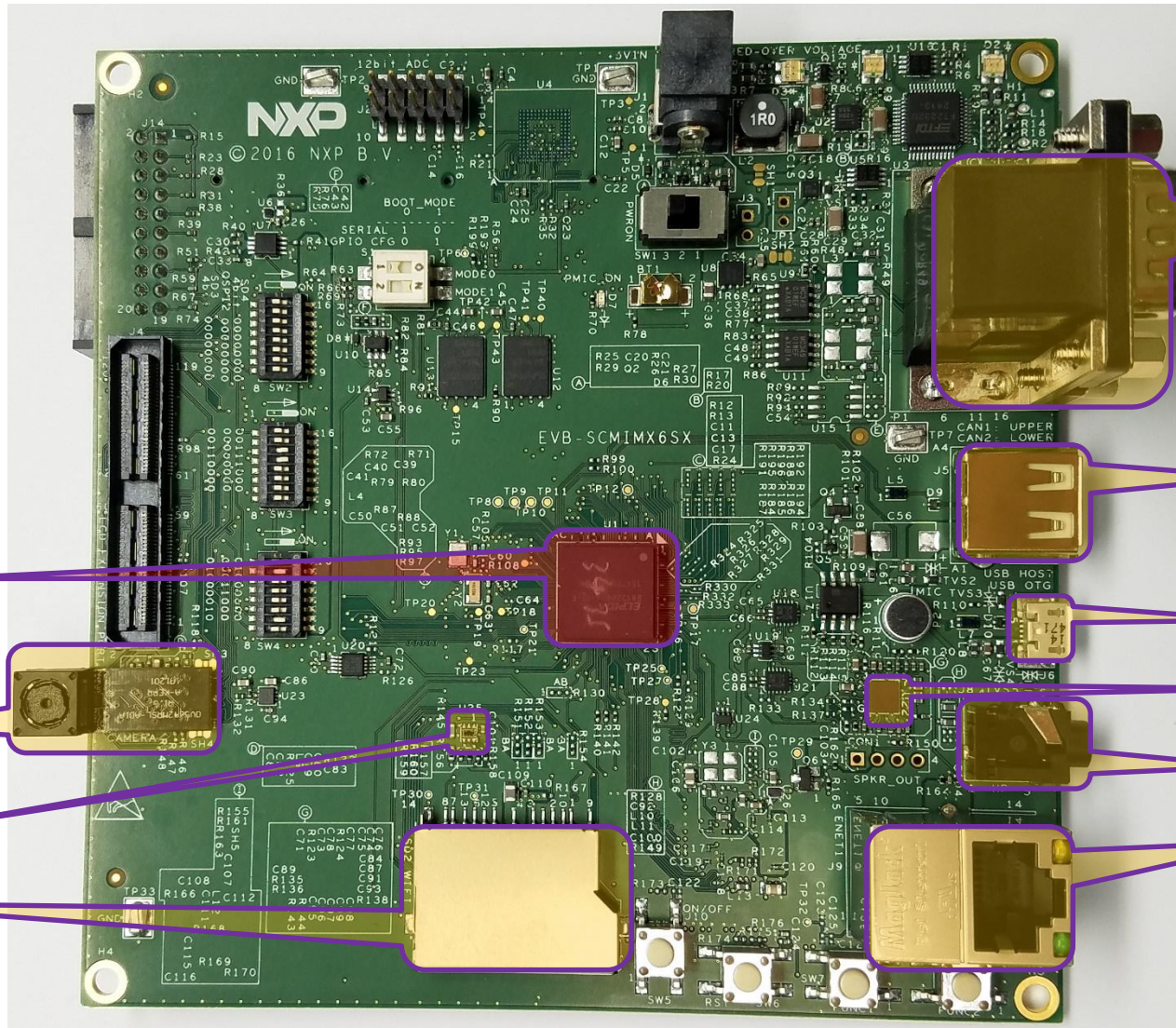
Power Management - MMPF0100		
SW1AB	SW1C*	SW2
SW3AB	SW4*	SWBST
VGEN1*	VGEN2*	VGEN3
VGEN4	VGEN5*	VGEN6

\* These features are either unavailable or reduced in functionality on the 265BGA.



# SCM-i.MX 6SX Evaluation Board

????



CAN ports

USB HOST

USB OTG

WM8962B Audio  
Codec  
Audio Headphone

RGMII

- NXP extranet site live with preliminary documentation, NDA required
  - [www.nxp.com/go/scm](http://www.nxp.com/go/scm)
  - Datasheet, fact sheet, SW users guide, Linux SW patch release (beta)
- Software Enablement
  - Linux (3.14.x kernel) beta release

EVB-SCMIMX6SX

# SCM-i.MX 6SX V-Link



# Motivation for Developing the SCM V-Link Hybrid Module

## What does the SCM provide

- Providing customers an integrated Application processor + PMIC + Memory
  - Address design and signal integrity challenges
- Smaller form factor with high level of functionality

## What would customers also like to have

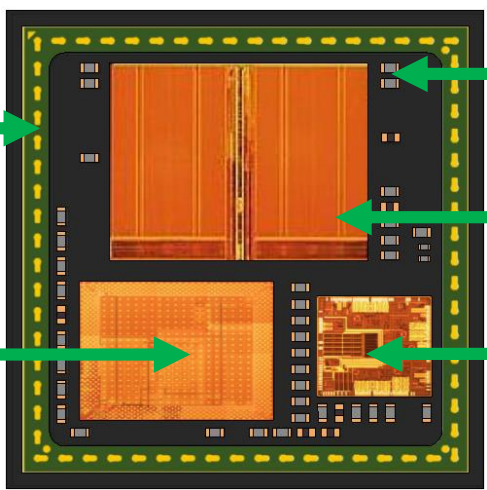
- Provide flexibility in adding their own features and functionality
  - Adding RF (Wi-Fi, BLE, NFC, etc), Sensors, Audio Codex, PHY interfaces, etc.
- Ability to use contract manufactures for their own ‘Top Board’
  - PCB or substrates with off the shelf surface mount components

# Family 3 SCM-i.MX 6SX V-Link (15.5mm x 15.5mm)

Available ALPHA

NXP Base SCM

V-Link Signal Bus

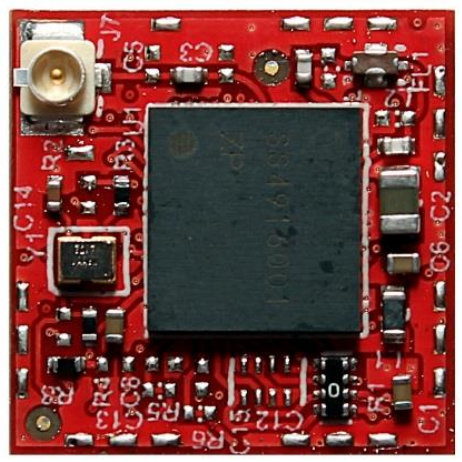


Discrete components

LPDDR2 Memory

PD0100 PMIC

i.MX 6SX Apps Processor

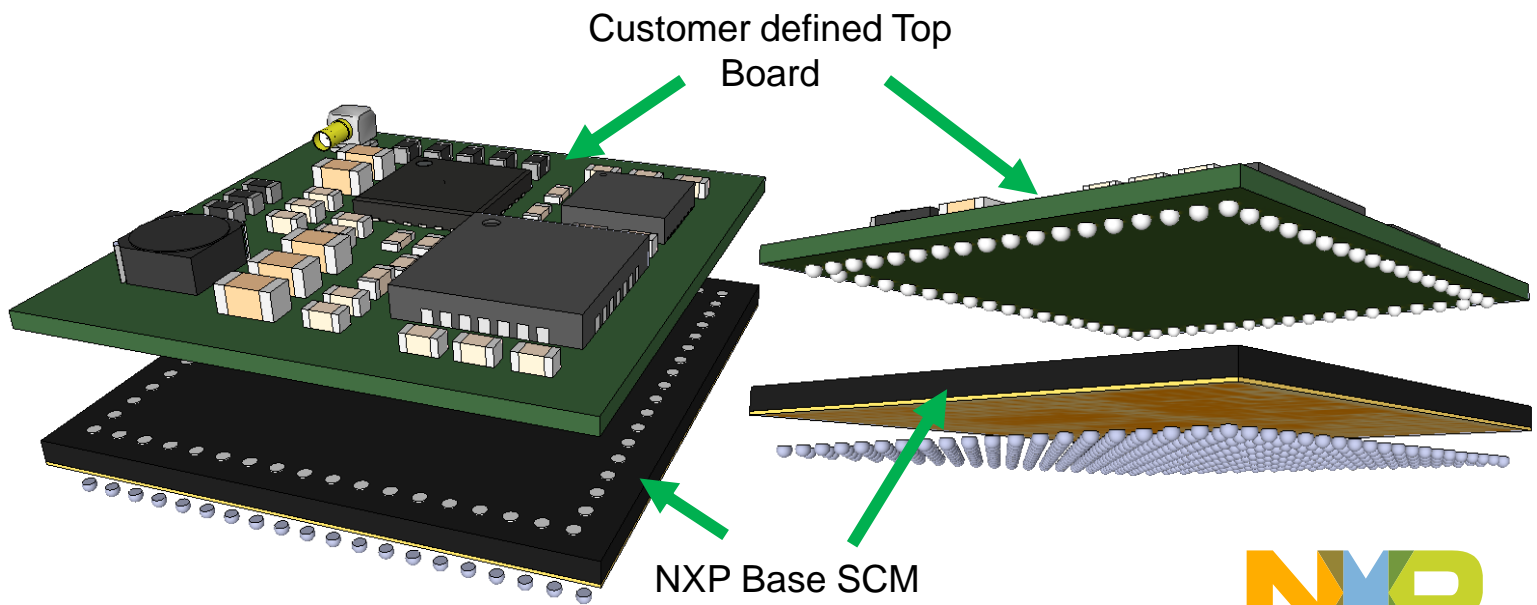


Custom Top Board (PCB or Substrate Based):

- RF, Sensors, Battery mgmt., PHY interface, Audio Codex, etc

0.75mm Ball pitch

BSP released  
Enabled for Linux



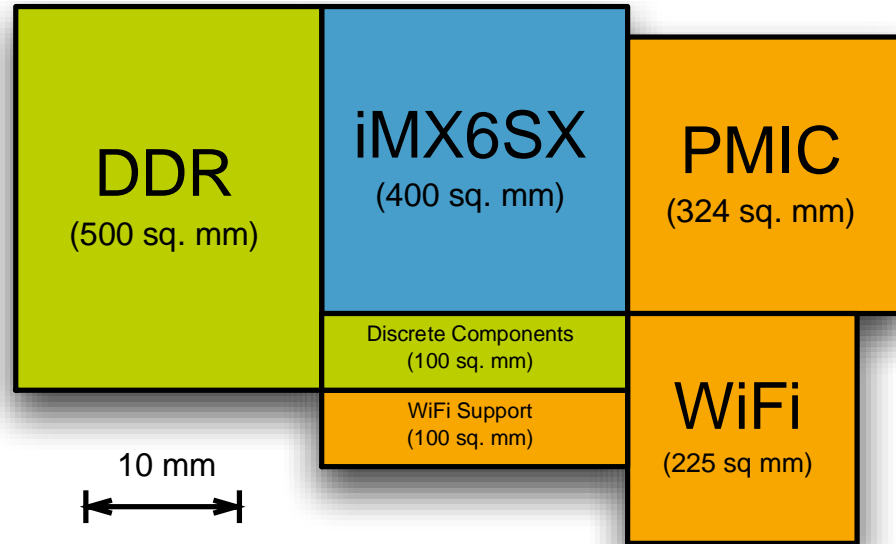
Customer defined Top Board

NXP Base SCM

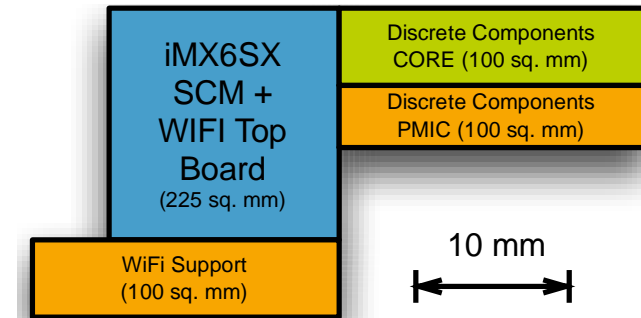


# Change in i.MX6 Design Topology

Traditional layout using discrete IC and components on a PCB board



Equivalent PCB Board area utilizing NXP SCM with the V-Link Top Board



- **67.9% reduction** in board area by utilizing the NXP Base SCM (i.MX6SX + PMIC + Memory + Discretetes)
- **69.2% reduction** in board area by utilizing the SCM Top Board for the WiFi + BT + Discrete module)

# SCM-i.MX 6SX V-Link BGA Interface

The SCMIMX6SX V-LINK modules supports the i.MX 6SX, PF0100, and LPDDR2 device interfaces

## Summary of features

### I.MX 6SX

- All user IO interfaces except the following
  - ADC2, RGMII2, VADC
- All PoP signals connected to the BGA for user selection

### PF0100

- All power interfaces, 6 switchers, 6 LDOs
- Switchers scaled to meet system requirements

### 512MB LPDDR2

- Fully embedded support
- Only 1.2 V power connection required on the PCB. (PMIC interface)

### POP Interface

- Two user defined power domains
- Ten Pass Thru signals for user defined IO interfaces. These pins connect from PoP to BGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	GN0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0
B	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0	CS0_DATA0
C	CS0_DATA0	CS0_DATA0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0
D	CS0_DATA0	CS0_DATA0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0
E	GN0	CS0_DATA0	KEY_ROW0	KEY_ROW0	GN0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0
F	CS0_DATA0	CS0_DATA0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0
G	CS0_DATA0	CS0_DATA0	KEY_ROW0	GN0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0
H	CS0_DATA0	CS0_DATA0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0
J	KEY_ROW0	GN0	KEY_ROW0	GN0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0
K	KEY_ROW0	GN0	KEY_ROW0	GN0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0
L	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0
M	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0
N	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0
P	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0
R	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0
T	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0
U	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0
V	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0
W	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0
Y	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0	KEY_ROW0



# SCM-i.MX6SX V-Link Bus Signaling

- V\_LINK Bus is a custom PoP interface with i.MX6 IOs and system power
- V-LINK was designed to directly support RF (Wi-Fi, BLE, NFC, 15.4, etc) Sensors and other common peripherals
- V-LINK additionally supports user defined bus signals to generate a robust customizable bus
- i.MX6 Interfaces supported:
  - SDIO – 4-bit
  - SPI
  - UART
  - I2C
  - SSI
  - CAN
- PMIC powers
- Two User Defined Power Supply Rails
- 10 User Defined Pass Thru Signals (BGA to PoP)

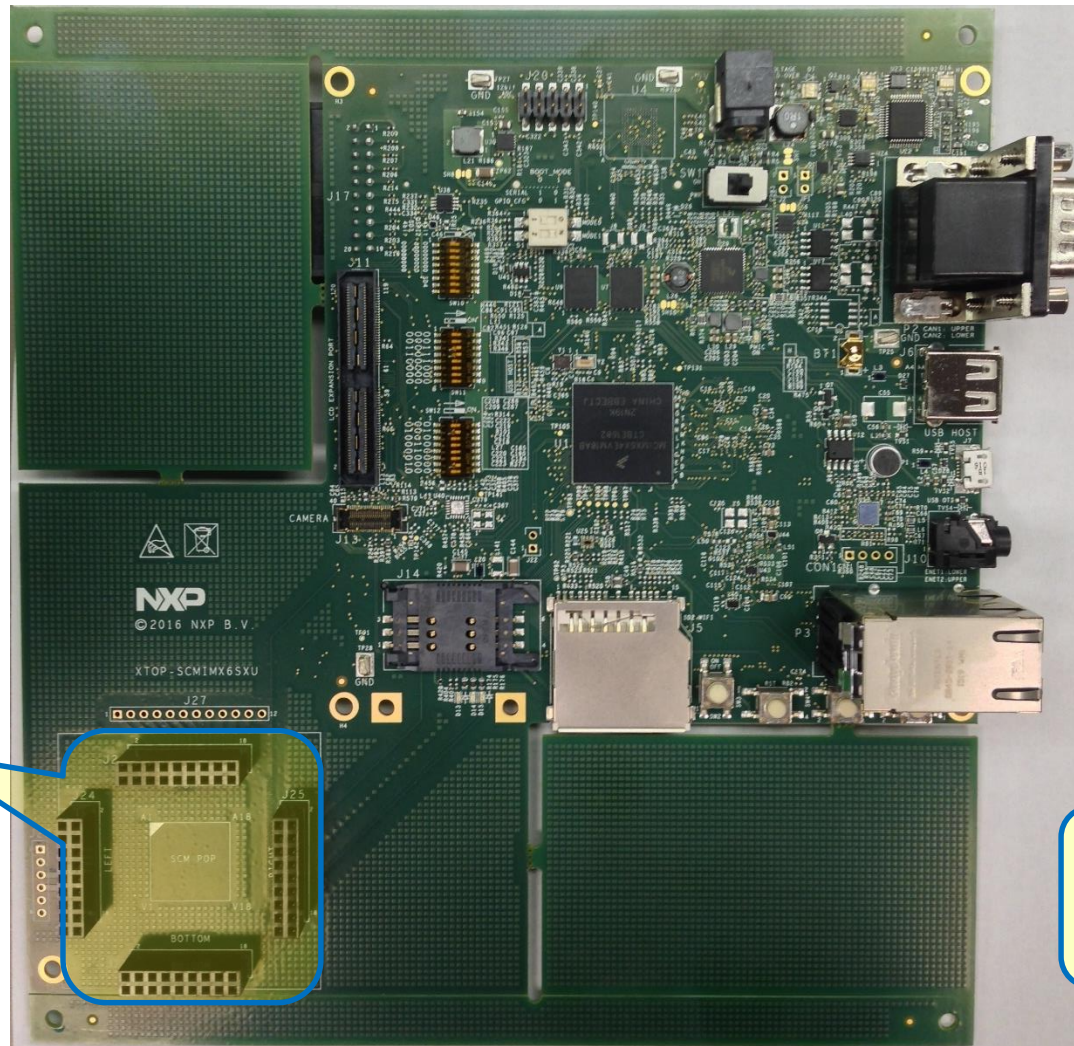
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	GN0	KEY_ROW2	KEY_COL2	POP_PASS_THRU1	GN0	POP_PASS_THRU2	POP_PASS_THRU3	POP_PASS_THRU4	GN0	POP_PASS_THRU5	POP_PASS_THRU6	POP_PASS_THRU7	POP_PASS_THRU8	GN0	POP_PASS_THRU9	POP_PASS_THRU10	POP_PASS_THRU11	GN0
B	KEY_ROW3																	SD2_DAT1
C	KEY_COL3																	SD2_DAT0
D	KEY_ROW4																	SD2_CLK
E	GN0																	GN0
F	KEY_COL4																	SD2_CMD
G	GPIO1_11																	SD2_DAT3
H	SYS_POR_B																	SD2_DAT2
J	GN0								Version 2									GN0
K	SYS_VGEN1_V1B																	NVCC_SD2
L	VGEN1																	GPIO1_00
M	POP_PWR2																	GPIO1_01
N	POP_PWR2																	NAND_DATA04
P	POP_PWR1																	NAND_DATA05
R	POP_PWR1																	NAND_DATA06
T	VGEN2																	NAND_DATA07
U	VGEN1							V1 to V2 change	V1 to V2 change	V1 to V2 change	V1 to V2 change	V1 to V2 change						NAND_ALE
V	GN0	GN0	GN0	GN0	POP_SPARE1	USB_H_DATA	USB_H_STROBE	NVCC_KEY	NAND_CE1_B	GN0	NAND_RE_B	NAND_CE0_B	NAND_WE_B	GN0	NAND_CLE	NAND_WP_B	NAND_READY_B	GN0



# SCM Development Support

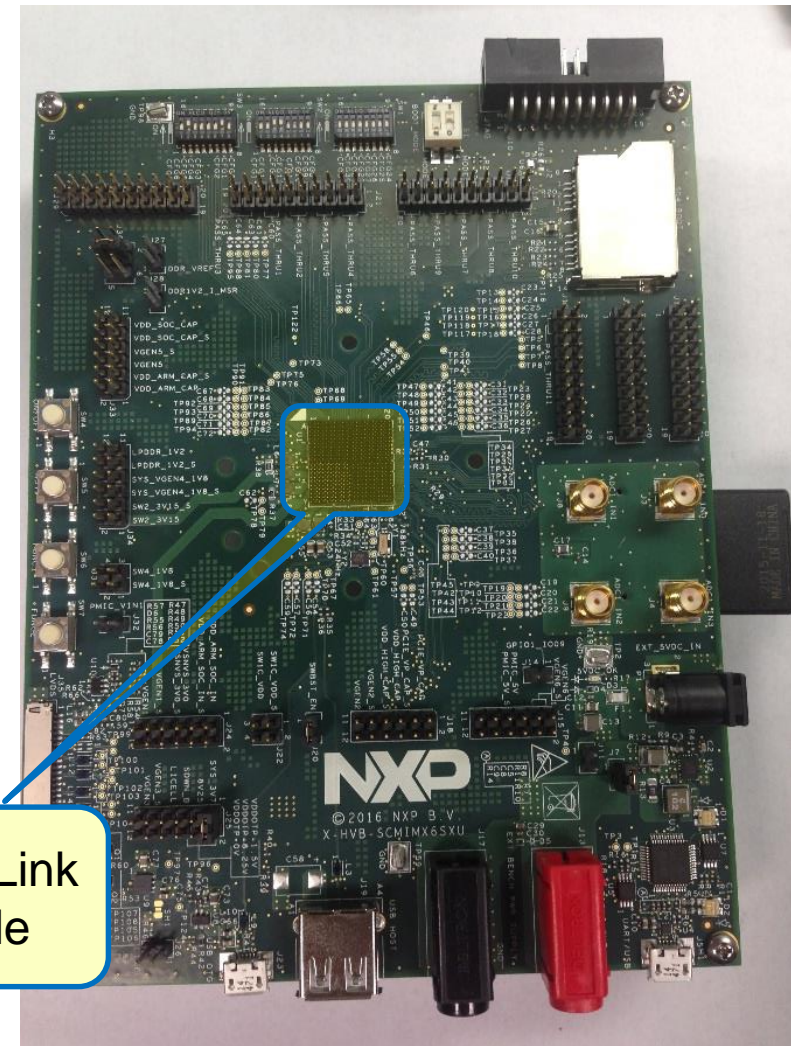
## Top Board SW Developer

- Alpha samples available
- ECO-Partner support in place
- Development boards available



Customer Top Board Slot

## HVB SCM V-Link Development Board



SCM V-Link Module

# PARTNER DEMOS

UTILIZING SCM-I.MX 6SX V-LINK



# BOUNDARY DEVICES



# Boundary Devices Introduction



- Headquarters: Chandler, Arizona USA
- Founded in 2003 (Privately Held)
- Our Business: NXP i.MX Family
- Multiple Single Board Computers and System on Modules (SOM) based on the i.MX family of processors
- Full Software Support package including Yocto, Ubuntu, Android 5.0, Buildroot, WinCE 7, and QNX Operating Systems
- NXP Proven Partner



**Nitrogen6X\_SOM**

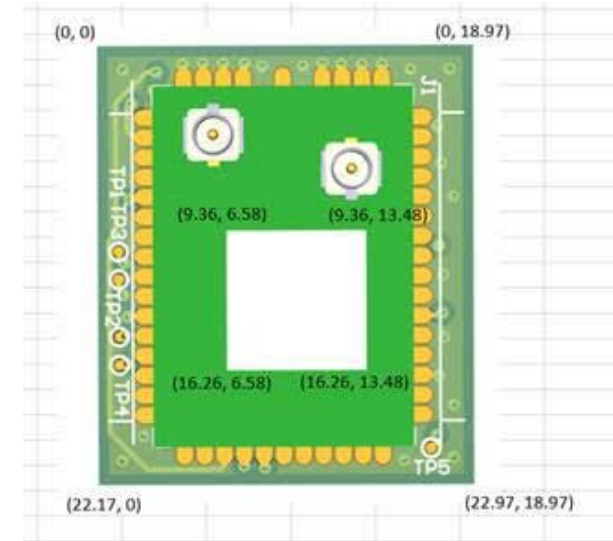


**SABRE Lite  
BD-SL-i.MX6**

# SCM Carrier Board + V-Link Top Board



- Adding WiFi+BT to SCM can be done in 2 ways: via Carrier board or Top board
- Carrier board requires horizontal space which many applications do not have.
- Space savings of 280 mm sq
- V-Link Top Board from Boundary Devices – QCA9377 802.11ac + BT4.1 module. Pre-certified and ready for production. Mounts on top of SCM which is ideal for space constrained applications. 22mm x 19mm board dimensions
- Available Linux/Android Drivers for easy WiFi+BT software integration for kernel 3.14.28 and above
- On 5GHz network utilizing SDIO 3.0, WiFi throughput is 90Mb/s



- V-Link Top board is ideal for handheld/space-constrained applications allowing customers to integrate vertically
- Boundary Devices demo is a handheld, battery powered wireless streaming application. The demo consists of NXP SoloX SCM + BD V-Link Top board with 802.11ac module + BD Carrier board with 5MP MIPI Camera and Battery.
- The demo application wirelessly streams data from the 5MP camera on the handheld device to a desktop board which shows the stream on a 7" display
- There is a point-to-point link from the handheld device to the desktop device
- Visit demo at the NXP booth in the Technology lab

# CODE

# PHALAX ULTRA-COMPACT BORDER ROUTER



# Sub-GHz Wireless Mesh Networks using 6SX V-Link

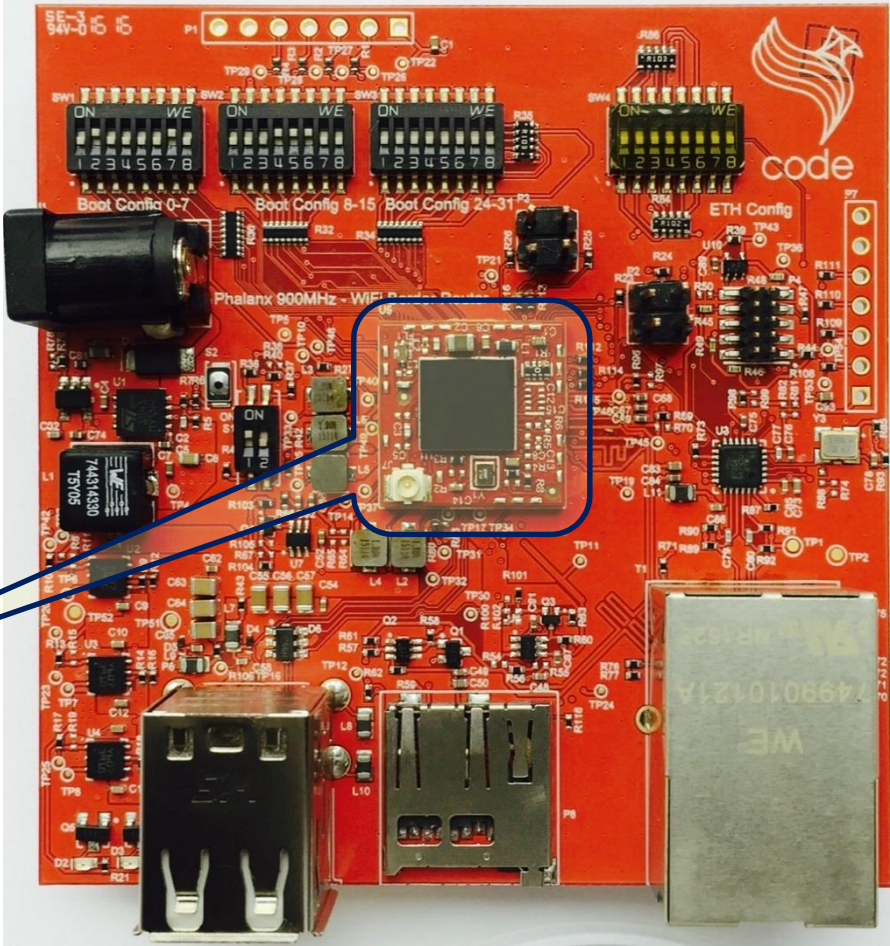
- **Ultra Compact Sub-GHz to WiFi Border Router solution**

- **Applications:**

- Home Automation
- Wireless Sensor Nodes
- Smart Lighting
- Smart City
- Smart Meters
- Smart Parking
- IoT



SCM-i.MX 6SX V-Link  
w/ Top Board





# Phalanx Ultra-Compact Border Router

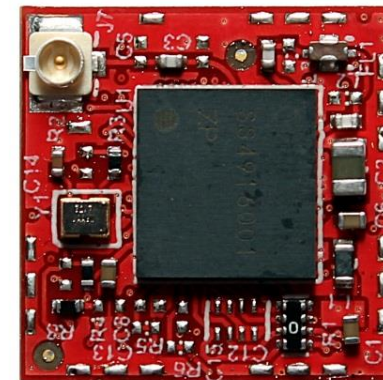
- **Top Board**

- 2.4 GHz & 5 GHz WiFi/BT 4.0 + EDR
- 802.11 a/b/g/n/ac
- Up to 390 Mbps
- U.FL standard antenna connector
- Broadcom BCM4339 Chipset
- iMX 6SX V-Link Top Board form factor
- 15.5 x 15.5 mm



- **Phalanx Border Router**

- Optimized mesh network for sensing and control applications
- Highly scalable, minimizing deployment costs
- 900 MHz Wireless
- A new, clever routing algorithm which reduces routing overhead.
- Fully IPv6



# Design Process

## Conceptualization

- The iMX 6SX V-Link is one of the most capable yet compact application processor platforms. We envisioned using this platform to open a wide range of IoT possibilities.

## Design

- iMX 6SX V-Link, presents the right choice of buses and IOMUX options which made the design straightforward. Our schematic and PCB capture time was less than 2 weeks of effort.
- V-Link technology allowed us to route all the needed connections easily and within electrical specs.

# Design Process

## Prototyping and Testing

- Top Board PCB is highly flexible, it was a pleasant surprise to find that all our components fitted nicely in the design.
- Testing was quite easy with all the software provided by NXP.

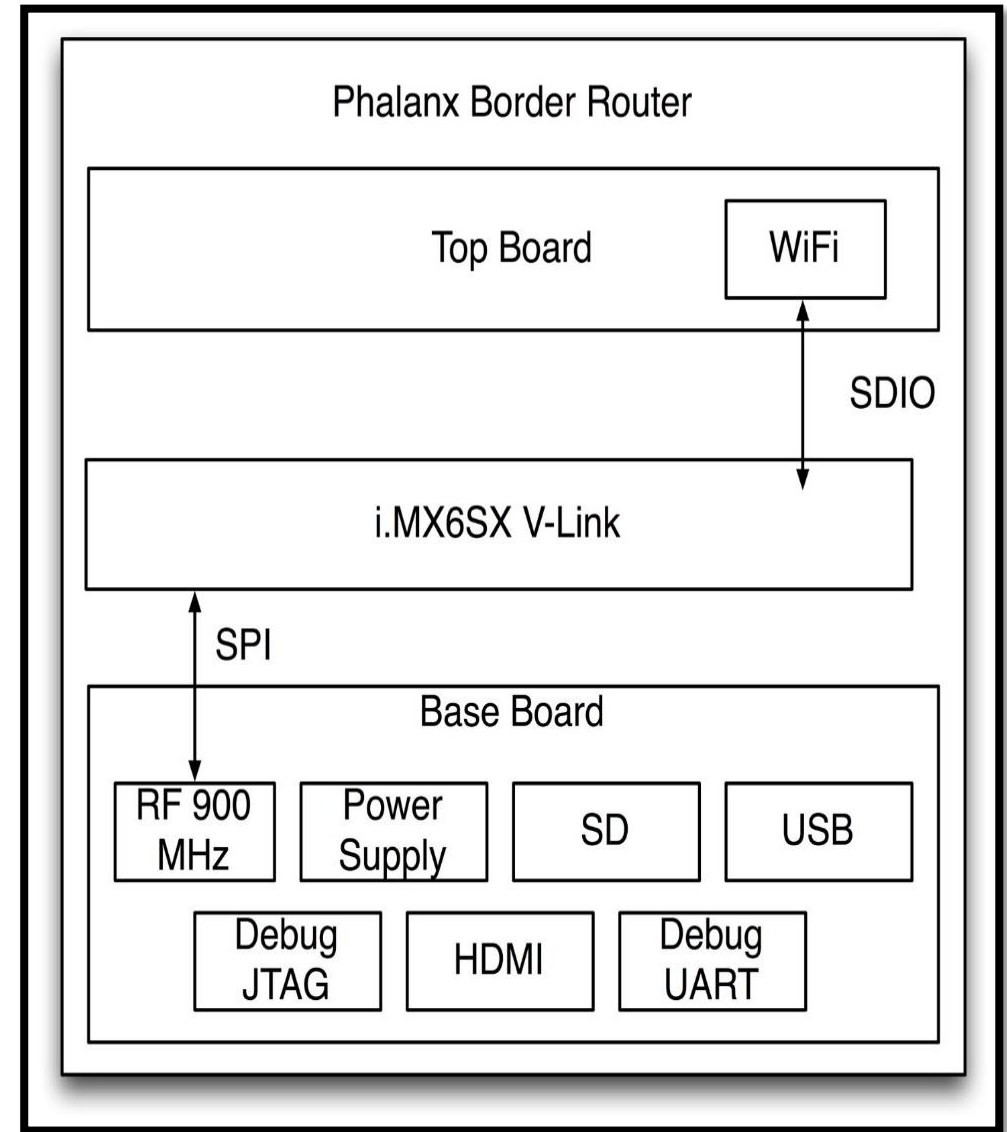
## Design Cycle time

- In just 2 months the whole solution was up and running, including software porting, PCB layout, manufacturing and assembly.
- The exceptional level of integration provided by this new NXP platform enabled us to add extra features to the design such as last generation 802.11 ac WiFi a conventional approach would have taken us around 4 to 6 months.
- Thus, we have reduced time to market by up to 4 months.

# Summary

## Benefits

- Ultra compact, ready to deploy IoT Top Board solution
- High level of hardware and software integration enables customers with a powerful solution and a very short time to market
- Phalanx software provides powerful low latency IoT IPv6 mesh technology
- Visit demo at the NXP booth in the Technology lab



# FIRSTVIEW

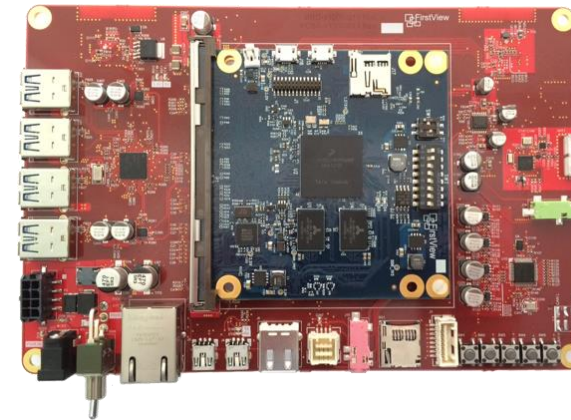
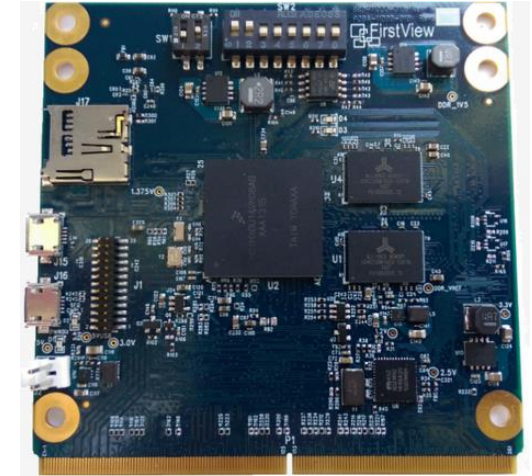
# MEDICAL WEARABLE GATEWAY



# FirstView Consultants Introduction



- NXP i.MX Family Experts
- Dozens of i.MX designs for clients including the FirstView i.MX6 SOM and Carrier Board
- Provide turn key solutions for hardware, software and manufacturing
- Software solution on Linux, Android, iOS and WinCE
- NXP, Arrow and Future Partner
- Based right here in Austin, Texas
- Founded 2010



# V-Link SCM enabling a Wearable Medical Monitoring Device.



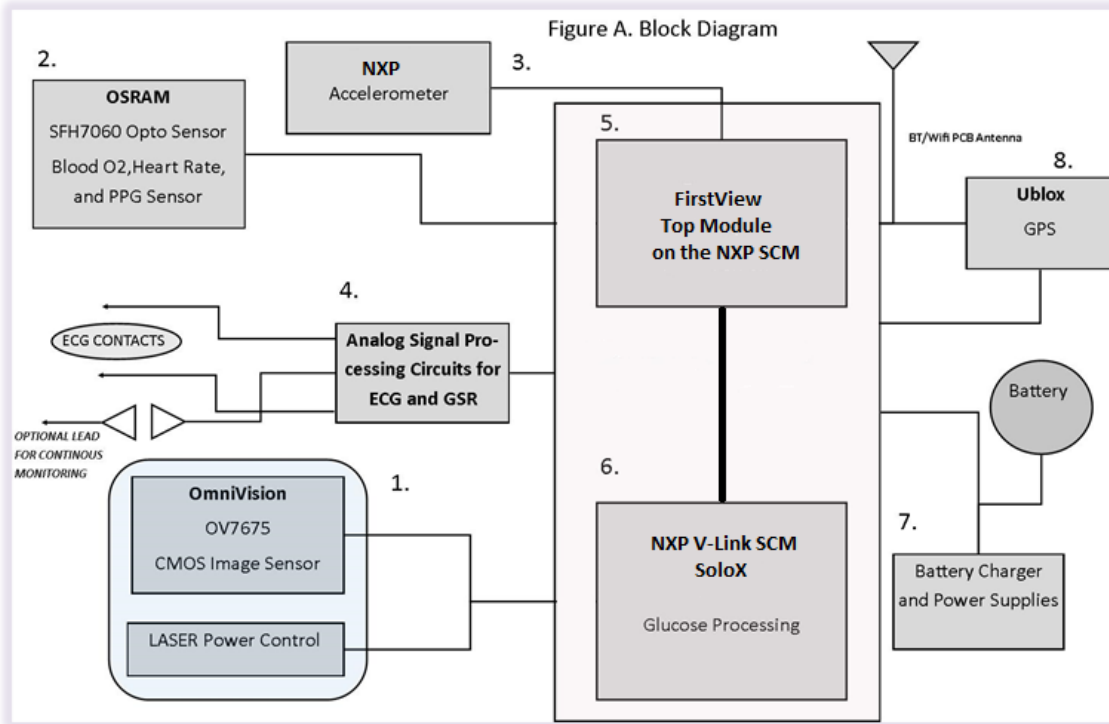
## Limitations of Monitoring devices available today

- Not convenient to wear for continuous monitoring
- Not directly connected to cloud to provide life saving alerts
- Require user to connect wires

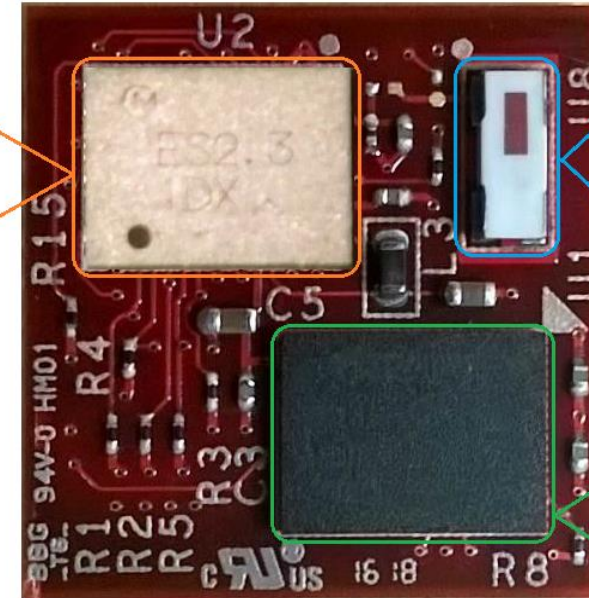
## GPS enabled medical monitor for detecting and transmitting via integrated Wi-Fi and Bluetooth

- Pulse Oximeter – Blood oxygen
- Galvanic Skin Response (GSR) – Stress levels
- Accelerometer – Fall detection
- Skin and ambient temperature
- Photoplethysmogram (PPG) – Heart rate and blood pressure
- Electrocardiogram (ECG)- Heart rate, heart duress
- Continuous Glucose Monitor- Blood sugar monitor

# Wearable Top Module and SCM Block Diagram



muRata WiFi and Bluetooth



Unique Antenna Operates Directly over Ground Plane

1Gb Non-volatile Storage for Linux

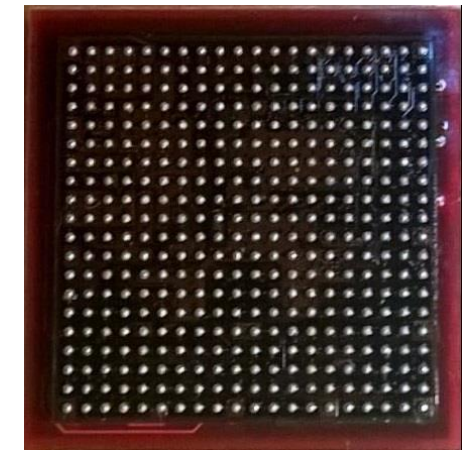
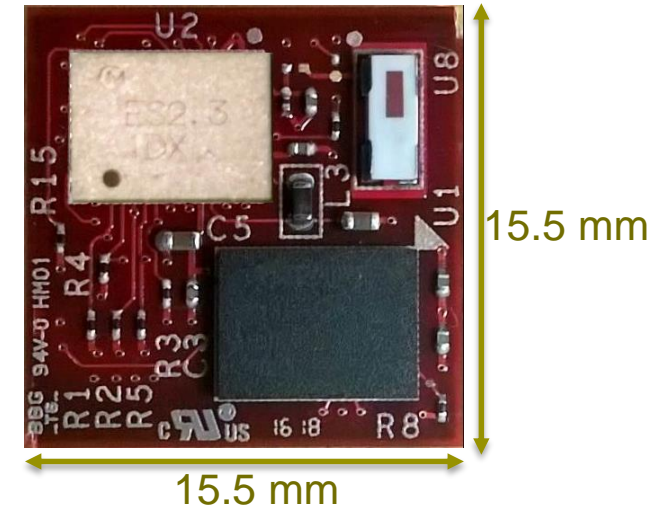
## High Level Block Diagram on the Wearable Design

## FirstView Top Module mounted on to the NXP V-Link SCM



# Benefits of V-link SCM and FirstView Top Module

- The SCM-i.MX 6SX V-Link has enabled FirstView to develop this product
  - The risk of DDR SDRAM integrity was completely removed as it is part of the SCM
  - The SCM has the High Speed RAM and Power Management Integrated which otherwise takes 2 months to design
  - Ultra-compact 15.5mm x 15.5mm
  - Existing reliable BSP with drivers available with V-Link SCM
- Summary the benefits of the wearable application
  - Cloud-Connected ECG
  - Battery Operated
  - IoT Medical ECG Alert
  - Life Saving Monitoring
  - Linux Based Platform Providing Extensibility
- Visit demo at the NXP booth in the Technology lab



# SUMMARY

# Summary

- SCM products are designed to enable the smallest form factor, feature enabled and highly integrated solution to help significantly ***reduce the customers complexity and time to market***
- NXP is launching multiple families of SCM Modules to meet different markets and customer needs
- Alpha, Beta and Production parts and development boards are available now.
  - Contact
    - Amanda McGregor: Product Marketing and Application Support
      - Tel: 512-895-8501
      - [Amanda.mcgregor@nxp.com](mailto:Amanda.mcgregor@nxp.com)

# SCM Demo's and Contact Info.

- **SCM Demo's in the Tech. Lab**

- SCM-i.MX6D/Q with ePoP (LPDDR2+eMMC)
- SCM-i.MX6SX
- SCM-i.MX6SX V-Link Boundry Devices
- SCM-i.MX6SX V-Link Code
- SCM-i.MX6SX V-Link Firstview
- SCM-i.MX6Dual / 6Quad integrated with NFC

Micron Technology Booth

Arrow & NXP Booth

NXP Booth

NXP Booth

NXP Booth

NXP Booth \*\* Win a Quickstart Board \*\*

- **Contact Info**

- Navjot Chhabra: Product and Business Development
  - Tel: 512-895-6470
  - [Navjot.chhabra@nxp.com](mailto:Navjot.chhabra@nxp.com)
- Amanda McGregor: Product Marketing and Application Support
  - Tel: 512-895-8501
  - [Amanda.mcgregor@nxp.com](mailto:Amanda.mcgregor@nxp.com)

- <http://www.nxp.com/products/single-chip-modules>

# Q & A



SECURE CONNECTIONS  
FOR A SMARTER WORLD

# ATTRIBUTION STATEMENT

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, CoolFlux, EMBRACE, GREENCHIP, HITAG, I2C BUS, ICODE, JCOP, LIFE VIBES, MIFARE, MIFARE Classic, MIFARE DESFire, MIFARE Plus, MIFARE Flex, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TrenchMOS, UCODE, Freescale, the Freescale logo, AltiVec, C 5, CodeTEST, CodeWarrior, ColdFire, ColdFire+, C Ware, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QorIQ, QorIQ Qonverge, Ready Play, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, SMARTMOS, Tower, TurboLink, and UMEMS are trademarks of NXP B.V. All other product or service names are the property of their respective owners. ARM, AMBA, ARM Powered, Artisan, Cortex, Jazelle, Keil, SecurCore, Thumb, TrustZone, and  $\mu$ Vision are registered trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere. ARM7, ARM9, ARM11, big.LITTLE, CoreLink, CoreSight, DesignStart, Mali, mbed, NEON, POP, Sensinode, Socrates, ULINK and Versatile are trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org. © 2015–2016 NXP B.V.

NXP Semiconductors is licensed by EPIC Technologies Inc. to make and sell packages that include Epic's "Chips First" technology and related patents.

