MCIMX6UL-CM

Schematics DevBoard

Table of Content

Revision History

Rev. Code	Date	By		Description
A	2015-02-28	Javen	1	Revision A release
B	2015-06-12	Javen	1	OSC issue: Add R518,R515,R513,Q501,Y503,r516,r517
			2	VDD_ARM_SOC_IN voltage: Change R706 to 215K, R707 to 147K, R708 to 1.5M Change R513,R517 to DCDC_3V3
			3	DDR3 write leveling issue: exchang DDR3 DRAM_DATA3 and DRAM_DATA11
			4	Add R519 for backup
C	2015-07-07	Javen	1	FCC update: Add C423,C415,R413,C414,C420,C417,C421,C416,C422,C418
			2	VDD_HIGH_IN power consumption update: Change R513 from 10K to 1M Change R513,R517 to DCDC_3V3
	2015-07-14	Javen	3	Add R520 for OSC vih Change R510,C505 connection for OSC backup
C1	2015-08-10	Javen	1	DNP C414 for LCD_CLK Change R520 to 499 OHM
C2	2015-10-28	Javen	1	Install: R510,R518,R516,Y501 DNP: R515,513,Q501,Y503,R517 Change: R514 from 1K to 0 OHM
C3	2016-05-09	Javen	1	Change U101 CPU part number to MCIMX6G2CVM05AA
C5	26-Jul-2016	Marek B.		New MFG_PN for U201: MT41K256M16TW-107:P MPU update to MCIMX6G2CVM05AA Title Blocks update

1. Unless Otherwise Specified:

   All resistors are in ohms, 10%, 1/8 Watt,0603
   All capacitors are in uF, 20%, 50V,0603
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

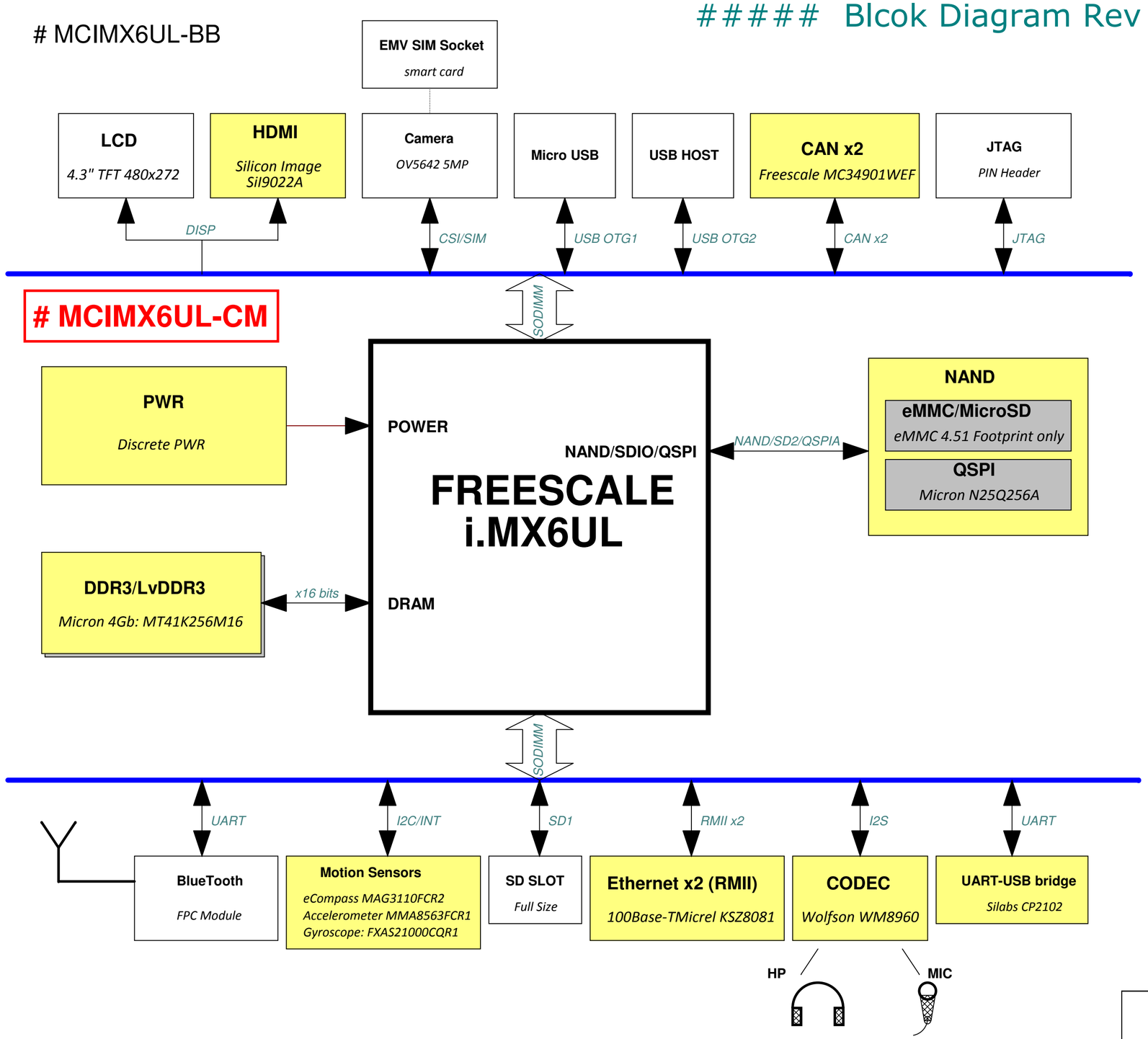
ICAP Classification: CP: IUO: X PUBI:

Designer: <Designer>	Drawing Title: **MCIMX6UL-CM**	
Drawn by: <DrawnBy>	Page Title: **Title and Rev History**	
Approved: <Approver>	Size C	Document Number SCH-28617 PDF: SPF-28617 Rev C5
	Date: Wednesday, September 07, 2016	Sheet 1 of 13

i.MX6UL EVK Block Diagram

Blcok Diagram Rev 1.0

MPN: MCIMX6UL-BB Agile No: 28616
MPN: MCIMX6UL-CM Agile No: 28617



ICAP Classification: CP: ___ IUO: X PUBI: ___

Drawing Title: **MCIMX6UL-CM**

Page Title: **Block Diagram**

Size	Document Number	Rev
C	SCH-28617 PDF: SPF-28617	C5

Date: Wednesday, September 07, 2016 Sheet 2 of 13

i.MX6UL EVK PWR TREE

WALL Adapter: 5V/3A

OVP

VSYS
5V/3A

MCIMX6UL-BB

Power sources

- LDO — RICHTEK RT9169 — 3.3V/100mA Iq = 4uA — Always ON → VDD_SNVS_IN
- DC/DC BUCK — MPS MP2144 — 3.3V/2A Iq=40uA — PMIC_ON_REQ → VDD_HIGH_IN
- DC/DC BUCK — MPS MP2159 — 1.275V/1A Iq=40uA — DCDC_3V3_PG → DCDC_3V3
- DC/DC BUCK — MPS MP2159 — 1.35V/1A Iq=40uA — DCDC_3V3_PG → VDDARM_IN
- HIGH PSRR LDO — RICHTEK RT9193 — 3.3V/300mA — DCDC_3V3 → VLDO_3V3
- LDO — UNION UM1750S — 1.8V/3.3V/300mA — DCDC_3V3_PG → NVCC_SD (3.3V/1.8V)
- LDO — UNION UM1750S — 2.8V/300mA — DCDC_3V3 → NVCC_CSI (1.8V/3.3V)
- LOAD SW — USB_OTGx_PWR → USB_OTG_VBUS, USB_HOST_VBUS
- LDO — RICHTEK RT9169 — 1.8V/100mA Iq = 4uA — # 1.8V for eMMC HS200 mode → NVCC_NAND

FSL i.MX6UL CPU

- VDD_SNVS_IN — 276uA — LDO_ARM_SOC → VDD_SNVS_CAP
- VDD_HIGH_IN — 125mA — LDO_1P1 → NVCC_PLL; LDO_2P5 → VDD_HIGH_CAP
- NVCC_GPIO/NVCC_ENET/NVCC_LCDIF
- NVCC_DRAM_2P5
- VDD_SOC_IN — 900mA — LDO_ARM_SOC → VDD_ARM_CAP, VDD_SOC_CAP
- NVCC_DRAM — 50mA
- NVCC_NAND
- VDDA_ADC_3P3
- NVCC_SD
- NVCC_CSI — # 1.8V for CSI: 1.8V/3.3V for SIM
- 50mA — USB_OTG1_VBUS, USB_OTG2_VBUS — LDO_USB → VDD_USB_CAP

Peripherals

- RGB LCD — TianMa TFT — VLCD_3V3 3.3V/23mA; 5S2P 16V/25mA — BACKLIGHT RICHTEK RT9293B — BLT_PWM
- HDMI — SILICON IMAGE SiI9022A — VHDMI_3V3 3.3V/10mA; VLDO_1V2 1.2V/69.2mA — LDO RICHTEK RT9169
- Audio Codec — WM8960 — VSPK_5V 5V/511mA; VAUD_3V3 3.3V/62.58mA
- SENSOR — eCompass/ G-sensor/Gyroscope — VSENSOR_3V3 3.3V/6.9mA
- CAN — FSL MC34901WEF — CAN_VIO_3V3 3.3V/1mA; CAN_VDD_5V 5V/65mA
- Ethernet x2 — Micrel KSZ8081RNB — VENET_3V3 3.3V/48.7mA — LOAD SW
- Camera/EMV SIM — CSI B2B CN — DVDD1V5, AVDD_2V8 — LDO UNION UM1750S 1.5V/300mA

Memory

- LvDDR3 — Micron: MT41K512M16
- eMMC 4GB — Micron MTFC8GLCDM — DCDC_3V3 3.3V/200mA
- QSPI — Micron N25Q256 — NVCC_NAND 3.3V/1.8V; DCDC_3V3 3.3V/20mA
- NAND — Micron MT29F32G08 — DCDC_3V3 3.3V/50mA

USB

- USB OTG — USB_OTG_VBUS
- USB HOST — USB_HOST_VBUS

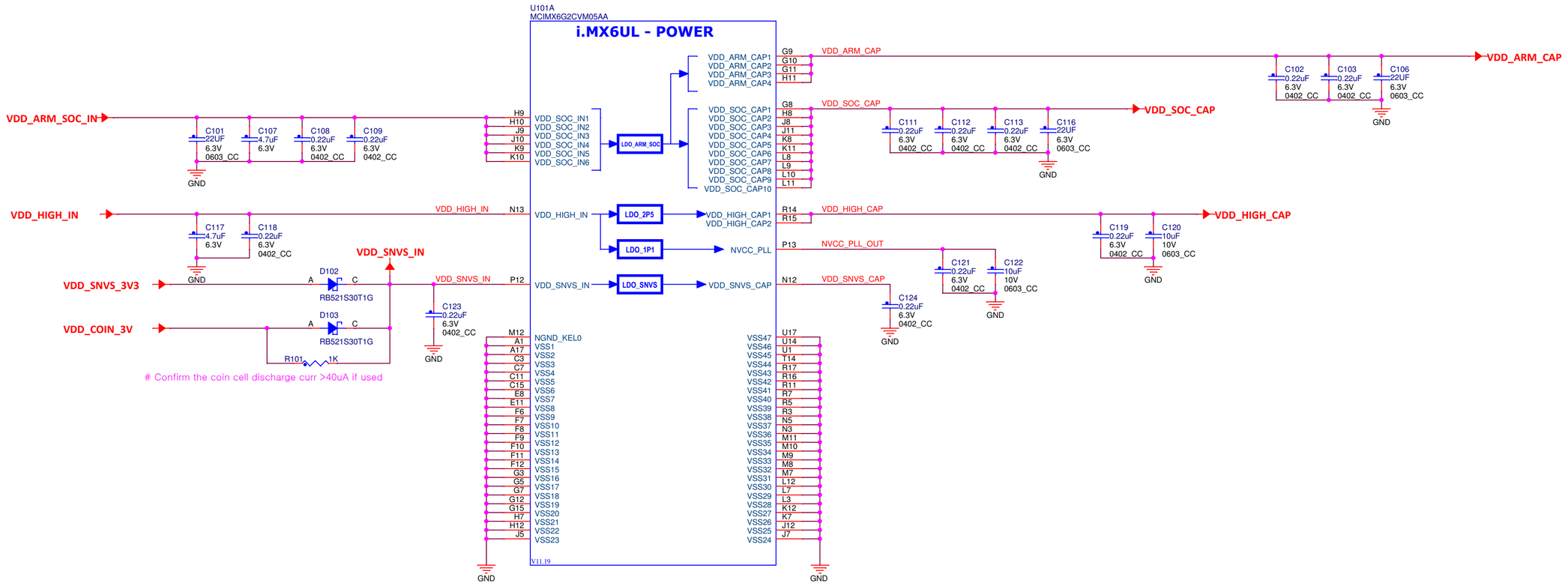
SD

- LOAD SW — SD1_nRST/POR_B
- SD Socket
- BT MOD

MCIMX6UL-CM

ICAP Classification:	CP: ___ IUO: X PUBI: ___
Drawing Title:	MCIMX6UL-CM
Page Title:	PWR TREE
Size: C	Document Number: SCH-28617 PDF: SPF-28617 Rev C5
Date:	Wednesday, September 07, 2016 Sheet 3 of 13

i.MX6UL PWR



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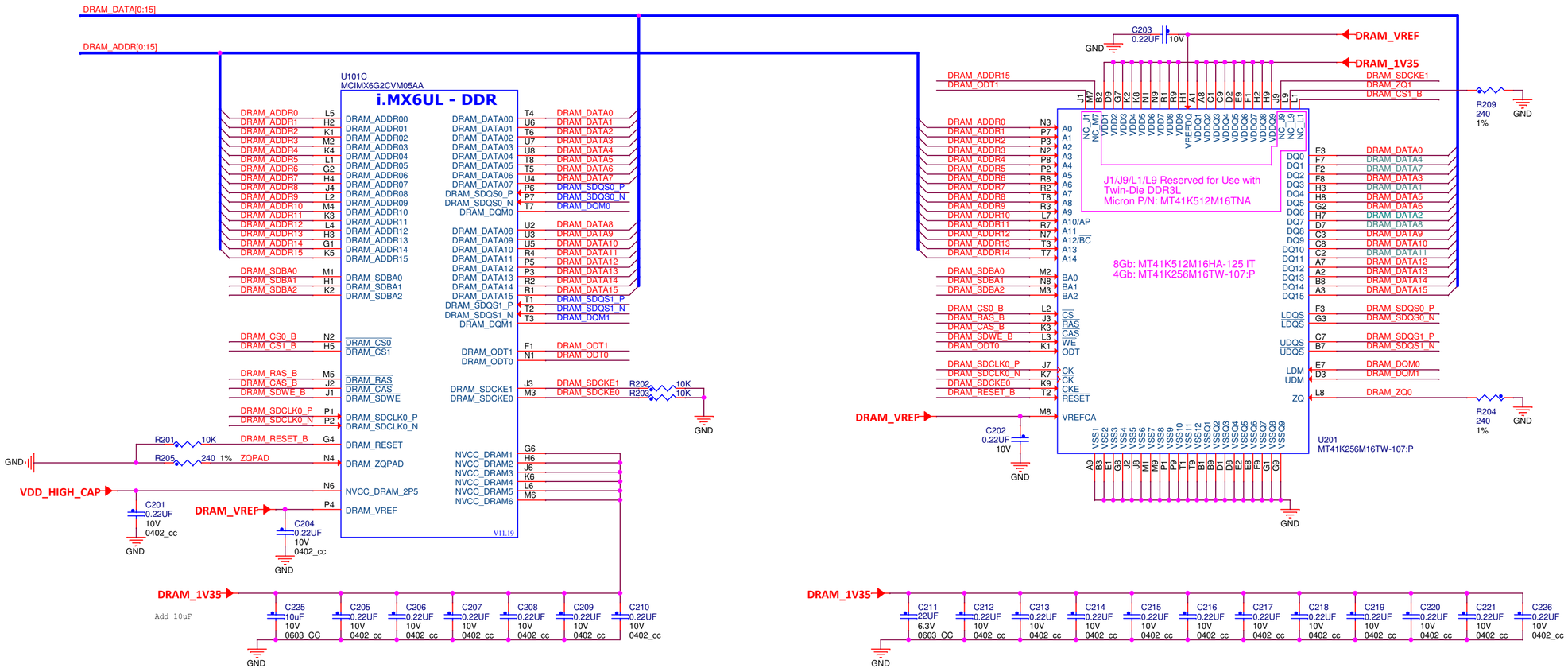
Drawing Title: **MCIMX6UL-CM**

Page Title: **CPU PWR**

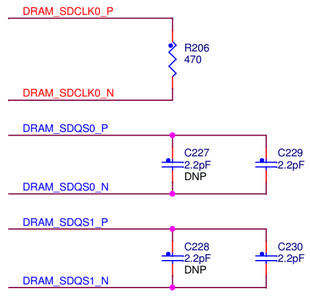
Size	Document Number	Rev
C	SCH-28617 PDF: SPF-28617	C5

Date:	Wednesday, September 07, 2016	Sheet	4	of	13

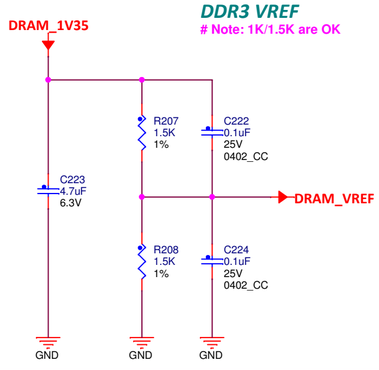
DDR3/LvDDR3



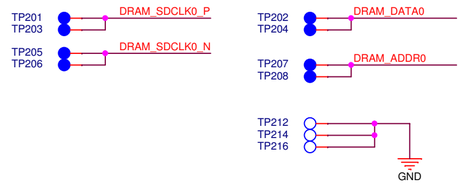
Note:
CLK termination: Place R54 close to U2.



DDR3 VREF
 # Note: 1K/1.5K are OK



DRAM Test Points

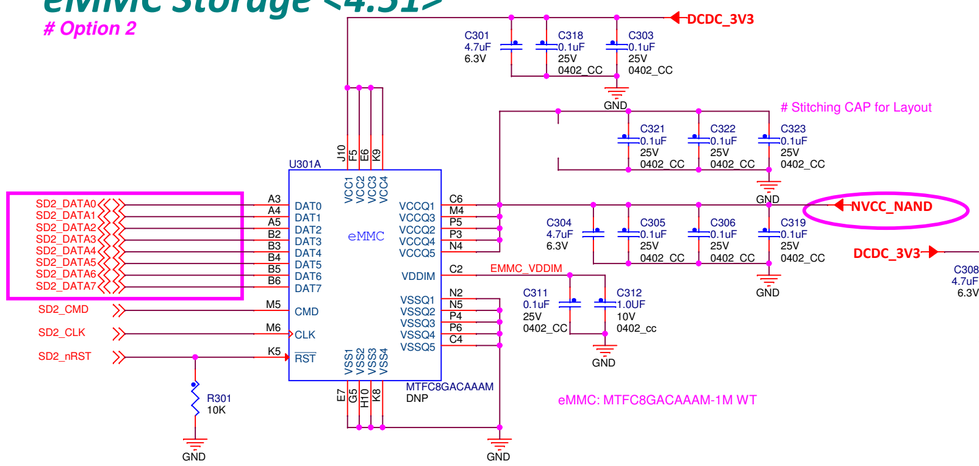


 # Note:
Test points for signal integrity measurement

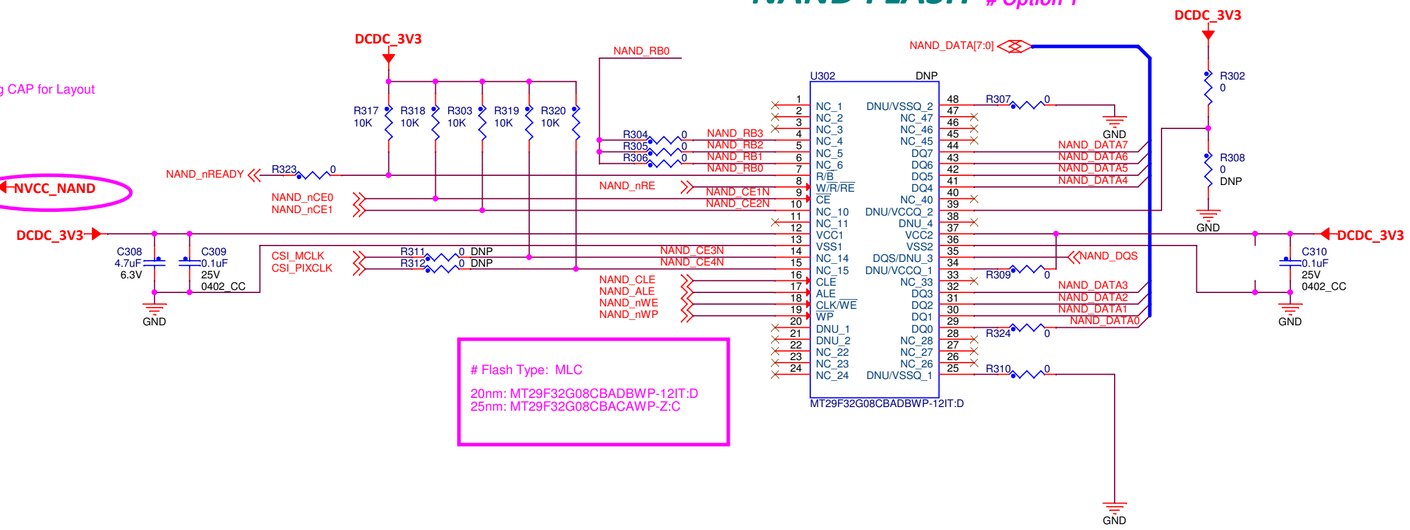
ICAP Classification:	CP: ___	IUO: X	PUBI: ___
Drawing Title:	MCIMX6UL-CM		
Page Title:	LvDDR3		
Size C	Document Number SCH-28617 PDF: SPF-28617		Rev C5
Date: Wednesday, September 07, 2016	Sheet 5 of 13		

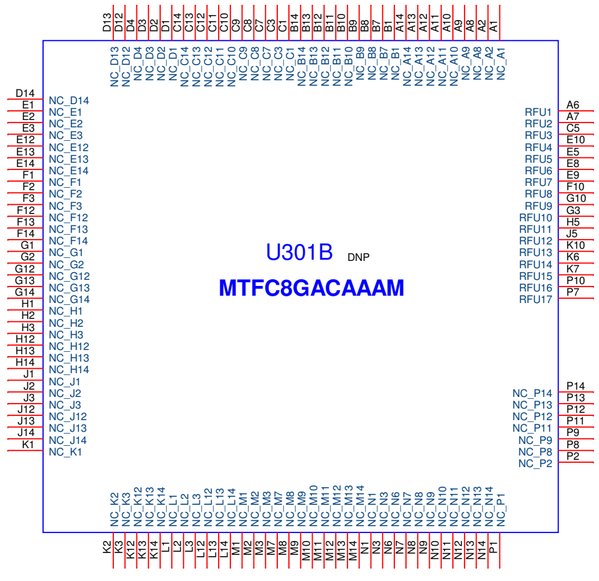
eMMC Storage <4.51>

 # Option 2



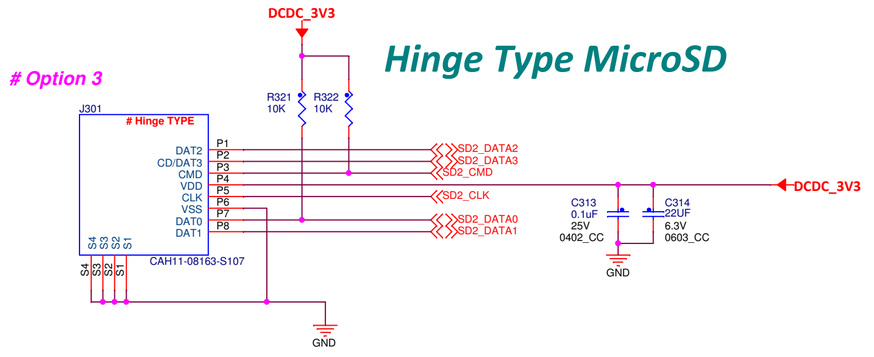
NAND FLASH *# Option 1*



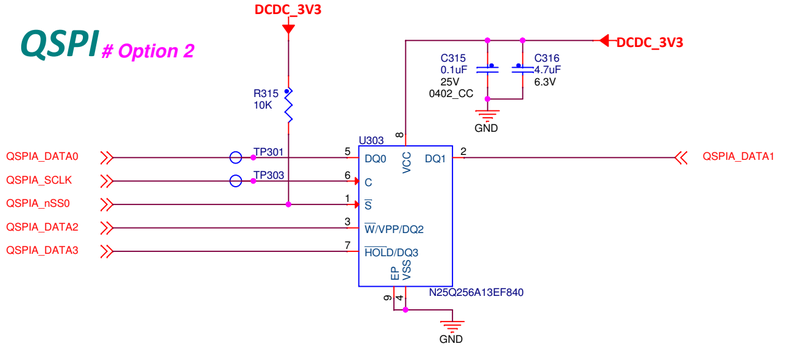


Hinge Type MicroSD

 # Option 3



QSPI *# Option 2*



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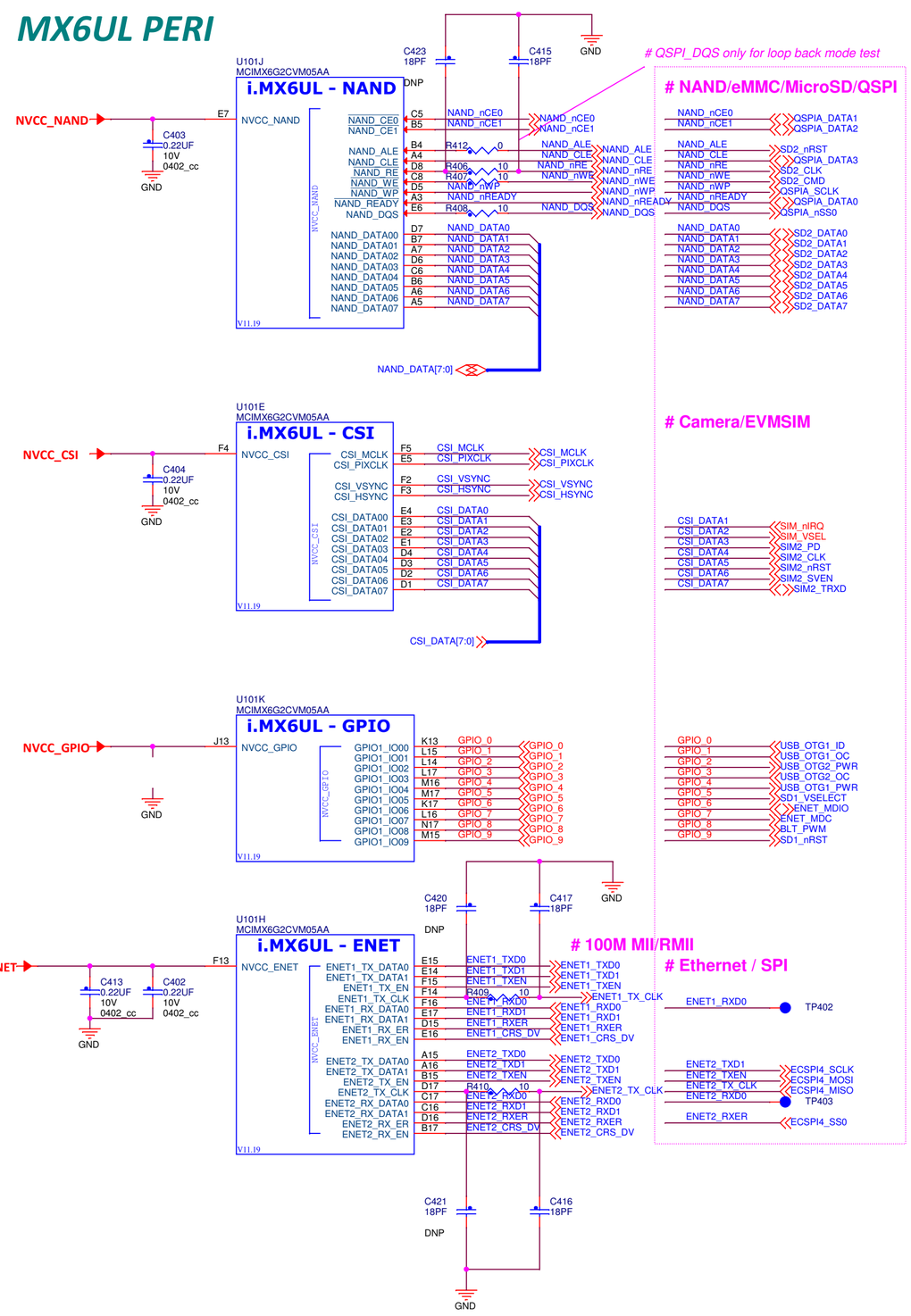
Page Title:	**FLASH**		
Size: C	Document Number: SCH-28617 PDF: SPF-28617		Rev: C5
Date: Wednesday, September 07, 2016	Sheet 6 of 13		

MX6UL PERI



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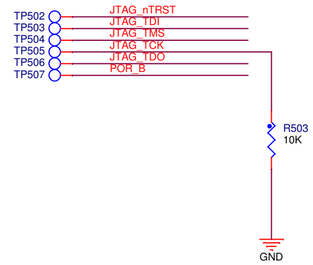
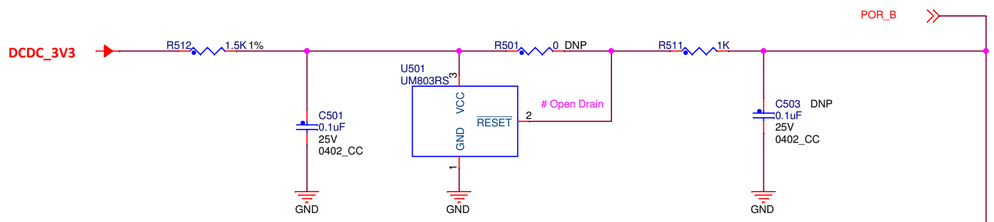
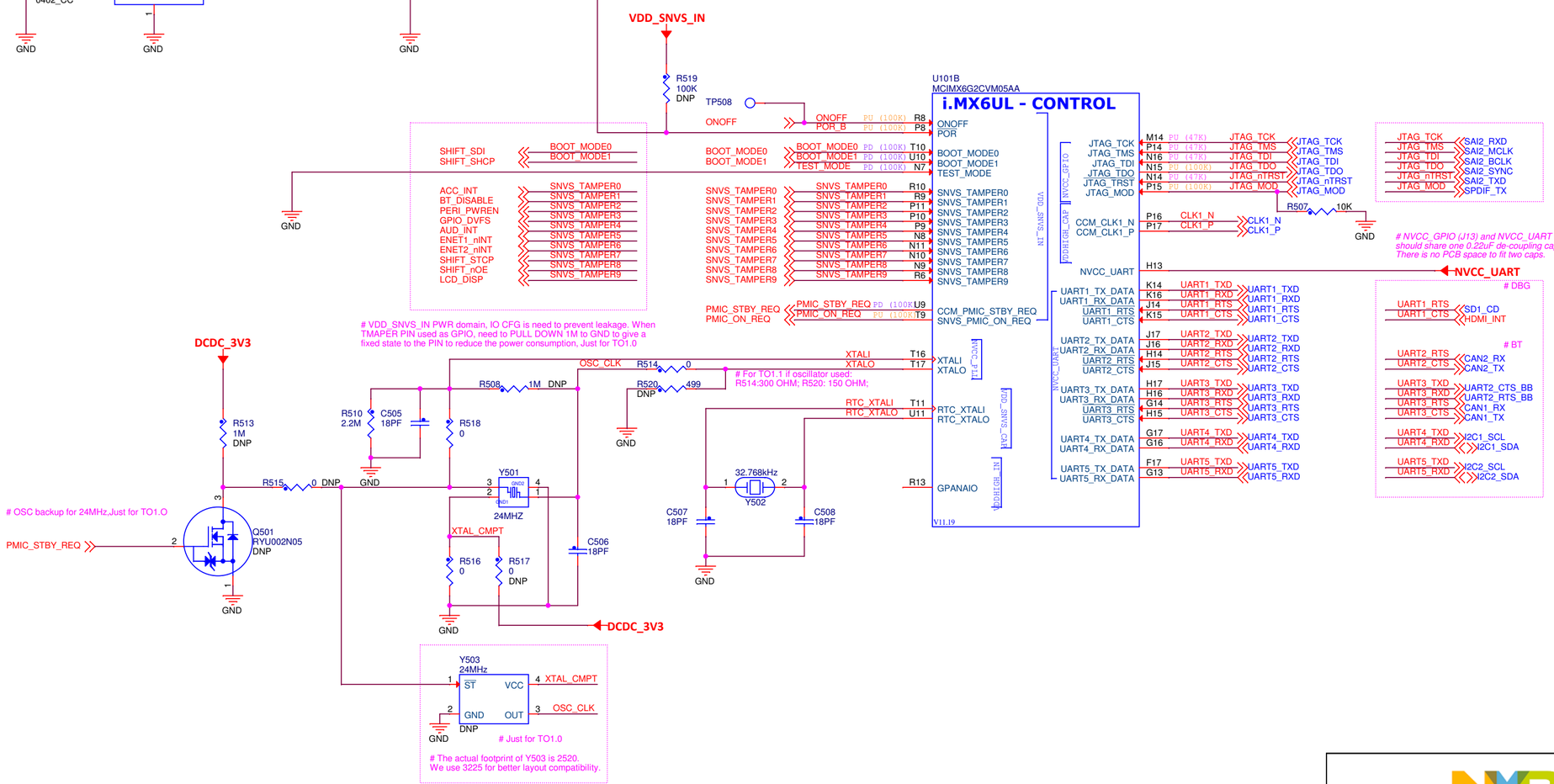
Drawing Title:	MCIMX6UL-CM
Page Title:	CPU PERI x1
Size: C	Document Number: SCH-28617 PDF: SPF-28617 Rev: C5
Date:	Wednesday, September 07, 2016 Sheet 7 of 13

JTAG Debug



i.MX6UL RESET





ICAP Classification:	CP: ___	IUO: X	PUBI: ___
Drawing Title:	MCIMX6UL-CM		
Page Title:	CPU PERI x2		
Size C	Document Number SCH-28617 PDF: SPF-28617		Rev C5
Date: Wednesday, September 07, 2016	Sheet 8 of 13		

FUSE MAP <Default: QSPI BOOT>

TYPE	BOOT_CFG1[7]	BOOT_CFG1[6]	BOOT_CFG1[5]	BOOT_CFG1[4]	BOOT_CFG1[3]	BOOT_CFG1[2]	BOOT_CFG1[1]	BOOT_CFG1[0]
	0/1	0/1	0/1	1	0	0	0	0
QSPI	0	0	0	1	Reserved	DDRSMP: "000" : Default "001-111"		
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved
SD/eSD	0	1	0	Fast Boot: 0 - Regular 1 - Fast Boot	SD/SDXC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		SD Power Cycle Enable '0' - No power cycle '1' - Enabled via USDHC_RST pad (uSDHC3 & 4 only)	SD Loopback Clock Source Sel(for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
MMC/eMMC	0	1	1	Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed 0 - Highl 1- Normal	Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled	SD Power Cycle Enable '0' - No power cycle '1' - Enabled via USDHC_RST pad (uSDHC3 & 4 only)	SD Loopback Clock Source Sel(for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
NAND	1	BT_TOGGLEMODE	Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand Number Of Devices: 00 - 1 01 - 2 10 - 4 11 - Reserved		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	

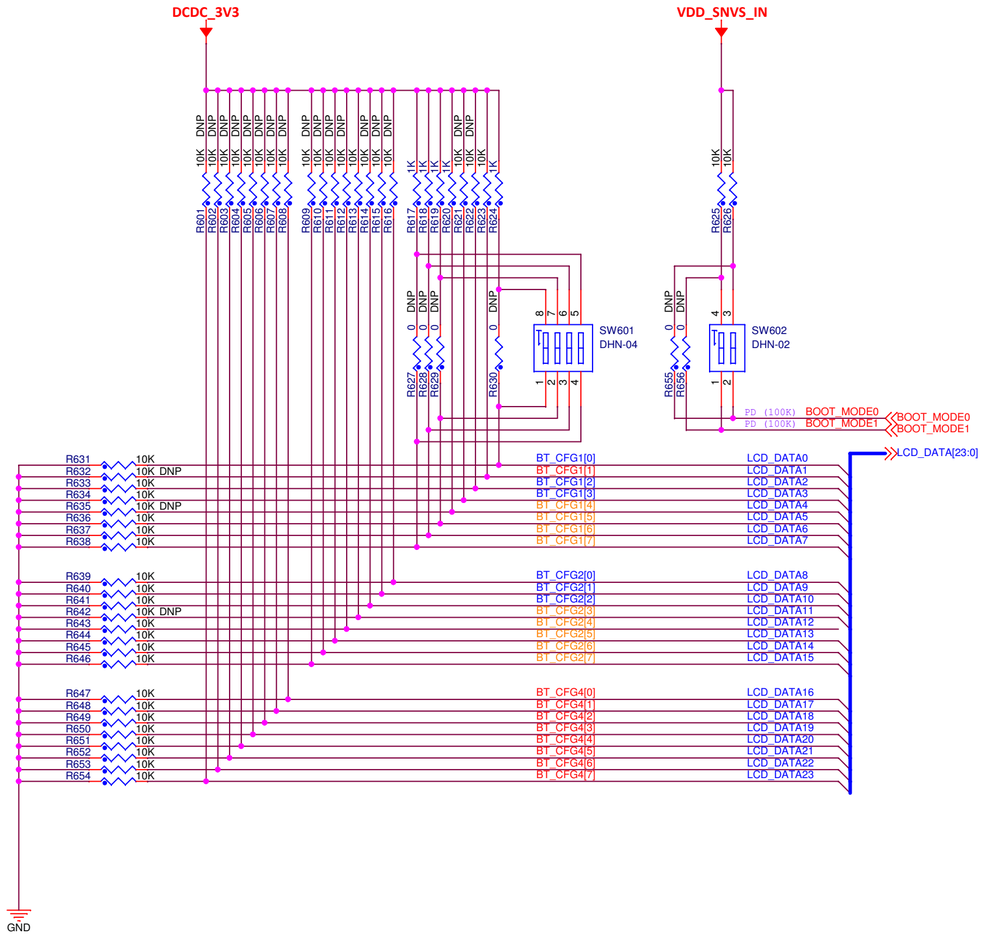
TYPE	BOOT_CFG2[7]	BOOT_CFG2[6]	BOOT_CFG2[5]	BOOT_CFG2[4]	BOOT_CFG2[3]	BOOT_CFG2[2]	BOOT_CFG2[1]	BOOT_CFG2[0]
	0	0	0	0	1	0	0	0
QSPI	Reserved	HSPHS: Half Speed Phase Selection 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	HSDLY: Half Speed Delay selection 0 : one clock delay 1: two clock delay	FSPHS: Full Speed Phase Selection 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	FSDLY: Full Speed Delay selection 0:one clock delay 1: two clock delay	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
WEIM	Muxing Scheme: 00 - A/D16 01 - A+DH 10 - A+DL 11- Reserved		OneNand Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved		Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
SD/eSD	SD Calibration Step '00' - 1 TBD		Bus Width: 0 - 1-bit 1 - 4-bit	Port Select:: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
MMC/eMMC	Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.			Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
NAND	Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles.			BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reset Time '0' - 12ms '1' - 22ms (LBA Nand)	Reserved

TYPE	BOOT_CFG4[7]	BOOT_CFG4[6]	BOOT_CFG4[5]	BOOT_CFG4[4]	BOOT_CFG4[3]	BOOT_CFG4[2]	BOOT_CFG4[1]	BOOT_CFG4[0]
	0	0	0	0	0	0	0	0
0x450	Infinit-Loop (Debug USE only) 0 - Disable 1- Enable	EEPROM Recovery Enable '0' - Disabled '1' - Enabled	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		SPI Addressing: 0 - 2-bytes (16-bit) 1 - 3-bytes (24-bit)		Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3 011 - eCSPI4 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved	
0x460	L2_HW_INVALIDATE_DISABLE	Reserved	FORCE_COLD_BOOT (Reflected in SBMR2)	BT_FUSE_SEL	DIR_BT_DIS	Reserved	SEC_CONFIG[1]	Reserved
0x460	Reserved (DDR3 config options)							
0x460	JTAG_SMODE[1:0]	WDOG_ENABLE '0' - Disabled '1' - Enabled	SJC_DISABLE	Reserved	Reserved	Reserved	Reserved	Reserved
0x460	Reserved	Reserved	Reserved	TZASC_ENABLE	JTAG_HEO	KTE	Reserved	DLL_ENABLE 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/Emmc
0x470	DLL Override: 0 - DLL Slave Mode for SD/eMMC 1 - DLL Override Mode for SD/eMMC	Reserved	SD2 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved	Disable SDMMC Manufacture mode 0 - Enable 1 - Disable	L1 I-Cache DISABLE	BT_MMU_DISABLE	Override Pad Settings (using PAD_SETTINGS value)
0x470	Reserved for unexpected requirements	eMMC 4.4 - RESET TO PRE-IDLE STATE	Override HYS bit for SD/MMC pads	USDHC_PAD_PULL_DOWN 0 - no action 1 - pull down	ENABLE_EMMC_22K_PULLUP 0 - 47K pullup 1 - 22K pullup	ADD_DS__SET_GPR1_16 0 - Set 1 - Don't set	USDHC_IOMUX_SION_BIT_ENABLE 0 - Disable 1 - Enable	USDHC IOMUX SRE Enable 0 - Disable 1 - Enable
0x470	USDHC_CMD_OE_PRE_EN (SD/MMC debug)	LPB_BOOT (Core / DDR- Bus) '00'- LPB Disable '01' - 1 GPIO (def freq) '10' - Div by2 '11' - Div by 4		BT_LPB_POLARITY (GPIO polarity)	POWER_MNG_CFG (LDO's DCDC's) (Reserved - NOT USED)			
0x470	Override NAND Pad Settings (using PAD_SETTINGS value)	MMC_DLL_DLY[6:0] Delay target for SD/eMMC DLL, it is applied to slave mode target delay or override mode target delay depends on DLL Override fuse bit value.						

 # NAND MT29F32G08CBACA
1 page = (4K + 224 bytes)
1 block = (4K + 224) bytes x 256 pages
= (1024K + 56K) bytes
1 plane = (1024K + 56K) bytes x 2048 blocks
= 17,280Mb
1 LUN = 17,280Mb x 2 planes
= 34,560Mb

BMODE[1:0]	BOOT TYPE
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot (Development)
11	Reserved

Boot Configuration



ICAP Classification:	CP: ___ IUO: X PUBI: ___
Drawing Title:	MCIMX6UL-CM
Page Title:	BOOT CFG
Size: C	Document Number: SCH-28617 PDF: SPF-28617 Rev: C5
Date: Wednesday, September 07, 2016	Sheet 9 of 13

i.MX6UL PWR

Power Rail	MIN	TYP	MAX	CURR
VDD_SNVS_IN	2.4	3	3.6	276uA
VDD_HIGH_IN	2.8	3	3.6	125mA
VDD_ARM_IN	0.9	1.275	1.5	400mA
VDD_SOC_IN	0.9	1.275	1.5	500mA
NVCC_DRAM	1.425	1.5	1.575	50mA
	1.283	1.35	1.45	
	1.14	1.2	1.3	
NVCC_xxx	1.65	1.8/2.5/3.3	3.6	
VDDA_ADC_3P3	3	3.3	3.6	
USB_OTG1_VBUS	4.4	5	5.25	50mA
USB_OTG2_VBUS				

DCDC_3V3 — R732 0 — VDD_HIGH_IN / NVCC_LCDIF / NVCC_GPIO / NVCC_ENET / NVCC_UART (NVCC_3V3)

DCDC_3V3 — R701 0 / R702 0 DNP — NVCC_NAND # 1.8V for eMMC HS200 mode

DCDC_3V3 / VLDO_1V8 — R703 0 DNP / R704 0 DNP — NVCC_CSI # CSI default 2.8V from the base board

DCDC_3V3 / VLDO_1V8 / VLDO_3V3 — R705 0 DNP / R709 0 — VDDA_ADC_3P3

DCDC_3V3 — R731 0 DNP — NVCC_SD # Install the R731,Remove U707 if no requirement for SD3.0 of SD1

ARM/SOC

Current 1A
I_Quiescent : 17¦ÌA

VSYS # 2.5V to 6V — C702 10uF 10V 0603_CC, C704 10uF 10V 0603_CC, C703 0.1uF 25V 0402_CC — U702 MP2159GJ (VIN, SW, OUT, FB, EN, PG, PGND, AGND) — L702 1uH — # 1.35V/1.05V/1.225V — VDD_ARM_SOC_IN — R729 0

DCDC_3V3_PG — R710 10K — EN; C707 0.1uF 25V 0402_CC

Vfb=0.6V / +-3%

Vo=Vfb*(R1+R2)/R2 = Vfb(1+R1/R2)

R1/R2 = (Vo-Vfb)/Vfb

1.4V: R1/R2 = 213K/160K
1.3V: R1/R2 = 186.7K/160K
0.925V: R1/R2 = 86.7K/160K

TP703 — ARM_SOC_PG

PMIC_STBY_REQ = 0, GPIO_DVFS = 0, output is 1.4V (1.375V + 25mV)
PMIC_STBY_REQ = 0, GPIO_DVFS = 1, output is 1.3V (1.275V + 25mV)
PMIC_STBY_REQ = 1, GPIO_DVFS = 0, output is 0.925V (0.9V + 25mV)

R706 215K — R707 147K — R708 1.5M — C705 22UF 6.3V 0603_CC — C706 0.1uF 25V 0402_CC — TP702 — R737 51

Q701 RYU002N05 — Q702 2SK3018 — Q707 2SK3018 — DISCHG_EN — DNP C745 1000pF 50V 0402_CC

1.035M OHM — 225K OHM — PD (100K) — GPIO_DVFS / PMIC_STBY_REQ

R713 160K 1% — R714 100K DNP — R715 100K

Important: GPIO_DVFS / PMIC_STBY_REQ should be PULL DN when system reboot to ensure the VDD_ARM_SOC_IN voltage is not effected by DVFS

SNVS

VSYS — C701 10uF 10V 0603_CC, C708 0.1uF 25V 0402_CC — U701 RT9169-33GVL (VIN, VOUT, GND) — TP701 — # 3.3V/100mA Iq = 4¦ÌA — VDD_SNVS_3V3

C709 4.7uF 6.3V, C710 0.1uF 25V 0402_CC

VDDHIGH / NVCC_xxx

Current 2A
I_Quiescent : 40¦ÌA

VSYS # 2.5V-to-5.5V — C711 10uF 10V 0603_CC, C712 10uF 10V 0603_CC, C713 0.1uF 25V 0402_CC — U703 MP2144GJ (VIN, SW, OUT, FB, EN, PG, PGND, AGND) — L701 1uH — TP705 — R730 0 — DCDC_3V3

R716 100K DNP

PMIC_ON_REQ — R733 10K

C737 0.22UF 10V 0402_cc

PG pin is pulled up to VIN by the internal resistor 500K OHM

R1/R2 = 9/2

Vfb=0.6V

R717 180K 1% — R718 40.2K 1% — C714 22UF 6.3V 0603_CC, C715 0.1uF 25V 0402_CC

R726 0 — DCDC_3V3_PG — TP706

DCDC_3V3 — R727 DNP — C743 DNP 1000pF 50V 0402_CC — C744 DNP 1000pF 50V 0402_CC

VDD_SNVS_3V3 — R734 51 — R735 100K — DISCHG_EN — R740 10K — Q705 2SK3018 — Q704 2SK3018 — C736 0.1uF 25V 0402_CC

DCDC_3V3 — # Stitching CAP for Layout — C741 0.1uF 25V 0402_CC, C742 0.1uF 25V 0402_CC

Reset Button — MX6_POR_B — R757 100 — D702 RB521S-30 — C739 1000pF 0402_CC

U708 (RESET, GND, VCC, MR) — UM805RE — R758 0 DNP — C740 0.1uF 25V 0402_CC — VDD_SNVS_3V3

GPIO/WDOG PWR OFF->ON — nWDOG — C738 1.0UF 10V 0402_cc — D705 RB521S-30 — R755 1M

ADC High PSRR

VSYS — C716 10uF 10V 0603_CC, C717 0.1uF 25V 0402_CC — U704 RT9193 (VIN, VOUT, EN, GND, BP) — TP704 — VLDO_3V3 — C718 4.7uF 6.3V, C719 0.1uF 25V 0402_CC

C720 0.022UF 16V 0402_CC

DCDC_3V3_PG — C747 DNP 1000pF 50V 0402_CC

1.8V PWR

RSV for eMMC HS200

DCDC_3V3 — C721 4.7uF 6.3V, C722 0.1uF 25V 0402_CC — D701 DNP, RB521S-30 — U705 RT9193-18GVL (VIN, VOUT, GND) — TP707 — # 1.8V/200mA Iq = 1.2¦ÌA — VLDO_1V8 — C723 4.7uF 6.3V, C724 0.1uF 25V 0402_CC

LvDDR3

Current 1A
I_Quiescent : 17¦ÌA

VSYS # 2.5V to 6V — C725 10uF 10V 0603_CC, C729 10uF 10V 0603_CC, C726 0.1uF 25V 0402_CC — U706 MP2159GJ (VIN, SW, OUT, FB, EN, PG, PGND, AGND) — L703 1uH — TP708 — R728 0 — DRAM_1V35

DCDC_3V3_PG — R722 10K — C735 0.1uF 25V 0402_CC

Vfb=0.6V

R719 200K 1% — R723 160K 1% — C727 22UF 6.3V 0603_CC, C728 0.1uF 25V 0402_CC

R1/R2 = 0.75/0.6

R736 51

DISCHG_EN — DNP C746 1000pF 50V 0402_CC — Q706 2SK3018

Update to MP2159

PG pin is pulled up to VIN by the internal resistor 550K OHM

TP710 — DRAM_PG

NVCC_SD <SD3.0>

VSYS — C730 10uF 10V 0603_CC, C731 0.1uF 25V 0402_CC — U707 UM1750S-00 (IN, OUT, SHDN, GND, FB) — Vfb=1V — TP709 — NVCC_SD # 1.8V/3.3V # Default: 3.3V

R720 464K — 499K — R721 243K — 330K — Q703 2SK3018 — R724 200K 1% — 160K — R725 100K — SD1_VSELECT

C732 4.7uF 6.3V, C733 0.1uF 25V 0402_CC

DCDC_3V3_PG

R1/R2 = (Vo-Vfb)/Vfb

FB = 0.8V — # 1.8V: R1/R2 = 1/0.8 : 200K/160K
3.3V: R1/R2 = 2.5/0.8 : 500K/160K

FB = 1.0V — # 1.8V: R1/R2 = 0.8/ 1: 160K/200K
3.3V: R1/R2 = 2.3/1 : 464K/200K

ICAP Classification: CP: ___ IUO: X PUBI: ___

Drawing Title: **MCIMX6UL-CM**

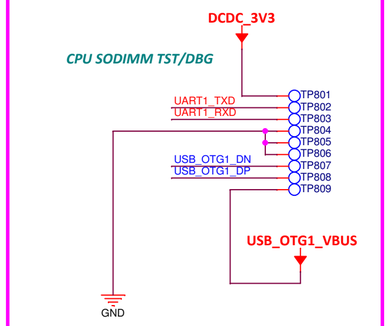
Page Title: **PWR MGR**

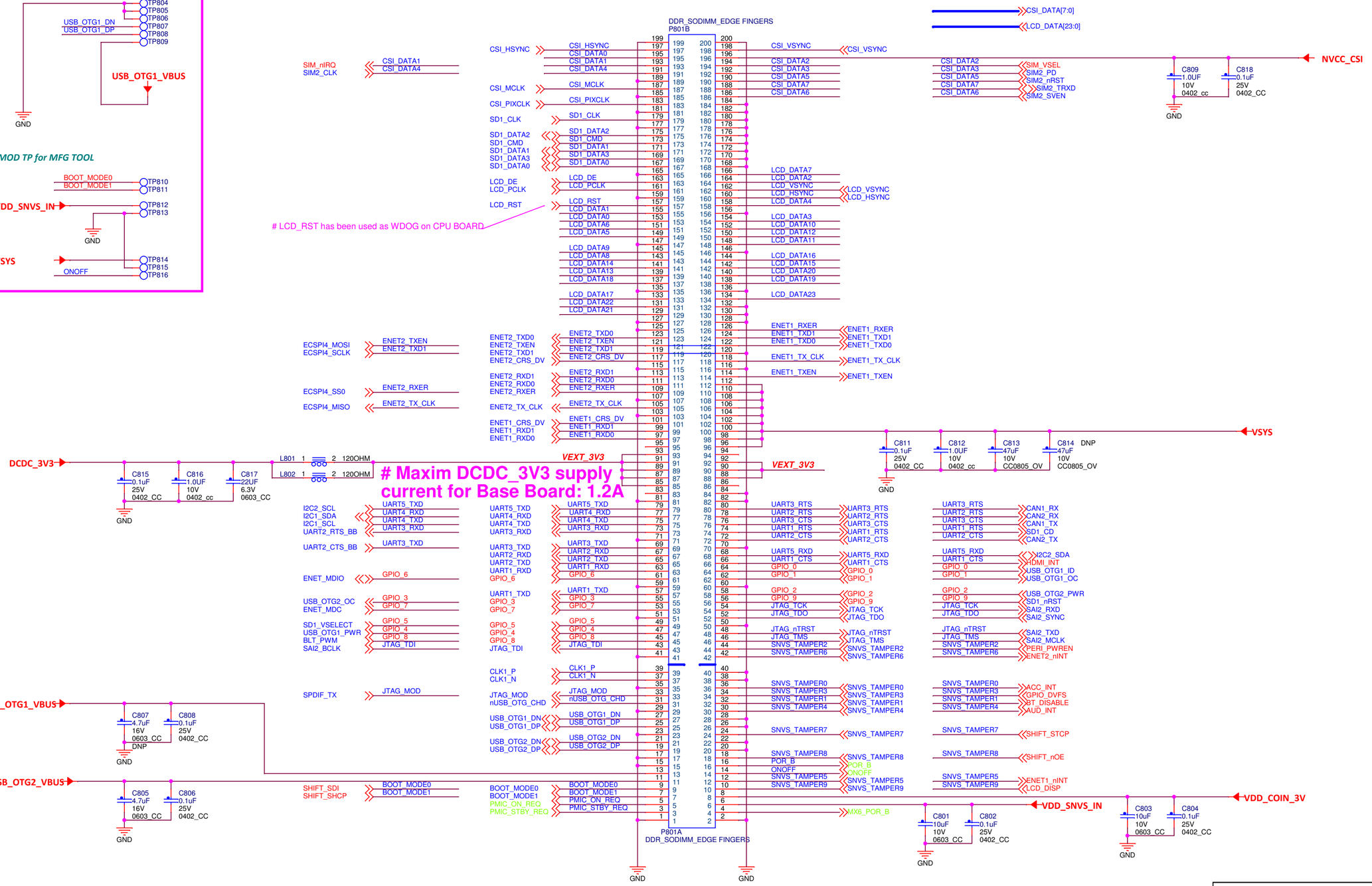
Size	Document Number	Rev
C	SCH-28617 PDF: SPF-28617	C5

Date: Wednesday, September 07, 2016 | Sheet 10 of 13

SODIMM 200

TP for SODIMM MFG





ICAP Classification:	CP: ___ IUO: X PUBI: ___	
Drawing Title:	MCIMX6UL-CM	
Page Title:	CPU-SODIMM200	
Size C	Document Number SCH-28617 PDF: SPF-28617	Rev C5
Date: Wednesday, September 07, 2016	Sheet 11 of 13	

NOTE:

All pins using ~reset as harden :

PAD	Default State	Simulation Value
UART3_TX_DATA	Output Buffer(LOW) during reset --> Output keeper + Input enable after reset done	0 in real silicon
LCD_DATA00~LCD_DATA23	100K pull down + input enable during reset --> Output keeper + Input enable after reset done (this is boot option, we don¡¯t need change)	0 in real silicon

PAD	Default State	Signal Path	PAD Simulation Value
UART3_TX_DATA	Output Buffer(LOW) during reset --> Output keeper + Input enable after reset done	sjc.ipt_jta_active --> PAD	0 in real silicon
		(note : sjc.ipt_jta_active also connected to snvs_hp.sec_vio_in_1. This is security related, we don¡¯t plan to change it.)	ALT7

All pins using ~src.en_system_clk as harden :

PAD	Default State	Simulation Value
GPIO1_IO03	100K pull down + input enable during reset --> Output keeper + Input enable after reset done	0 in real silicon

PAD	Default State	Signal Path	PAD Simulation Value
GPIO1_IO03	100K pull down + input enable during reset --> Output keeper + Input enable after reset done	PAD --> ccmsrcmix. src_tester_ack	0 in real silicon
		This is the requirement of TE test	ALT7

All pins using snvs_hp.snvs_sec_vio_in_5_en as harden :

PAD	Default State	Simulation Value
CSI_PIXCLK	Output keeper + Input enable (snvs_sec_vio_in_5_en is 1¡¯b0 in normal state, so harden is not triggerd in normal state). snvs_sec_vio_in_5_en is controlled by SNVS register. It can be disable or enable.	X (0 or 1 in real silicon)

ICAP Classification: CP: ___ IUO: X PUBI: ___
Drawing Title: MCIMX6UL-CM
Page Title: NOTE
Size C | Document Number SCH-28617 PDF: SPF-28617 | Rev C5
Date: Wednesday, September 07, 2016 | Sheet 12 of 13

i.MX6UL IOMUX

NAME	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	PAD DFU
TEST_MODE	tcu.TEST_MODE	tcu.TEST_MODE									100K PD
POR_B	src.POR_B	src.POR_B									100K PU
ONOFF	src.RESET_B	src.RESET_B									100K PU
SNVS_PMIC_ON_REQ	snvs_lp_wrapper.SNVS_WAKEUP_ALARM	snvs_lp_wrapper.PMIC_ON_REQ									100K PU
CCM_PMIC_STBY_REQ	ccm.PMIC_VSTBY_REQ	ccm.PMIC_VSTBY_REQ									100K PD
BOOT_MODE0	src.BOOT_MODE[0]	src.BOOT_MODE[0]									100K PD
BOOT_MODE1	src.BOOT_MODE[1]	src.BOOT_MODE[1]									100K PD
SNVS_TAMPER0	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[0]					gpio5.IO[10]				Keeper
SNVS_TAMPER1	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[1]					gpio5.IO[11]				Keeper
SNVS_TAMPER2	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[2]					gpio5.IO[0]				Keeper
SNVS_TAMPER3	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[3]					gpio5.IO[1]				Keeper
SNVS_TAMPER4	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[4]					gpio5.IO[2]				Keeper
SNVS_TAMPER5	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[5]					gpio5.IO[3]				Keeper
SNVS_TAMPER6	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[6]					gpio5.IO[4]				Keeper
SNVS_TAMPER7	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[7]					gpio5.IO[5]				Keeper
SNVS_TAMPER8	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[8]					gpio5.IO[6]				Keeper
SNVS_TAMPER9	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[9]					gpio5.IO[7]				Keeper
JTAG_MOD	sjc.MOD	sjc.MOD					gpio5.IO[8]				Keeper
JTAG_TMS	sjc.TMS	sjc.TMS					gpio5.IO[9]				Keeper
JTAG_TDO	sjc.TDO	sjc.TDO					gpio1.IO[10]	sdma.EXT_EVENT[0]			100K PU
JTAG_TDI	sjc.TDI	sjc.TDI					gpio1.IO[11]	sdma.EXT_EVENT[1]		epit1.OUT	47K PU
JTAG_TCK	sjc.TCK	sjc.TCK					gpio1.IO[12]	mqs.RIGHT		epit2.OUT	100K PU
JTAG_TRST_B	sjc.TRSTB	sjc.TRSTB					gpio1.IO[13]	mqs.LEFT		sim1.POWER_FAIL	47K PU
GPIO1_IO00	gpio1.IO[0]	i2c2.SCL					gpio1.IO[14]	osc32k.32K_OUT		sim2.POWER_FAIL	47K PU
GPIO1_IO01	gpio1.IO[1]	i2c2.SDA					gpio1.IO[15]	anatop.24M_OUT		caam_wrapper.RNG_OSC_OBS	47K PU
GPIO1_IO02	gpio1.IO[2]	i2c1.SCL					gpio1.IO[0]	enet1.1588_EVENT0_IN	src.SYSTEM_RESET	wdog3.WDOG_B	Keeper
GPIO1_IO03	gpio1.IO[3]	i2c1.SDA					gpio1.IO[1]	enet1.1588_EVENT0_OUT	src.EARLY_RESET	wdog1.WDOG_B	Keeper
GPIO1_IO04	gpio1.IO[4]	anatop.ENET_REF_CLK1					gpio1.IO[2]	sdma.EXT_EVENT[0]	src.ANY_PU_RESET	uart1.TX	Keeper
GPIO1_IO05	gpio1.IO[5]	anatop.ENET_REF_CLK2					gpio1.IO[3]	ccm.DI0_EXT_CLK	src.TESTER_ACK	uart1.RX	Keeper
GPIO1_IO06	gpio1.IO[6]	enet1.MDIO					gpio1.IO[4]	enet2.1588_EVENT0_IN	ccm.PLL2_BYP	uart5.TX	Keeper
GPIO1_IO07	gpio1.IO[7]	enet1.MDC					gpio1.IO[5]	enet2.1588_EVENT0_OUT	ccm.PLL3_BYP	uart5.RX	Keeper
GPIO1_IO08	gpio1.IO[8]	pwm1.OUT					gpio1.IO[6]	ccm.WAIT	ccm.REF_EN_B	uart1.CTS_B	Keeper
GPIO1_IO09	gpio1.IO[9]	pwm2.OUT					gpio1.IO[7]	ccm.STOP	ecspi1.TESTER_TRIGGER	uart1.RTS_B	Keeper
UART1_TXD	gpio1.IO[16]	uart1.TX					gpio1.IO[8]	ccm.PMIC_RDY	ecspi2.TESTER_TRIGGER	uart5.RTS_B	Keeper
UART1_RXD	gpio1.IO[17]	uart1.RX					gpio1.IO[9]	usdhc1.RESET_B	ecspi3.TESTER_TRIGGER	uart5.CTS_B	Keeper
UART1_CTS	gpio1.IO[18]	uart1.CTS_B					gpio1.IO[16]	anatop.USBPHY1_TSTI_TX_LS_MODE	ecspi4.TESTER_TRIGGER	spdif.OUT	Keeper
UART1_RTS	gpio1.IO[19]	uart1.RTS_B					gpio1.IO[17]	anatop.USBPHY1_TSTI_TX_HS_MODE	usdhc1.TESTER_TRIGGER	spdif.IN	Keeper
UART2_TXD	gpio1.IO[20]	uart2.TX					gpio1.IO[18]	anatop.USBPHY1_TSTI_TX_DN	usdhc2.TESTER_TRIGGER	usdhc2.WP	Keeper
UART2_RXD	gpio1.IO[21]	uart2.RX					gpio1.IO[19]	anatop.USBPHY1_TSTO_RX_SQUELCH	qspi.TESTER_TRIGGER	usdhc2.CD_B	Keeper
UART2_CTS	gpio1.IO[22]	uart2.CTS_B					gpio1.IO[20]	anatop.USBPHY1_TSTO_RX_DISCON_DET	rawnand.TESTER_TRIGGER	ecspi3.SS0	Keeper
UART2_RTS	gpio1.IO[23]	uart2.RTS_B					gpio1.IO[21]	anatop.USBPHY1_TSTO_RX_HS_RXD	sjc.DONE	ecspi3.SCLK	Keeper
UART3_TXD	gpio1.IO[24]	uart3.TX					gpio1.IO[22]	anatop.USBPHY2_TSTO_RX_FS_RXD	sjc.DE_B	ecspi3.MOSI	Keeper
UART3_RXD	gpio1.IO[25]	uart3.RX					gpio1.IO[23]	anatop.USBPHY1_TSTO_RX_FS_RXD	sjc.FAIL	ecspi3.MISO	Keeper
UART3_CTS	gpio1.IO[26]	uart3.CTS_B					gpio1.IO[24]	anatop.USBPHY1_TSTI_TX_DP	sjc.JTAG_ACT	anatop.OTG1_ID	Keeper
UART3_RTS	gpio1.IO[27]	uart3.RTS_B					gpio1.IO[25]	anatop.USBPHY1_TSTI_TX_EN	sim_m.HADDR[0]	epit1.OUT	Keeper
UART4_TXD	gpio1.IO[28]	uart4.TX					gpio1.IO[26]	anatop.USBPHY1_TSTI_TX_HIZ	sim_m.HADDR[1]	epit2.OUT	Keeper
UART4_RXD	gpio1.IO[29]	uart4.RX					gpio1.IO[27]	anatop.USBPHY2_TSTO_RX_HS_RXD	sim_m.HADDR[2]	wdog1.WDOG_B	Keeper
UART5_TXD	gpio1.IO[30]	uart5.TX					gpio1.IO[28]	anatop.USBPHY1_TSTO_PLL_CLK20DIV	sim_m.HADDR[3]	ecspi2.SCLK	Keeper
UART5_RXD	gpio1.IO[31]	uart5.RX					gpio1.IO[29]	anatop.USBPHY2_TSTO_PLL_CLK20DIV	sim_m.HADDR[4]	ecspi2.SS0	Keeper
ENET1_RXD0	gpio2.IO[0]	enet1.RDATA[0]	uart4.RTS_B	spdif.OUT	anatop.ENET_REF_CLK_25M	ccm.PMIC_RDY	gpio1.IO[30]	anatop.USBPHY2_TSTO_RX_SQUELCH	sim_m.HADDR[5]	ecspi2.MOSI	Keeper
ENET1_RXD1	gpio2.IO[1]	enet1.RDATA[1]	uart4.CTS_B	sai2.MCLK	ccm.CLKO1	ccm.WAIT	gpio1.IO[31]	anatop.USBPHY2_TSTO_RX_DISCON_DET	sim_m.HADDR[6]	ecspi2.MISO	Keeper
ENET1_CRS_DV	gpio2.IO[2]	enet1.RX_EN	uart5.RTS_B	sai2.TX_SYNC	ccm.CLKO2	ccm.STOP	gpio2.IO[0]	kpp.ROW[0]	sim_m.HADDR[7]	usdhc1.LCTL	Keeper
ENET1_TXD0	gpio2.IO[3]	enet1.TDATA[0]	uart5.CTS_B	sai2.TX_BCLK	ccm.OUT0	pwm6.OUT	gpio2.IO[1]	kpp.COL[0]	sim_m.HADDR[8]	usdhc2.LCTL	Keeper
ENET1_TXD1	gpio2.IO[4]	enet1.TDATA[1]	uart6.CTS_B	sai2.RX_DATA	ccm.OUT1	pwm7.OUT	gpio2.IO[2]	kpp.ROW[1]	sim_m.HADDR[9]	usdhc1.VSELECT	Keeper
ENET1_TXEN	gpio2.IO[5]	enet1.TX_EN	uart6.RTS_B	sai2.TX_DATA	ccm.OUT2	pwm8.OUT	gpio2.IO[3]	kpp.COL[1]	sim_m.HADDR[10]	usdhc2.VSELECT	Keeper
ENET1_TXCLK	gpio2.IO[6]	enet1.TX_CLK	uart7.CTS_B	anatop.OTG1_ID	anatop.ENET_REF_CLK1	mqs.RIGHT	gpio2.IO[4]	kpp.ROW[2]	sim_m.HADDR[11]	wdog1.WDOG_RST_B_DEB	Keeper
ENET1_RXER	gpio2.IO[7]	enet1.RX_ER	uart7.RTS_B	pwm8.OUT	anatop.ENET_REF_CLK2	mqs.LEFT	gpio2.IO[5]	kpp.COL[2]	sim_m.HADDR[12]	wdog2.WDOG_RST_B_DEB	Keeper
ENET2_RXD0	gpio2.IO[8]	enet2.RDATA[0]	uart6.TX	sim1.PORT0_TRXD	i2c3.SCL	enet1.MDIO	gpio2.IO[6]	kpp.ROW[3]	sim_m.HADDR[13]	gpt1.CLK	Keeper
ENET2_RXD1	gpio2.IO[9]	enet2.RDATA[1]	uart6.RX	sim1.PORT0_CLK	i2c3.SDA	enet1.MDC	gpio2.IO[7]	kpp.COL[3]	sim_m.HADDR[14]	gpt1.CAPTURE2	Keeper
ENET2_CRS_DV	gpio2.IO[10]	enet2.RX_EN	uart7.TX	sim1.PORT0_RST_B	i2c4.SCL	weim.ADDR[26]	gpio2.IO[8]	kpp.ROW[4]	sim_m.HADDR[15]	usb.OTG1_PWR	Keeper
ENET2_TXD0	gpio2.IO[11]	enet2.TDATA[0]	uart7.RX	sim1.PORT0_SVEN	i2c4.SDA	weim.EB_B[2]	gpio2.IO[9]	kpp.COL[4]	sim_m.HADDR[16]	usb.OTG1_OC	Keeper
ENET2_TXD1	gpio2.IO[12]	enet2.TDATA[1]	uart8.TX	sim2.PORT0_TRXD	ecspi4.SCLK	weim.EB_B[3]	gpio2.IO[10]	kpp.ROW[5]	sim_m.HADDR[17]	anatop.ENET_REF_CLK_25M	Keeper
ENET2_TXEN	gpio2.IO[13]	enet2.TX_EN	uart8.RX	sim2.PORT0_CLK	ecspi4.MOSI	weim.ACLK_FREERUN	gpio2.IO[11]	kpp.COL[5]	sim_m.HADDR[18]	anatop.24M_OUT	Keeper
ENET2_TXCLK	gpio2.IO[14]	enet2.TX_CLK	uart8.CTS_B	sim2.PORT0_RST_B	ecspi4.MISO	anatop.ENET_REF_CLK2	gpio2.IO[12]	kpp.ROW[6]	sim_m.HADDR[19]	usb.OTG2_PWR	Keeper
ENET2_RXER	gpio2.IO[15]	enet2.RX_ER	uart8.RTS_B	sim2.PORT0_SVEN	ecspi4.SS0	weim.ADDR[25]	gpio2.IO[13]	kpp.COL[6]	sim_m.HADDR[20]	usb.OTG2_OC	Keeper
LCD_CLK	gpio3.IO[0]	lcdif.CLK	lcdif.WR_RWN	uart4.TX	sai3.MCLK	sai3.TX_SYNC	gpio2.IO[14]	kpp.COL[7]	sim_m.HADDR[21]	anatop.OTG2_ID	Keeper
LCD_ENABLE	gpio3.IO[1]	lcdif.ENABLE	lcdif.RD_E	uart4.RX	sai3.TX_SYNC	weim.CS2_B	gpio2.IO[15]	ocotp_ctrl_wrapper.FUSE_LATCHED	sim_m.HADDR[22]	global wdog	Keeper
LCD_HSYNC	gpio3.IO[2]	lcdif.HSYNC	lcdif.RS	uart4.CTS_B	sai3.TX_BCLK	wdog3.WDOG_RST_B_DEB	gpio3.IO[0]	anatop.TESTI[0]	sim_m.HADDR[23]	wdog1.WDOG_RST_B_DEB	Keeper
LCD_VSYNC	gpio3.IO[3]	lcdif.VSYNC	lcdif.BUSY	uart4.RTS_B	sai3.RX_DATA	wdog2.WDOG_B	gpio3.IO[1]	anatop.TESTI[1]	sim_m.HADDR[24]	ecspi2.RDY	Keeper
LCD_RESET	gpio3.IO[4]	lcdif.RESET	lcdif.CS	ca7_platform.EVENTI	sai3.TX_DATA	global wdog	gpio3.IO[2]	anatop.TESTI[2]	sim_m.HADDR[25]	ecspi2.SS1	Keeper
LCD_DATA00	gpio3.IO[5]	lcdif.DATA[0]	pwm1.OUT	ca7_platform.TRACE[0]	enet1.1588_EVENT2_IN	i2c3.SDA	gpio3.IO[3]	anatop.TESTI[3]	sim_m.HADDR[26]	ecspi2.SS2	Keeper
LCD_DATA01	gpio3.IO[6]	lcdif.DATA[1]	pwm2.OUT	ca7_platform.TRACE[1]	enet1.1588_EVENT2_OUT	i2c3.SCL	gpio3.IO[4]	src.BT_CFG[0]	sim_m.HADDR[27]	ecspi2.SS3	Keeper
LCD_DATA02	gpio3.IO[7]	lcdif.DATA[2]	pwm3.OUT	ca7_platform.TRACE[2]	enet1.1588_EVENT3_IN	i2c4.SDA	gpio3.IO[5]	src.BT_CFG[1]	sim_m.HADDR[28]	sai1.MCLK	Keeper
LCD_DATA03	gpio3.IO[8]	lcdif.DATA[3]	pwm4.OUT	ca7_platform.TRACE[3]	enet1.1588_EVENT3_OUT	i2c4.SCL	gpio3.IO[6]	src.BT_CFG[2]	sim_m.HADDR[29]	sai1.TX_SYNC	Keeper
LCD_DATA04	gpio3.IO[9]	lcdif.DATA[4]	uart8.CTS_B	ca7_platform.TRACE[4]	enet2.1588_EVENT2_IN	spdif.SR_CLK	gpio3.IO[7]	src.BT_CFG[3]	sim_m.HADDR[30]	sai1.TX_BCLK	Keeper
LCD_DATA05	gpio3.IO[10]	lcdif.DATA[5]	uart8.RTS_B	ca7_platform.TRACE[5]	enet2.1588_EVENT2_OUT	spdif.OUT	gpio3.IO[8]	src.BT_CFG[4]	sim_m.HADDR[31]	sai1.RX_DATA	Keeper
LCD_DATA06	gpio3.IO[11]	lcdif.DATA[6]	uart7.CTS_B	ca7_platform.TRACE[6]	enet2.1588_EVENT3_IN	spdif.LOCK	gpio3.IO[9]	src.BT_CFG[5]	sim_m.HBURST[0]	sai1.TX_DATA	Keeper
LCD_DATA07	gpio3.IO[12]	lcdif.DATA[7]	uart7.RTS_B	ca7_platform.TRACE[7]	enet2.1588_EVENT3_OUT	spdif.EXT_CLK	gpio3.IO[10]	src.BT_CFG[6]	sim_m.HBURST[1]	ecspi1.SS1	Keeper
LCD_DATA08	gpio3.IO[13]	lcdif.DATA[8]	spdif.IN	ca7_platform.TRACE[8]	csi.DATA[16]	weim.DATA[0]	gpio3.IO[11]	src.BT_CFG[7]	sim_m.HBURST[2]	ecspi1.SS2	Keeper
LCD_DATA09	gpio3.IO[14]	lcdif.DATA[9]	sai3.MCLK	ca7_platform.TRACE[9]	csi.DATA[17]	weim.DATA[1]	gpio3.IO[12]	src.BT_CFG[8]	sim_m.HMASTLOCK	ecspi1.SS3	Keeper
LCD_DATA10	gpio3.IO[15]	lcdif.DATA[10]	sai3.RX_SYNC	ca7_platform.TRACE[10]	csi.DATA[18]	weim.DATA[2]	gpio3.IO[13]	src.BT_CFG[9]	sim_m.HPROT[0]	can1.TX	Keeper
LCD_DATA11	gpio3.IO[16]	lcdif.DATA[11]	sai3.RX_BCLK	ca7_platform.TRACE[11]	csi.DATA[19]	weim.DATA[3]	gpio3.IO[14]	src.BT_CFG[10]	sim_m.HPROT[1]	can1.RX	Keeper
LCD_DATA12	gpio3.IO[17]	lcdif.DATA[12]	sai3.TX_SYNC	ca7_platform.TRACE[12]	csi.DATA[20]	weim.DATA[4]	gpio3.IO[15]	src.BT_CFG[11]	sim_m.HPROT[2]	can2.TX	Keeper
LCD_DATA13	gpio3.IO[18]	lcdif.DATA[13]	sai3.TX_BCLK	ca7_platform.TRACE[13]	csi.DATA[21]	weim.DATA[5]	gpio3.IO[16]	src.BT_CFG[12]	sim_m.HPROT[3]	can2.RX	Keeper
LCD_DATA14	gpio3.IO[19]	lcdif.DATA[14]	sai3.RX_DATA	ca7_platform.TRACE[14]	csi.DATA[22]	weim.DATA[6]	gpio3.IO[17]	src.BT_CFG[13]	sim_m.HREADYOUT	ecspi1.RDY	Keeper
LCD_DATA15	gpio3.IO[20]	lcdif.DATA[15]	sai3.TX_DATA	ca7_platform.TRACE[15]	csi.DATA[23]	weim.DATA[7]	gpio3.IO[18]	src.BT_CFG[14]	sim_m.HRESP	usdhc2.RESET_B	Keeper
LCD_DATA16	gpio3.IO[21]	lcdif.DATA[16]	uart7.TX	ca7_platform.TRACE_CLK	csi.DATA[1]	weim.DATA[8]	gpio3.IO[19]	src.BT_CFG[15]	sim_m.HSIZE[0]	usdhc2.DATA4	Keeper
LCD_DATA17	gpio3.IO[22]	lcdif.DATA[17]	uart7.RX	ca7_platform.TRACE_CTL	csi.DATA[0]	weim.DATA[9]	gpio3.IO[20]	src.BT_CFG[24]	sim_m.HSIZE[1]	usdhc2.DATA5	Keeper
LCD_DATA18	gpio3.IO[23]	lcdif.DATA[18]	pwm5.OUT	ca7_platform.EVENTO	csi.DATA[10]	weim.DATA[10]	gpio3.IO[21]	src.BT_CFG[25]	sim_m.HSIZE[2]	usdhc2.DATA6	Keeper
LCD_DATA19	gpio3.IO[24]	lcdif.DATA[19]	pwm6.OUT	global wdog	csi.DATA[11]	weim.DATA[11]	gpio3.IO[22]	src.BT_CFG[26]	sim_m.HWRITE	usdhc2.DATA7	Keeper
LCD_DATA20	gpio3.IO[25]	lcdif.DATA[20]	uart8.TX	ecspi1.SCLK	csi.DATA[12]	weim.DATA[12]	gpio3.IO[23]	src.BT_CFG[27]	tpsmp.CLK	usdhc2.CMD	Keeper
LCD_DATA21	gpio3.IO[26]	lcdif.DATA[21]	uart8.RX	ecspi1.SS0	csi.DATA[13]	weim.DATA[13]	gpio3.IO[24]	src.BT_CFG[28]	tpsmp.HDATA_DIR	usdhc2.CLK	Keeper
LCD_DATA22	gpio3.IO[27]	lcdif.DATA[22]	mqs.RIGHT	ecspi1.MOSI	csi.DATA[14]	weim.DATA[14]	gpio3.IO[25]	src.BT_CFG[29]	tpsmp.HTRANS[0]	usdhc2.DATA0	Keeper
LCD_DATA23	gpio3.IO[28]	lcdif.DATA[23]	mqs.LEFT	ecspi1.MISO	csi.DATA[15]	weim.DATA[15]	gpio3.IO[26]	src.BT_CFG[30]	tpsmp.HTRANS[1]	usdhc2.DATA1	Keeper
NAND_RE_B	gpio4.IO[0]	rawnand.RE_B	usdhc2.CLK	qspiB_SCLK	kpp.ROW[0]	weim.EB_B[0]	gpio3.IO[27]	src.BT_CFG[31]	tpsmp.HDATA[0]	usdhc2.DATA2	Keeper
NAND_WE_B	gpio4.IO[1]	rawnand.WE_B	usdhc2.CMD	qspiB_SS0_B	kpp.COL[0]	weim.EB_B[1]	gpio3.IO[28]	anatop.TESTO[0]	tpsmp.HDATA[1]	usdhc2.DATA3	Keeper
NAND_DATA00	gpio4.IO[2]	rawnand.DATA00	usdhc2.DATA0	qspiB_SS1_B	kpp.ROW[1]	weim.AD[8]	gpio4.IO[0]	anatop.TESTO[1]	tpsmp.HDATA[2]	ecspi3.SS2	Keeper
NAND_DATA01	gpio4.IO[3]	rawnand.DATA01	usdhc2.DATA1	qspiB_DQS	kpp.COL[1]	weim.AD[9]	gpio4.IO[1]	anatop.TESTO[2]	tpsmp.HDATA[3]	ecspi3.SS3	Keeper
NAND_DATA02	gpio4.IO[4]	rawnand.DATA02	usdhc2.DATA2	qspiB_DATA[0]	kpp.ROW[2]	weim.AD[10]	gpio4.IO[2]	anatop.TESTO[3]	tpsmp.HDATA[4]	ecspi4.RDY	Keeper
NAND_DATA03	gpio4.IO[5]	rawnand.DATA03	usdhc2.DATA3	qspiB_DATA[1]	kpp.COL[2]	weim.AD[11]	gpio4.IO[3]	anatop.TESTO[4]	tpsmp.HDATA[5]	ecspi4.SS1	Keeper
NAND_DATA04	gpio4.IO[6]	rawnand.DATA04	usdhc2.DATA4	qspiB_DATA[2]	ecspi4.SCLK	weim.AD[12]	gpio4.IO[4]	anatop.TESTO[5]	tpsmp.HDATA[6]	ecspi4.SS2	Keeper
NAND_DATA05	gpio4.IO[7]	rawnand.DATA05	usdhc2.DATA5	qspiB_DATA[3]	ecspi4.MOSI	weim.AD[13]	gpio4.IO[5]	anatop.TESTO[6]	tpsmp.HDATA[7]	ecspi4.SS3	Keeper
NAND_DATA06	gpio4.IO[8]	rawnand.DATA06	usdhc2.DATA6	sai2.RX_BCLK	ecspi4.MISO	weim.AD[14]	gpio4.IO[6]	anatop.TESTO[7]	tpsmp.HDATA[8]	uart2.TX	Keeper
NAND_DATA07	gpio4.IO[9]	rawnand.DATA07	usdhc2.DATA7	qspiA_SS1_B	ecspi4.SS0	weim.AD[15]	gpio4.IO[7]	anatop.TESTO[8]	tpsmp.HDATA[9]	uart2.RX	Keeper
NAND_ALE	gpio4.IO[10]	rawnand.ALE	usdhc2.RESET_B	qspiA_DQS	pwm3.OUT	weim.ADDR[17]	gpio4.IO[8]	anatop.TESTO[9]	tpsmp.HDATA[10]	uart2.CTS_B	Keeper
NAND_WP_B	gpio4.IO[11]	rawnand.WP_B	usdhc1.RESET_B	qspiA_SCLK	pwm4.OUT	weim.BCLK	gpio4.IO[9]	anatop.TESTO[10]	tpsmp.HDATA[11]	uart2.RTS_B	Keeper
NAND_READY_B	gpio4.IO[12]	rawnand.READY_B	usdhc1.DATA4	qspiA_DATA[0]	ecspi3.SS0	weim.CS1_B	gpio4.IO[10]	anatop.TESTO[11]	tpsmp.HDATA[12]	ecspi3.SS1	Keeper
NAND_CE0_B	gpio4.IO[13]	rawnand.CE0_B	usdhc1.DATA5	qspiA_DATA[1]	ecspi3.SCLK	weim.DTACK_B	gpio4.IO[11]	anatop.TESTO[12]	tpsmp.HDATA[13]	ecspi3.RDY	Keeper
NAND_CE1_B	gpio4.IO[14]	rawnand.CE1_B	usdhc1.DATA6	qspiA_DATA[2]	ecspi3.MOSI	weim.ADDR[18]	gpio4.IO[12]	anatop.TESTO[13]	tpsmp.HDATA[14]	uart3.TX	Keeper
NAND_CLE	gpio4.IO[15]	rawnand.CLE	usdhc1.DATA7	qspiA_DATA[3]	ecspi3.MISO	weim.ADDR[16]	gpio4.IO[13]	anatop.TESTO[14]	tpsmp.HDATA[15]	uart3.RX	Keeper
NAND_DQS	gpio4.IO[16]	rawnand.DQS	csi.FIELD	qspiA_SS0_B	pwm5.OUT	weim.CRE	gpio4.IO[14]	anatop.TESTO[15]	tpsmp.HDATA[16]	uart3.CTS_B	Keeper
SD1_CMD	gpio2.IO[16]	usdhc1.CMD	gpt2.COMPARE1	sai2.RX_SYNC	spdif.OUT	weim.ADDR[19]	gpio4.IO[15]	sdma.EXT_EVENT[0]	tpsmp.HDATA[17]	uart3.RTS_B	Keeper
SD1_CLK	gpio2.IO[17]	usdhc1.CLK	gpt2.COMPARE2	sai2.MCLK	spdif.IN	weim.ADDR[20]	gpio2.IO[16]	sdma.EXT_EVENT[1]	tpsmp.HDATA[18]	spdif.EXT_CLK	Keeper
SD1_DATA0	gpio2.IO[18]	usdhc1.DATA0	gpt2.COMPARE3	sai2.TX_SYNC	can1.TX	weim.ADDR[21]	gpio2.IO[17]	ccm.OUT0	observe_mux.OUT[0]	usb.OTG1_PWR	Keeper
SD1_DATA1	gpio2.IO[19]	usdhc1.DATA1	gpt2.CLK	sai2.TX_BCLK	can1.RX	weim.ADDR[22]	gpio2.IO[18]	ccm.OUT1	observe_mux.OUT[1]	usb.OTG1_OC	Keeper
SD1_DATA2	gpio2.IO[20]	usdhc1.DATA2	gpt2.CAPTURE1	sai2.RX_DATA	can2.TX	weim.ADDR[23]	gpio2.IO[19]	ccm.OUT2	observe_mux.OUT[2]	anatop.OTG1_ID	Keeper
SD1_DATA3	gpio2.IO[21]	usdhc1.DATA3	gpt2.CAPTURE2	sai2.TX_DATA	can2.RX	weim.ADDR[24]	gpio2.IO[20]	ccm.CLKO1	observe_mux.OUT[3]	usb.OTG2_PWR	Keeper
CSI_MCLK	gpio4.IO[17]	csi.MCLK	usdhc2.CD_B	rawnand.CE2_B	i2c1.SDA	weim.CS0_B	gpio2.IO[21]	ccm.CLKO2	observe_mux.OUT[4]	usb.OTG2_OC	Keeper
CSI_PIXCLK	gpio4.IO[18]	csi.PIXCLK	usdhc2.WP	rawnand.CE3_B	i2c1.SCL	weim.OE	gpio4.IO[17]	snvs_hp_wrapper.VIO_5_CTL	anatop.OTG2_ID	anatop.OTG2_ID	Keeper
CSI_VSYNC	gpio4.IO[19]	csi.VSYNC	usdhc2.CLK	sim1.PORT1_CLK	i2c2.SDA	weim.RW	gpio4.IO[18]	snvs_hp_wrapper.VIO_5	tpsmp.HDATA[20]	uart6.TX	Keeper
CSI_HSYNC	gpio4.IO[20]	csi.HSYNC	usdhc2.CMD	sim1.PORT1_PD	i2c2.SCL	weim.LBA_B	gpio4.IO[19]	pwm7.OUT	tpsmp.HDATA[21]	uart6.RX	Keeper
CSI_DATA00	gpio4.IO[21]	csi.DATA[2]	usdhc2.DATA0	sim1.PORT1_RST_B	ecspi2.SCLK	weim.AD[0]	gpio4.IO[20]	pwm8.OUT	tpsmp.HDATA[22]	uart6.RTS_B	Keeper
CSI_DATA01	gpio4.IO[22]	csi.DATA[3]	usdhc2.DATA1	sim1.PORT1_SVEN	ecspi2.SS0	weim.AD[1]	gpio4.IO[21]	src.INT_BOOT	tpsmp.HDATA[23]	uart6.CTS_B	Keeper
CSI_DATA02	gpio4.IO[23]	csi.DATA[4]	usdhc2.DATA2	sim1.PORT1_TRXD	ecspi2.MOSI	weim.AD[2]	gpio4.IO[22]	sai1.MCLK	tpsmp.HDATA[24]	uart5.TX	Keeper
CSI_DATA03	gpio4.IO[24]	csi.DATA[5]	usdhc2.DATA3	sim2.PORT1_PD	ecspi2.MISO	weim.AD[3]	gpio4.IO[23]	sai1.RX_SYNC	tpsmp.HDATA[25]	uart5.RX	Keeper
CSI_DATA04	gpio4.IO[25]	csi.DATA[6]	usdhc2.DATA4	sim2.PORT1_CLK	ecspi1.SCLK	weim.AD[4]	gpio4.IO[24]	sai1.RX_BCLK	tpsmp.HDATA[26]	uart5.RTS_B	Keeper
CSI_DATA05	gpio4.IO[26]	csi.DATA[7]	usdhc2.DATA5	sim2.PORT1_RST_B	ecspi1.SS0	weim.AD[5]	gpio4.IO[25]	sai1.TX_SYNC	tpsmp.HDATA[27]	uart5.CTS_B	Keeper
CSI_DATA06	gpio4.IO[27]	csi.DATA[8]	usdhc2.DATA6	sim2.PORT1_SVEN	ecspi1.MOSI	weim.AD[6]	gpio4.IO[26]	sai1.TX_BCLK	tpsmp.HDATA[28]	usdhc1.WP	Keeper
CSI_DATA07	gpio4.IO[28]	csi.DATA[9]	usdhc2.DATA7	sim2.PORT1_TRXD	ecspi1.MISO	weim.AD[7]	gpio4.IO[27]	sai1.RX_DATA	tpsmp.HDATA[29]	usdhc1.CD_B	Keeper
							gpio4.IO[28]	sai1.TX_DATA	tpsmp.HDATA[30]	usdhc1.RESET_B	Keeper
									tpsmp.HDATA[31]	usdhc1.VSELECT	Keeper

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Date: Wednesday, September 07, 2016 Sheet 13 of 13