Expanding Gigabit Ethernet on I.MX6 PCIe

NXP TIC team Weidong Sun

2016-04-12

Introductions

We know that PCIe interface is supported on i.MX6, due to PCIe's wide applicaion in computer field, we can expand many functions based on the interface, such as Gigabit ethernet, SATA disk, PCIe switch , multiple video input etc.

Since i.MX6 series processor released, some customers used PCIe interface to expand external devices. The document will introduce a way to design Gigabit ethernet on i.MX6 PCIe.

The following is technical feathers of i.MX6 PCIe:

①**i.MX6 PCIe**---PCI Express includes the following cores:

- PCI Express Dual Mode (DM) core
- PCI Express Root Complex (RC) core
- PCI Express Endpoint (EP) core
- The PCIe interface complies with PCIe specification Gen2 x1 lane and supports the PCI Express 1.1/2.0 standard.

<For more information, see i.MX6 reference manual, please!>

According to parameters of i.MX6 PCIe, we can select a Gigabit ethernet PHY with PCIe Gen2 x1 Lane.

For the design, we will select intel8274(intel82574IT part can be selected for industrial applicaition), let us see it's fundamental parameters.

②**Intel82574**---Product features:

- **PCI Express* (PCIe*)**
  - 64-bit address master support for systems using more than 4 GB of physical memory
  - Programmable host memory receive buffers (256 bytes to 16 KB)
  - Intelligent interrupt generation features to enhance driver performance
  - Descriptor ring management hardware for transmit and receive software controlled reset (resets everything except the configuration space)
  - Message Signaled Interrupts (MSI and MSI-X)
  - Configurable receive and transmit data FIFO, programmable in 1 KB increments
- **MAC**
  - Flow Control Support compliant with the 802.3X Specification
  - VLAN support compliant with the 802.1Q Specification
  - MAC Address filters: perfect match unicast
  - filters; multicast hash filtering, broadcast filter
  - and promiscuous mode
  - Statistics for management and RMOM
  - MAC loopback
- **PHY**
  - Compliant with the 1 Gb/s IEEE 802.3 802.3u 802.3ab Specifications
  - IEEE 802.3ab auto negotiation support
  - Full duplex operation at 10/100/1000 Mb/s
  - Half duplex at 10/100 Mb/s
  - Auto MDI, MDI-X crossover at all speeds
- **High Performance**
  - TCP segmentation capability compatible with Large Send offloading features
  - Support up to 256 KB TCP segmentation (TSO v2)
  - Fragmented UDP checksum offload for packet reassemble
  - IPv4 and IPv6 checksum offload support (receive, transmit, and large send)
  - Split header support
  - Receive Side Scaling (RSS) with two hardware receive queues
  - 9 KB jumbo frame support
  - 40 KB packet buffer size
- **Manageability**
  - NC-SI for remote management core
  - SMBus advanced pass through interface
- **Low Power**
  - Magic Packet* wake-up enable with unique MAC address
  - ACPI register set and power down functionality supporting D0 andD3 states
  - Full wake up support (APM and ACPI 2.0)
  - Smart power down at S0 no link and Sx no link
  - LAN disable function
- **Technology**
  - 9 mm x 9 mm 64-pin QFN package with Exposed Pad*
  - Configurable LED operation for customization of LED displays
  - TimeSync offload compliant with the 802.1as specification
  - Wider operating temperature range; -40 °C to 85 °C (82574IT only)

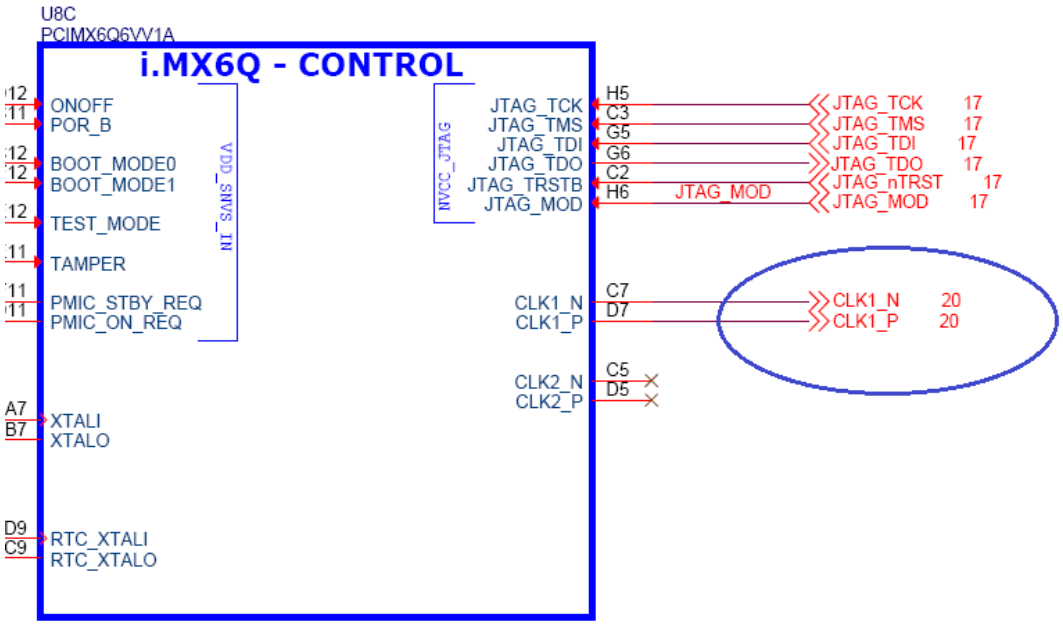
For more detail, see intel82574 datasheet, please!

Hardware design

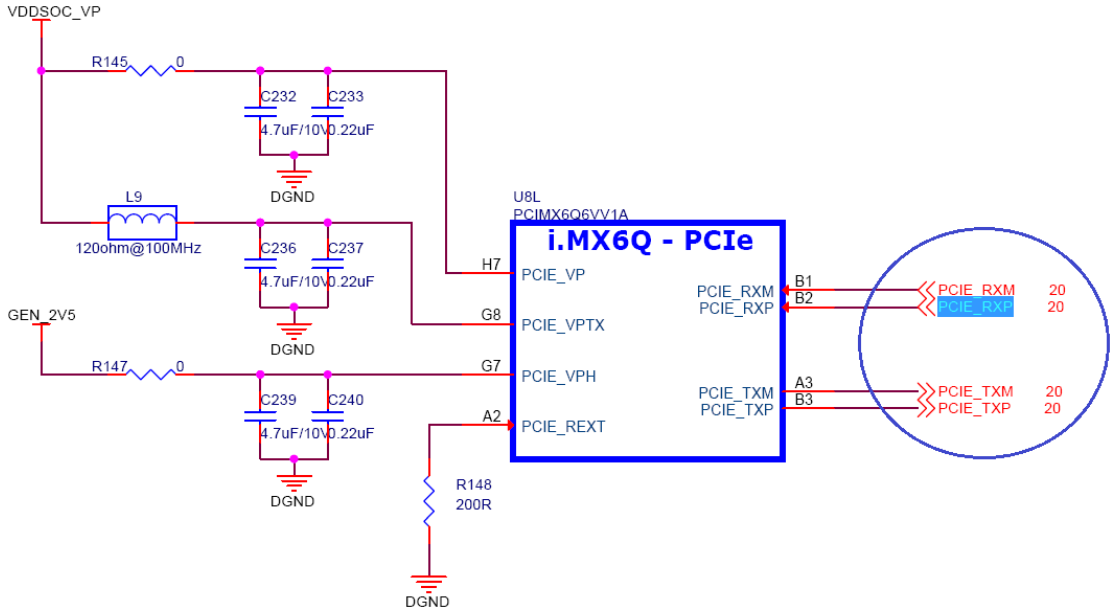
See following schematics:

1. CPU side

(1) Differential clock: the clock is used to be clock input of intel82574IT



(2) Differential signals : comunications with intel82574IT

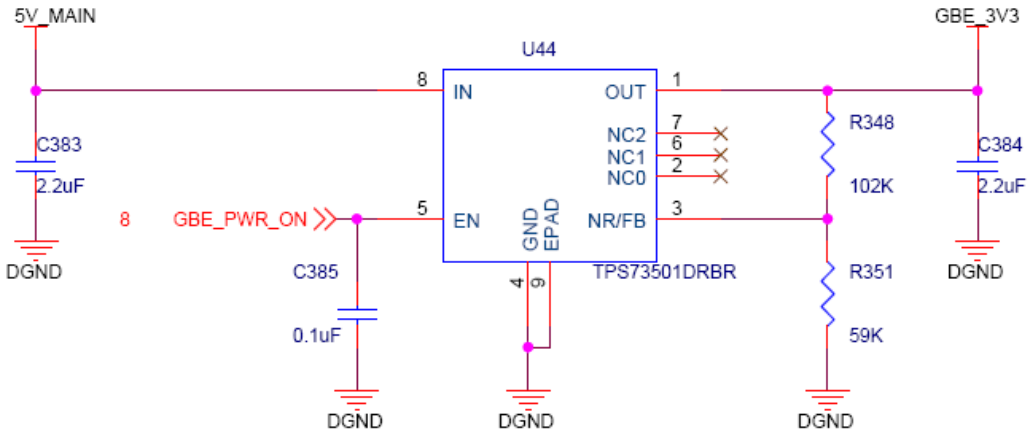


Here PCIE_RXM & PCIE_RXP are input for CPU, and PCIE_TXM & PCIE_TXP are input for CPU.

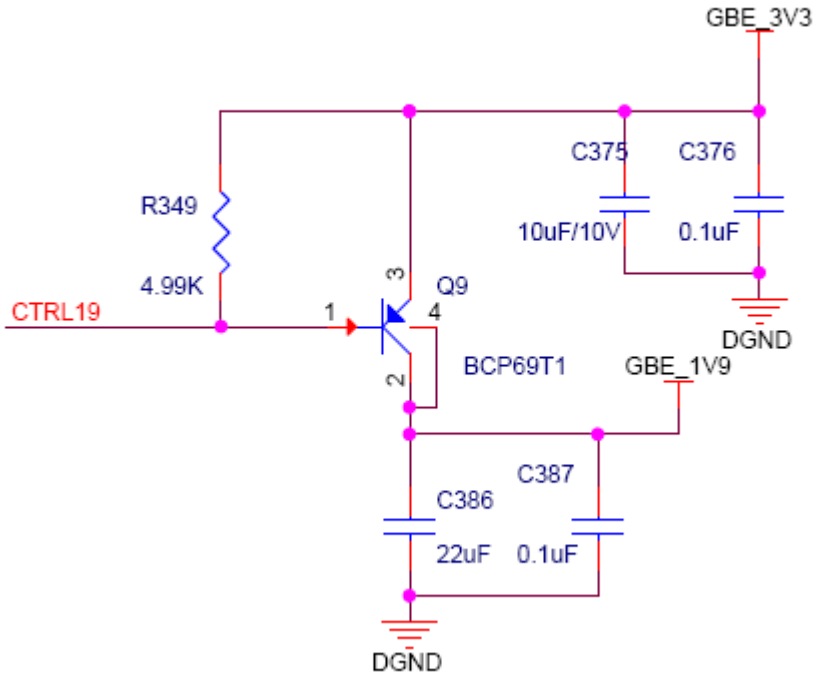
So CPU's input should be connected to intel82574's output, and CPU's output should be connected to intel82574's input. We must pay more attention to this conditions during designing schematics. PE_Tp & PE_Tn of intel82574 are output pins, PE_Rp & PE_Rn of intel82574 are input pins.

2. Intel82574IT side

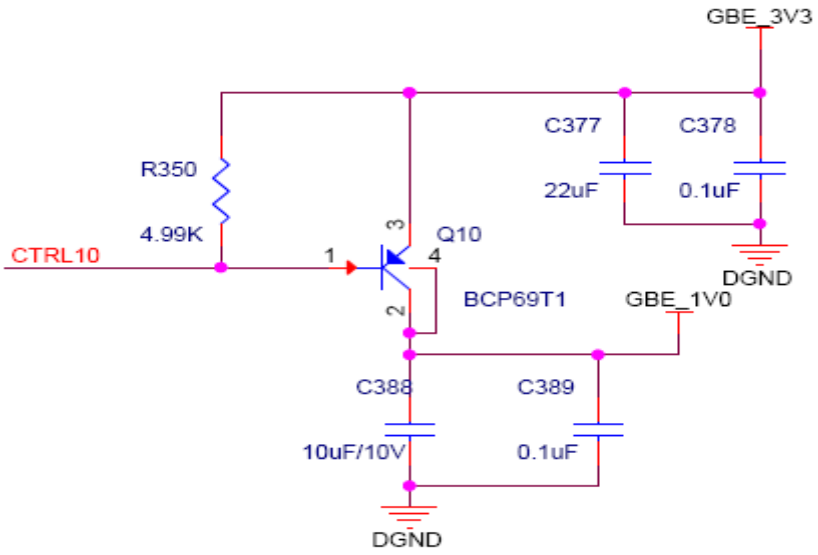
(1) Power (5V_MAIN is main power from wall adapter)



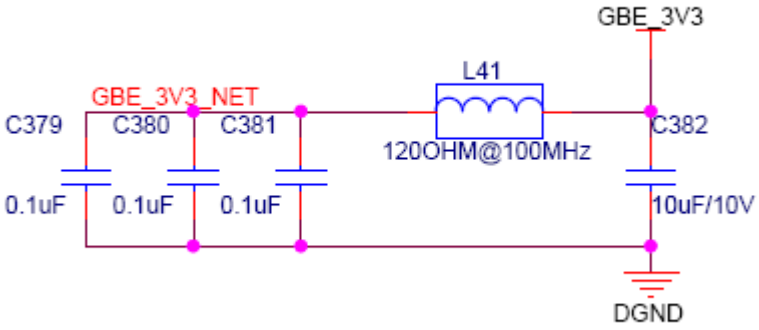
(2) Generating powers for intel82574 from 3.3V



3.3V-->1.9V

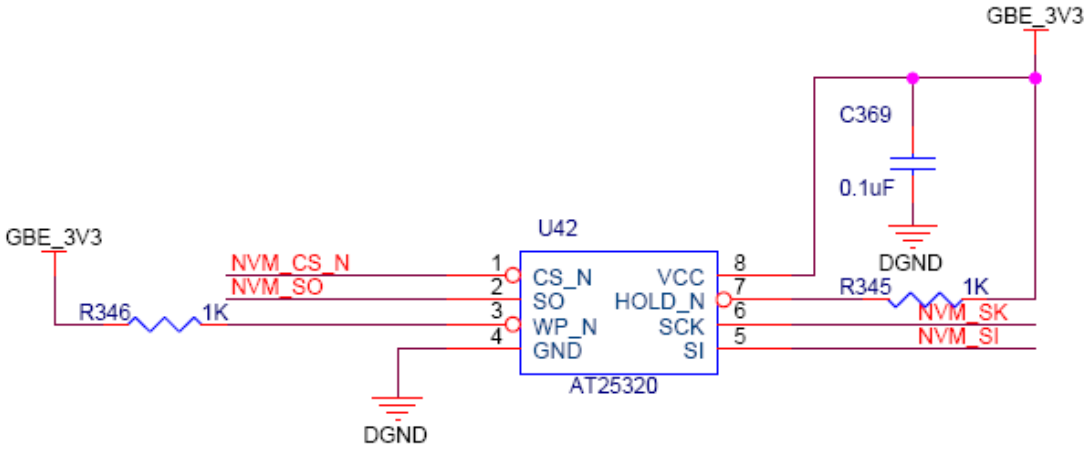


3.3V-->1.0V

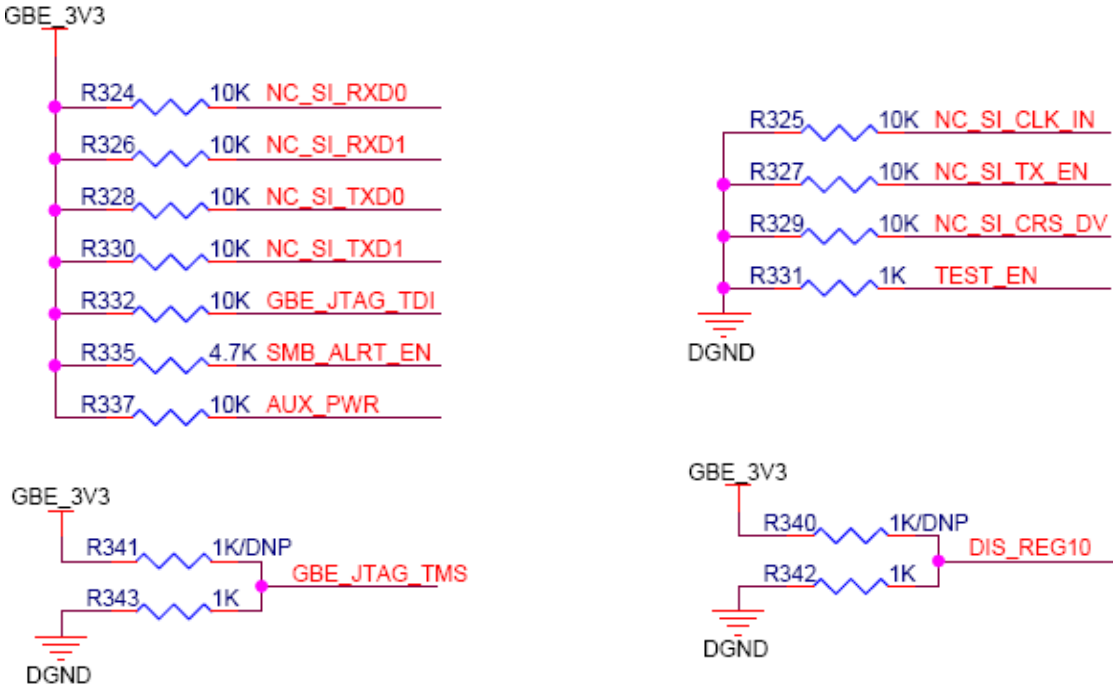


3.3V supply intel82574

(3)EEPROM(used to store intialization code)



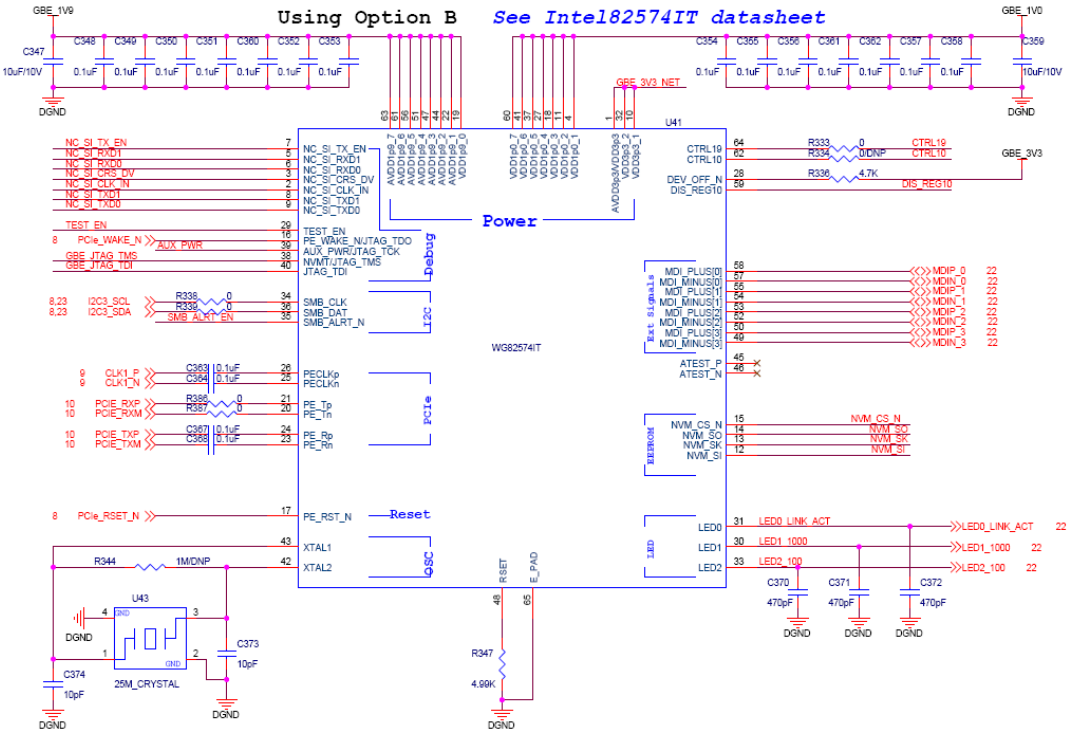
(4)Other signals



[Note] DNP means NC.

(5)Intel82574IT

`Intel82574IT`



The schematic is suitable for those customers who want to design all-in-one board. Our design team has validated network card based on intel82574 being sold in electronic market, It can normally work in linux BSP.