FTF 2016
TECHNOLOGY FORUM

CONSIDERING AN 8-BIT MCU? THINK AGAIN

LEARN THE CLEAR ADVANTAGES OF WHY AND HOW LPC MCUS BASED ON CORTEX®-M0/M0+ CORES BRING SIGNIFICANT VALUE TO EMBEDDED APPLICATIONS

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APPLICATIONS MANAGER
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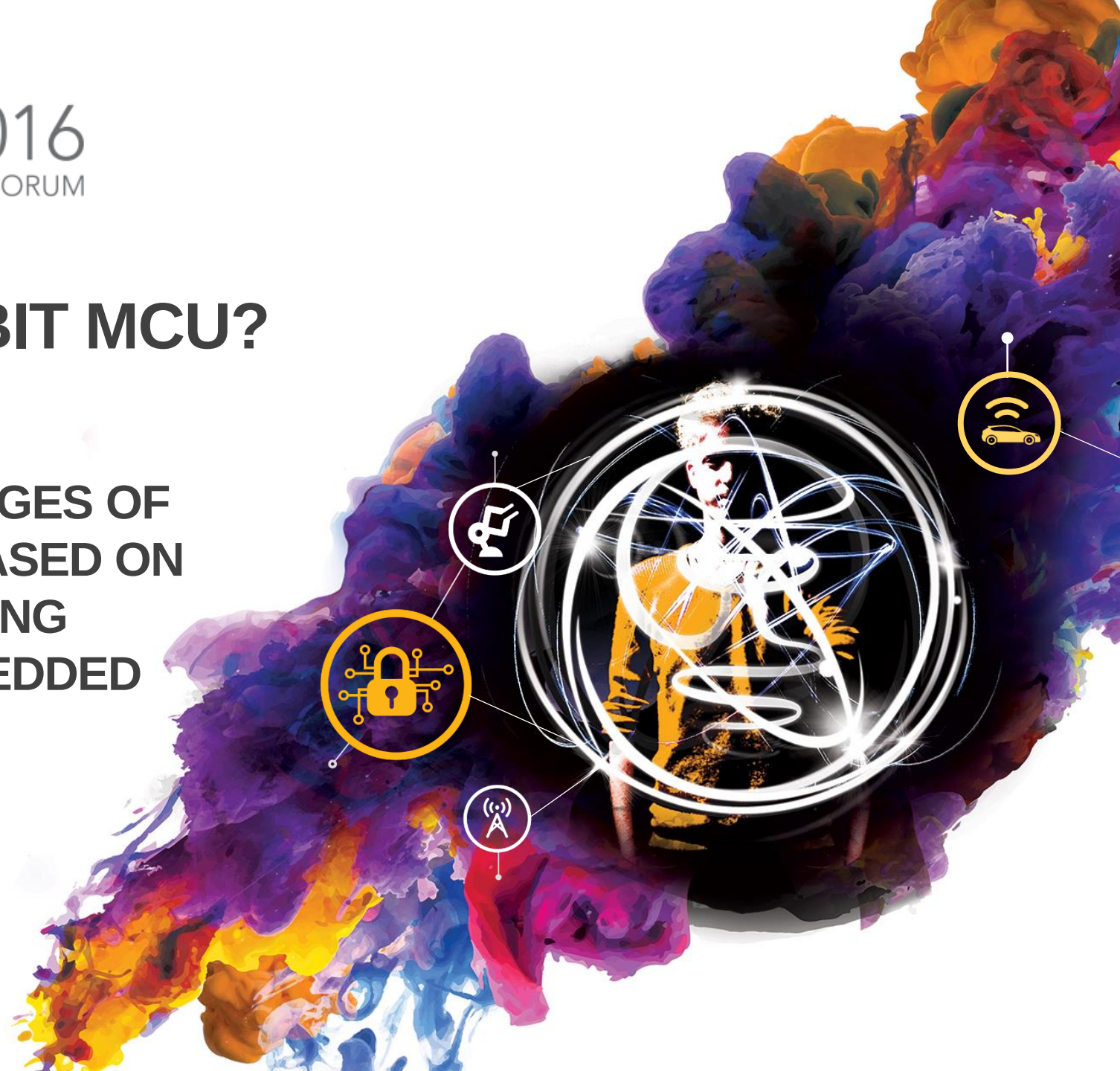
MAY 17, 2016



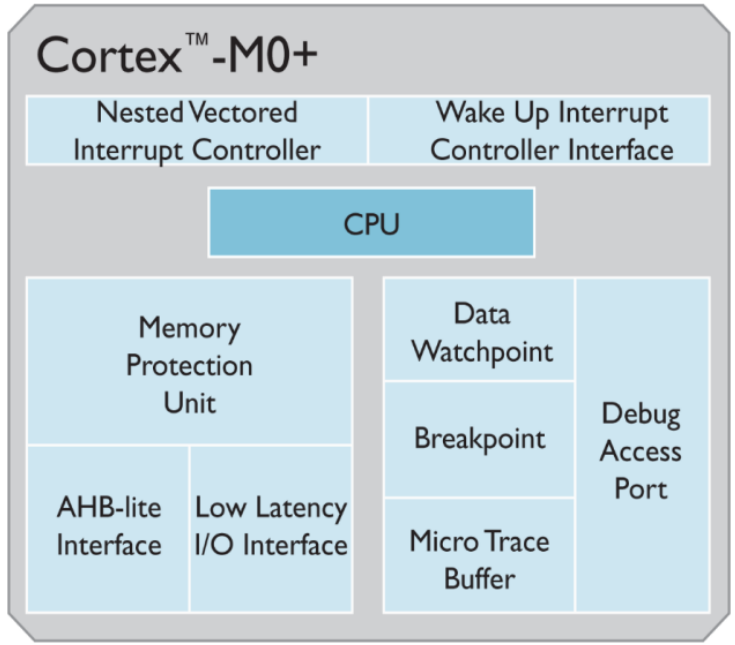
AGENGA

- LPC800 and LPC1100 Introduction
- Cortex-M0+ Introduction
- LPC1100 Technical Introduction
- LPC800 Technical Introduction
- LPC800 Tools and Support
- Questions

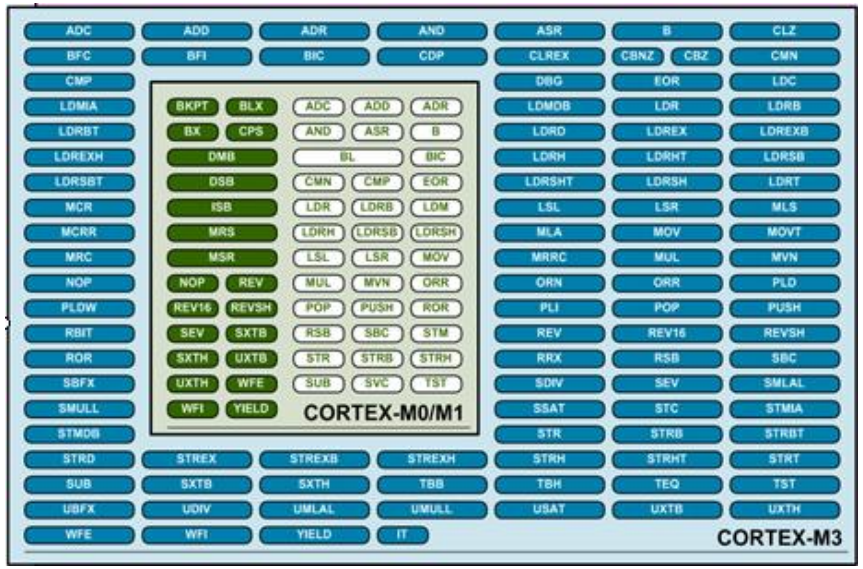
CORTEX-M0+/M0 OVERVIEW

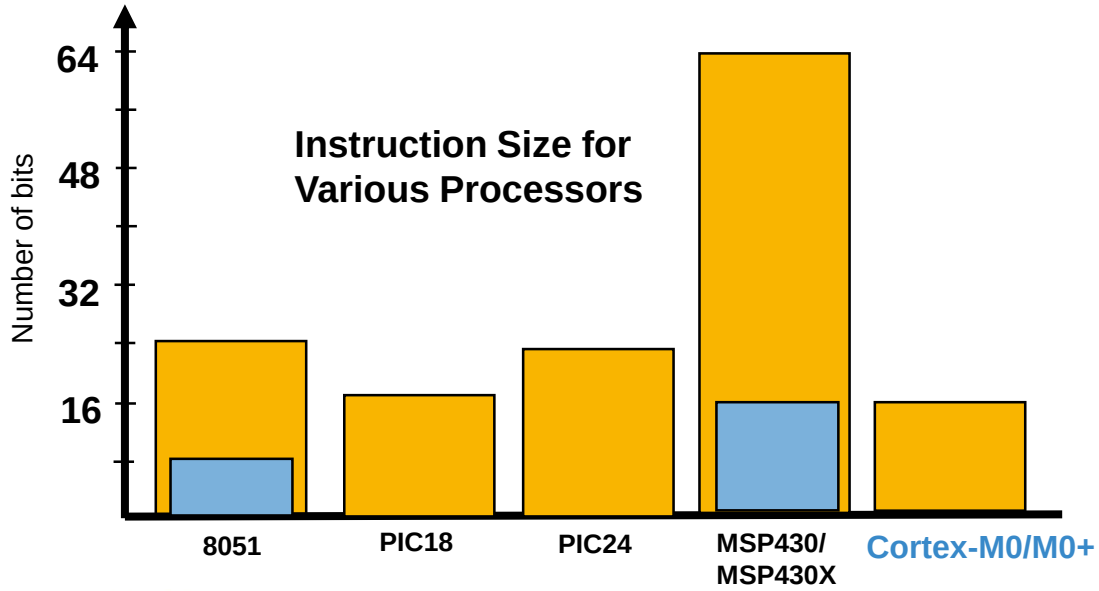
Cortex-M0+ Overview

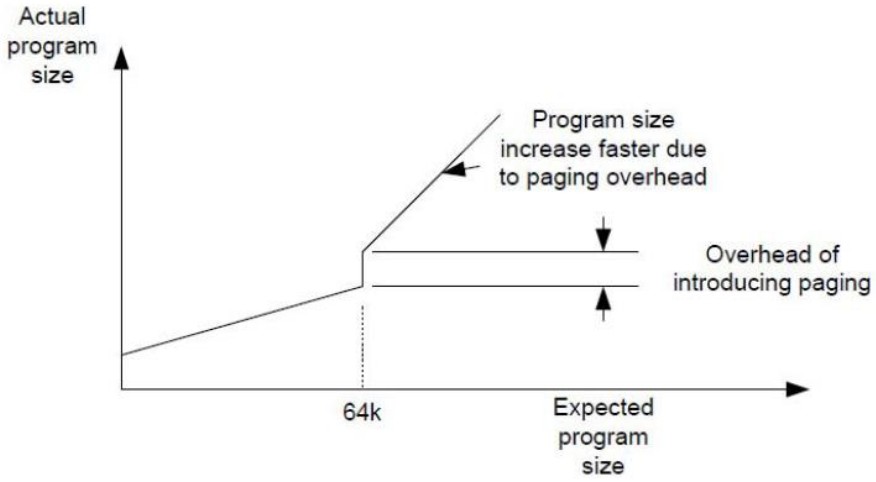
- High performance 32-bit CPU
- 2 stage pipeline
- Performance efficiency
  - 1.77 CoreMark/MHz - 0.93 DMIPS/MHz
- Deterministic operation
- Single cycle IO
- Built-in Nested Vectored Interrupt Controller (NVIC) with Wake-up Interrupt Controller (WIC)
- Debug using 2 pins with up to 4 breakpoints and 2 watchpoints
- Micro Trace Buffer (MTB)
- Vector Table relocation
- Thumb2 instructions (56 instructions)



Superior Code Density







- Leading to superior code density:
  - In Cortex-M0/M0+ all instructions (except BL) are **16 bits wide** instructions
  - **Over 64kB of address space,** 8- and 16- processors have to introduce paging, leading to extra overhead in code

Superior Code Density (e.g. 16-bit Multiply)

8-bit (8051)	16-bit (MSP430)	ARM Cortex-M0/M0+

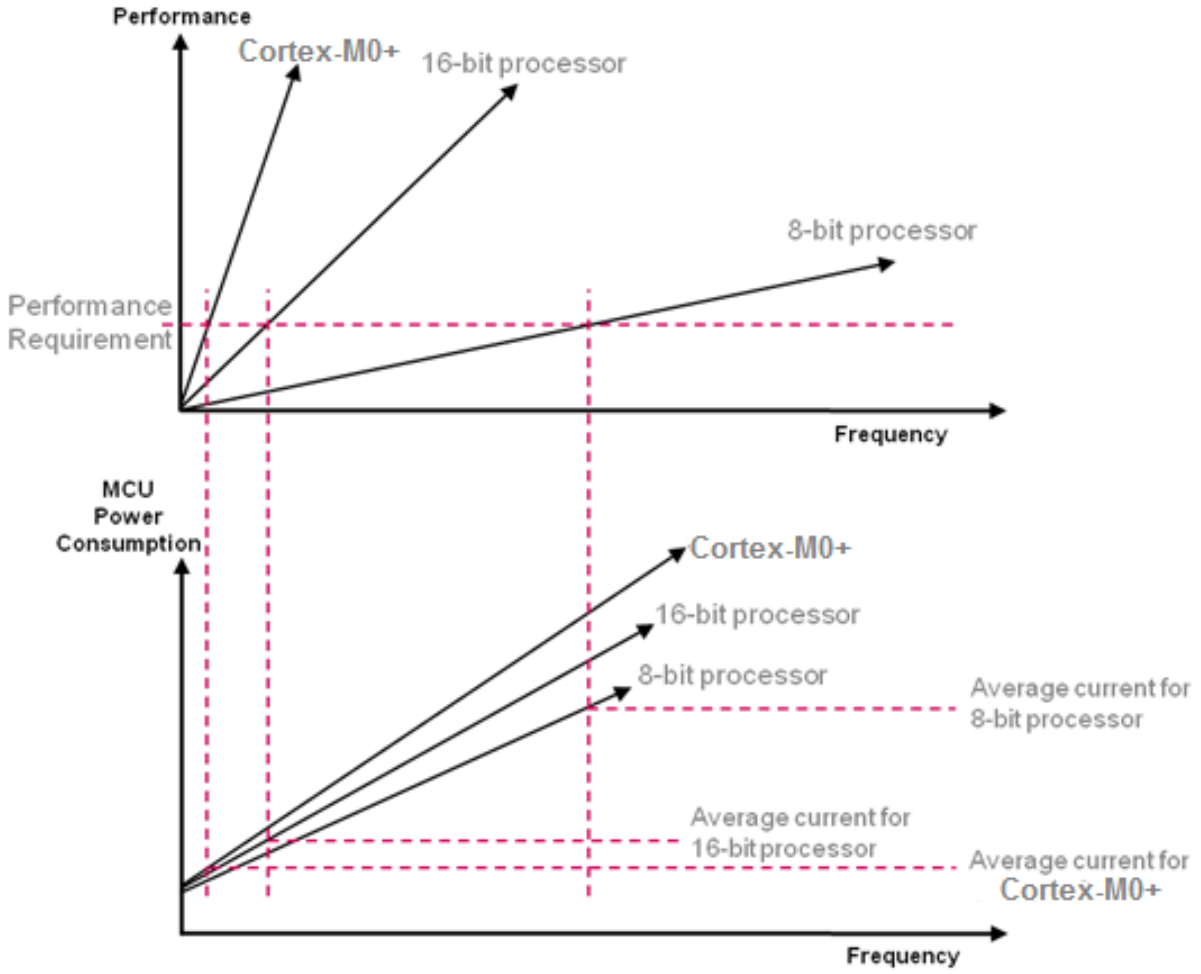
MOV A, XL; 2 bytes
MOV B, YL; 3 bytes
MUL AB; 1 byte
MOV R0, A; 1 byte
MOV R1, B; 3 bytes
MOV A, XL; 2 bytes
MOV B, YH; 3 bytes
MUL AB; 1 byte
ADD A, R1; 1 byte
MOV R1, A; 1 byte
MOV A, B ; 2 bytes
ADDC A, #0; 2 bytes
MOV R2, A; 1 byte
MOV A, XH; 2 bytes
MOV B, YL; 3 bytes
MUL AB; 1 byte
ADD A, R1; 1 byte
MOV R1, A; 1 byte
MOV A, B ; 2 bytes
ADDC A, R2; 1 bytes
MOV R2, A; 1 byte
MOV A, XH; 2 bytes
MOV B, YH; 3 bytes
MUL AB; 1 byte
ADD A, R2; 1 byte
MOV R2, A; 1 byte
MOV A, B ; 2 bytes
ADDC A, #0; 2 bytes
MOV R3, A; 1 byte
	MOV R4,&0130h
	MOV R5,&0138h
	MOV SumLo,R6
	MOV SumHi,R7
	(Operands are moved to and from a memory mapped hardware multiply unit)
		MULS r0,r1,r0

29 Instructions	**4 Instructions**	**1 Instruction**
Time: 48 instruction cycles **Code size: 48 bytes**	**Time: 8 clock cycles** **Code size: 8 bytes**	**Time: 1 clock cycle** **Code size: 2 bytes**

Cortex-M0/Cortex-M0+ Has Lower Power Consumption

- Cortex-M0/M0+ runs at a much slower clock frequency for the same required performance

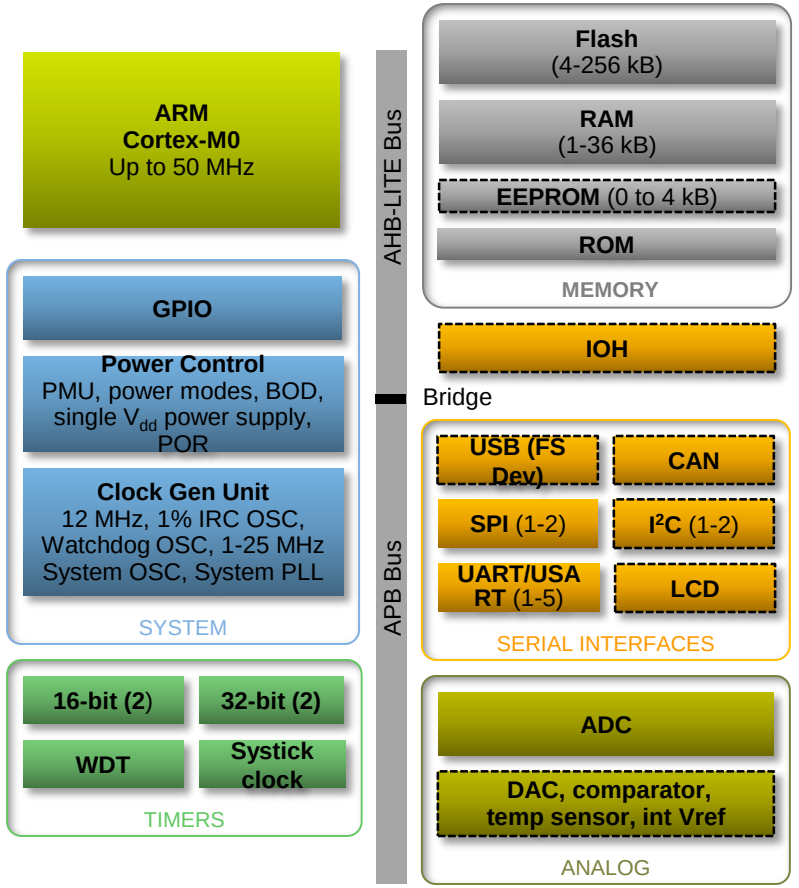
- Cortex-M0/M0+ can sleep most of the time, or it can handle additional tasks



LPC1100 TECHNICAL OVERVIEW

LPC1100 Family Block Diagram

- Cortex-M0+ processor, up to 50MHz
- Low Active Current 150 µA/MHz
- Single VDD power supply (1.8V to 3.6V)
- Memory
  - Up to 256 kB Flash, up to 36 kB RAM
  - ROM:
    USB, USART, I2C, Power Profile, integer divide, ISP/IAP Drivers, DMA drivers
- Wide range of connectivity options
  - LPC11xx: Basic control and serial connectivity
  - LPC11xxLV: Low voltage (1.8V VDD)
  - LPC 11Axx: 10-bit DAC, comparators
  - LPC11Cxx: CAN with/without integrated transceiver
  - LPC11Dxx: LCD display controller
  - LPC11Exx: EEPROM
  - LPC11Uxx: Full Speed USB device; certified ROM driver
- ADC, DAC and temperature sensor
- Innovative low-pin-count packages

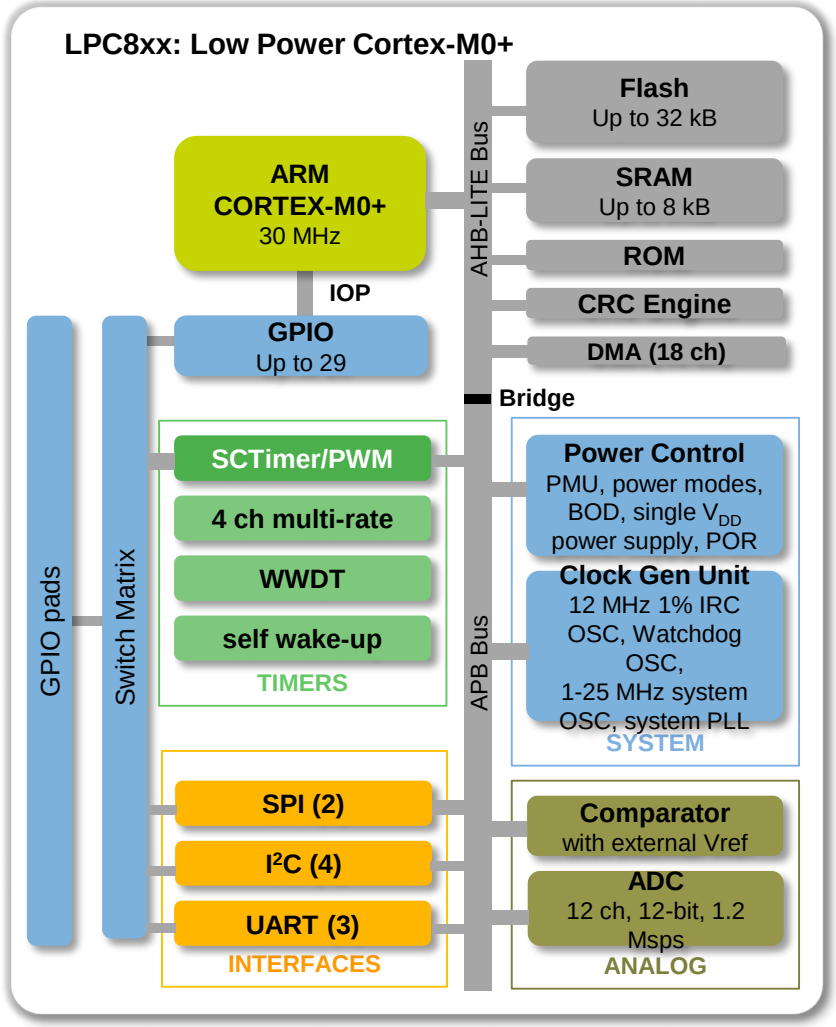


LPC800 TECHNICAL OVERVIEW

LPC81x and LPC82x Block Diagram

- Cortex-M0+ processor, up to 30MHz
- Low Active Current 100 µA/MHz
- Single VDD power supply (1.8V to 3.6V)
- Memory:
  - LPC81x - 16kB Flash, 4kB SRAM
  - LPC82x - 32kB Flash, 8kB SRAM
  - ROM:
    USART, I2C, Power Profile, integer divide (LPC82x), ISP/IAP Drivers, SPI (LPC82x), ADC (LPC82x)

- Peripherals:
  - Switch matrix for peripheral configurations
  - SCTimer/PWM
  - Pattern matching engine (GPIO)
  - 3 USART, 2 SPI, up to 4 I2C
  - Comparator with external Vref
  - 4-channel Multi-Rate Timer (MRT)
  - Self wake-up timer, Systick timer, Watchdog timer
  - High-speed GPIO with up to 29 GPIOs
  - 1.5% accuracy, 12 MHz IRC oscillator
  - 12-bit ADC with up to 12 channels (LPC82x)
  - DMA with 18 channels and 9 trigger inputs (LPC82x)
- LPC81x - TSSOP16/20, SO20 and DIP8
- LPC82x - HVQFN33, and TSSOP20



LPC800 CLOCK GENERATION UNIT

LPC800 Clock Generation Unit

Clock Sources	Characteristics
IRC Oscillator	System clock by default Stable power up and power down 12 MHz (±1.5% over specified temperature and voltage)
Watchdog Oscillator	Low power operation Low frequency oscillator 9.3 kHz – 2.3 MHz (+/- 40%)
MAIN Oscillator	1 MHz – 25 MHz
CLKIN	1 MHz – 25 MHz
SYS PLL	Multiplies the clock source (IRC, Main Osc, CLKIN) Up to 100 MHz and divide down to 30 MHz or less
Low Power Oscillator	Low power operation Low frequency oscillator 10 kHz (+/- 40%)

LPC800 GPIO

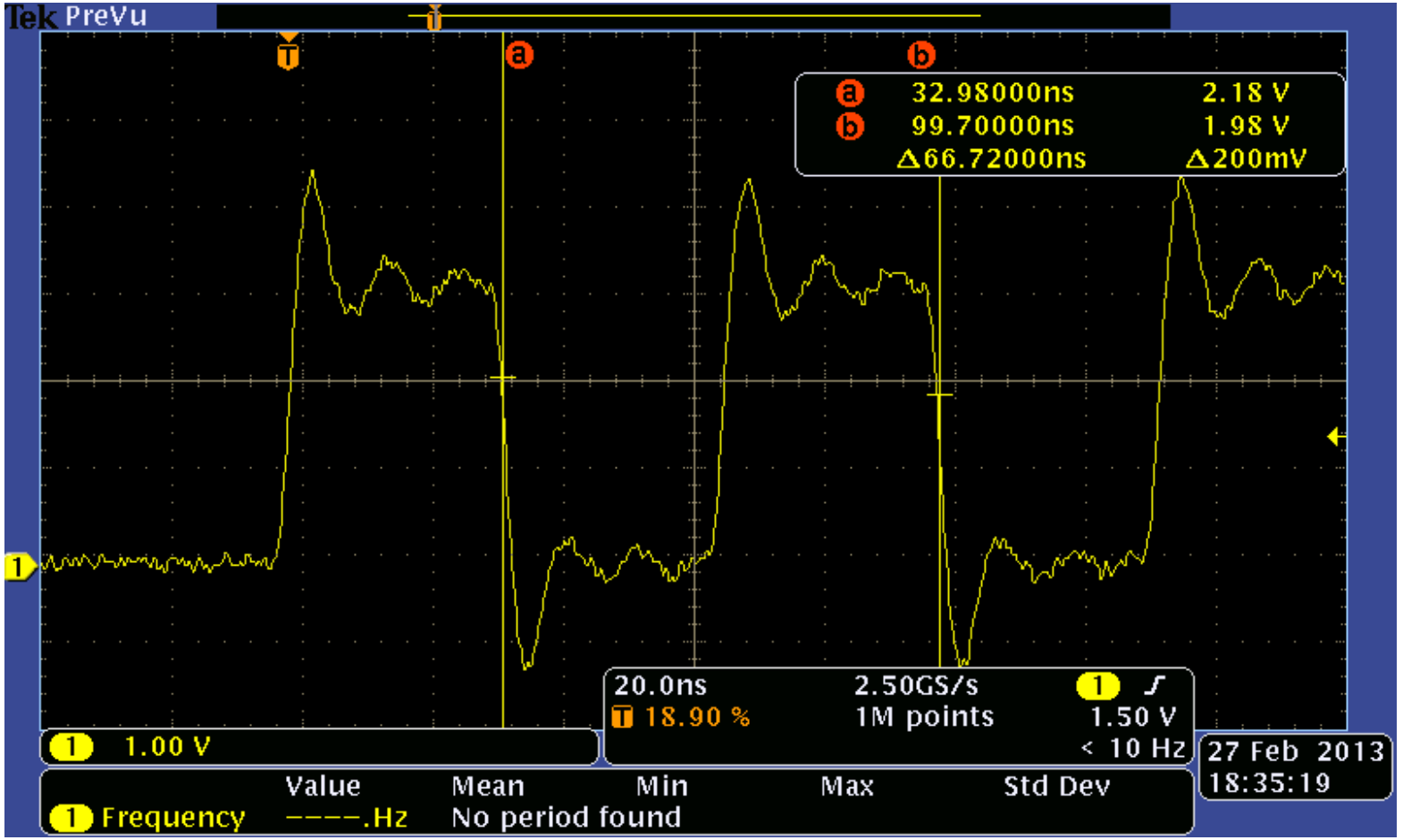
LPC800: Flexible I/O Port

- I/O Port
  - Up to 29 GPIOs
  - **Single cycle** access to all port pins
  - **Support high frequency I/O toggling** – As fast as CPU_Clock/2 = 15MHz!
  - **Enhanced GPIO Pin Manipulation** – Capable of simultaneously reading Bit/Byte/Word or toggling up to 29 I/Os per instruction
  - Up to 8 pins can be selected from all GPIO pins as edge- or level-sensitive **interrupt** requests
  - **Programmable** Internal pull-up/pull-down resistor, open-drain function, input inverter, and repeater mode
  - All GPIO pins are equipped with a **programmable digital glitch filter**. The filter rejects input pulses with a selectable duration of shorter than one, two, or three cycles of a filter clock
  - High-current source output driver (20 mA) on four pins
  - High-current sink driver (20 mA) on two true open-drain pins

Enhanced GPIO Pin Manipulation

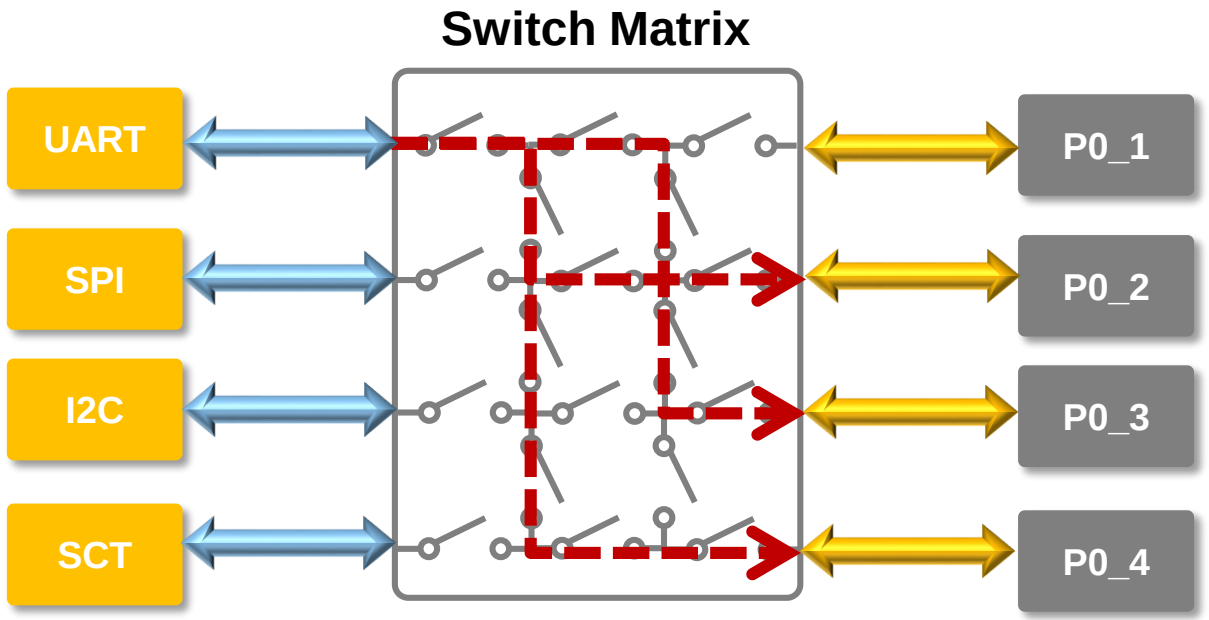
- **Support high frequency I/O toggling** – as fast as CPU_Clock/2= 15MHz!

- This scope trace shows the single cycle IO port access allowing 15 MHz with a core clock of 30 MHz



Switch Matrix

- **Movable functions**
  - Can be assigned to any external pin that is not power or ground
  - UART, SPI, I²C, SCT, comparator output, CLKOUT, pattern match output
- **Fixed pin functions**
  - Oscillator pins, comparator input, GPIOs
  - Can be replaced by movable functions



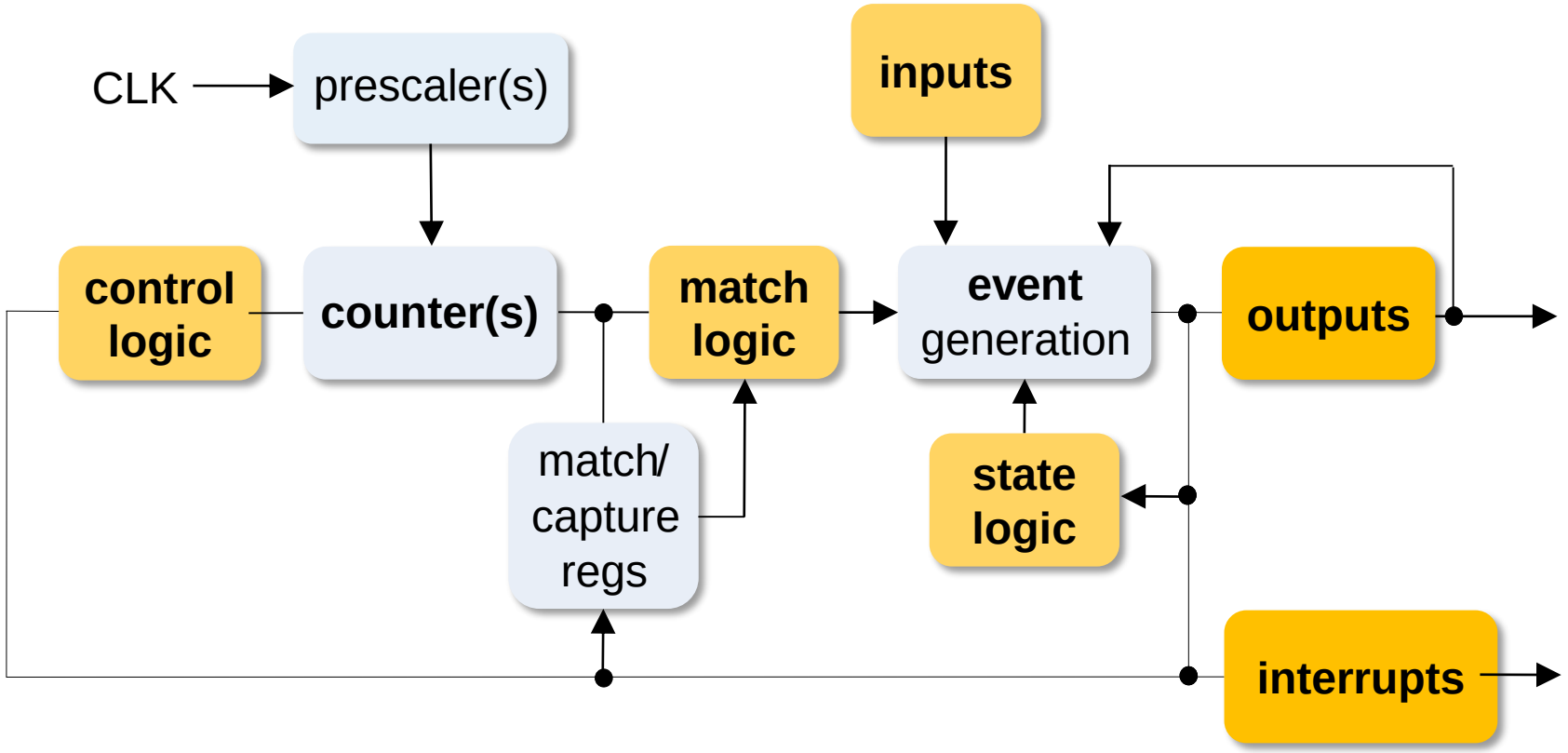
LPC800 PERIPHERALS

Timers

- Multi-Rate timer (MRT)
  - Timer with four independent channels
  - Each channel can generate interrupts
    - Repeat interrupt mode
    - One-shot interrupt mode
- Self wake-up timer (WKT)
  - A non-zero value in this 32-bit timer initiates a countdown sequence. Wake-up source from low-power modes
- Windowed watchdog timer (24-bit timer)
- Systick Timer (24-bit timer)

State Configurable Timer/PWM (SCTimer/PWM)

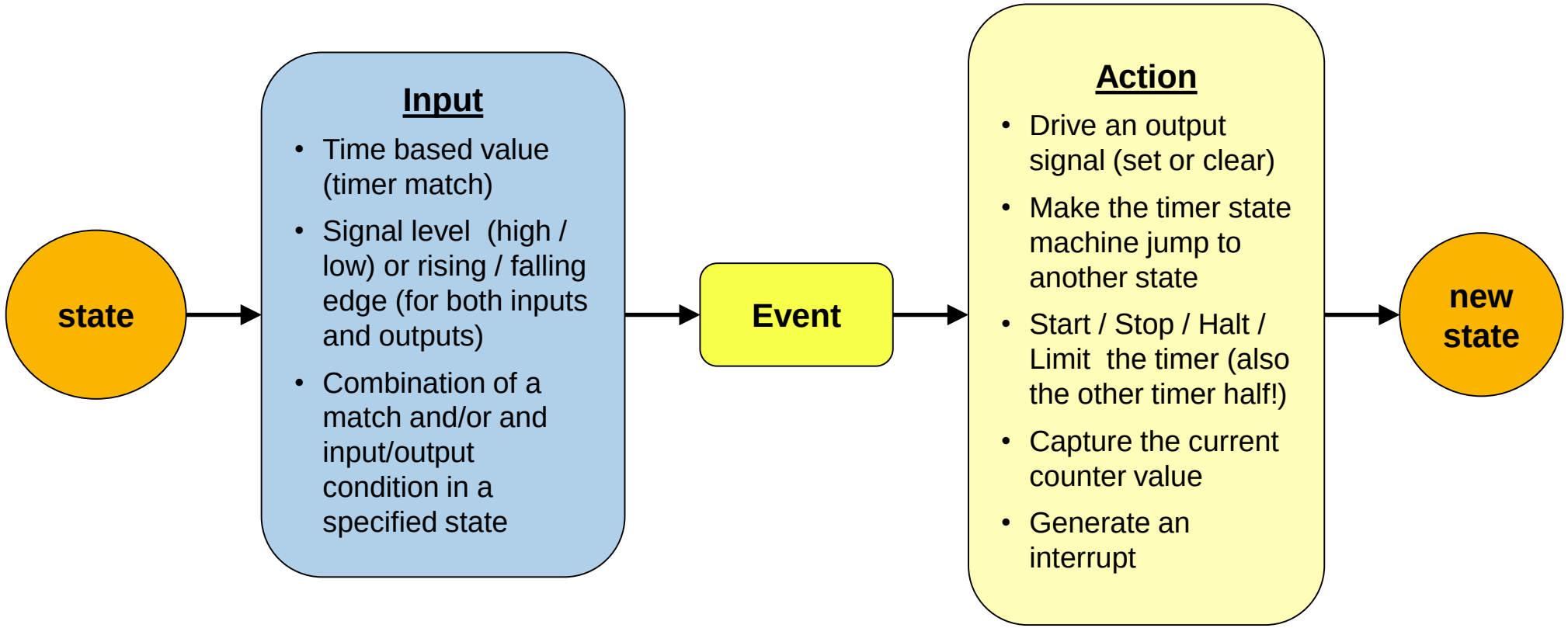
- State Configurable Timer/PWM (SCTimer/PWM) is a timer/capture unit coupled with a highly flexible event driven state machine block.
- Can be configured as 32-bit counter or two 16-bit counters with a configurable state machine



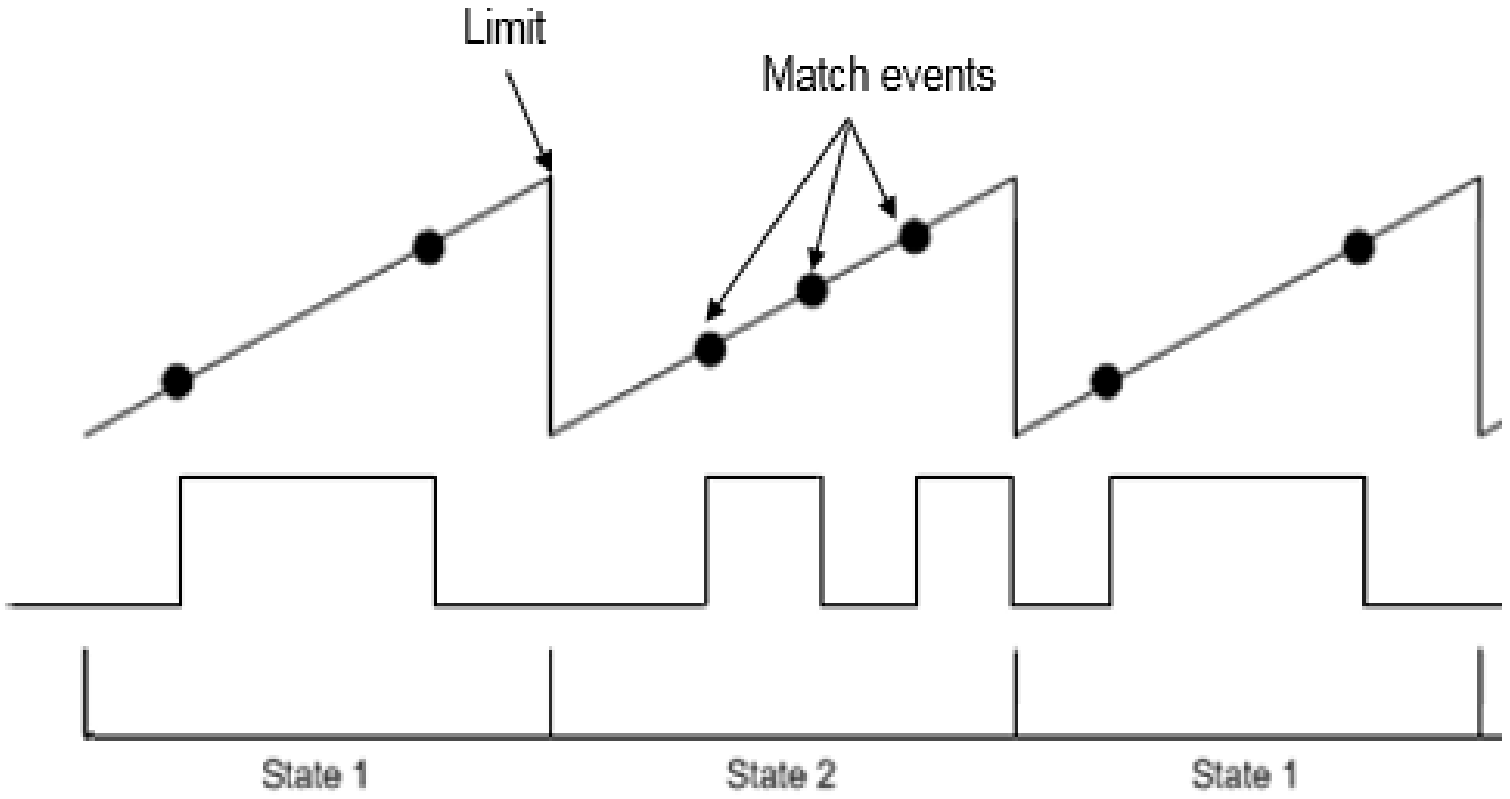
State Configurable Timer/PWM (SCTimer/PWM)

- Allows a wide variety of timing, counting, output modulation, and input capture operations
- Key Features:
  - 4 inputs
  - 4 outputs
  - 5 match/capture registers
  - 6 events with state machine support
  - 2 states

How Does the SCT Work?



SCTimer/PWM – Examples



2-channel PWM with Dead-time Control Using SCT

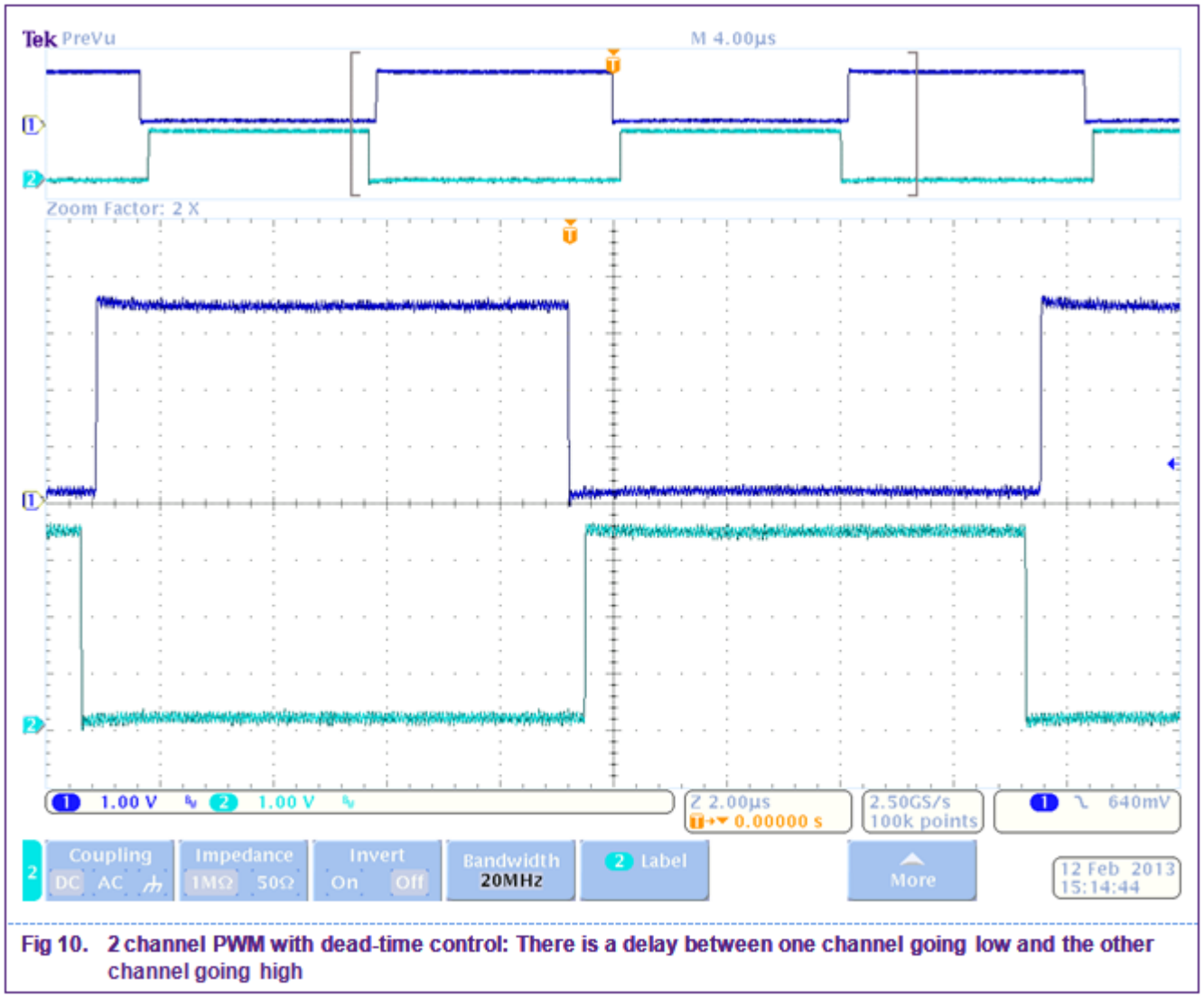


Fig 10. 2 channel PWM with dead-time control: There is a delay between one channel going low and the other channel going high

SCTimer/PWM Cookbook

- Collection of code examples (both LPCXpresso and Keil)
- Each code example summarized in Cookbook document
- Available so far (and more to follow):
  - SCT_blinky_irq : generate 10 msec timer tick
  - SCT_blinky_match : toggle output every 10 msec
  - SCT_match_toggle : same using conflict resolution
  - SCT_pwm : generate PWM output
  - SCT_pwm_um : PWM with two different duty cycles
  - SCT_pwm_deadtime : PWM and dead time generation (for HB control)
  - SCT_pwm_4ch : 4 channel PWM + abort input
  - SCT_pwm_decode : pulse width measurement
  - SCT_rc5_send : modulate RC5 code at 36 kHz carrier
  - SCT_rc5_receive : decode RC5 frame (Manchester coding)

State Configurable Timer/PWM (SCTimer/PWM)

- Implements virtually any timing or PWM function found on popular 8-bit MCUs without loading the CPU
  - Wide variety of counting, output, input, and control operations
  - Dead time insertion
  - High resolution PWMs
- GUI-based configuration tool (Redstate)
  - Integrated into LPCXpresso
  - Choose pre-configured timing functions or build your own

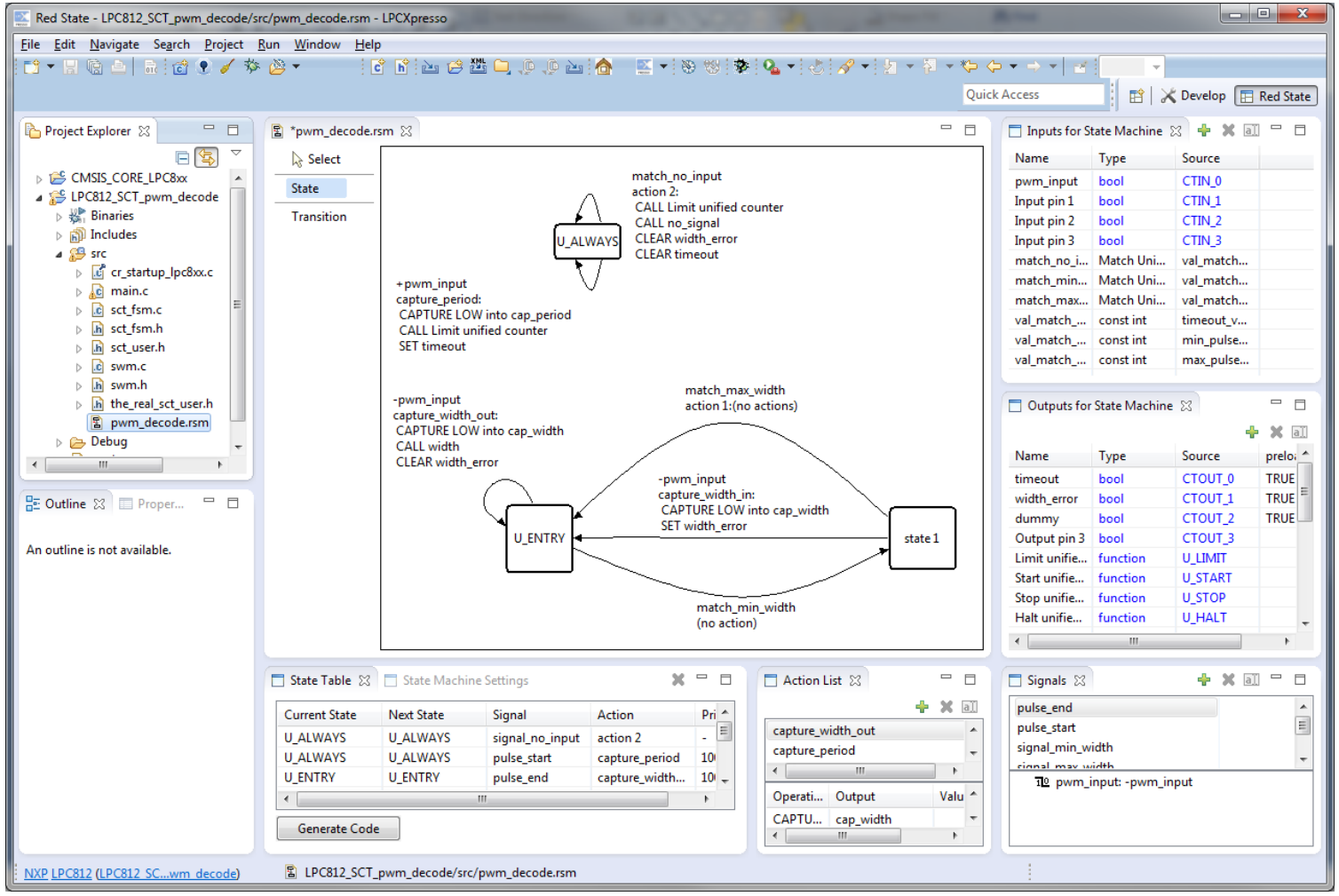
Motor Control PWM
Generating PWM outputs with programmable dead-time

Lighting
Modulated PWM outputs, reaction to lamp sensor

Custom sampling of input signals for:
- Frequency detection
- Pulse width detection
- Phase detection

Custom control signals in hardware:
- Clock or signal gating
- Complex modulation of outputs
- Pulse sequences

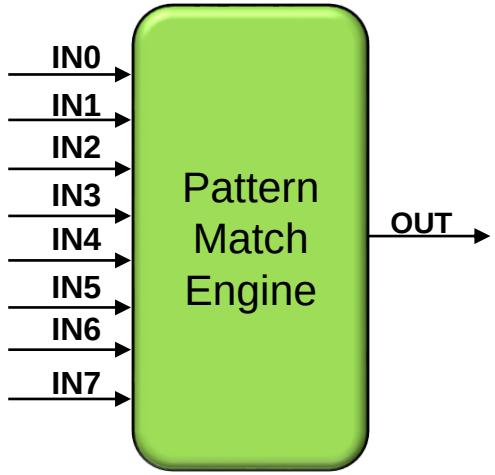
Red State – Graphical SCT Configuration Tool



Pattern Match Engine (PME)

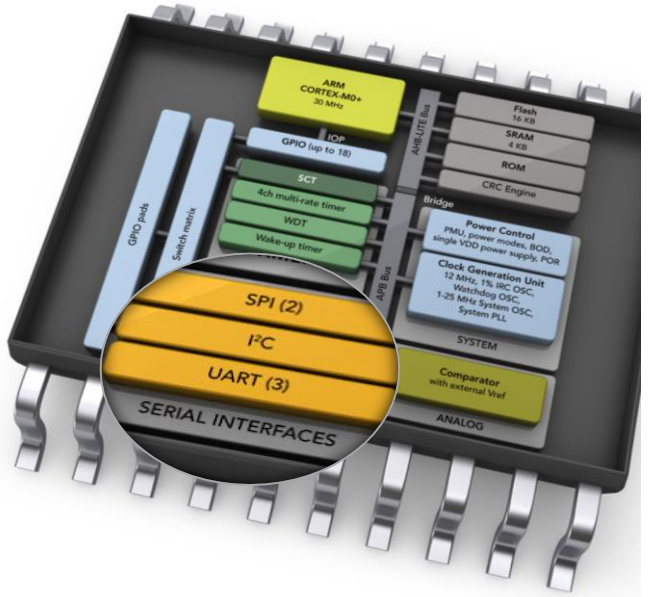
- Pin Interrupt generator
  - Up to 8 pins can be selected to generate interrupts to the core
- Pattern match feature
  - The same 8 pins (above) can be selected from all GPIO pins to contribute to a Boolean expression
- Example:
  `(IN0)~(IN1)(IN3)^+(IN4)(IN5)+(IN0)~(IN3)~(IN4)`

  `where: ~=low; ^=rising edge; +=OR`
  - The PME keeps polling these pins and generates an interrupt to the core when one or more of the bit slices match
- Both the pin interrupt and pattern match blocks are mutually exclusive



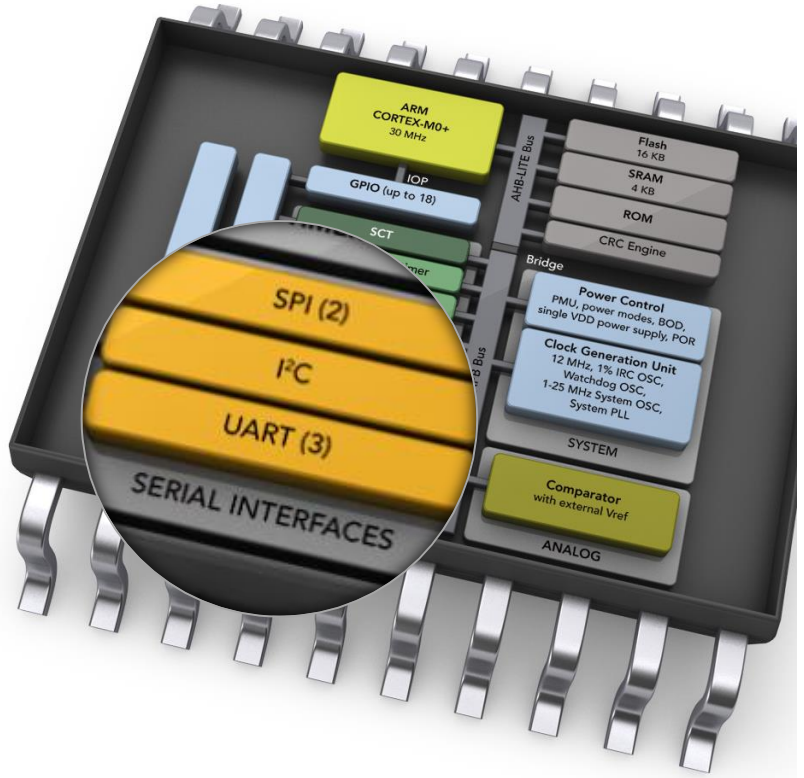
USART

- Synchronous operations on all 3 UARTs
- Maximum bit rates of 1.875 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode for USART functions
- *ROM drivers to configure USART*
- 7, 8, or 9 data bits and 1 or 2 stop bits
- Multiprocessor/multi-drop (9-bit) mode with software address compare
- Parity generation and checking: odd, even, or none
- RTS/CTS for hardware signaling for automatic flow control
- Fractional rate divider is shared among all USARTs
- Built-in baud rate generator
- Wake from sleep, deep-sleep, or power-down mode



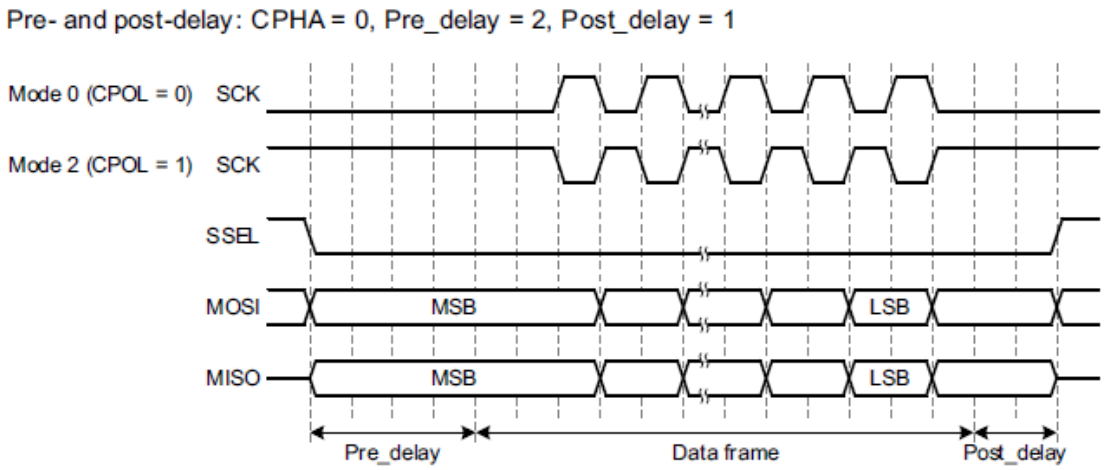
I²C

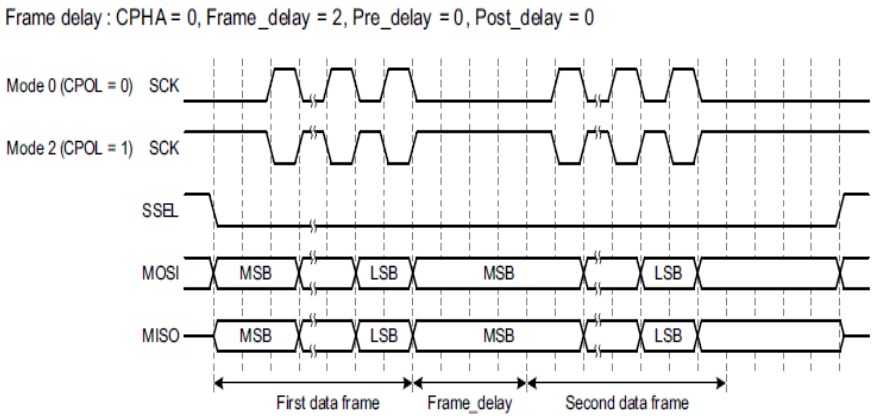
- I²C operation can be routed to dedicated open-drain pins (by routing the functions using switch matrix), or any other pin
- Fast-mode Plus (up to 1Mbit/s) capability on the open-drain pins
- Not software compatible with I²C in other devices in the LPC portfolio
- Independent master, slave, and monitor functions
- Time-out register
- ROM drivers to configure I²C
- Wake-up from low power modes from I²C interrupt



SPI

- Maximum data rate of 30 Mbit/s in master and 25 Mbit/s in slave
  - Programmable pre and post delays
  - Programmable frame delay
  - ROM drivers to configure the SPI
  - Wake from sleep, deep-sleep, or power-down mode





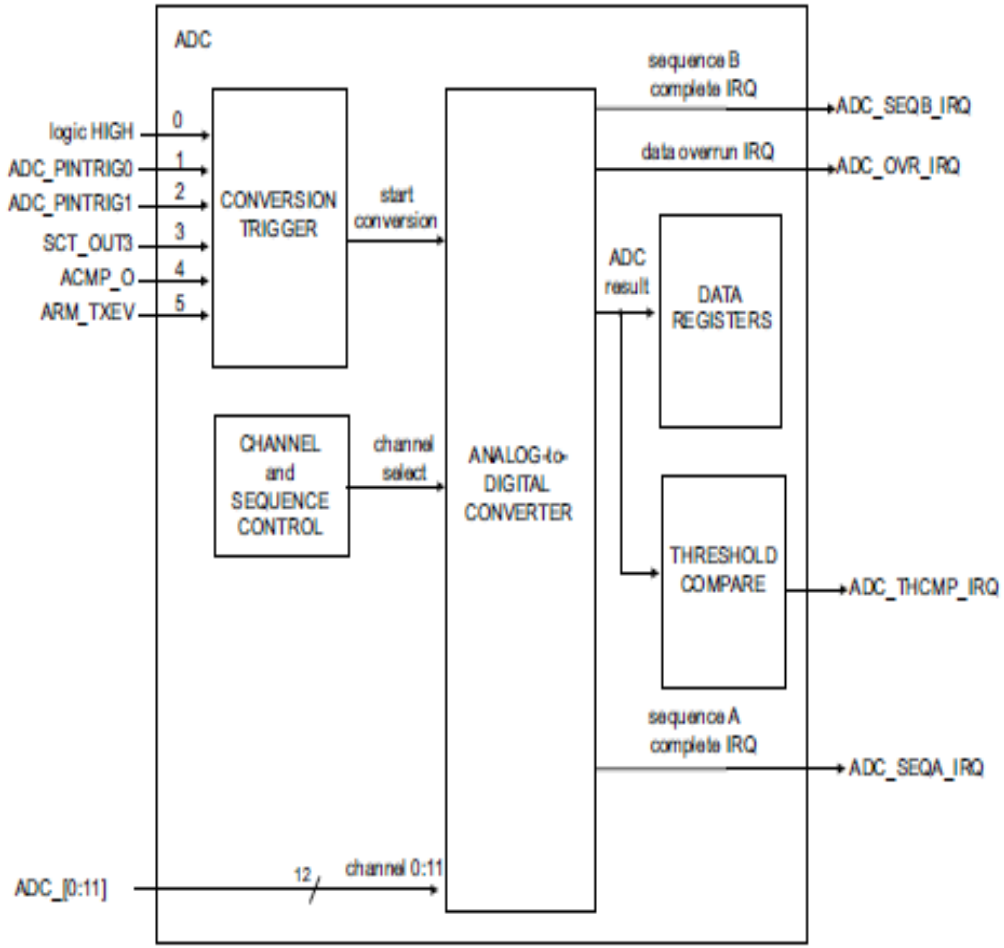
DMA

- 18 channel DMA: all connected to peripheral request inputs and outputs
  - 18 sources from USART, SPI and I2C peripherals
  - SCT request 0&1, ADC sequence A&B, ACMP, pin interrupt 0&1
- Supports single transfers up to 1024 words
- Operates in sleep mode
- Priority is user selectable for each channel
- Continuous priority arbitration
- Address cache with four entries
- Address increment options allow packing and/or unpacking data

LPC800 ANALOG

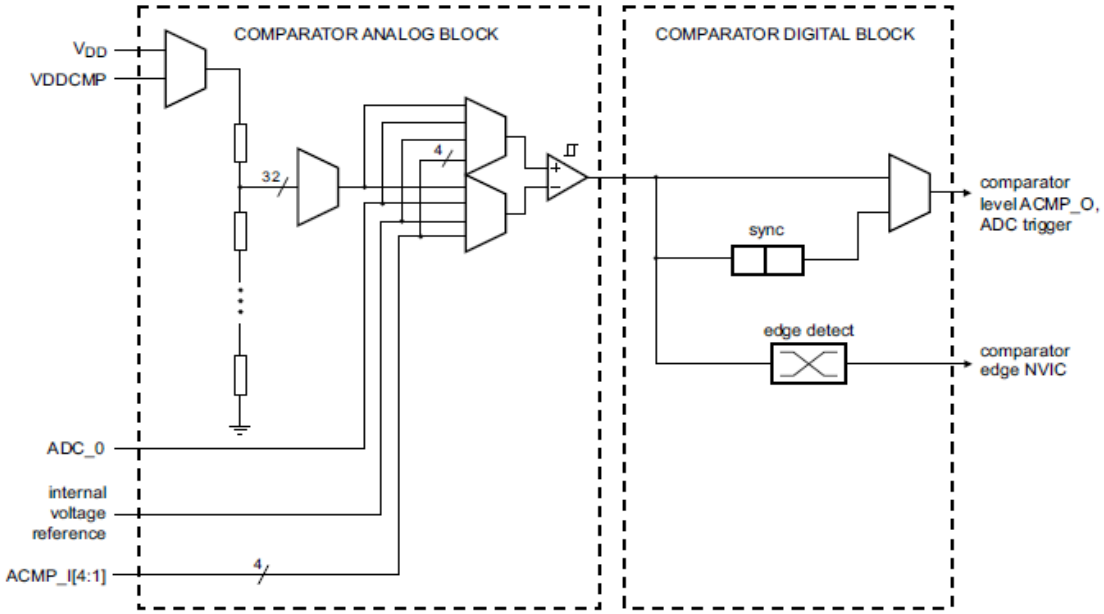
Analog to Digital Converter

- 12-bit successive approximation
- Input multiplexing among 12 pins and one internal source
- 12-bit conversion rate up to 1.2 Msps
- Two configurable conversion sequences with independent triggers
- Optional automatic high/low threshold comparison and “zero crossing” detection
- Power down mode and low-power operating mode
- Burst conversion mode for single and multiple inputs
- DMA support



Analog Comparator

- Compares voltage levels on external pins and internal voltages
- 4 inputs are multiplexed separately to the positive voltage input and negative inputs
- The Internal voltage reference (0.9 V bandgap reference) can be used as either the positive or negative input of the comparator
- Voltage ladder source selectable between the supply pin VDD or VDDCMP pin
- 32 levels of Comparator reference voltage for fine grain comparison
- Edge and level Comparator output signals connected to State Configurable Timer (SCT) using the Switch matrix, allows for the recording of event comparison – “timestamps”



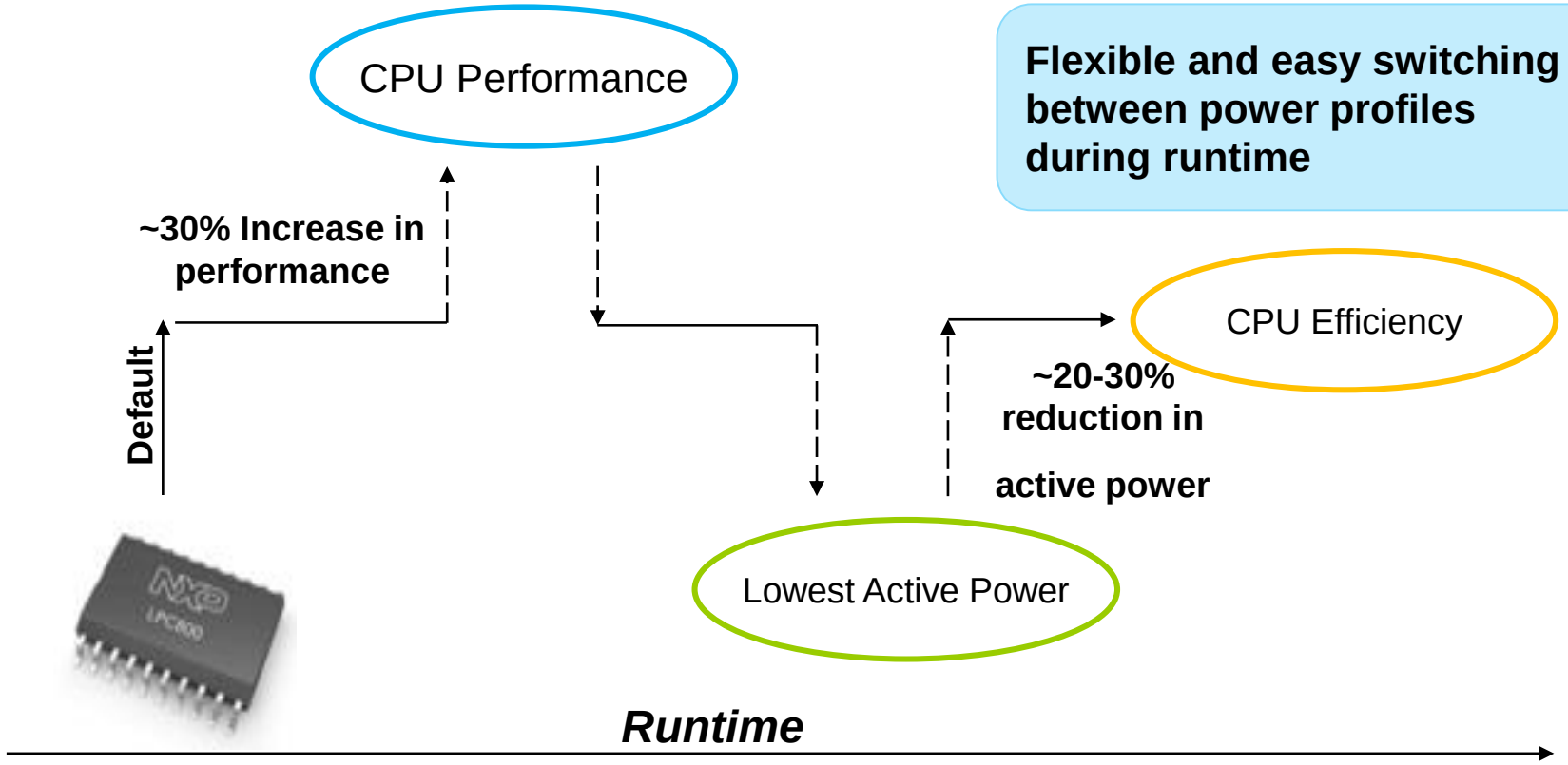
LPC800 ROM DRIVERS

ROM Drivers

- On-chip ROM contains the boot loader and the following application programming interfaces (API):
  - In-system programming (ISP) and in-application programming (IAP) support for flash programming
  - USART driver API routines
    - Send or receive characters using any of the USART blocks in asynchronous mode
  - I^2C-bus driver API routines
    - Send or receive data on the I2C bus in master and slave modes
  - SPI drivers (LPC82x)
    - Control multiple SPI slave devices through this standardized API
  - ADC drivers (LPC82x)
    - ADC calibration, triggered AD conversions and Interrupt handling
  - Power profiles for optimizing power consumption and PLL settings
  - Integer divide routines

Power Profiles

- An easy-to-use API driven interface for dynamic current management at runtime
- Application can be focused towards:



Power Profile Results
Using Keil v4.70

Power Profile	12 MHz			24 MHz		
	Current (mA)	CoreMark	CoreMark/ MHz	Current (mA)	CoreMark	CoreMark/ MHz
Default	2.50	16.88	1.41	4.40	33.76	1.41
CPU Performance	1.98	24.62	2.05	4.27	49.24	2.05
Efficiency	1.98	24.62	2.05	4.27	49.24	2.05
Low Current	1.56	12.93	1.08	3.15	25.85	1.08

- **Note:**
  - The current consumption is improved by using Power Profiles
  - The CoreMark scores are improved by using Power Profiles

CoreMark Benchmark Results (EEMBC)

Processor	CoreMark/MHz	CoreMark
NXP LPC800* (24 MHz)	2.05	49.24
Atmel ATmega644 (20 MHz)	0.54	10.81
Microchip PIC24FJ64 (32MHz)	0.75	23.87
TI MSP430F5438A (25 MHz)	0.78	19.56

http://www.coremark.org/benchmark/index.php?pg=benchmark

*Not yet uploaded to CoreMark website

LPC800 LOW POWER MODES

LPC800 Low Power Modes

Low Power Mode	Impact	Wake-Up Sources	Current Consumption
Sleep	System Clock to Cortex-M0+ is stopped. Peripherals and memories are active. Processor state and registers, peripheral registers, and internal SRAM are maintained, and the logic levels of the pins remain static	Any peripherals interrupts (SCT, MRT, USART, SPI, I2C, CMP) Pin interrupts & Pattern Match Engine BOD interrupt and reset WWDT interrupt and reset External Reset Self Wake-up Timer	600 µA *
Deep Sleep	Peripherals receive no internal clocks. Flash is in stand-by mode. Peripherals and memories are active. Processor state/registers, peripheral registers, and internal SRAM contents are maintained, and the logic levels of the pins remain static	Interrupts from USART, SPI, I2C Pin interrupts BOD interrupt and reset WWDT interrupt and reset External Reset Self Wake-up Timer	170 µA
Power-Down	Peripherals receive no internal clocks. The flash memory is powered down. Processor state/registers, peripheral registers, and internal SRAM contents are maintained, and the logic levels of the pins remain static	Interrupts from USART, SPI, I2C) Pin interrupts BOD interrupt and reset WWDT interrupt and reset External Reset Self Wake-up Timer	1.8 µA
Deep Power-Down	The entire system is shut down except for four 32-bit general purpose registers in the PMU and the self wake-up timer. Register states and internal SRAM contents are lost	Wake up on a pulse on the WAKEUP pin or when the self wake-up timer times out. On wake-up, the part reboots.	220 nA

** 12 MHz, peripherals disabled, low current mode*

LPC800 MEMORY

Memory Block

- Flash: 1kB sectors with 64-byte page program/erase

Sector number	Sector size [kB]	Page number	Address range	4 kB	8 kB	16 kB
0	1	0 -15	0x0000 0000 - 0x0000 03FF	yes	yes	yes
1	1	16 - 31	0x0000 0400 - 0x0000 07FF	yes	yes	yes
2	1	32 - 47	0x0000 0800 - 0x0000 0BFF	-	yes	yes
3	1	48 - 63	0x0000 0C00 - 0x0000 0FFF	-	yes	yes
4	1	64 - 79	0x0000 1000 - 0x0000 13FF	-	yes	yes
5	1	80 - 95	0x0000 1400 - 0x0000 17FF	-	yes	yes
6	1	96 - 111	0x0000 1800 - 0x0000 1BFF	-	yes	yes
7	1	112 - 127	0x0000 1C00 - 0x0000 1FFF	-	yes	yes
8	1	128 - 143	0x0000 2000 - 0x0000 23FF	-	yes	yes
9	1	144 - 159	0x0000 2400 - 0x0000 27FF	yes	yes	yes
10	1	160 - 175	0x0000 2800 - 0x0000 2BFF	yes	yes	yes
11	1	176 - 191	0x0000 2C00 - 0x0000 2FFF	yes	yes	yes
12	1	192 - 207	0x0000 3000 - 0x0000 33FF	yes	yes	yes
13	1	208 - 223	0x0000 3400 - 0x0000 37FF	yes	yes	yes
14	1	224 - 239	0x0000 3800 - 0x0000 3BFF	yes	yes	yes
15	1	240 - 255	0x0000 3C00 - 0x0000 3FFF	yes	yes	yes

Code Read Protection Levels

- Four levels of the Code Read Protection
- This feature allows user to enable different levels of security in the system so that access to the on-chip flash and use of the SWD and ISP can be restricted
- When needed, CRP is invoked by programming a specific pattern into a dedicated flash location
- Program CRP pattern at location @2FC

	Read Code	Full Chip Erase	Erase Sectors	Program Sectors	SWD Access
NO CRP	**Enabled**	**Enabled**	**Enabled**	**Enabled**	**Enabled**
CPR 1	Disabled	**Enabled**	**Enabled**	**Enabled**	Disabled
CRP 2	Disabled	**Enabled**	Disabled	**Enabled**	Disabled
CRP 3	Disabled	Disabled	Disabled	Disabled	Disabled
NO_ISP	No Protection (SWD can read)	Disabled	Disabled	Disabled	**Enabled**

Cyclic Redundancy Check (CRC) Engine

- Supports three common polynomials CRC-CCITT, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Accept any size of data width per write: 8, 16 or 32-bit
  - 8-bit write: 1-cycle operation
  - 16-bit write: 2-cycle operation (8-bit x 2-cycle)
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle)

LPC800 DEBUG MODULE

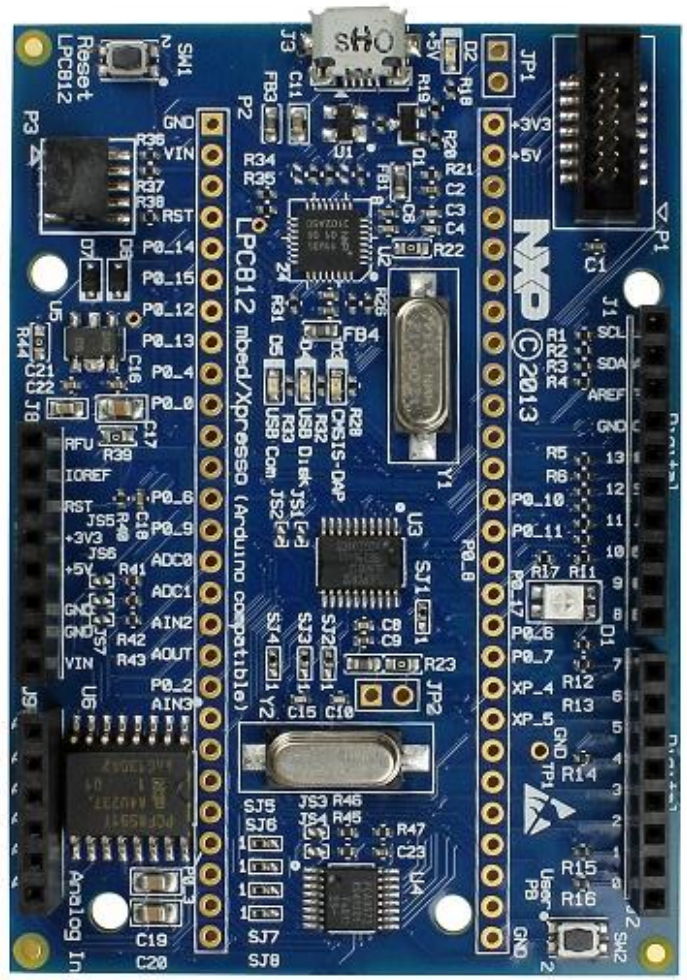
Emulation and Debugging

- Debug and trace functions are integrated into the ARM Cortex-M0+
- Serial wire debug (SWD: 2 pins)
- Supports up to four breakpoints and two watchpoints
- Micro Trace Buffer (MTB) supported
- Standard JTAG pins (5 pins) supports ONLY boundary scan testing

LPC800 TOOLS AND SUPPORT

LPCXpresso812MAX* (OM13055)

- LPC812 in TSSOP20 package
- Works with LPCXpresso IDE, Keil, IAR and other 3rd party tools
- mbed compatible
- On-board CMSIS-DAP debug probe or optional external probe (e.g. J-Link, LPC-Link2, ULINK etc.)
- Arduino UNO R3-compatible expansion
- Original mbed/LPCXpresso connectors
- RGB user LED
- User push button

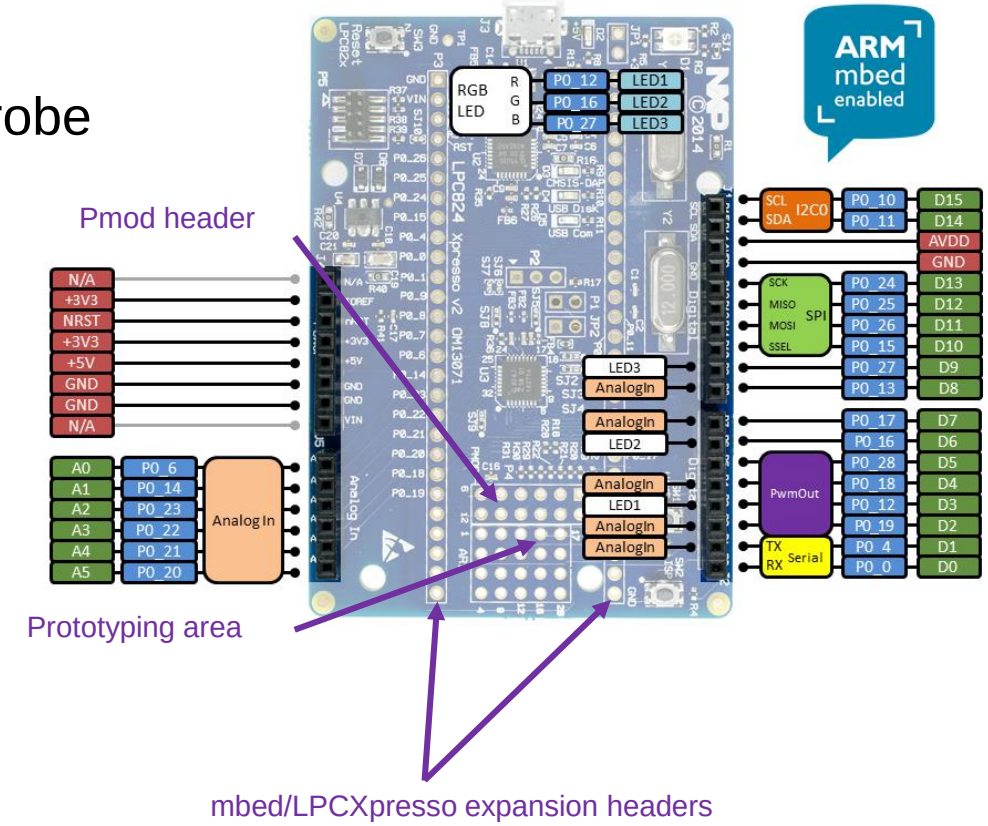


*Originally known as LPC800MAX

End customer price: ~$18.75 USD
Order: OM13055
Information: http://www.nxp.com/demoboard/OM13055.html

LPCXpresso824MAX Development Board (OM13071)

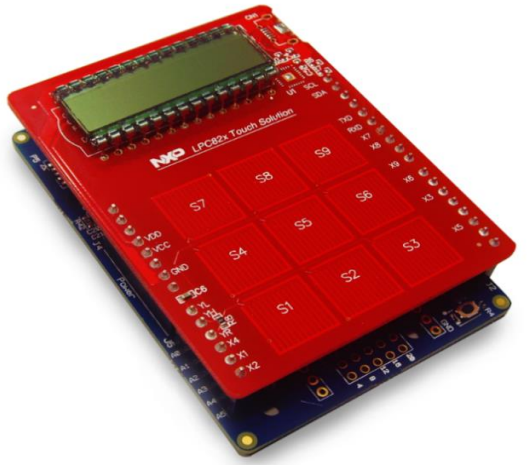
- LPC824 in HVQFN33 package
- Works with LPCXpresso IDE, Keil, IAR and other 3rd party tools
- mbed enabled platform
- On-board CMSIS-DAP debug probe or optional external probe (e.g. J-Link, LPC-Link2, ULINK etc.)
- Expansion options
  - Arduino UNO R3-compatible connectors
  - Original mbed/LPCXpresso connectors
  - Pmod header
  - Prototyping area
- Other features
  - RGB user LED
  - (UART) ISP and Wake buttons
  - Virtual com port (Target UART connection via USB)

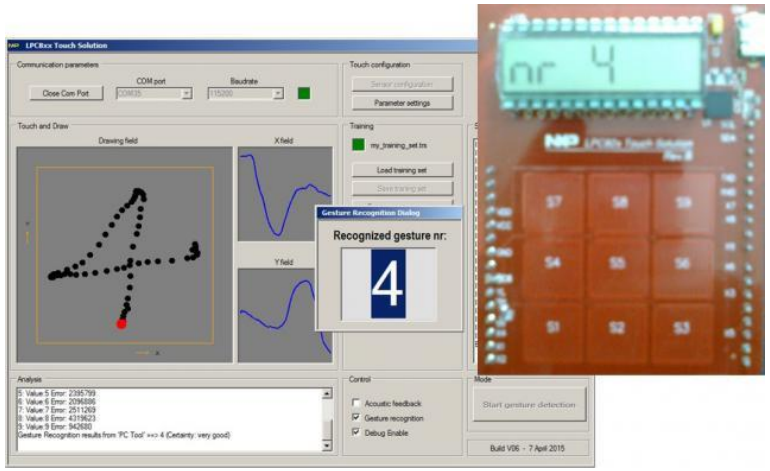


End customer price: ~$18.75 USD
Order: OM13071
Information: http://www.nxp.com/demoboard/OM13071.html

LPC82x Touch Solution Kit (with Gesture Library)

- NXP's Capacitive Touch Solution based on Switched Capacitor Integration
  - Based on LPCXpresso824MAX capacitive touch shield w/ integrated LCD
- Full software provided:
  - Downloadable touch library
  - Auto-calibration to adapt for different environments
  - API programming guide, design guide & sample project for quick prototyping and easy development.
  - PC hosted GUI to visualize/analyze the touch data
  - PC hosted Gesture Library
- USB Drag and Drop Programming





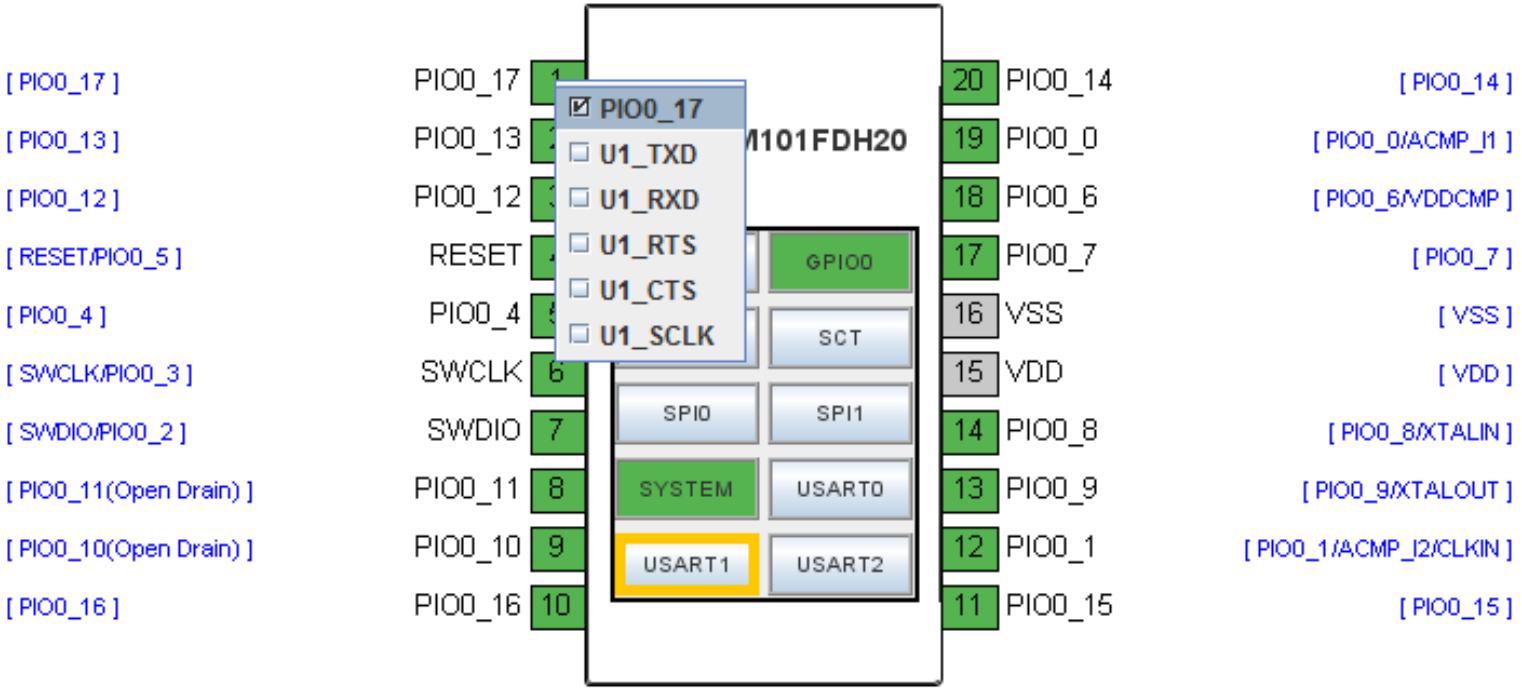
- More information: http://www.nxp.com/demoboard/om13081.html
- Software: http://www.lpcware.com/lpc82x_touch_solution

End customer price: ~$25 USD
Order: OM13081
Information: http://www.nxp.com/demoboard/OM13081.html

Switch Matrix Configuration Tool

3. Click on the pin where you would like to place the peripheral function

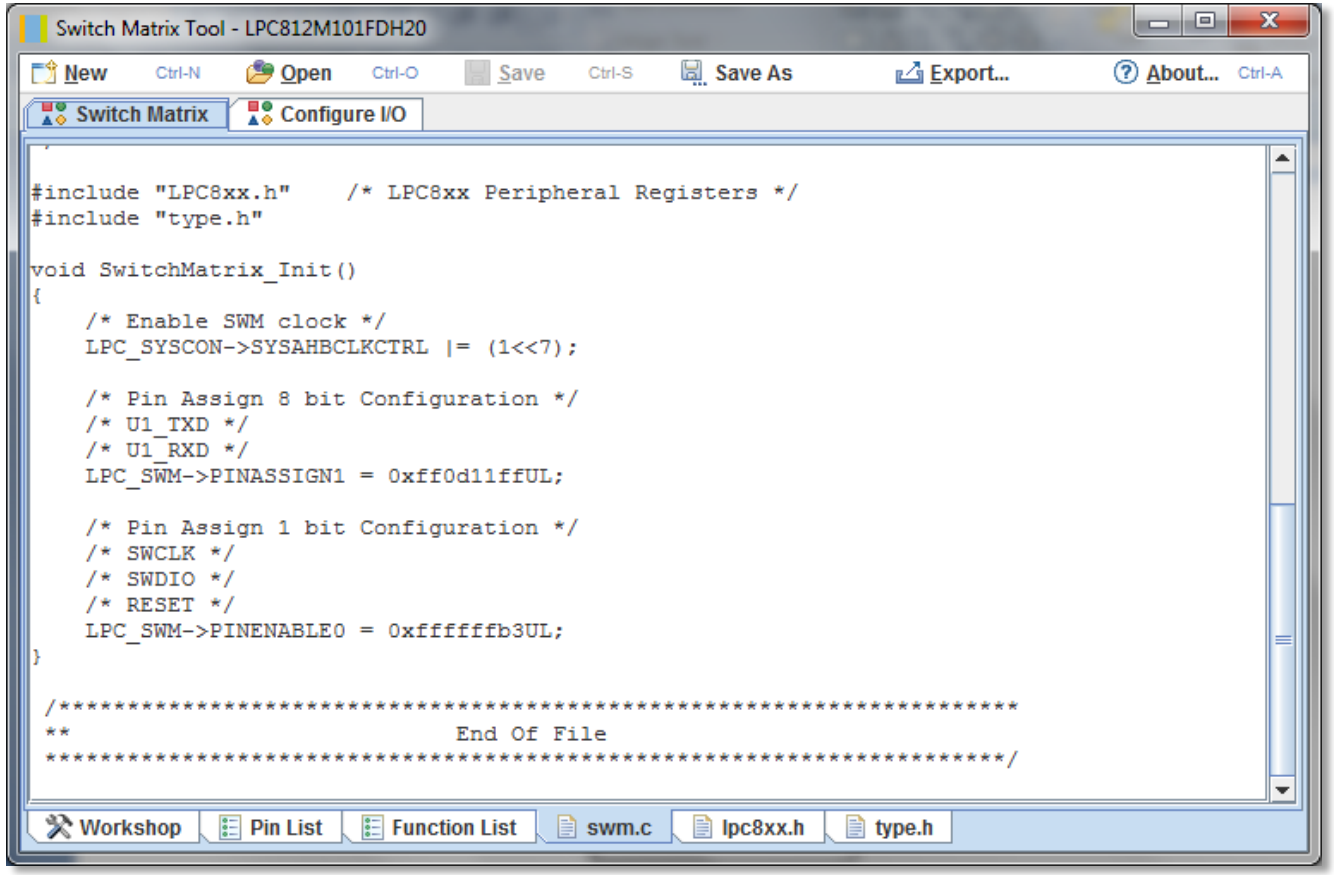
   In this example, we will check U1_TXD



Switch Matrix Configuration Tool

- The code for configuring the PINASSIGNx registers will be shown in the swm.c tab, as shown below. This can be copied into your source code
- Don’t forget to enable the SWM clock!

Hint: you can disable the clock to the Switch Matrix after configuration to save power!!



Where to Get Started?

- www.nxp.com/microcontrollers
  - MCU homepage

- www.nxp.com/lpcxpresso
  - Low-cost development

- www.lpcware.com
  - Engineering community

LPC800 SUMMARY

LPC800 Summary

- Simplicity
- High performance at a low price point
- 2-10x higher performance than 8/16-bit MCUs
- 2-3x power saving compared to 8/16-bit MCUs
- 40-50% smaller code size than 8/16-bit MCUs
- Single cycle IO access
- Easy to use and flexible peripherals: SCTimer/PWM, Multi Rate Timer, Switch Matrix, USART, I2C, SPI

Software, Professional Support & Services

Complimentary Software & Tools

- Kinetis Design Studio, Software Development Kit, Pin Config, Power Estimator/Analyzer
- THREAD, BLE, ZigBee, Bootloader, RTOS
- Linux & Android BSP…

Professional Services

- Managing Skills Gaps & Engineering Capacity
- Global Staffing Capability
- Vested Interest in Mutual Success
- Graphic, Security, Linux/Android, Cloud, Connectivity

Complimentary Support

- NXP Boards
- Communities
- Technical Information Center
- Customer Application & Technical Support
- Distributor technical support

Hardware Services

- 1st Time Boot
- Schematics & Layout Review

Software Products / Technology

- AVB, Miracast, HDCP2.x, TRLE, TEE, Home Kit, CarPlay, Android Auto, MICROEJ, Sensor Fusion, AUTOSAR, Connected Audio Solution, Graphic Tools, VisionECG, GPU Driver, AGL, Genivi, XBMC, HAB

Professional Support

- Risk Reduction
- Fast Answers
- Hot Fixes

SECURE CONNECTIONS
FOR A SMARTER WORLD

ATTRIBUTION STATEMENT