FTF FREESCALE TECHNOLOGY FORUM 2015

PCB Design Techniques to **Improve ESD Robustness**

FTF-DES-F1307

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Agenda

- Introduction
- What is ESD?
- EOS vs ESD
- Electromagnetic field behavior
- Designing robust PCBs
- PCB layout considerations
  - Some new “rules of thumb“
- Closing remarks and reference materials
  - PCB design is not a black art!

Introduction

PCB Design Techniques to Improve ESD Robustness

- Smaller device geometries and higher current switching capabilities have thrust us all into the world of RF, HF, UHF and microwave **energy management**

- Rise times on even the lowest tech devices now exhibit gigahertz impact

- These changes directly impact product functionality and reliability

What Has Changed?

- IC technology was described as % shrink from Integer
  - Design rules
  - Circuit-based approach usually was close enough
  - IC technology now described in nanometers
  - Circuit-based approach completely falls apart
  - EM field (physics) based approach essential
  - EMC standards have changed
  - Lower frequency compliance requirements
  - Higher frequency compliance requirements
  - Lower emission levels allowed
  - Greater immunity required

The playing field and the equipment have changed.
This really is a brand new game!

What Can We Do?

- The skills required are only taught in a few universities
  - Missouri University of Science and Technology (formerly the University of Missouri-Rolla) http://www.mst.edu/
  - Clemson University http://www.cvel.clemson.edu/emc

- Our most savvy mentors may not be able to help
- Nearly every rule of thumb is wrong
- To gain the skills needed, you have to actively seek them
- Industry conferences
  - PCB East and West
  - IEEE EMC Society events
- Seminars hosted by your favorite semiconductor supplier! **Freescale, of course!**

What Can We Do?

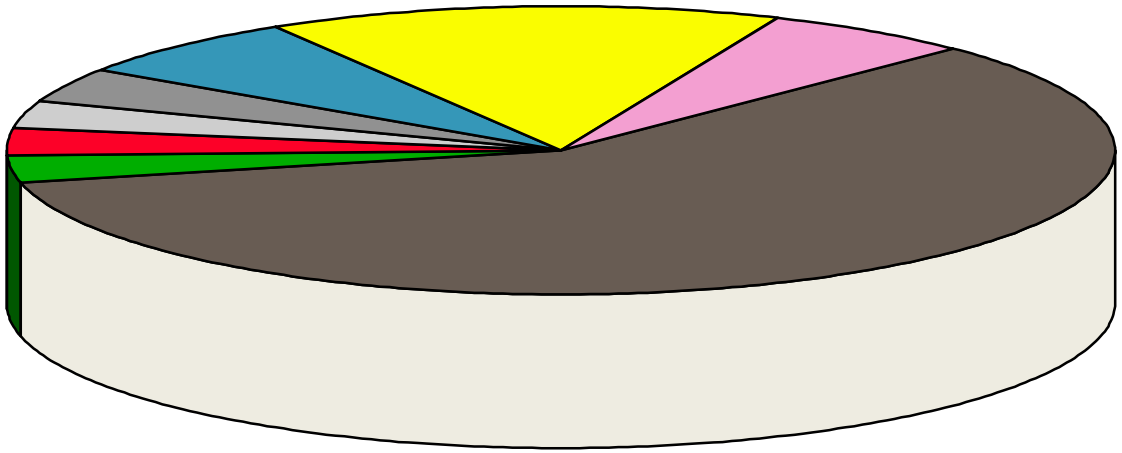
About Me: Daniel Beeker

- 34+ years experience at Motorola/Freescale designing and working with microprocessor and microcontroller development systems
- 28+ years working with automotive customers in one of the most demanding embedded control environments
- Championing the cause for increased awareness of advanced design technologies
- Used to believe in *black magic*, but Ralph Morrison set me straight!
- Firmly entrenched in physics-based design philosophy

What is ESD?

Ranking of Semiconductor Failure Causes

- EOS/ESD is the #1 Cause of Semiconductor Failure
  - Source: Semiconductor Reliability News, March 1993



EOS/ESD 59%

Electrical testing 3%

Oxide/passivation failure 3%

Conductor failure 3%

Die fracture 4%

Lead short/open 7%

Wire bonds 15%

Others 6%

EMC Requirements and Key Design Considerations

Radiated Emissions

- 1 HF GND
- Risetime Control
- Filtered I/O
- Adequate Decoupling
- Balance Control

Radiated Susceptibility

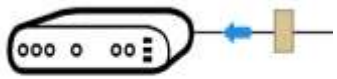
- 1 HF GND
- Filtered I/O
- Adequate Decoupling
- Balance Control

Transient Immunity

- LF Current Path Control
- Chassis GND on board
- Filtered I/O
- Adequate Decoupling

Electrostatic Discharge

- LF Current Path Control
- Chassis GND on board
- Filtered I/O
- Adequate Decoupling



Bulk Current Injection

- 1 HF GND
- Chassis GND on board
- Filtered I/O
- Adequate Decoupling
- Balance Control

Designing a product that is guaranteed to meet all of these requirements is relatively easy. Fixing a non-compliant product can be difficult and costly.

Slide compliments of Dr.Todd Hubing

PCB Design Techniques to Improve ESD Robustness

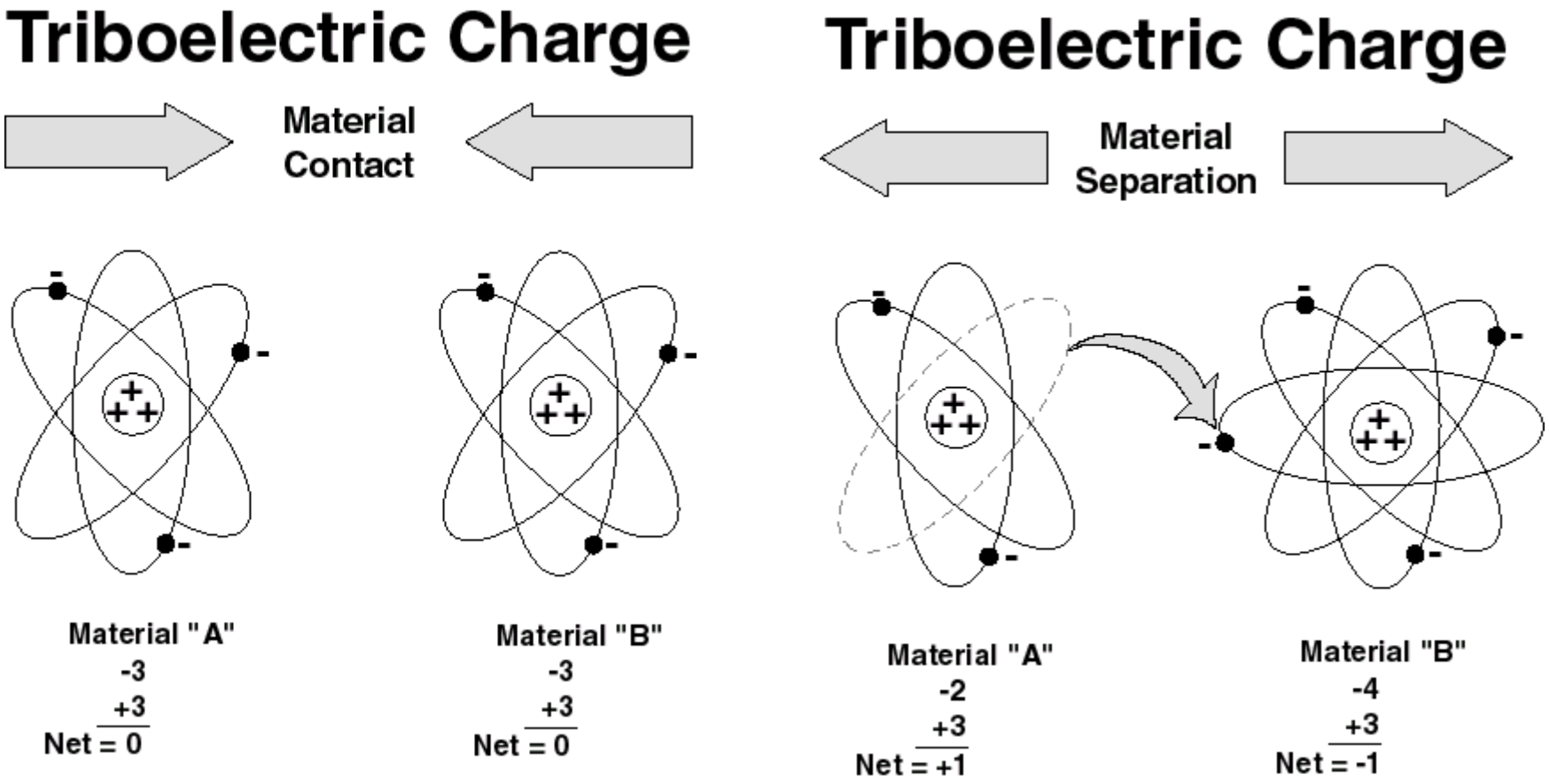
- Static electricity
  - Electrical charge caused by an imbalance of electrons on the surface of a material. This imbalance of electrons produces an electric field that can be measured and that can influence other objects at a distance.

- Electrostatic discharge
  - Transfer of charge between bodies at different electrical potentials

Triboelectric Charging

- Creating electrostatic charge by **contact and separation** of materials is known as "**triboelectric** charging."
- *It involves the transfer of electrons between materials.*
- When the two materials are placed in contact and then separated, negatively charged electrons are transferred from the surface of one material to the surface of the other material.
  - Which material loses electrons and which gains electrons will depend on the nature of the two materials
    - The material that loses electrons becomes positively charged
    - The material that gains electrons is negatively charged

Triboelectric Charging



Human Perceptions of ESD

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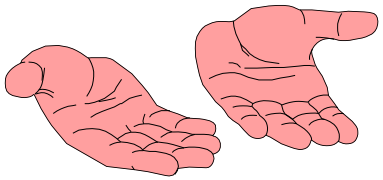
- At 3000 volts, you can  ESD
- At 5000 volts, you can  ESD
- At 10000 volts, you can  ESD

Slide compliments of 3M

Typical Electrostatic Voltages

	ELECTROSTATIC VOLTAGES	
Means of Static generation	10 to 20 percent Relative humidity	65 to 90 percent Relative humidity
Walking across carpet	**35,000**	**1,500**
Walking over vinyl floor	**12,000**	**250**
Worker at bench	**6,000**	**100**
Vinyl envelopes for work Instructions	**7,000**	**600**
Common poly bag picked up From bench	**20,000**	**1,200**
Work chair padded with Polyurethane foam	**18,000**	**1,500**

Slide compliments of Owen j. Mcateer, Military electronics/countermeasures

EOS vs. ESD

What is EOS?

- Electrical overstress (EOS) is the misapplication of excessive voltage or current to the external leads of an integrated circuit.
- The damage caused by EOS is actually a result of the total energy applied to the device.
- Externally, the damage will result in open, short or leaking pins.
  - It can also affect the devices functionality.
  - Internally, the result is typically seen as fused bond wires or damage to the die metallization.

EOS vs. ESD

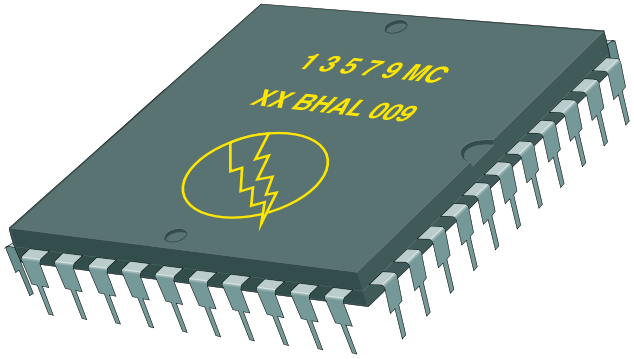
- The key difference between EOS and electrostatic discharge (ESD) is the rise time of the energy pulse.
  - Rise times associated with an ESD event are in the 5-20 ns range
  - Rise times for EOS events tend to be much longer.
- Failure mechanisms associated with both types of events are strictly due to localized heating.
- Where the localized heating occurs is key to understanding the failure mechanisms.
  - Damage seen on bond wires and die metallization are typically associated with EOS
    - **slow rise time, high energy**
  - Junction degradation, poly melt filaments and contact damage are associated with ESD
    - **fast rise time, high energy**

ESD Damage: How Devices Fail

- Electrostatic damage to electronic devices can occur at any point from manufacture to field service.
- Damage results from handling the devices in uncontrolled surroundings or when poor ESD control practices are used.
- Generally damage is classified as either a catastrophic failure or a latent defect.

Types of ESD Failures to Electronic Devices

- Catastrophic Failure
  - Device no longer operates
  - Represents **10%** of ESD failures



- Intermittent / Walking Wounded
  - Device is operational, but erratic and will cause field failures
  - Represents **90%** of ESD failures

Slide compliments of 3M

Catastrophic Failure

- When an electronic device is exposed to an ESD event, it may no longer function
- The ESD event may have caused a metal melt, junction breakdown, or oxide failure
- The device's circuitry is permanently damaged causing the device to stop functioning
- Such failures usually can be detected when the device is tested before shipment
- If a damaging level ESD event occurs after test, the part may go into production and the damage will go undetected until the device fails in product

Latent Defect

- It is relatively easy with the proper equipment to confirm that a device has experienced catastrophic failure.
  - Basic performance tests will substantiate device damage.

- A latent defect, on the other hand, is more difficult to identify.
  - A device that is exposed to an ESD event may be partially degraded, yet continue to perform its intended function.
  - The operating life of the device may be reduced dramatically.

PCB Design Techniques to Improve ESD Robustness

- ESD can only be dealt with in a few ways:
  - You can prevent it (preferred)
  - You can shield against it (expensive)
  - You can absorb it (things have the smoke let out of them)

- Most solutions end up being a hybrid of all 3
  - Balance between cost and robustness
  - Transmission line design techniques required
  - Maximize the effect of the copper you use
  - It will cost more to survive in high stress environments

PCB Design Techniques to Improve ESD EMC Robustness

- OK, why all the stuff about ESD? I thought this was an EMC class?
- **ESD is the most extreme form of EMI you have to survive**
  - **(and it kills parts…)**
- Techniques for improving ESD survival will result in better EMC testing results!
- It is all about proper placement of filters and reducing the impedance of the transmission lines on the PCB

Electromagnetic Field Behavior

What is Electricity?

- Fields are basic to all circuit operation
- Volts and amperes make things practical
  - We easily can measure volts and amperes
  - More difficult to measure “E” and “H” fields
- In high clock rate (and rise time) circuits, once the "quasistatic” approximation does not hold true anymore, field control plays a critical role
- This must be a carefully considered part of any design

Slide compliments of Ralph Morrison, Consultant

PCB Design Techniques to Improve EMC Robustness

Maxwell's Equations:

$$\oint \mathbf{E} \cdot d\mathbf{A} = \frac{q_{enc}}{\varepsilon_0}$$

$$\oint \mathbf{B} \cdot d\mathbf{A} = 0$$

$$\oint \mathbf{E} \cdot d\mathbf{s} = -\frac{d\Phi_B}{dt}$$

$$\oint \mathbf{B} \cdot d\mathbf{s} = \mu_0 \varepsilon_0 \frac{d\Phi_E}{dt} + \mu_0 i_{enc}$$

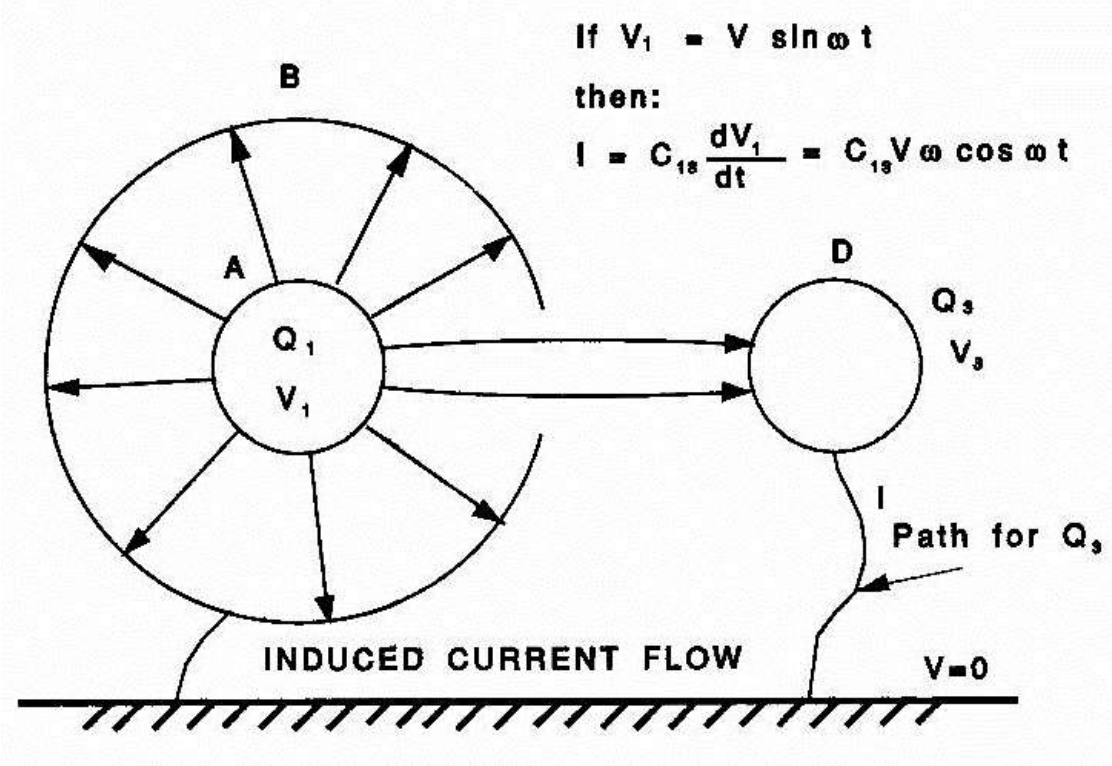
Slide compliments of http://www.physics.udel.edu/~watson/phys208/ending2.html

PCB Design Techniques to Improve EMC Robustness

Maxwell *was* smart!

A Loose Field is *Not* a Friendly Field

- A shielded enclosure with an opening

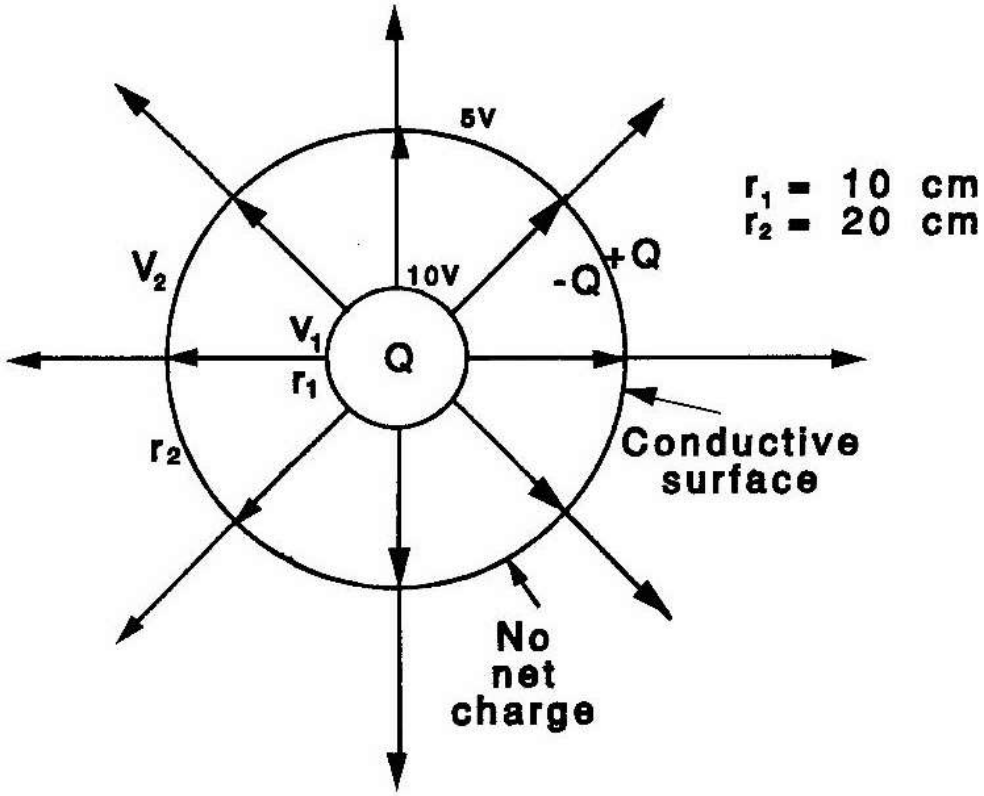


Field is not contained and looks for trouble

Slide compliments of Ralph Morrison, Consultant

Contained Fields are Friendly!

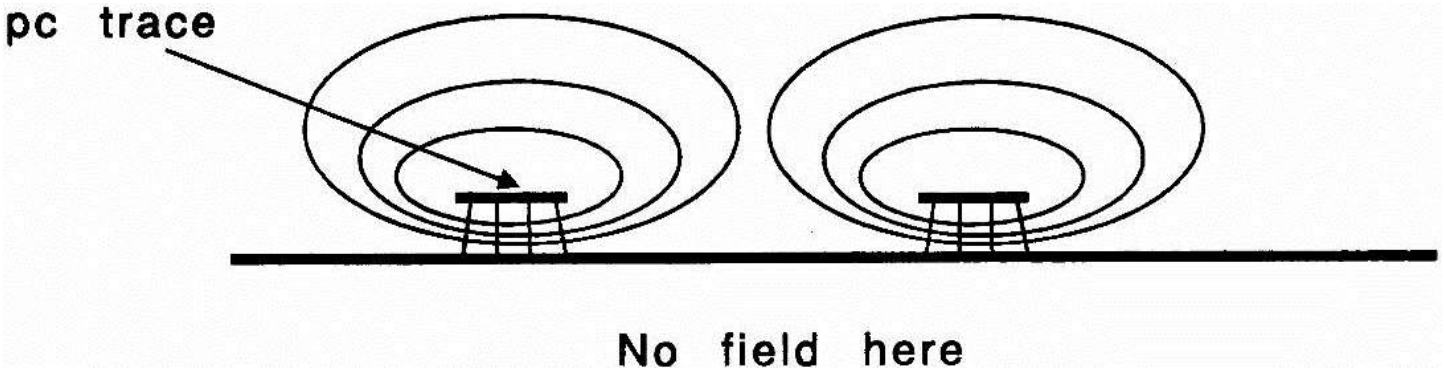
- An equipotential surface around a charged sphere



Slide compliments of Ralph Morrison, Consultant

Contained Fields are Friendly!

Fields concentrate under the traces and there is little crosstalk.



Fields do not penetrate the plane

Slide compliments of Ralph Morrison, Consultant

Well-Defined Transmission Line

- Signal trace *must* be one dielectric away from the return!
  - Adjacent to planar copper
  - Adjacent to ground trace
    - Any deviation from this *must* be an engineered compromise, *not* an accident of signal routing
    - Any deviation from this *will* increase radiated emissions, degrade signal integrity and decrease immunity

This is a very serious problem and a big change from normal board design philosophy.

PCB Design Techniques to Improve EMC Robustness

- Fields store energy in *space!*
- Energy is *not* stored in or on the conductors

A capacitor is:

A conductor geometry that concentrates the storage of electric field energy

In a capacitor:

Field energy is stored in the space between the plates

An inductor is:

A conductor geometry that concentrates the storage of magnetic field energy

In an inductor:

Field energy is stored in the space around wires and in gaps

Slide compliments of Ralph Morrison, Consultant

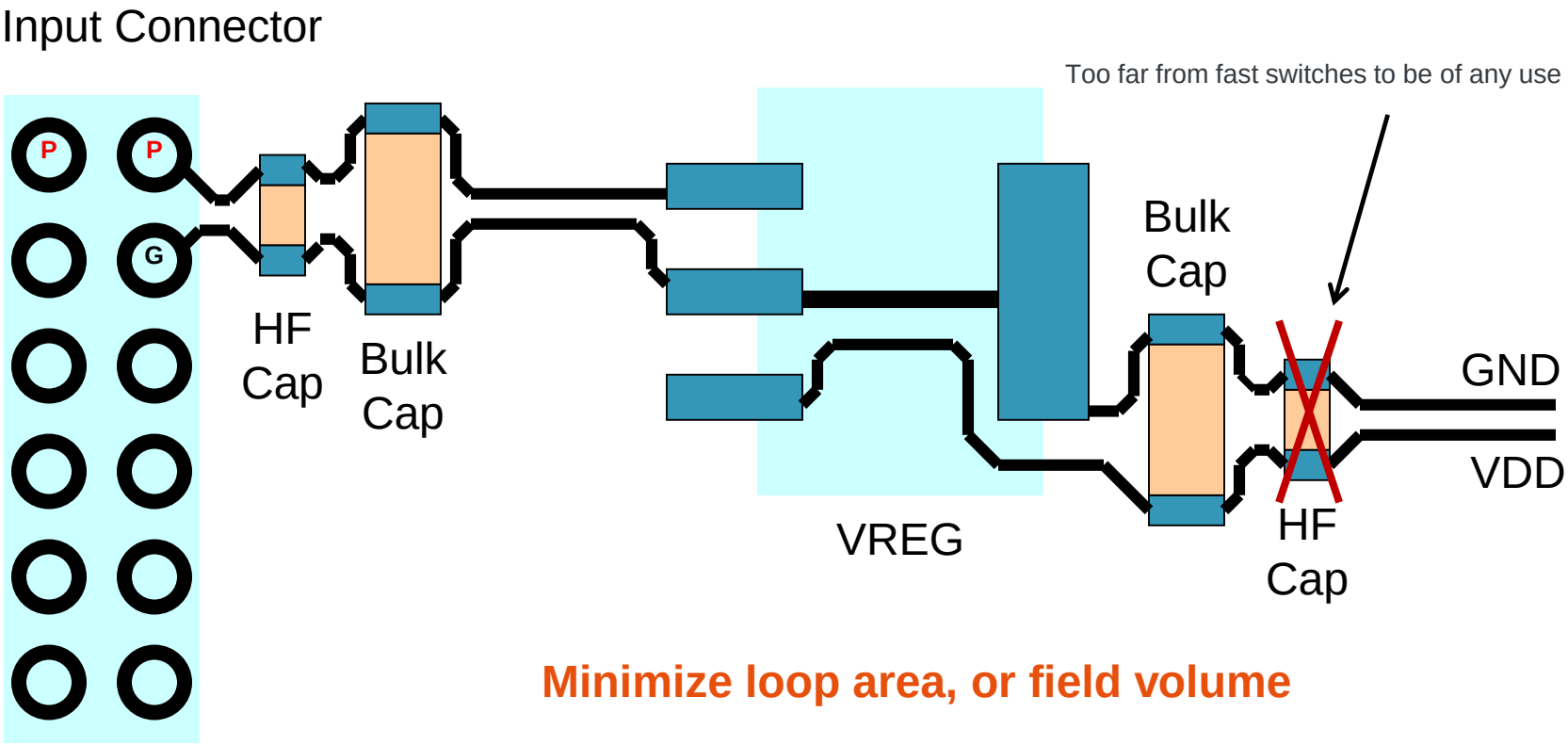
Designing Robust PCBs

PCB Design Techniques to Improve EMC Robustness

PCB ~~signal~~ transmission line routing

- The first and most important job is to route the power distribution network – it is the source of all of the electromagnetic energy you will be managing on the PCB
- On low layer count boards, with no dedicated ground plane, the power lines *must be routed in pairs*
  - Power and ground
  - Side by side
    - Trace width determined by current requirements
    - Spaced as close as manufacturing will allow them
  - Daisy chain from source to destination, connecting to each component, then finally to target devices
- Minimize the *volume* of the *power transmission* network

PCB ~~signal~~ Transmission Line Routing



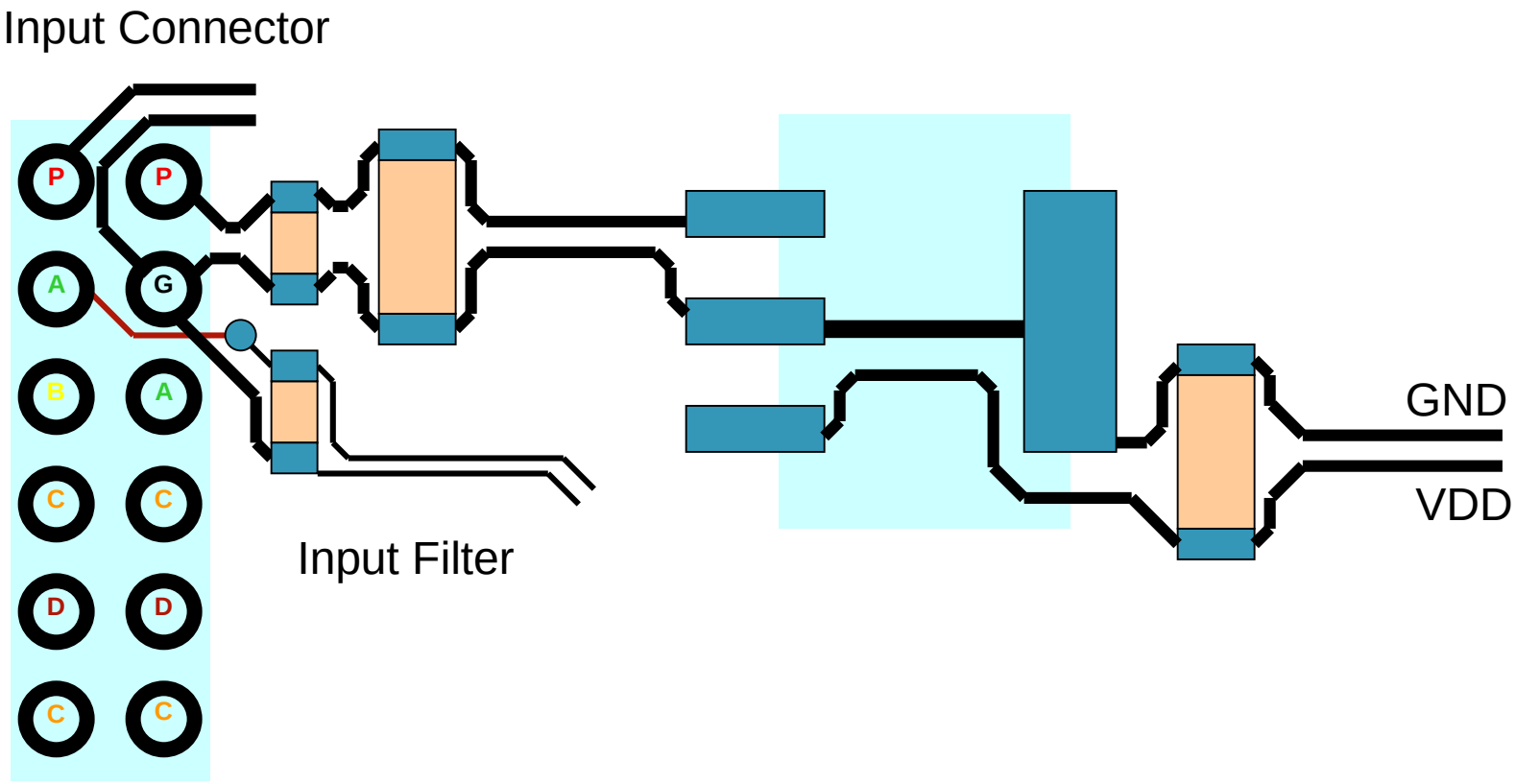
Minimize loop area, or field volume

PCB Design Techniques to Improve EMC Robustness

PCB ~~signal~~ transmission line **routing**

- Route power and ground traces as close as manufacturing allows
- Internal and customer separation requirements
- PCB fabrication limits for chosen supplier
  - Yes, you do need to know what the supplier can manufacture
  - Can have big impact on PCB cost
- Small changes in routing can have a large impact on performance
- Component placement is critical
  - Staying within lumped distance
    - Reduces component count
    - Reduces system cost
    - Improves EMC performance
    - Minimize the volume of the power transmission network

PCB ~~signal~~ Transmission Line Routing

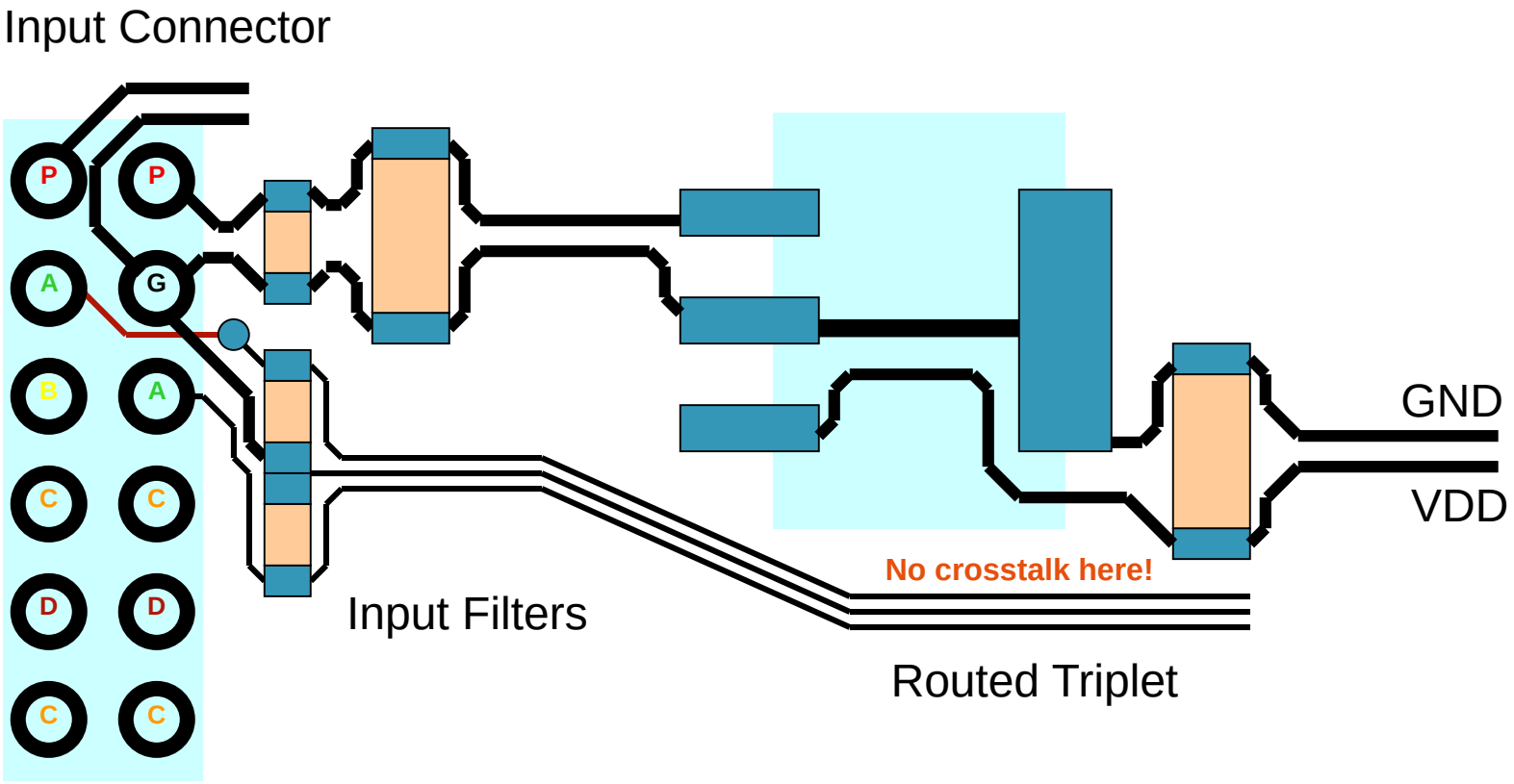


PCB Design Techniques to Improve EMC Robustness

PCB ~~signal~~ transmission line **routing**

- Input filters must be placed as close as allowable to connectors
- Connections must be directly to the connector ground pins
- Route traces with well defined return path
- Minimize the volume of the signal transmission network

PCB ~~signal~~ Transmission Line Routing



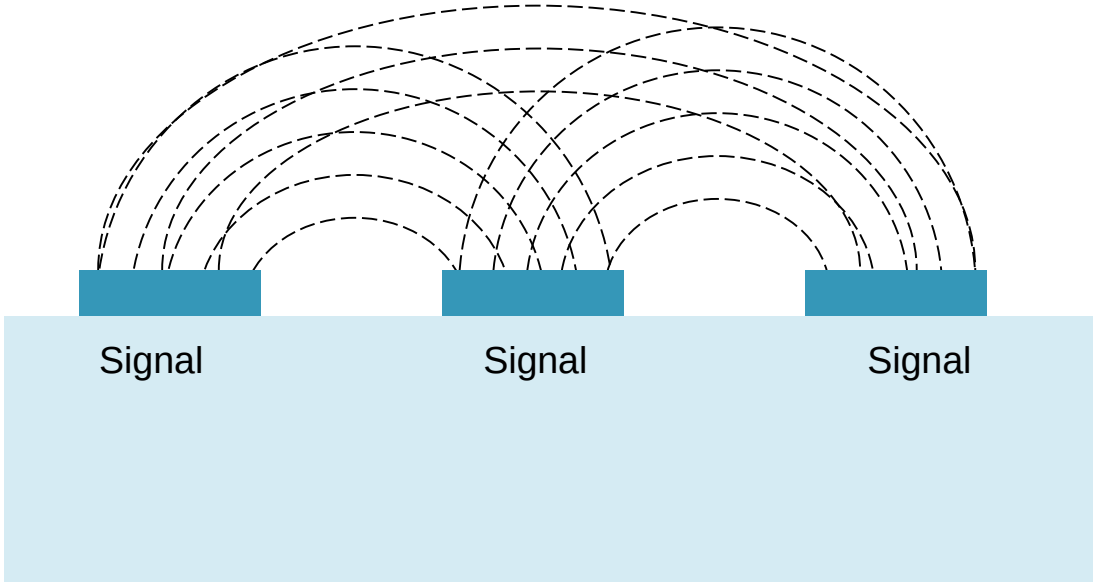
PCB Design Techniques to Improve EMC Robustness

PCB ~~signal~~ transmission line **routing**

- Routing in “triplets” (**S**-**G**-**S**) provide good signal coupling with relatively low impact on routing density
- Ground trace needs to be connected to the ground pins on the source and destination devices for the signal traces
- Spacing should be as close as manufacturing will allow
- Minimize the volume of the signal transmission network

PCB Design Techniques to Improve EMC Robustness

- You really want to make sure that the field energy is coupling to the conductor you choose!



All field lines actually terminate at 90 degree angles

PCB Design Techniques to Improve EMC Robustness

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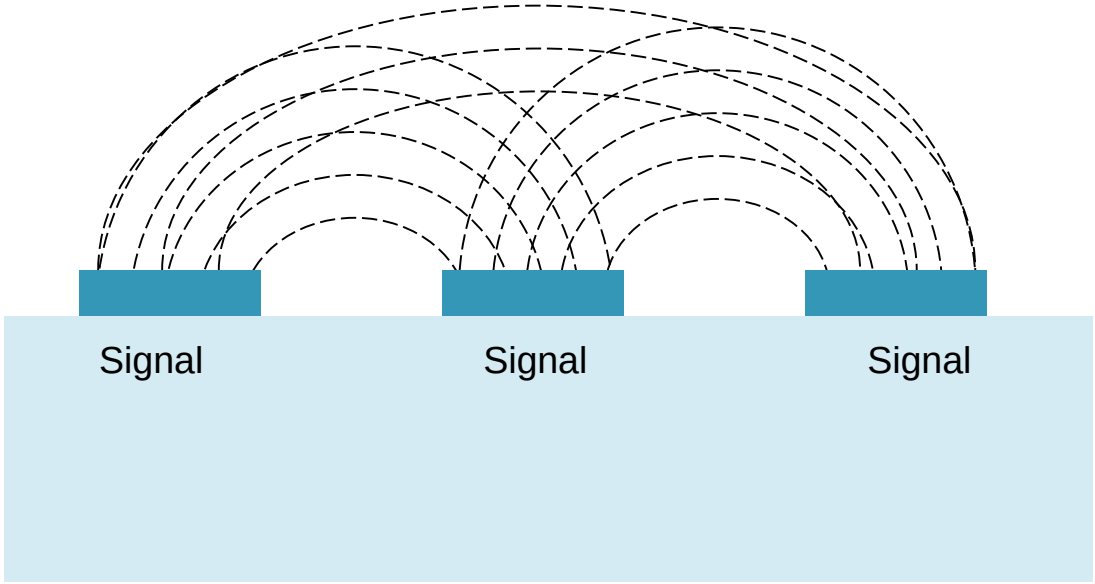
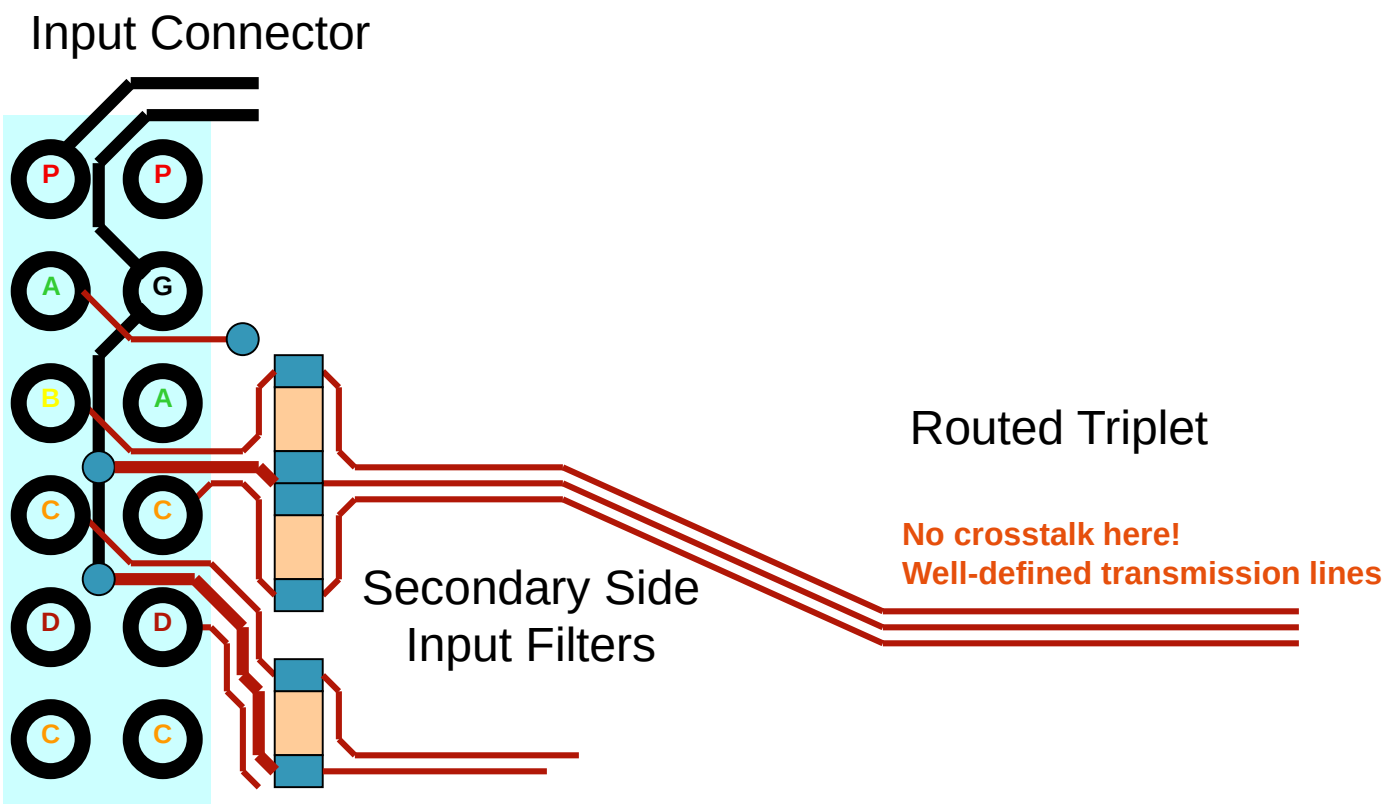


All field lines actually terminate at 90 degree angles

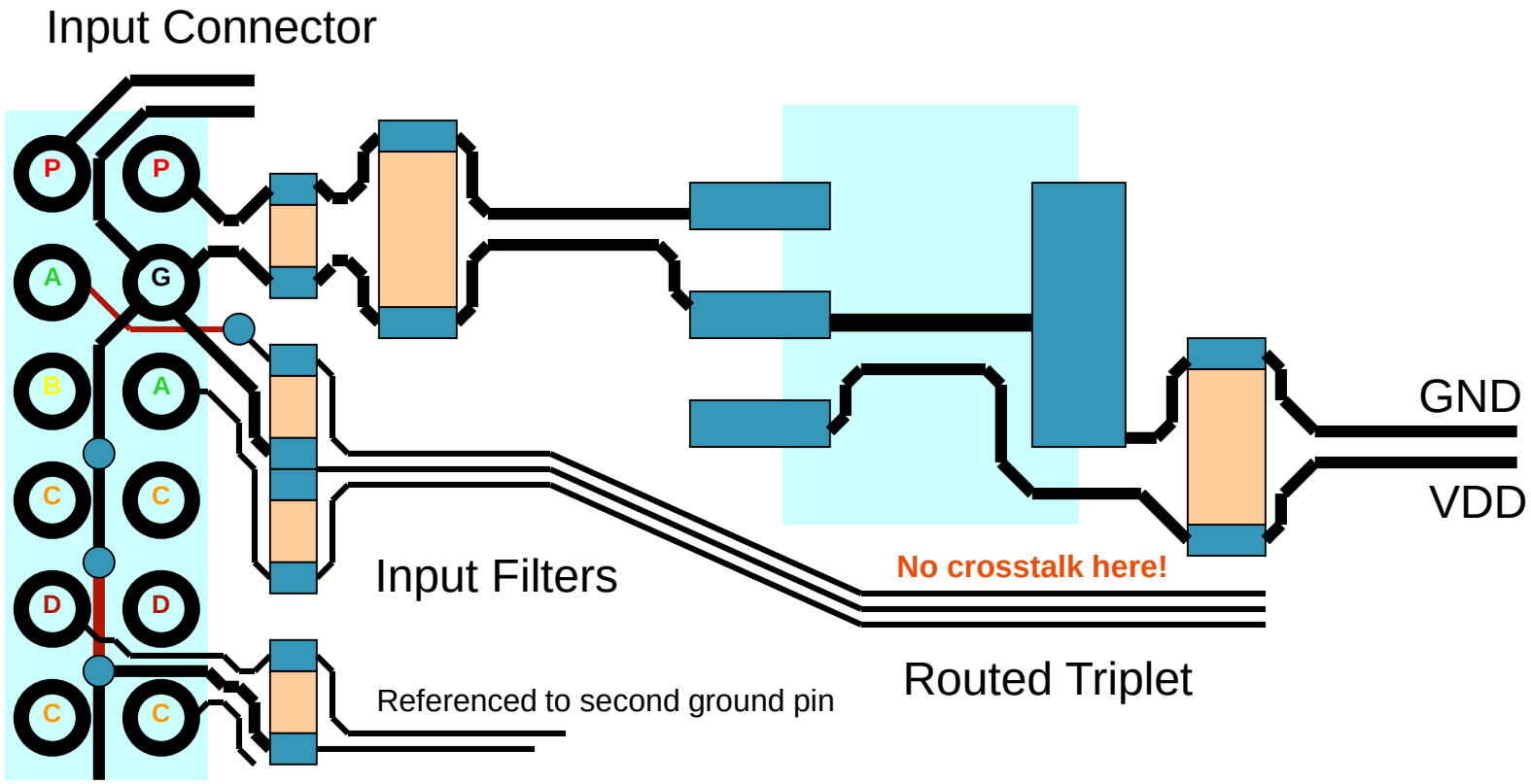
Maybe a “triplet” makes sense?

PCB Design Techniques to Improve EMC Robustness

PCB ~~signal~~ transmission line routing

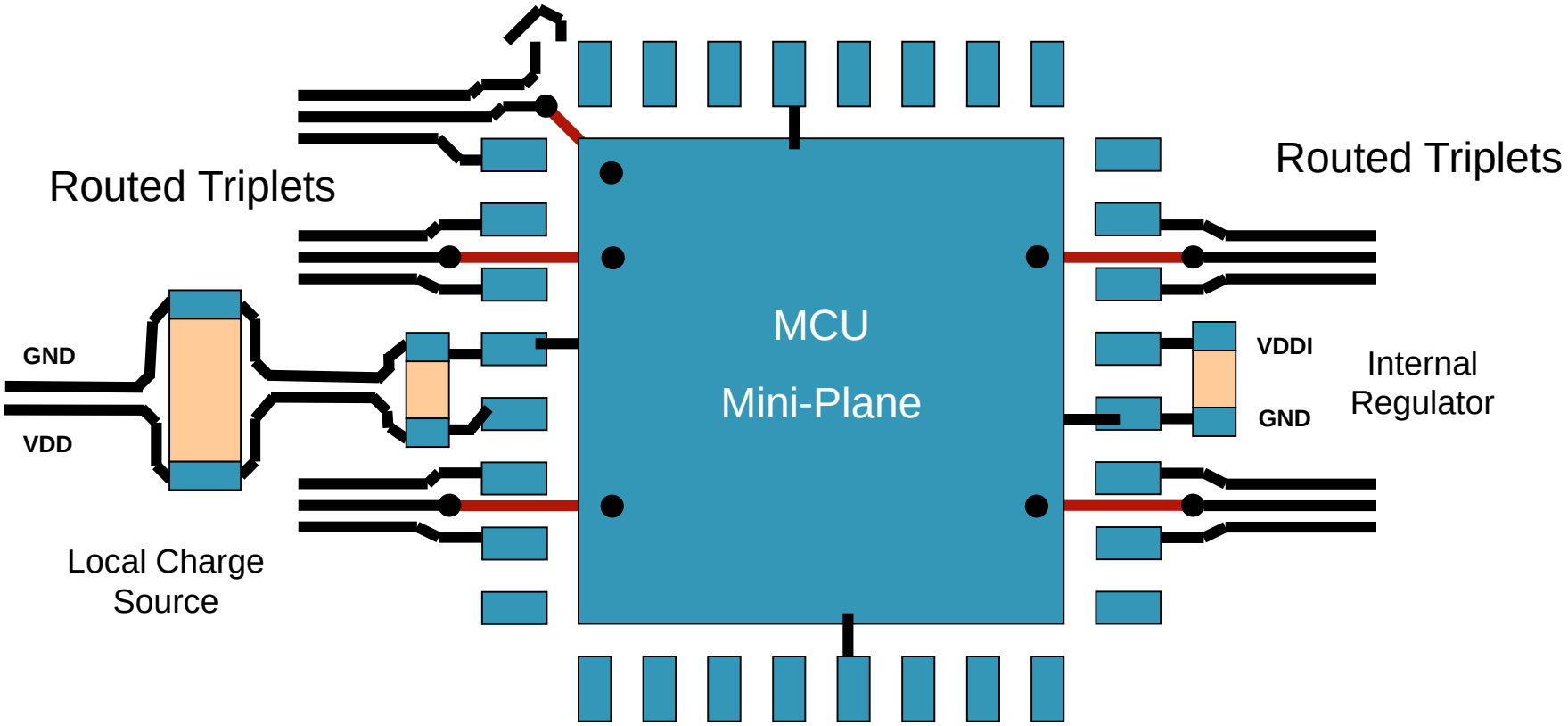


PCB ~~signal~~ Transmission Line Routing



PCB Design Techniques to Improve EMC Robustness

PCB ~~signal~~ transmission line routing



PCB Design Techniques to Improve EMC Robustness

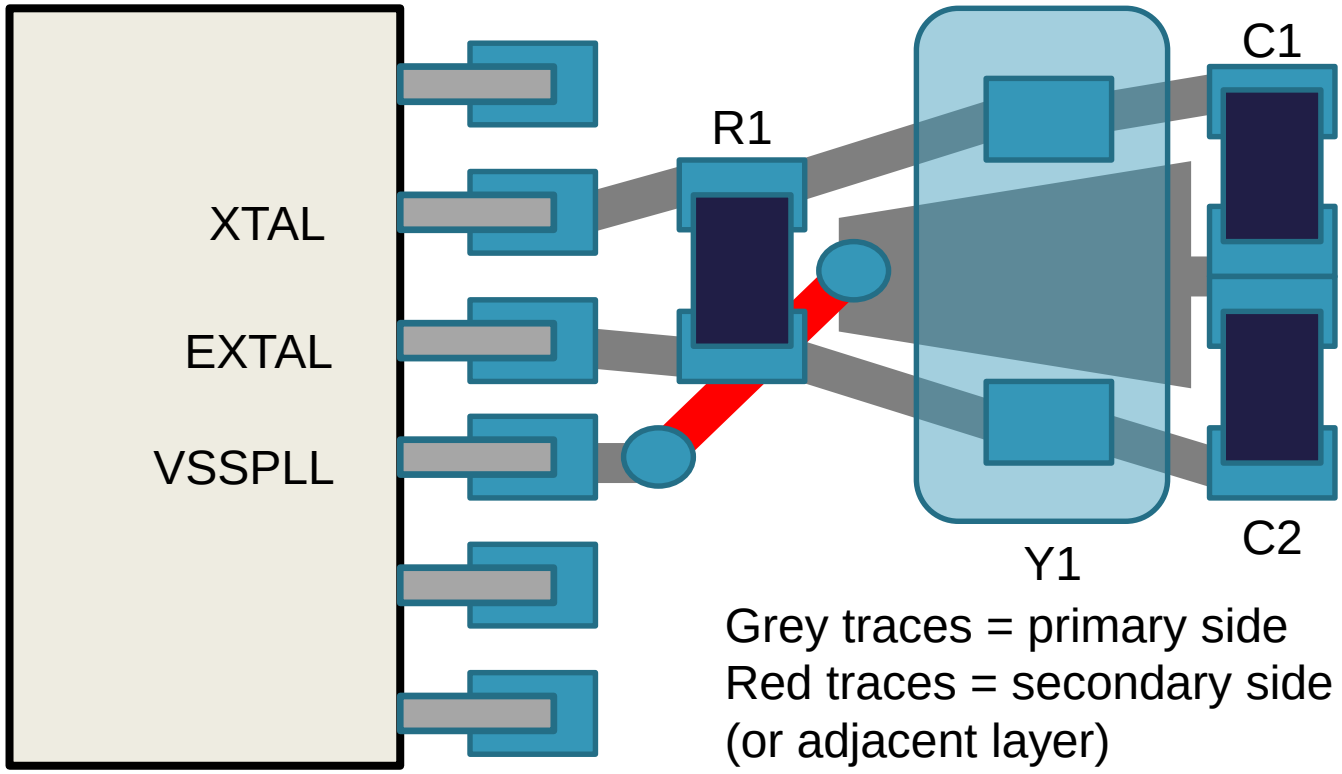
PCB ~~signal~~ transmission line **routing**

- Lead frame and wire bonds are parts of transmission lines, too
- Mini-plane under the QFP provides improved EMC
- Triplet ground traces can be easily coupled to the mini-plane on secondary side
- In high density applications, even routing with “quints” (**S**-**S**-**G**-**S**-**S**) will provide some improvement
  - You know where most of the field energy is going!
- Last but not least, flood everything with ground copper!
  - Must be able to tie each “island” with at least two via to adjacent layer ground
- Minimize the volume of the signal transmission network

PCB Design Techniques to Improve EMC Robustness

PCB ~~signal~~ transmission line routing

- Oscillator ground must be routed to MCU pin, not tied to System Ground
- Connect System Ground on the opposite side of the MCU pin



PCB Design Techniques to Improve EMC Robustness

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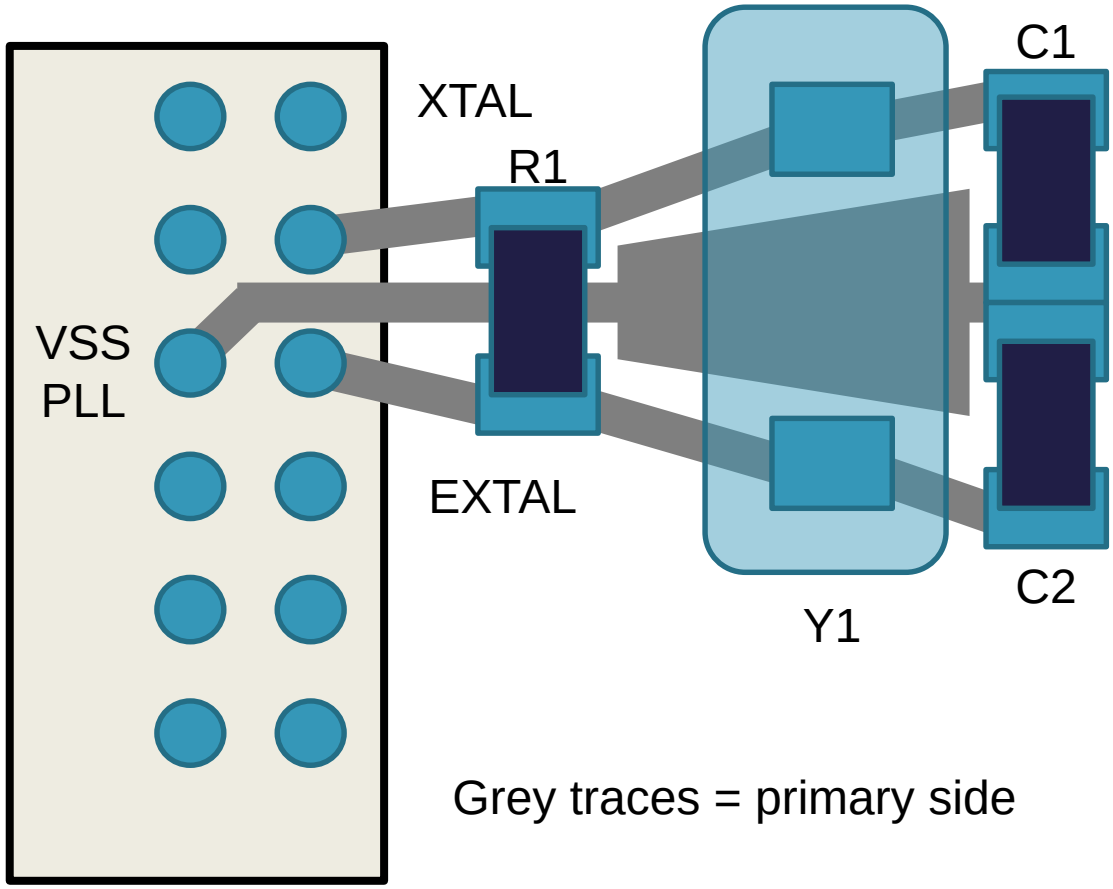


Grey traces = primary side

Why This Works

- Crystal output from MCU is the POWER source
  - Energy flows out, between the MCU output signal trace and MCU oscillator ground trace to the crystal or resonator
- Crystal becomes POWER source
  - Energy flows back, between the crystal output signal trace and the oscillator ground trace to the MCU input pin
- This is a closed loop system, and SYSTEM ground is not required
  - Lower impedance for the connecting transmission lines
  - Smaller loop area
  - Significantly improved robustness
- It is always about “Where does the energy come from?”
- This rule should be applied to the entire design
  - Ground for any signal is determined by the power source return
- Another important fact is that this is a low amplitude, low frequency, analog circuit. It is not required to be placed as close as possible to the MCU, just that it must be connected with transmission lines as described above. Moving these components can allow for placement and routing of more critical components in the area near the MCU.

PCB Layout Considerations: Some New “Rules of Thumb"

Flooding Unused Spaces on the PCB with Ground

- Properly implemented, will improve EMC performance
- Reduce cost by increasing PCB manufacturing yield
  - Less etch required, so less chemical is used
  - Balanced copper improves plating and
- **Balanced copper improves final assembly yield**
  - Reduced board warping
- Remember to stitch the ground islands and planes together
  - Trying to make a pseudo-Faraday cage!

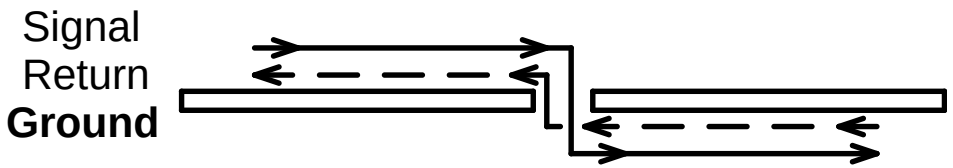
Use Minimum Trace Widths and Spacing for Signal Lines

- Refer to PCB fabricator's capabilities without adding cost
- Same thing goes for drill sizes and pad rings
- Provides maximum trace density
- May be defined by either customer or internal requirements
- Wider traces for power supply transmission line pairs
- Spread out the traces to increase the ground flood coverage

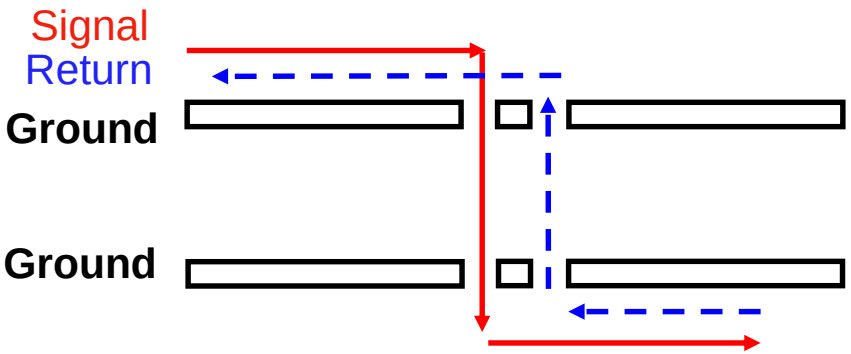
- Make room for all of those ground traces!

PCB Design Techniques to Improve EMC Robustness

- When moving signals *between layers*, route on either side of the same plane, as much as possible!



- When moving signals *between two different planes*, use a transfer via very near the signal via.



Slide compliments of Rick Hartley, Consultant

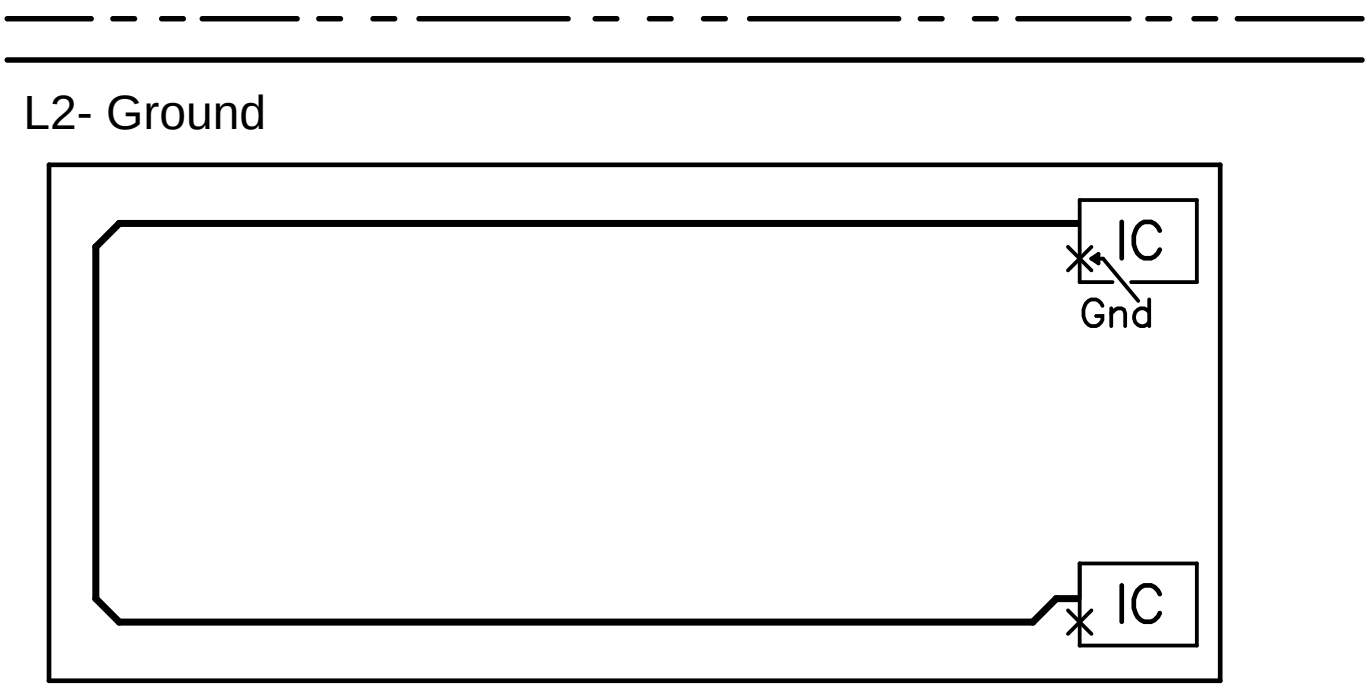
PCB Design Techniques to Improve EMC Robustness

- Using planes
- Splitting ground planes is almost never a good idea
  - Only when required by customer or internal specifications
  - Question those requirements!
- If you have to split a plane, do *not* route traces across the split!
  - If you must, then you absolutely have to route a following ground trace across the split next to the signal trace

Splits in planes are very efficient slot antennas!

Signal Return Path

- Two-layer microwave style PCB board

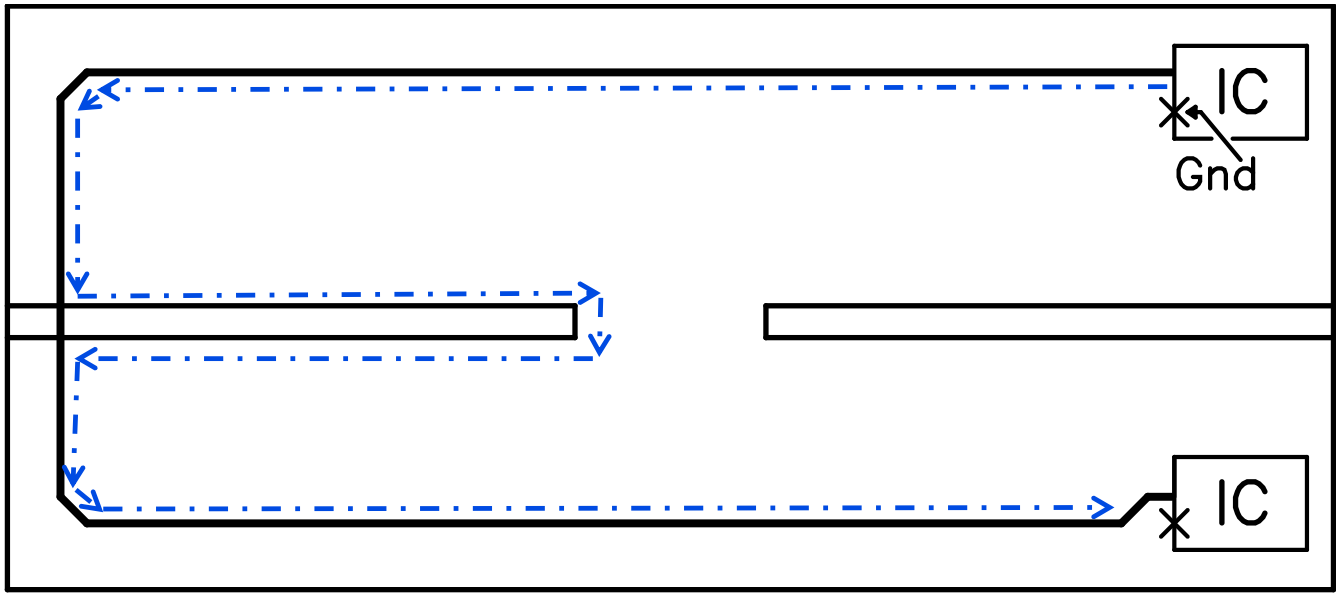


Where does signal's return current flow?

Slide compliments of Rick Hartley, Consultant

Signal Return Path

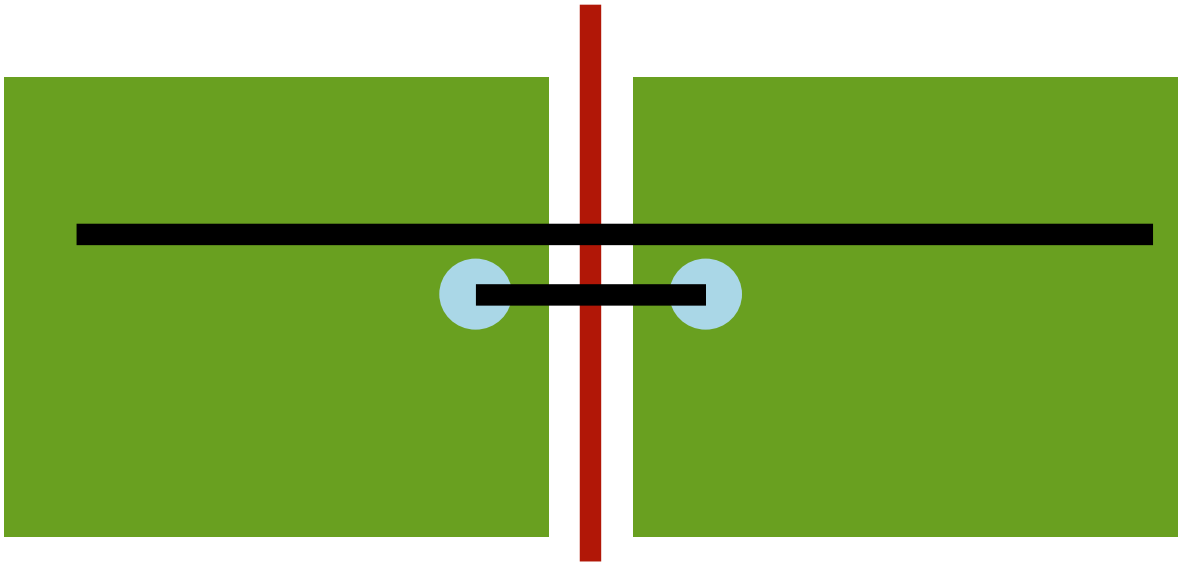
- What happens if return plane is split?
- Now where does return current flow?



Slide compliments of Rick Hartley, Consultant

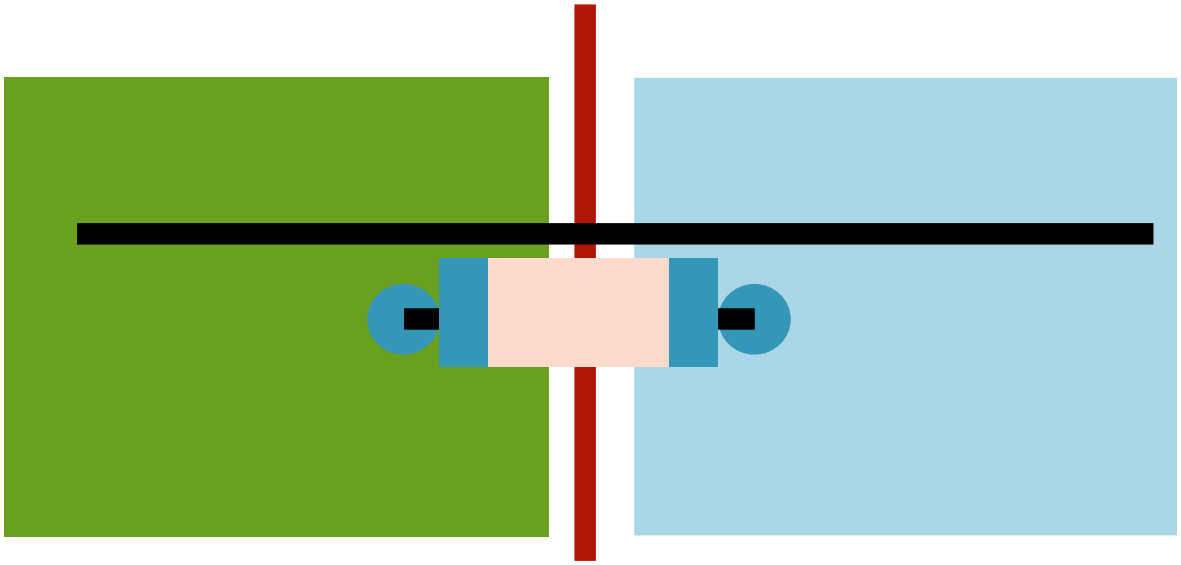
PCB Design Techniques to Improve EMC Robustness

- Routing over split planes, same potential
- Just use a bridge tied to each plane
- Better to just not split it, but sometimes you have to route a trace in the split



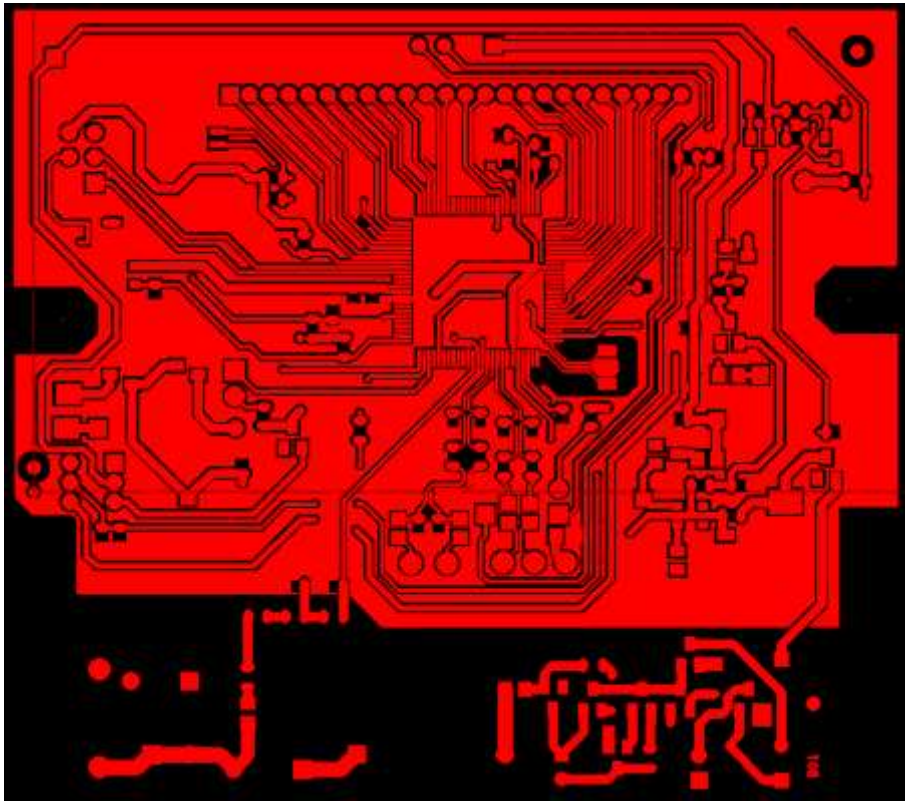
PCB Design Techniques to Improve EMC Robustness

- Routing over split planes, different potential
- Have to bridge with a capacitor



Photon AC Power Meter

- This board was validated to 25KV
  - 2 Layer PCB with Kinetis MCU and LCD
  - Routed triplets, maximum Ground Flood, closed loop oscillator design



Closing Remarks and Reference Materials

PCB Design is *Not* a Black Art!

PCB Design Techniques to Improve EMC Robustness

- ESD can result in operational issues and possible component damage
- Proper placement of capacitors and other protection devices is critical
- Well-defined transmission lines result in significantly improved EMC performance and ESD Robustness
- Careful routing of transmission lines can result in behavior similar to that gained by adding extra PCB ground layers

- The *black magic* is tamed!

Special Thanks to My Mentors

- Rick Hartley (PCB designer extraordinaire) started me down this trail in 2004 at PCB West

- Ralph Morrison (author, inventor and musician) has patiently and steadily moved me from the fuzzy realm of “circuit theory” and “black magic” into the solid world of physics.

- Dr. Todd Hubing (researcher and professor) whose research at UMR and Clemson has provided solid evidence that Maxwell and Ralph have got it right.

- Finally, my team at Freescale. We really have come a long way!

High Speed Design Reading List

- *Right the First Time: A Practical Handbook on High Speed PCB and System Design* Volumes I & II, Lee W. Ritchey. Speeding Edge, ISBN 0-9741936-0-7
- *High Speed Digital System Design: A Handbook of Interconnect Theory and Practice*, Hall, Hall and McCall. Wiley Interscience 2000, ISBN 0-36090-2
- *High Speed Digital Design: A Handbook of Black Magic*, Howard W. Johnson & Martin Graham. Prentice Hall, ISBN 0-13-395724-1
- *High Speed Signal Propagation: Advanced Black Magic*, Howard W. Johnson & Martin Graham. Prentice Hall, ISBN 0-13-084408-X
- *Signal Integrity Simplified*, Eric Bogatin. Prentice Hall, ISBN 0-13-066946-6
- *Signal Integrity Issues and Printed Circuit Design*, Doug Brooks. Prentice Hall, ISBN 0-13-141884-X

Slide compliments of Rick Hartley, Consultant

EMI Reading List

- PCB Design for Real-World EMI Control, Bruce R. Archambeault. Kluwer Academic Publishers Group, ISBN 1-4020-7130-2
- Digital Design for Interference Specifications: A Practical Handbook for EMI Suppression, David L. Terrell & R. Kenneth Keenan. Newnes Publishing, ISBN 0-7506-7282-X
- Noise Reduction Techniques in Electronic Systems, 2nd Edition, Henry Ott. John Wiley and Sons, ISBN 0-471-85068-3
- Introduction to Electromagnetic Compatibility, Clayton R. Paul. John Wiley and Sons, ISBN 0-471-54927-4
- EMC for Product Engineers, Tim Williams. Newnes Publishing. ISBN 0-7506-2466-3
- Grounding & Shielding Techniques, 5th Edition, Ralph Morrison. John Wiley & Sons, ISBN 0-471-24518-6

Slide compliments of Rick Hartley, Consultant

Additional References

- Ralph Morrison's New Book: Digital Circuit Boards: Mach 1 GHz. Available from Wiley and Amazon
- The Best PCB design conference website: http://pcbwest.com/
- Doug Smith's website: http://www.emcesd.com/ (He is the best at finding what is wrong! Lots of useful app notes.)
- IEEE EMC Society website: http://www.emcs.org/
- Clemson's Automotive Electronics website: http://www.cvel.clemson.edu/auto
- Clemson's EMC website: http://www.cvel.clemson.edu/emc
- Missouri University of Science and Technology website: http://www.mst.edu/about/
- IPC — Association Connecting Electronics Industries website: http://www.ipc.org/default.aspx

Thank You and Remember:

**“Buildings have walls and halls.
People travel in the halls not the walls.**

**Circuits have traces and spaces.
Energy and signals travel in the spaces not the traces.”**

- Ralph Morrison

Please take time to fill out the course evaluation forms before you leave!

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