Addressing Vision Processing with the S32V MCUs

AMF-ACC-T1716

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External Use

Your Presenter

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Agenda

- Automotive Safety Trends / Euro NCAP
- Introduction to S32V for ADAS
- Vision Processing for Automotive Applications
- Pedestrian Detection
- Questions / Discussion

Automotive Safety Trends / Euro NCAP

Freescale AMPG for ADAS: Trends and Solutions Map

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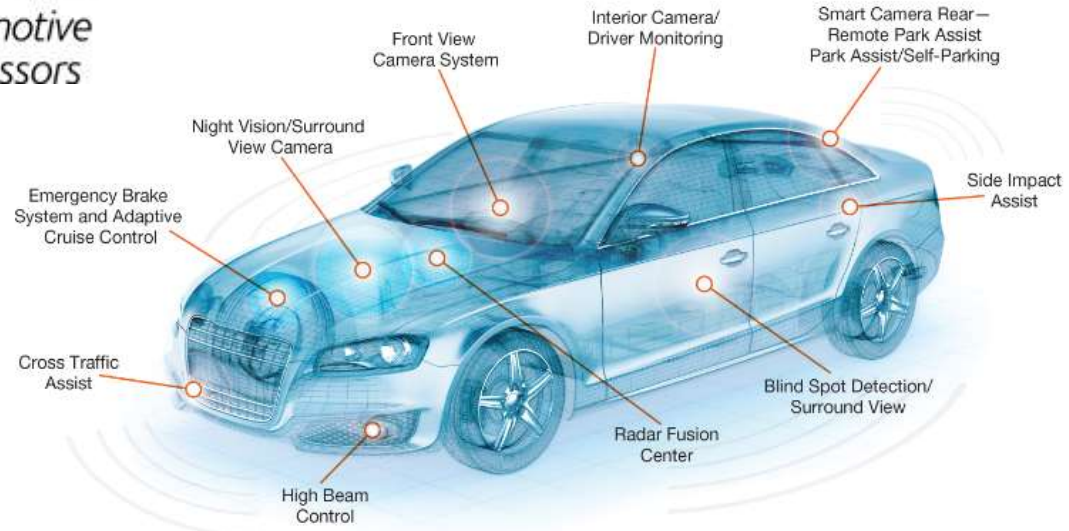
S32 Automotive Processors

Safe, Secure, Reliable solutions for Automotive ADAS



Assisted	Semi Automated	Fully Automated
• Sensor • Driver Active • Fail Safe	• Sensor Fusion & Maps • Co-Pilot • Dependable & Reliable	• Sensors & Maps & V2X • Driverless • Fail Operational

AMPG: Automotive Microcontroller Product Group

Euro NCAP Roadmap Driver / Pedestrian

Assisted

- *NCAP 2016: Lane detect, pedestrian detection, ACC*
- *Automotive safety (ASIL B) as driver is active*
- *Classic machine learning for mono front view rear view*
- *2D/3D surround view*

Semi-Automated

- *Active **steering**, active emergency **braking**, HW platoon and self park*
- *Automotive safety (ASIL B - C) with security*
- *Optical flow, sensor fusion & sophisticated classifiers*

Fully Automated

- *360° **Sensing**; 3D high accuracy environmental model*
- *Fully automated vehicle & fail operational system*
- *Deep learning and advanced machine vision with integrated V2X*

Driver Protection

AEB City

Front + Side Update

Farside Occupant Protect

Pedestrian Protection

Bonnet

Flex Bumber

Upper Leg

AEB Pedestrian

AEB Cyclist

2013 2014 2015 2016 2017 2018 2019

Source: The European New Car Assessment Programme / Freescale

Introduction to S32V MCU for ADAS

Key Features of the S32V

- **Performance:** Complementary high performance processing units working in parallel to deliver best in class computational capability at lowest power
- **Quality:** Committed to the highest levels of product quality through zero defect methodology, quality certifications and product qualification
- **Safety & Security:** Designed from the ground up to meet the highest automotive functional safety standard (ISO 26262); embedded security against IP theft and hacking
- **Flexibility:** Open programming models, supported by off-the-shelf RTOS & tools, Enabled by 360º EcoSystem – allows customers to differentiate and reduces cost/time-to-market

S32V a New Class of Chips for Vision in Automotive

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S32 Automotive Processors

The first automotive vision SoC with the requisite reliability, safety and security measures to automate and 'co-pilot' a self-aware car.

Applications

Front Camera

Rear Camera

360° Surround View

Sensor Data Fusion

Freescale's S32V234:

- *Designed to exacting automotive requirements*
- *Manufactured for robustness and long term automotive reliability*
- *Designed for but not limited to ISO 26262 ASIL B*
- *Hardware security encryption to protect against malicious hacking*
- *Easy to program*

Freescale S32V Processors: Building the Foundation

- Simplify The Experience

  “It can take up to 50-man-years to move my ADAS vision application from one HW platform to another....”

  Freescale customer

Key Freescale Eco-System Partnerships:

IP — cognivue CORPORATION

- Partnership to deliver image processing IP and software
- APEX Partner Program
- CogniVue was acquired by FSL in 2015

RTOS Tools — Green Hills SOFTWARE

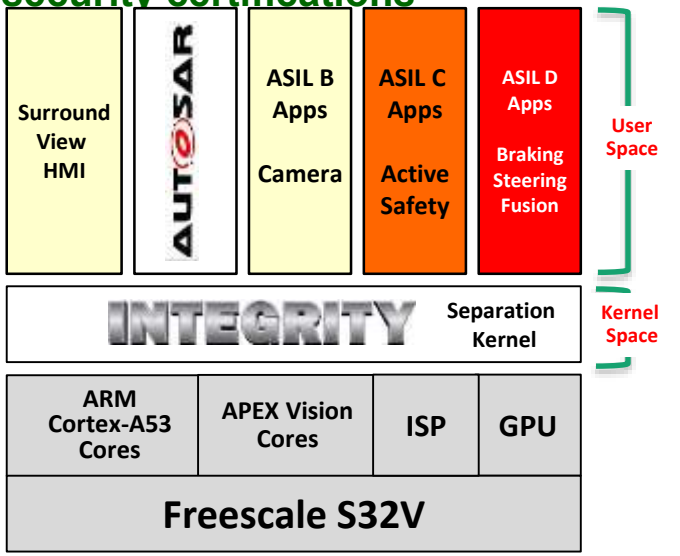
- Partnership to deliver RTOS & Toolchain
- Dependable, Reliable, Predictable

Soft-ware — Neusoft Automotives

- Partnership to deliver algorithms, demo’s and full vision applications

Green Hills SW Platform for ADAS – S32V200

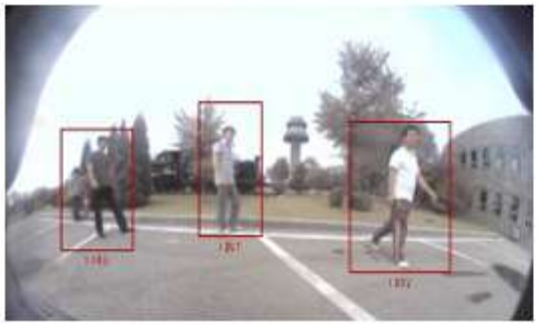
- **Proven safety and security – the world's highest safety & security certifications**
  - Experts in ISO 26262, IEC 61508, EN 50128
  - EAL6+ Common Criteria Separation Kernel Protection Profile
  - Safety OS & BSP, Certified Dev. Tools, Safety Consulting/Training
- **Trusted Execution Platform**
  - Safely isolate applications in secure partitions for guaranteed Freedom From Interference
  - Concurrently execute applications with mixed ASIL levels
  - Run AUTOSAR applications in secure partition
  - Securely run guest OSes Linux/Android on Multivisor hypervisor
- **Optimized for S32V Acceleration Units**
  - Dual APEX 2 vision processing cores
  - Image Signal Processing (ISP) core
  - 64-bit Quad ARM Cortex®-A53 + NEON SIMD unit
  - 3D GPU, OpenCV, GPGPU processing
- **Powerful 64-bit development tools**
  - High performance EEMBC® record-setting 64-bit C/C++ compilers
  - MULTI multicore debugger, TimeMachine Trace Suite
  - Code quality tools MISRA C/C++, Run-Time Error Checking and DoubleCheck™ static analyzer
- **GHS Ecosystem**
  - Neusoft ADAS software – Pedestrian Detection, Traffic Sign Recognition, Lane Departure Warning, Surround View
  - Freescale Vision SDK integration
  - OpenGL graphics partners
  - Support for ARM® Fast Model simulator



Mature and proven separation kernel assures Freedom from Interference

ADAS Applications by Neusoft Automotives for S32V

Neusoft Automotives



Pedestrian Detection

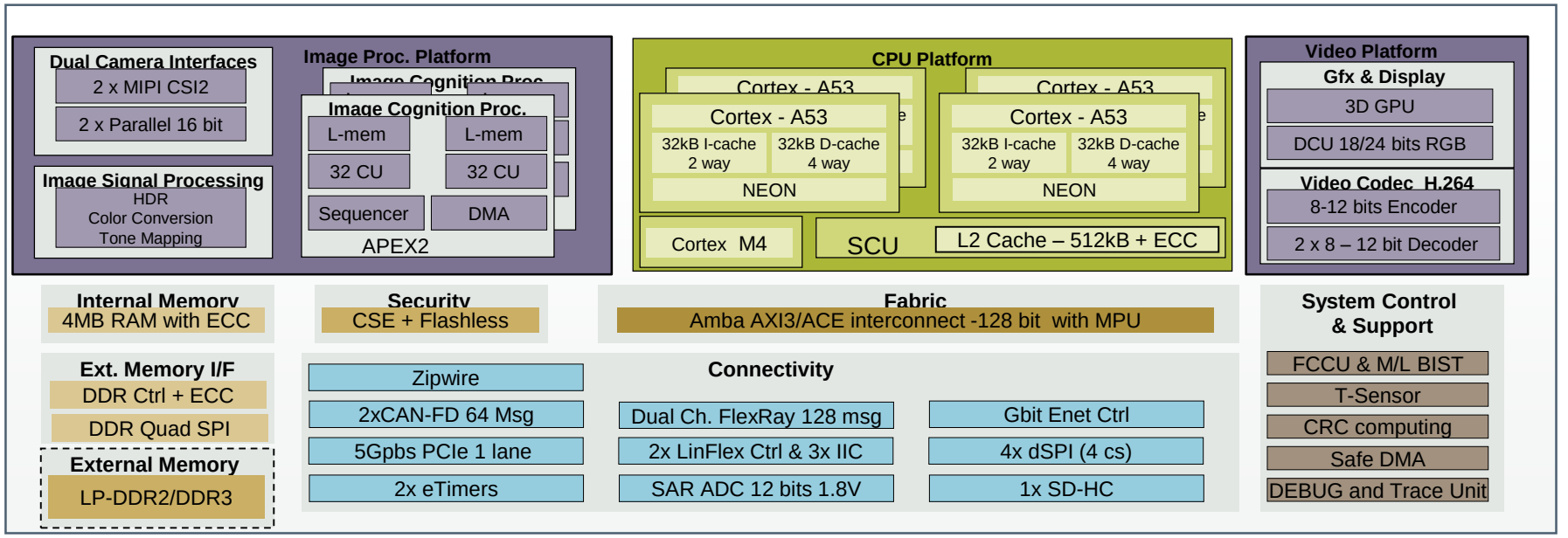
Traffic Sign Detection

Lane Detection

- ADAS Application Selection offer:
  - Surrounding assessment from camera input
  - Real-time performance
  - Robustness

Vision Processing for Automotive Applications

S32V234 – ADAS MCU – Performance, Safety and Flexibility



Specifications:

- **CPU1-4:** ARM Cortex-A53 @1GHz, L1/L2 cache with ECC & Neon
- **CPU5:** Cortex -M4 for IO control with I/D Cache and ECC
- **ICP:** 2 x APEX2 (APU-64 CU each) at 500MHz
- **GPU:** GC3000 from Vivante
- **Package:** 17x17**FC-BGA**
- **Temp Range (Ta):** -40 to 105°C, 125 °C Tj, AEC-Q100 Grade 2
- **Main Supply:** 3.3V IO and 0.94V Core - external PMU + DDR rails

Key Features:

- **F. Safety:** developed as per ISO 26262 with target ASILB
- **SW Enablement:** OpenCL Tools for ICP, GPU, NEON.
- **Video Codec:** H.264 Encoder (8-12 bit) + Decoder (8-12 bit)
- **DRAM:** External LPDDR2 & DDR3 supported
- **Security:** SHE compliant Crypto Security Engine
- **Surround 3D**: 3D unified architecture. 19/38Gflops at 600MHz
- **Video dist. Network**: 2X Mipi CIS2 – 4 Virtual channels each
- **Connectivity**: Gigabit Ethernet, PCIe, FD-Can & Flexray

Use Cases:

- **Front-vision camera**
- **4 cameras Smart surround view**
- **Fusion Box**

The Vision Pipeline

Each engine offers the best efficiency for certain type of functions. To let the complete system work at highest efficiency, each engine needs to work in parallel in pipeline mode.

Image sensor → Processing and Conditioning → Filtering → Edge Extraction → Transformation Feature Classification → Info Extraction → Other algos

GPU → Display

Typical ISP functions

Black level and dead pixel processing
Black level, vignetting
Exposure control, color balance analysis
Geometric distortion corrections,
Chromatic aberration correction
HDR
De-mosaic Bayer pattern
RGB->YUV420, channel gain
Spatial de-noise
Gamma correction
Image xcaling

Typical *APEX* functions

Sobel
Median, Laplace, Gaussian
Histogram
Integral image
FAST
BRIEF
ORB
FIR
Kirsch
Color conversion: RGB to YUV…
Harris corner
Shi–Tomasi corner
Lens correction
Canny,
Block matching

ARM53 Neon
APEX2

ARM53 Neon

The Vision Pipeline

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Image sensor

play

traction

Other algos

Typical ISP
Black level and dead
Black level, vignetting
Exposure control, colo
Geometric distortion c
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Gamma correction
Image xcaling

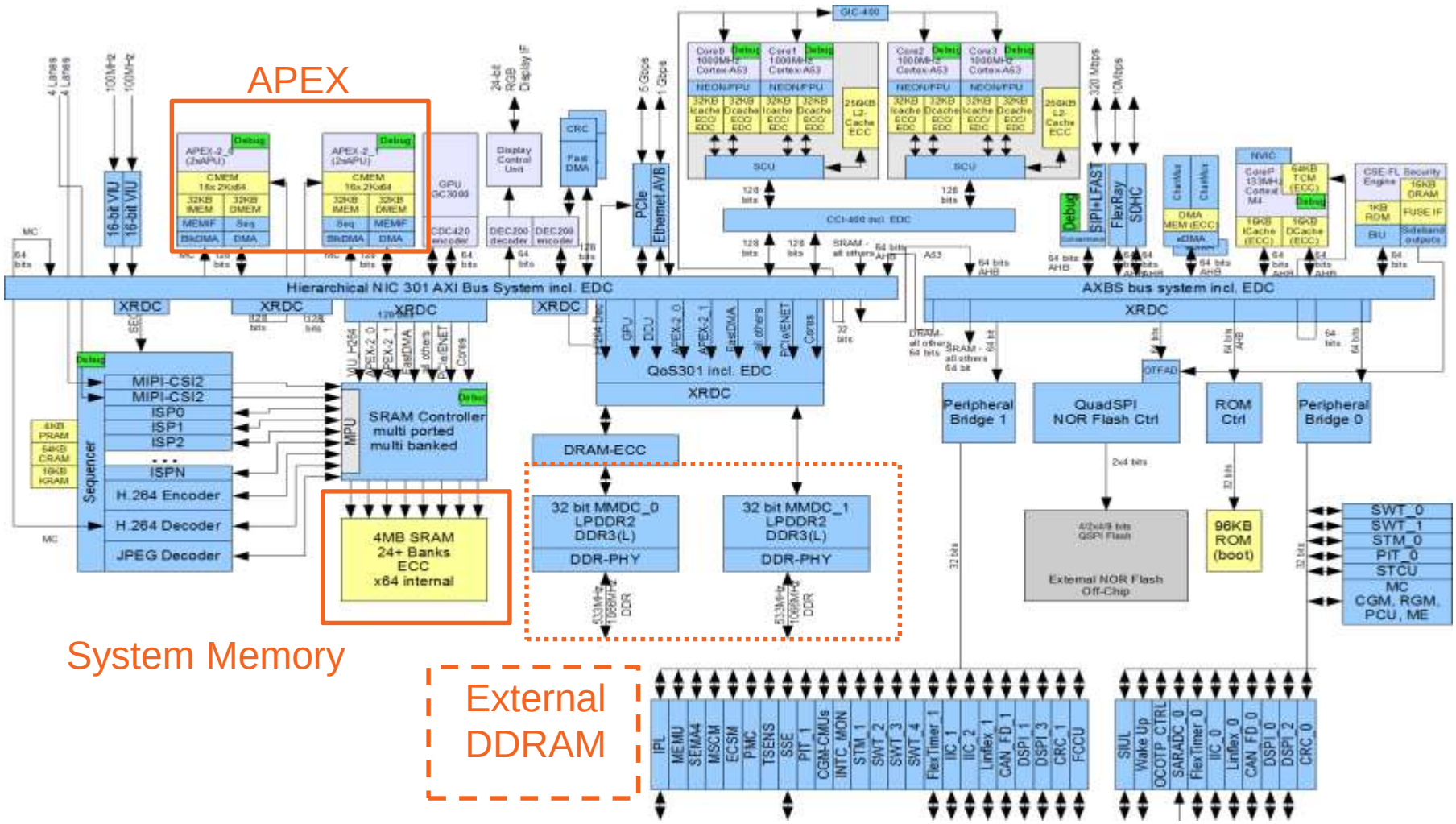
ARM53
Neon

Lens correction
Canny,
Block matching

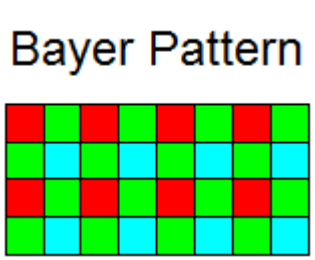
S32V family brings:

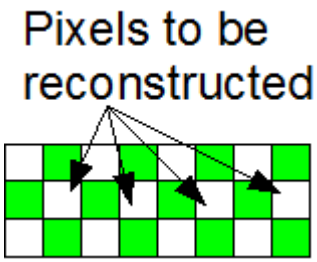
- **High Performance**
- **Low Power**
- **Functional Safety (ISO 26262)**

S32V234 Block diagram



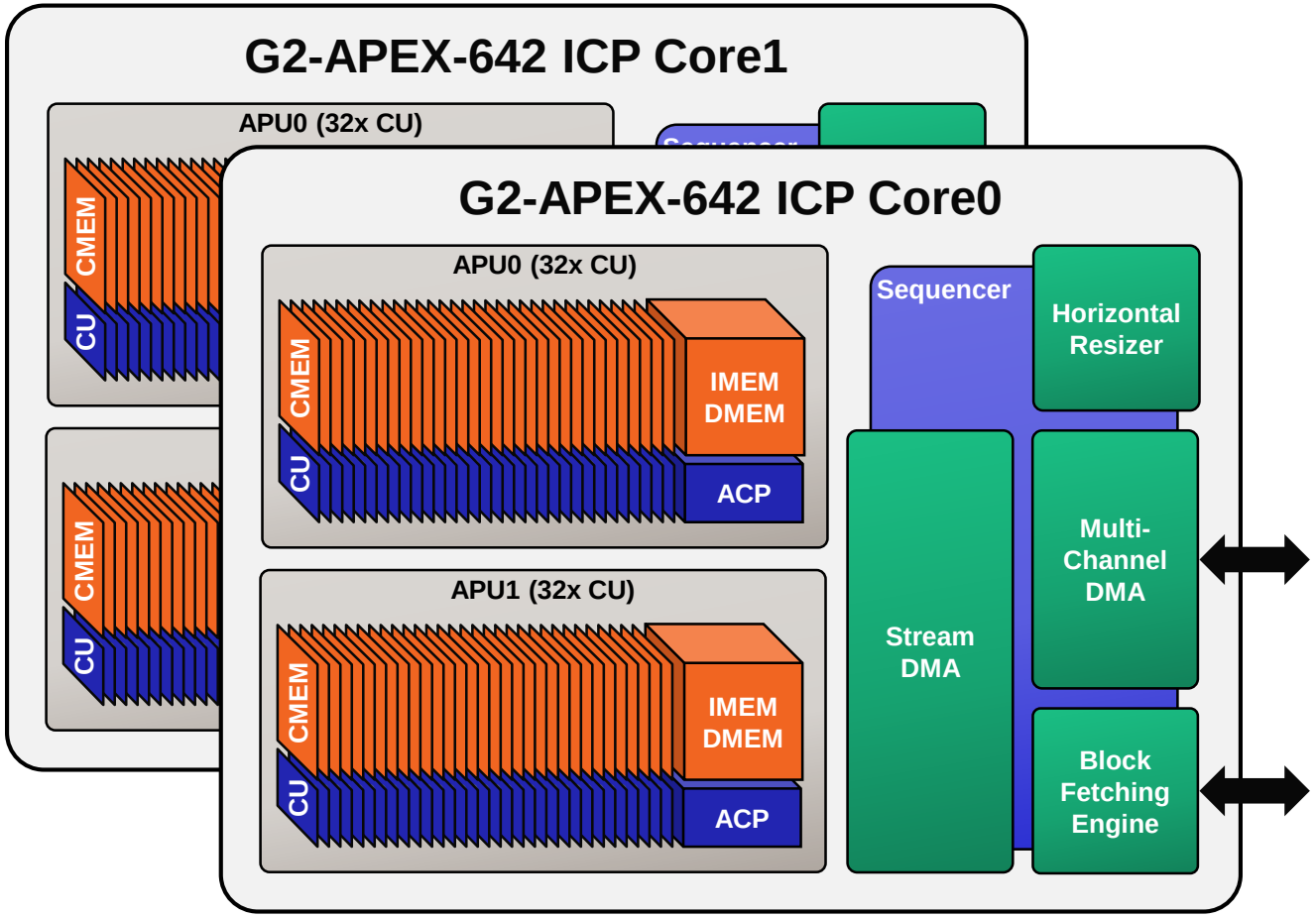
ISP – HDR, Tone Mapping, Color Balancing, ….





Function	Type
Black level and dead pixel processing	LUT, linked list
Black level, Vignetting	2D LUT (low res)
Exposure control, color balance analysis	Histogram/stats
Geometric distortion corrections, chromatic aberration	Calibrated per color, 2D LUT (low res), bi-linear interpolation
HDR	LUT, α-blending, conditional selection of exposure plane
De-mosaic Bayer pattern	Reconstruct missing green values based on edge direction
RGB->YUV420, channel gain	Matrix multiplication, factors based on histogram
Spatial de-noise	Edge aware thresholding
Gamma correction	LUT
Image scaling	Anti-alias (FIR), bi-linear interpolation

G2-APEX-642 (aka APEX2) – Image Cognition Processor

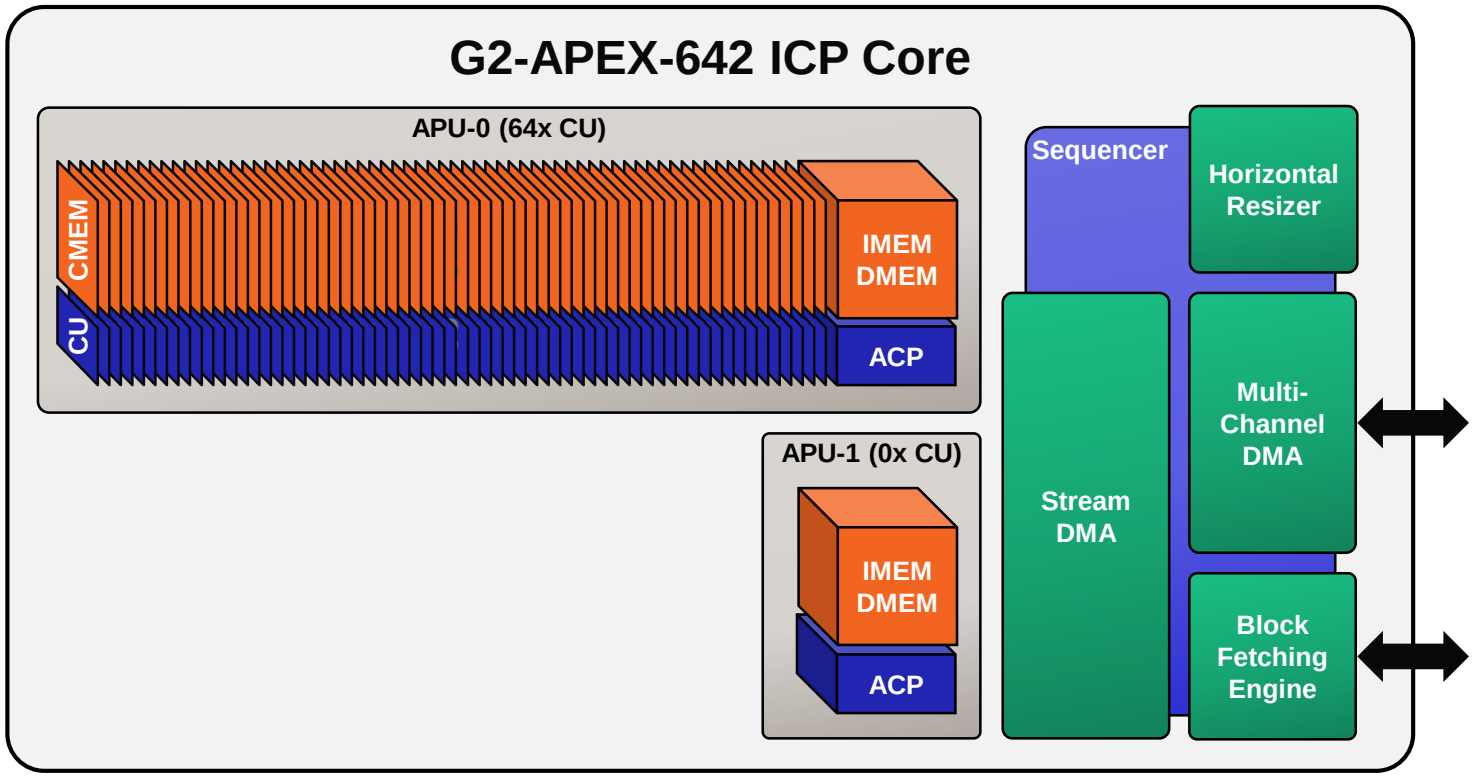


S32V234 has 2x G2-APEX-642 cores

2x APEX-642 = 2 x (2x 32 CUs , 2x ACP, 256KByte ram) =

128 CUs 4 ACP 512KByte ram + 2 complex DMA engines

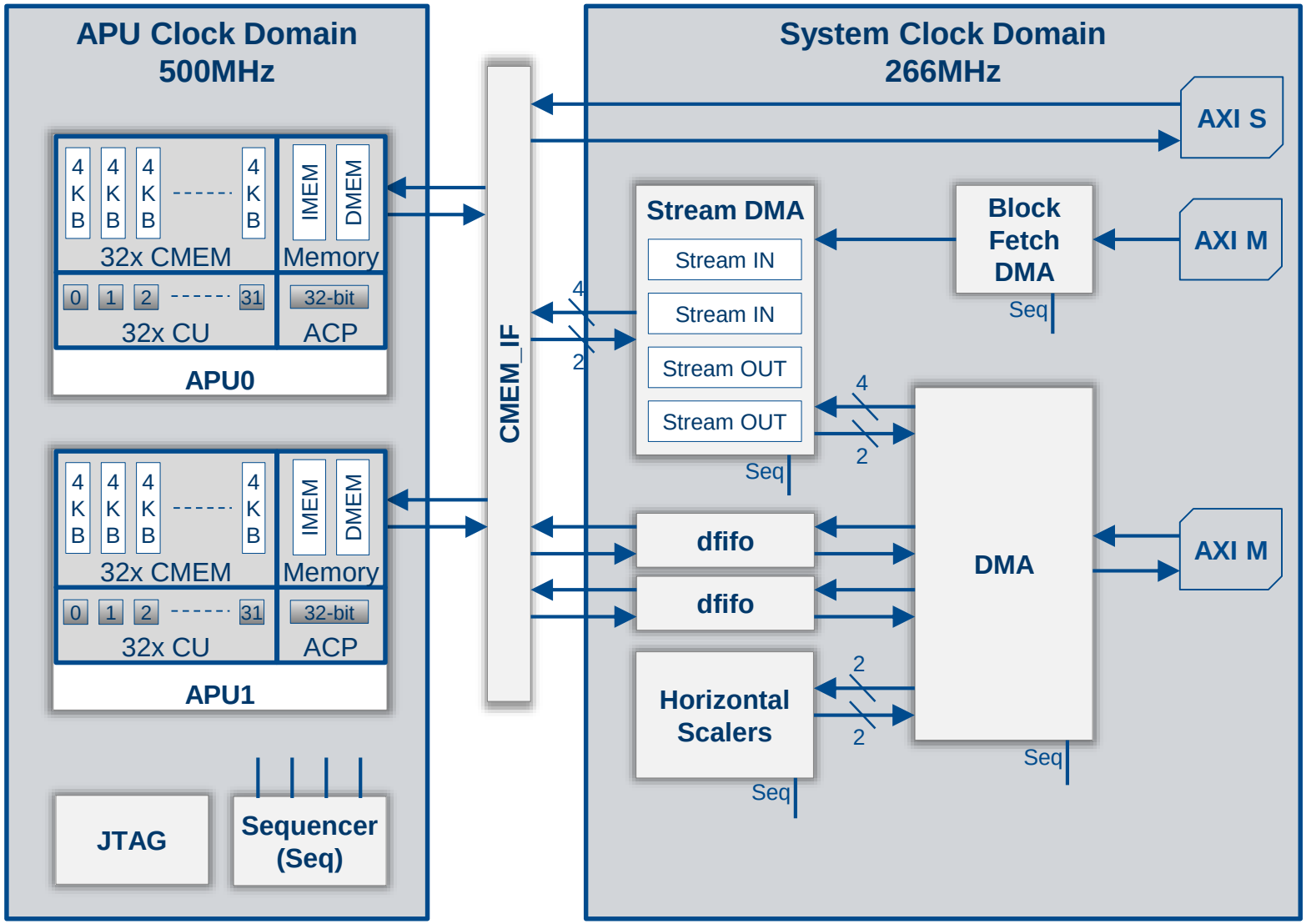
Configurable Image Cognition Processor



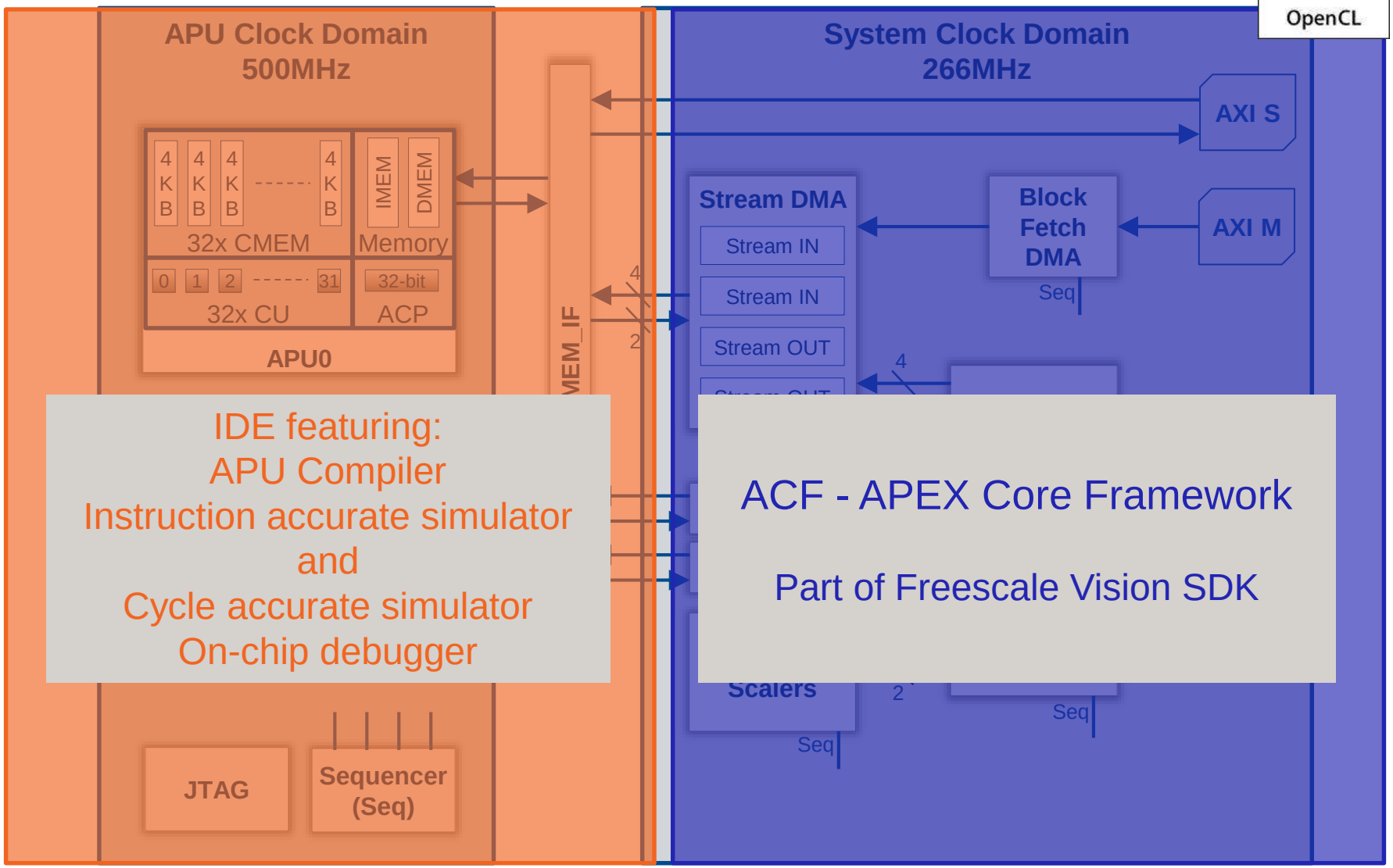
Each G2-APEX-642 APU can borrow the CUs from other APU within the same core

The other ACP remains functional but can't perform vector operations

G2-APEX-642 Hardware Architecture



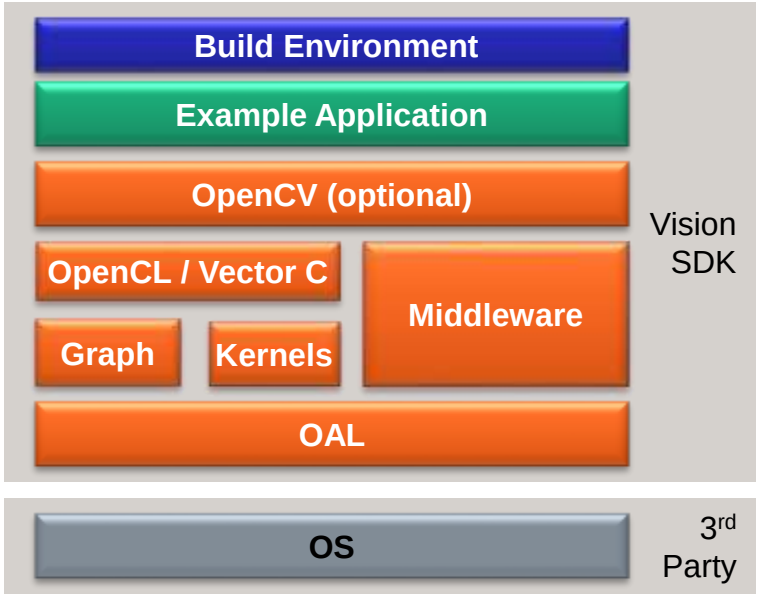
G2-APEX-642 Core Programming Tools



Programming APEX core is as easy as any other MCU

- C/C++ high level programming language
  - Compiler handles the appropriate generation of scalar/vectors unified instructions and manages registers and memory references
  - The scalar processing unit is programmed liked any other MCU
  - The vector processing unit handles vector data with equivalent scalar instructions
  - Dedicated vector instructions also exists such as vif, vany, vall, vget, vput, as well as optimized intrinsics for some operations
- NO ASSEMBLER required
  - Compiler has internal optimized inline assembler instructions as well as in-code compiler annotations such as for loop optimization
- Optimized Vision Library
  - APEX-CV provides high level algorithms and low level kernels for the APEX core to speed up vision application development

Vision SDK Overview



- **Build Environment**
  - Makefile based
  - Single point of build for all components
- **Rich set of demo applications including source code**
  - Face detection
  - ORB homography
  - LDW
  - And many more

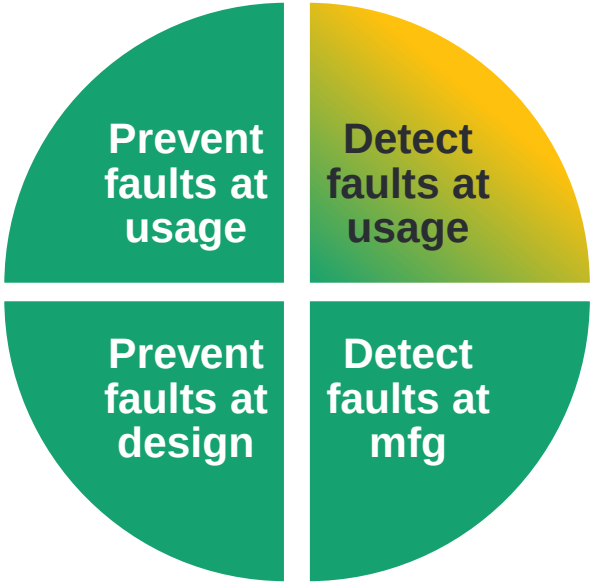
- **Basic example applications including sources**
  - Histogram
  - Gaussian blur
  - Rotate
  - Image/movie capture, display control
- **Rich set of optimized kernels including source code**
  - Arithmentic: add, diff, dot division, dot sqr, max, min, ...
  - Filter: gauss, gratient, saturate, median, sobel, ...
  - Object/feature detection: haar, lbp, fast9, harris, sad
  - Geometry: bilinear interpolation, hough transform, rotate, ...
  - Full list of kernels included in Vision SDK
- **OpenCV Integration**
  - Seamless integration of HW accelerators with OpenCV (for supported OSs)
  - Integration of sensor drivers and display output
- **Middleware**
  - Driver and SW integration of Vision processing pipeline (HW accelerators, sensor I/O, display)
- **OS Support**
  - OS Abstraction Layer allows for easy support of arbitrary operating systems
  - Greenhills INTEGRITY support
  - Linux OS support
  - Bare metal
- **Not included**
  - Operating System
  - Commercial tools (compiler, debugger)

ISO 26262 Fault Prevention and Control Measures

... implemented as **product** features
against **random** faults (architecture, function)

- ***Examples***:
  - *Triple voted flip flops*
  - *ECC on memories*
  - *Redundant vias*
  - *Ultra low alpha mould compound to reduce effect of radiation*

- ***Examples***:
  - *ISO Design Process*
  - *Design Margin*
  - *Process Margin*
  - *Automotive Process Package*



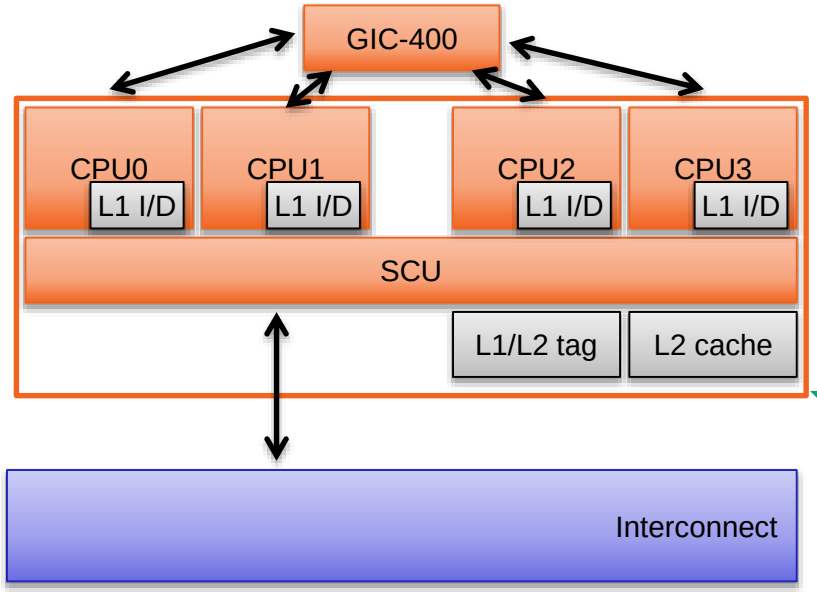
- ***Examples***:
  - *Independent compute engines – 2 x MP2 cluster*
  - *Independent checker engine – Safe State engine*
  - *EDC on memory and buses*
  - *Logic BIST/Memory BIST*
  - *Voltage/temperature monitors*

- ***Examples***:
  - *Wafer level stress testing*
  - *Test in Burn-In*
  - *Iddq testing*
  - *AEC-Q100 qualification*

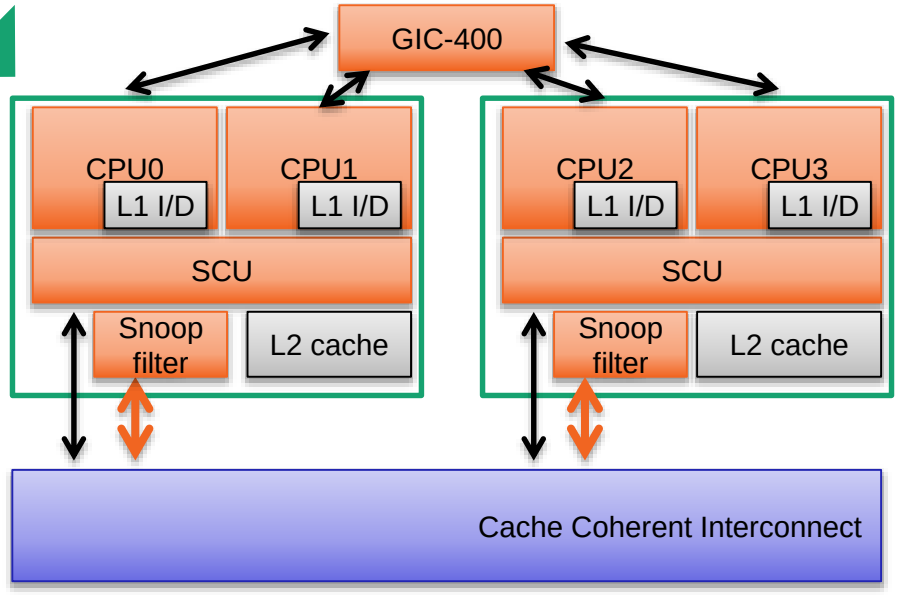
... during **develoment** and **production**
against **systematic** faults (process, procedures)

ISO 26262 can NOT be retro-fitted to a device

Core-Cluster Separation



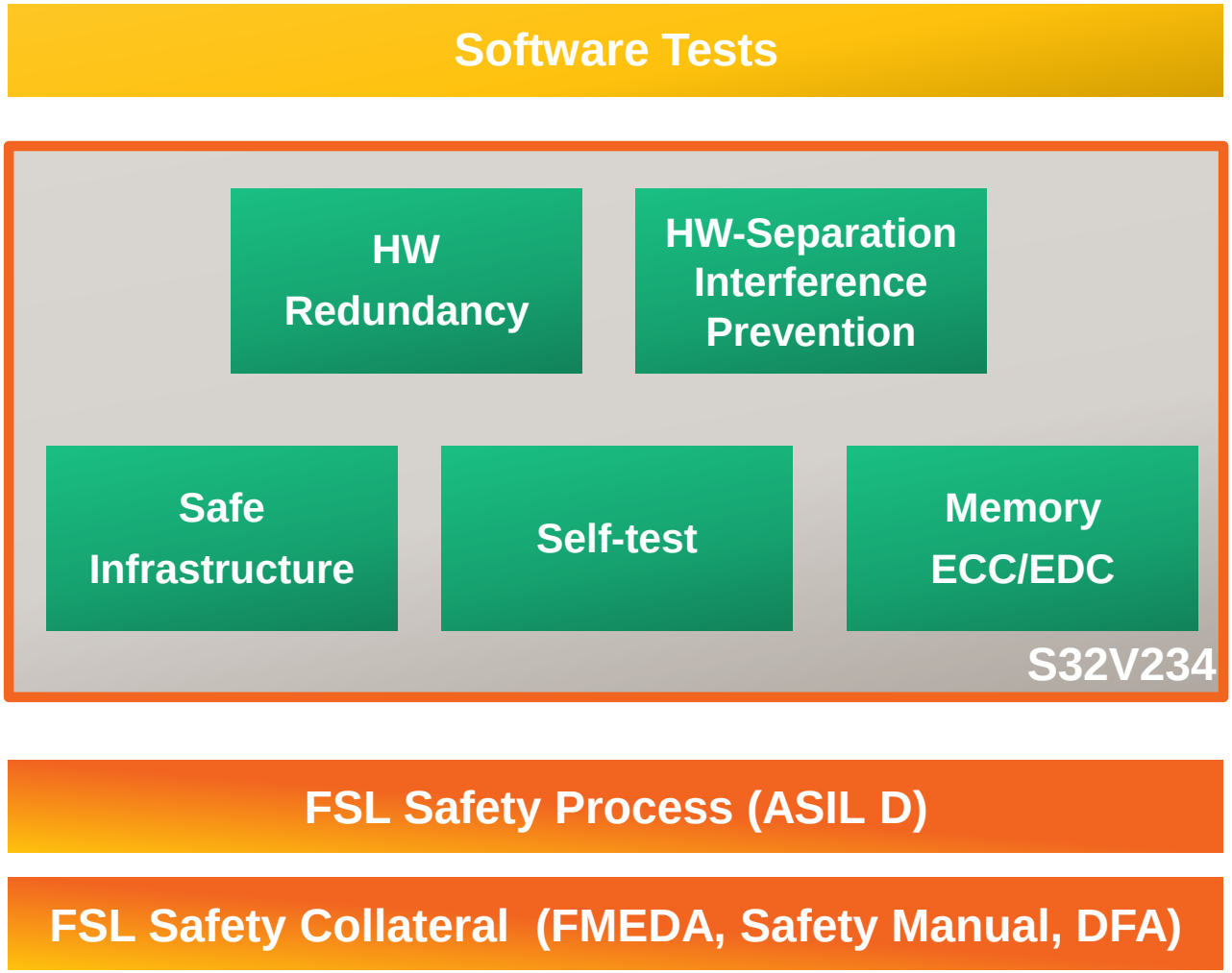
- SCU is a potential common cause of failure for all CPUs
- L1/L2 tag RAM & control failures affect all CPUs
- L2 data RAM failures affect all CPUs



- CPU can snoop data from other cluster
- Snoop can be disabled for predefined regions
- HW-separation of clusters

SCU: Snoop Control Unit

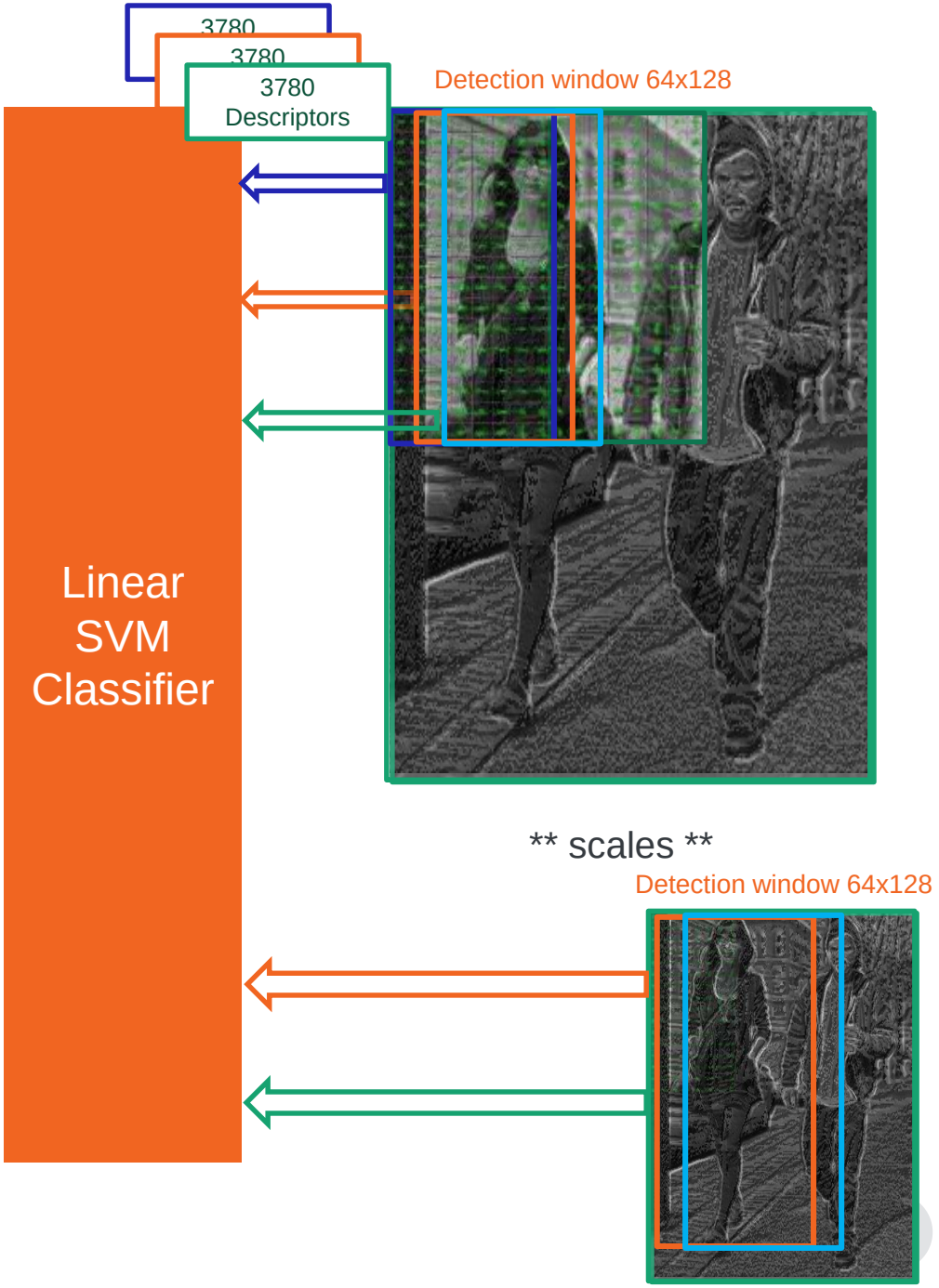
S32V234: targeting – but not limited to – ASIL B applications



Pedestrian Detection

HOG + SVM

- Detection window is moved around the image
- HOG descriptor are collected at each detection window and
- Given to Linear SVM for classification



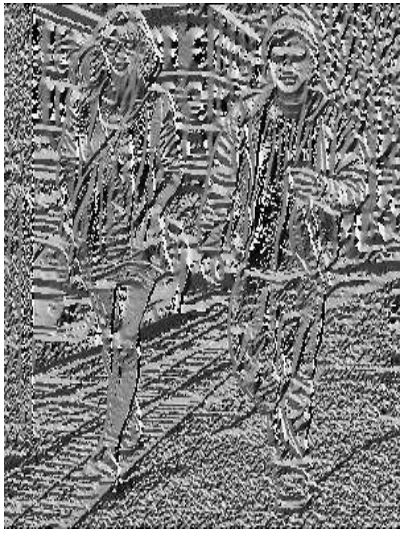
Processing steps involved to obtain Histogram of oriented Gradients(HOG)

Source Image

Dx = Sobel X $[-1, 0, 1]$

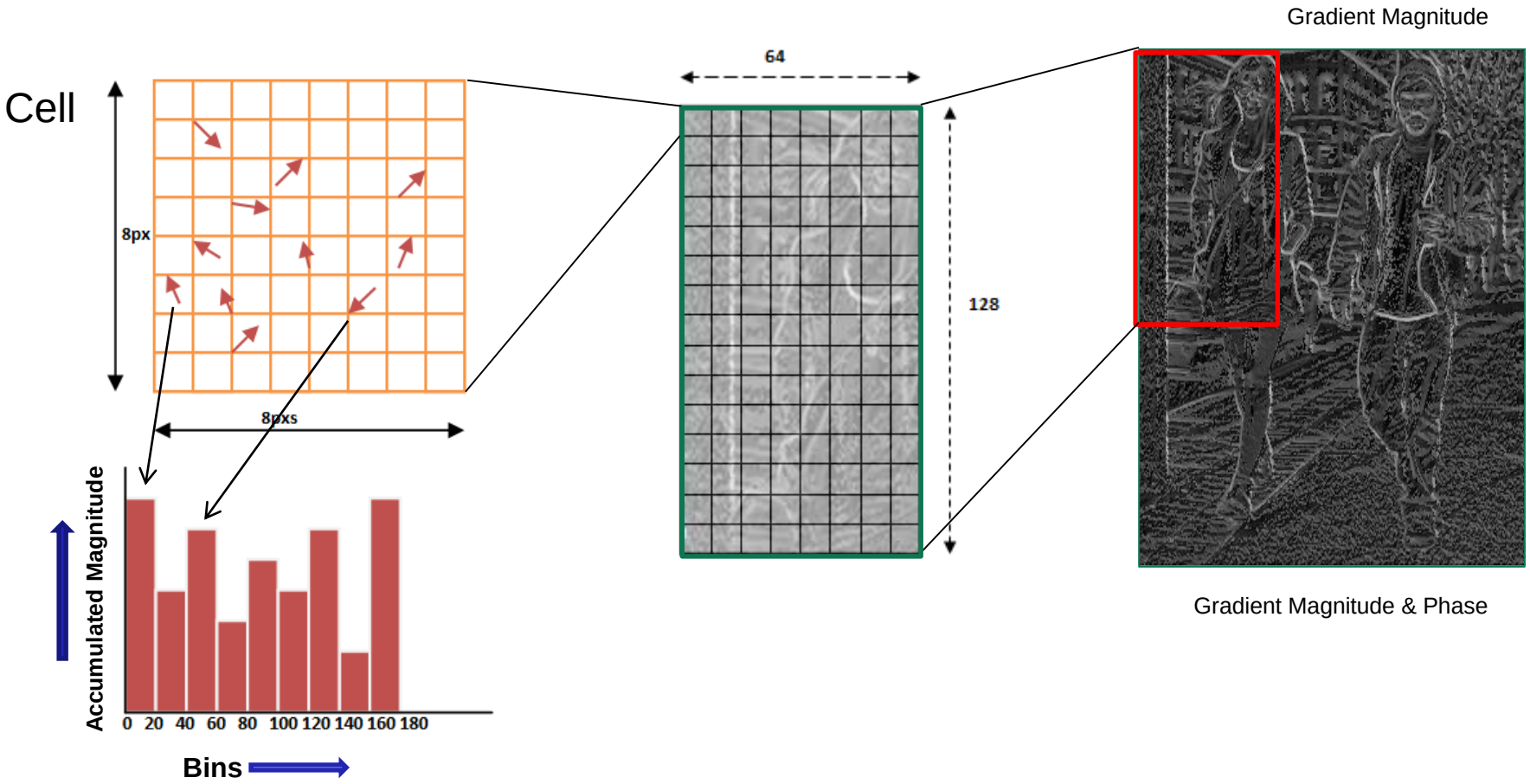
Dy = Sobel Y $\begin{bmatrix} -1 \\ 0 \\ 1 \end{bmatrix}$

Gradient Magnitude **= abs(Dx) + abs(Dy)**

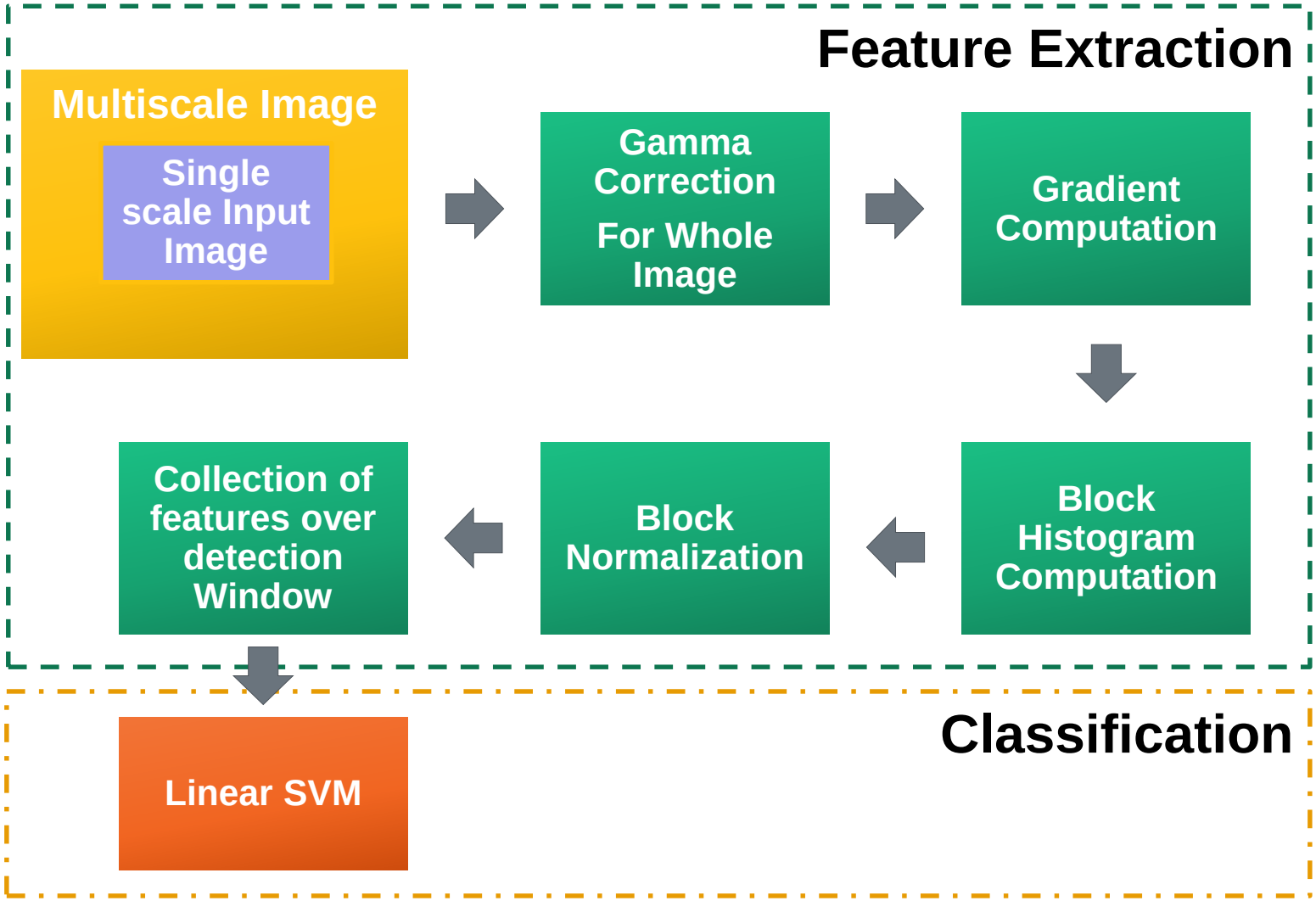


Gradient phase **= atan2(Dy,Dx)**

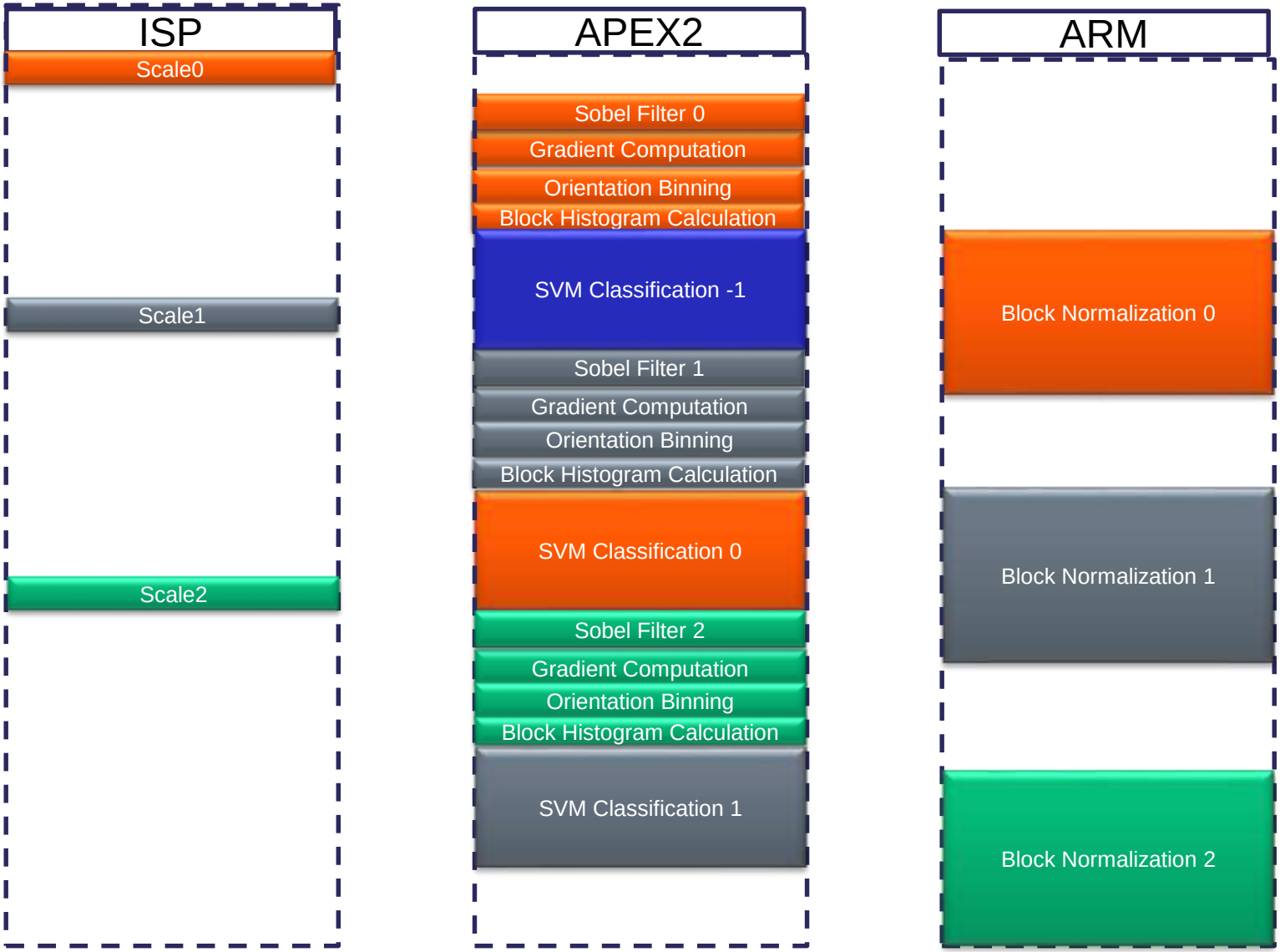
What are Histogram of Oriented Gradients



Overview of HOG Algorithm



Pedestrian Detection Pipeline



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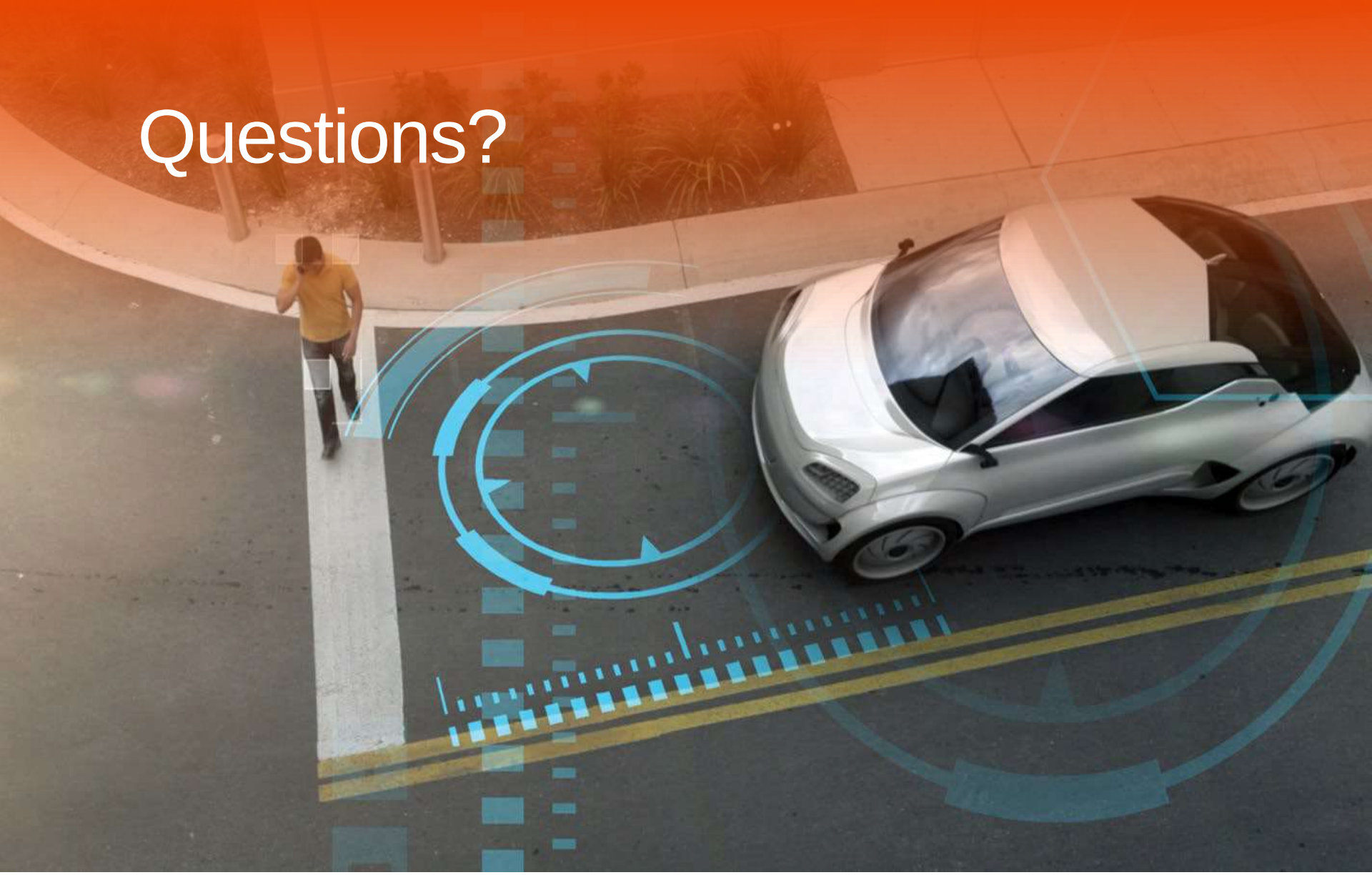
Questions?



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