



DRAM Controller Optimization for i.MX Applications Processors

AMF-ACC-T1661

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Overview

- This presentation is covering the tools used by the Freescale engineers to optimize and debug DRAM interface on i.MX
 - This is not a deep dive in to various i.MX DRAM controller designs
 - This is not a training on various DRAM technologies
 - Please refer to the JEDEC specs
- These tools are available for use by our customers through the assigned Freescale FAE's.
- New Information:
 - The Processor Expert tool will not be modified to perform the DDR Stress calibration routines and the actual stress testing.
 - Only the “unsupported” tools will be available.



Agenda

- Board bring-up: where DRAM bring-up fits in
 - Introduce the tools used for DRAM bring-up
- DDR3 Script Aid/DRAM Register Programming Aid
 - Introduction/Overview
 - Walkthrough
- DRAM Stress Test
 - Introduction/Overview
 - How to run; deep dive into sub-tests
- DRAM Calibration Overview
- Board Design Considerations

Checklist Item	Details	owner	Findings & Status
The following items need to be completed serially			
Visual Inspection	Check major components to make sure nothing has been misplaced or rotated before applying power.		
Verify all SoC voltage rails	Confirm that the voltages match to what is required in the data sheet. Be sure to check voltages not only at the voltage source, but also as close to the SoC as possible, like on a bypass capacitor. This will reveal any IR drops on the board which will later cause issues. Ideally all of the SoC voltage rails should be checked, but noteworthy voltages include those that power the core, internal logic, boot devices, and DRAM (which is often overlooked).		
Verify power up sequence	Verify that Power On Reset (POR) is de-asserted (high) after all power rails have come up and are stable. Refer to the SoC data sheet for details on power up sequencing. This is an important if not overlooked process as many complex processors may be very sensitive to the proper power up sequencing.		
Measure/probe input clocks (32kHz, 24MHz, others)	Without a properly running clock, the SoC will not function properly. Look for jitter and noise.		
JTAG connectivity (RV-ICE, Lauterbach, Macraigor, etc)	This is one of the most fundamental and basic access points to the SoC to allow the debug and execution of low level code.		
Access internal RAM	Verify basic operation of the SoC in system. The on chip internal RAM starts at an address defined in the reference manual (normally in the Memory Map chapter) and includes the density of the on chip RAM. A basic test would simply be to perform a write-read-verify to the internal RAM via a JTAG debugger. No software initialization should be necessary to access internal RAM.		
Run basic DDR initialization and test memory	Assuming the use of a JTAG debugger, run the DDR initialization and open a debugger memory window pointing to the DDR memory map starting address. Try writing a few words and verify if they can be read correctly. If not, re-check the DDR initialization sequence and if the DDR has been correctly soldered onto the board. It is also recommended to re-check the schematic to ensure the DDR memory has been connected to the SoC correctly. In some cases, a DRAM calibration routine may need to be executed, see next row.		
Run DRAM Stress test (some SoC's include a DRAM calibration routine)	A unit test that focuses on the robustness of the DRAM interface. Downloaded through JTAG debugger into internal RAM. Some SoC's DRAM stress test, like MX6Q, includes option to run DRAM calibration.		
The following items may be worked on in parallel with other bring up tasks			
Verify CLKO outputs (measure and verify default clock frequencies for desired clock output options); this assumes that the board design supports probing of the CLKO pin.	This ensures that the corresponding clock is working and that the PLLs are working. This step does require some chip initialization, for example via the JTAG debugger, to properly set up the IOMUX to output CLKO and to set up the Clock Control Module to output the desired clock. Refer to the External Signals and Pin Multiplexing, CCM, and IOMUX sections of the SoC's reference manual for further details.		
Measure boot mode frequencies (set the boot mode switch for each boot mode and measure the following, depending on what is available in the system): - NAND (probe CE to verify boot, measure RE frequency) - SPI-NOR (probe slave select and measure clock freq) - MMC/SD (measure clock freq)	This verifies connectivity (at least for a few signals) between the SoC and boot device and that the boot mode signals are properly set.		
Run other unit tests	Once the DRAM interface has been verified as stable, the next step is to run other stand-alone unit tests to ensure the robustness of other peripherals and external components.		

Tools for DRAM Bring-up and Debug

DRAM Register Programming aid

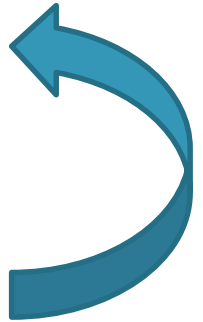
Run basic DDR initialization and test memory

Assuming the use of a JTAG debugger, run the **DDR initialization** and open a debugger memory window pointing to the DDR memory map starting address. Try writing a few words and verify if they can be read correctly. If not, re-check the **DDR initialization** sequence and if the DDR has been correctly soldered onto the board. It is also recommended to re-check the schematic to ensure the DDR memory has been connected to the SoC correctly. In some cases, a DRAM calibration routine may need to be executed, see next row.

Run DRAM Stress test (some SoC's include a DRAM calibration routine)

A unit test that focuses on the robustness of the DRAM interface. Downloaded through JTAG debugger into internal RAM. Some SoC's **DRAM stress test**, like MX6Q, includes option to run DRAM calibration.

DRAM Stress Test



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DDR3 Script Aid – Intro

- Tool to help create DRAM init scripts for specific memory types
 - Mainly used to help program JEDEC timing parameters
 - tRCD, tRC, tRFC, etc...
 - and for different DRAM parameters like rows, cols, and chip selects
 - Excel spread sheet based, transparent, ease-of-use
 - “Automatically” creates RVD init script (.inc or .ds file)
 - Easy to convert RVD to Lauterbach script format.

DDR3 Script Aid – Intro

(Continued)

- Based on scripts provided by design/validation
- Anyone can use it, change it, fix it, etc...
- Each Programming Aid tool based on DRAM tech (DDR3, DDR2, LPDDR2, etc)
- What's been created to date:
 - MX7D: DDR3, LPDDR3
 - MX6DQ: DDR3, LPDDR2; MX6DL: DDR3, LPDDR2; MX6SL: DDR3, LPDDR2; MX6SX: DDR3, LPDDR2
 - MX50: mDDR, LPDDR2, DDR2
 - MX28: mDDR, DDR2

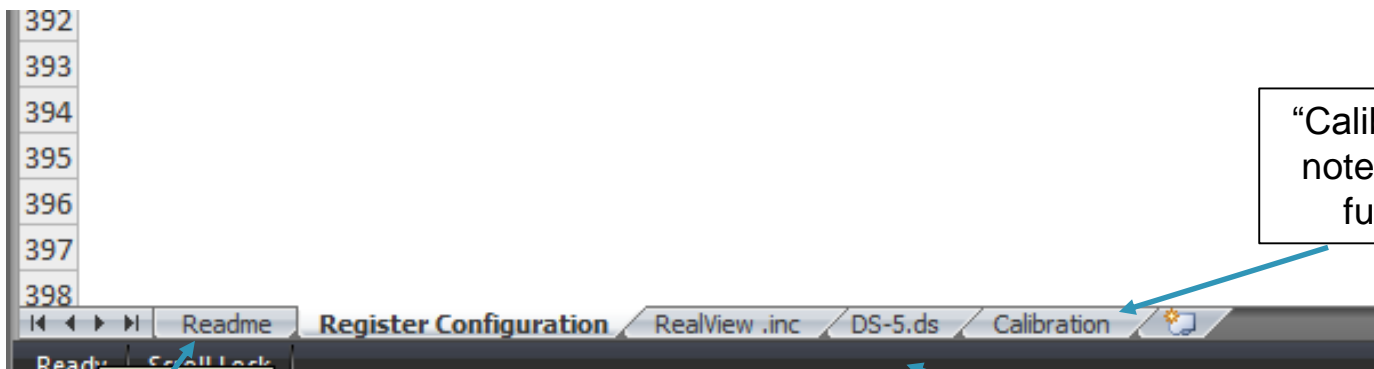
DDR3 Script Aid – Intro

(Continued)

- Originated due to Denali controller on MX28 and MX50
 - Denali controller complex, many registers to program
 - Required use of Denali-specific tools available only to factory engineers (due to Denali license); burden on factory support
 - Register programming aid offers more visibility on how the DRAM controller is being programmed
- Register programming aid tool concept carried over to i.MX FIL base controllers, starting with MX53 and MX6 series
- Tools are available to customers through assigned FAE's and the Community <https://community.freescale.com/docs/DOC-236354>

DDR3 Script Aid – Usage Overview

- There is a different Script Aid for each DRAM variety. For this training, we will focus on DDR3.



The screenshot shows the DDR3 Script Aid tool interface. The top bar contains several tabs: "Readme", "Register Configuration", "RealView .inc", "DS-5.ds", and "Calibration". A vertical scroll bar on the left shows line numbers 392 through 398. A gear icon is visible on the right side of the tool bar. Five callout boxes with arrows point to specific tabs, providing detailed information about their contents.

Start with “Readme” tab for overview on how to use the tool

“Register Configuration” tab is where the user inputs various DRAM parameters

“RealView .inc” tab contains the automatically generated DRAM initialization in the ARM RVD vernacular

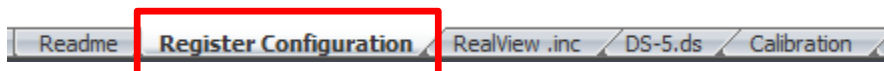
“DS-5.ds” tab contains the automatically generated DRAM initialization in the ARM DS5 format

“Calibration” tab contains notes on the calibration function in the tool

DDR3 Script Aid – Usage Overview

(Continued)

- Step 1: Obtain the desired DRAM data sheet from the DRAM vendor.
- Step 2: Update the Device Information table to include the DRAM information



Device Information	
Manufacturer:	Micron
Memory part number:	MT41K128M16JT-125
Memory type:	DDR3-1600
DRAM density (Gb)	2
DRAM Bus Width	16
Number of Banks	8
Number of ROW Addresses	14
Number of COLUMN Addresses	10
Page Size (K)	2
Self-Refresh Temperature (SRT)	Normal
tRCD=tRP=CL (ns)	13.75
tRC Min (ns)	48.75
tRAS Min (ns)	35

This information calculates the timing information required for the "RealView .inc" and "DS-5.ds" tabs.

DDR3 Script Aid – Usage Overview

(Continued)

- Step 2 continued:

Manufacturer: Type chip vendor name in the row

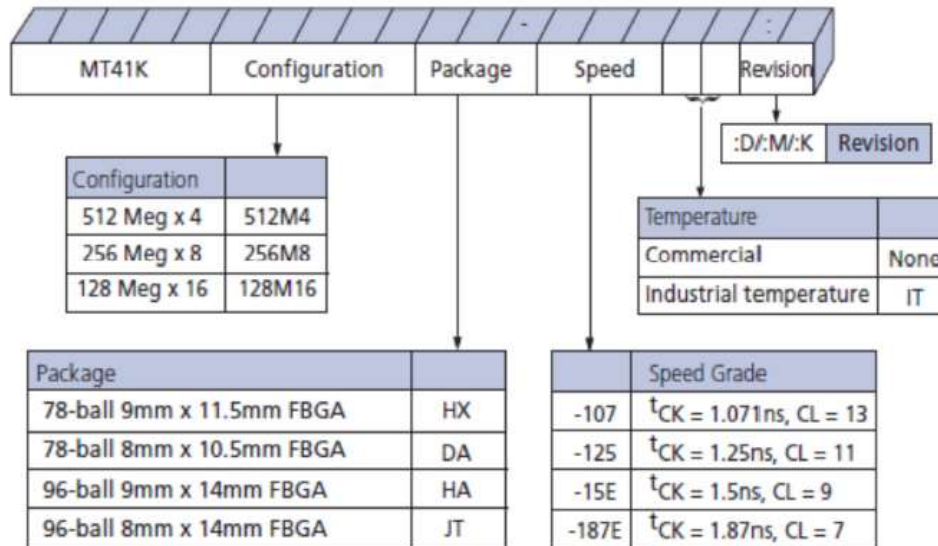
Memory part number: Type full part number of chip

Memory Type: Select chip type in the list of this row

Memory type:	DDR3-1600
DRAM density (Gb)	DDR3-800 DDR3-1066 DDR3-1333 DDR3-1600
DRAM Bus Width	
Number of Banks	

Device Information	
Manufacturer	Micron
Memory part number	MT41K128M16JT-125
Memory type	DDR3-1600
DRAM density (Gb)	2
DRAM Bus Width	16
Number of Banks	8
Number of ROW Addresses	14
Number of COLUMN Addresses	10
Page Size (K)	2
Self-Refresh Temperature (SRT)	Normal
tRCD=tRP=CL (ns)	13.75
tRC Min (ns)	48.75
tRAS Min (ns)	35

Example Part Number: MT41K256M8DA-125:K



DDR3 Script Aid – Usage Overview

(Continued)

- Step 2 continued:

DRAM density (Gb): Select density of each chip

DRAM density (Gb)	2
DRAM Bus Width	1
Number of Banks	2
Number of ROW Addresses	4
	8

DRAM Bus Width: Select bus width of each chip

DRAM Bus Width	16
Number of Banks	4
Number of ROW Addresses	8
	16

Number of Banks: Type band numbers of chip in this row
MT41K128M16JT-125 Datasheet shows 16Mx16x8banks

Number of Banks	8
-----------------	---

Device Information	
Manufacturer	Micron
Memory part number	MT41K128M16JT-125
Memory type	DDR3-1600
DRAM density (Gb)	2
DRAM Bus Width	16
Number of Banks	8
Number of ROW Addresses	14
Number of COLUMN Addresses	10
Page Size (K)	2
Self-Refresh Temperature (SRT)	Normal
tRCD=tRP=CL (ns)	13.75
tRC Min (ns)	48.75
tRAS Min (ns)	35

DDR3L SDRAM

MT41K512M4 – 64 Meg x 4 x 8 banks

MT41K256M8 – 32 Meg x 8 x 8 banks

MT41K128M16 – 16 Meg x 16 x 8 banks

DDR3 Script Aid – Usage Overview

(Continued)

- Step 2 continued:

Number of ROWs: Select number of Rows

Number of COLUMNs: Select number of Columns

MT41K128M16JT-125 Datasheet shows below info.

Parameter	128 Meg x 16
Configuration	16 Meg x 16 x 8 banks
Refresh count	8K
Row address	16K A[13:0]
Bank address	8 BA[2:0]
Column address	1K A[9:0]

Device Information	
Manufacturer	Micron
Memory part number	MT41K128M16JT-125
Memory type	DDR3-1600
DRAM density (Gb)	2
DRAM Bus Width	16
Number of Banks	8
Number of ROW Addresses	14
Number of COLUMN Addresses	10
Page Size (K)	2
Self-Refresh Temperature (SRT)	Normal
tRCD=tRP=CL (ns)	13.75
tRC Min (ns)	48.75
tRAS Min (ns)	35

Number of ROW Addresses	14
Number of COLUMN Addresses	11
Page Size (K)	12
Self-Refresh Temperature (SRT)	13
tRCD=tRP=CL (ns)	14
	15
	16

Number of COLUMN Addresses	10
Page Size (K)	9
Self-Refresh Temperature (SRT)	10
tRCD=tRP=CL (ns)	11
	12

DDR3 Script Aid – Usage Overview

(Continued)

- Step 2 continued:

Page Size (K): Select page size of chip in the list of this row

Page Size (K)	2
Self-Refresh Temperature (SRT)	1
	2

Self-Refresh Temperature (SRT): Select SRT type of chip in the list of this row

Self-Refresh Temperature (SRT)	Normal
tRCD=tRP=CL (ns)	Normal
	Extended

Device Information	
Manufacturer	Micron
Memory part number	MT41K129M16JT-125
Memory type	DDR3-1600
DRAM density (Gb)	2
DRAM Bus Width	16
Number of Banks	8
Number of ROW Addresses	14
Number of COLUMN Addresses	10
Page Size (K)	2
Self-Refresh Temperature (SRT)	Normal
tRCD=tRP=CL (ns)	13.75
tRC Min (ns)	48.75
tRAS Min (ns)	35

DDR3 Script Aid – Usage Overview

(Continued)

- Step 2 continued:

tRCD=tRP=CL (ns): tRCD/tRP/CL parameters

tRC Min (ns): Type tRC parameter of chip in this row

tRAS Min (ns): Type tRAS parameter of chip in this row

MT41K128M16JT-125 Datasheet shows below info.

Device Information	
Manufacturer	Micron
Memory part number	MT41K128M16JT-125
Memory type	DDR3-1600
DRAM density (Gb)	2
DRAM Bus Width	16
Number of Banks	8
Number of ROW Addresses	14
Number of COLUMN Addresses	10
Page Size (K)	2
Self-Refresh Temperature (SRT)	Normal
tRCD=tRP=CL (ns)	13.75
tRC Min (ns)	48.75
tRAS Min (ns)	35

Speed Grade	Data Rate (MT/s)	Target tRCD-tRP-CL	tRCD (ns)	tRP (ns)	CL (ns)
-125 ^{1,2}	1600	11-11-11	13.75	13.75	13.75

DDR3L-1600 Speed Bin		-125 ¹		Unit
CL-tRCD-tRP		11-11-11		
Parameter	Symbol	Min	Max	
ACTIVATE-to-ACTIVATE or REFRESH command period	t _{RC}	48.75	–	ns
ACTIVATE-to-PRECHARGE command period	t _{RAS}	35	9 x t _{REFI}	ns

DDR3 Script Aid – Usage Overview

(Continued)

- Step 3: Input System Information

System Information	
i.Mx Part	i.Mx6Q
Bus Width	64
Density per chip select (Gb)	8
Number of Chip Selects used	1
Total DRAM Density (Gb)	8
DRAM Clock Freq (MHz)	528
DRAM Clock Cycle Time (ns)	1.894
Address Mirror (for CS1)	Disable

All this information can be found on the schematic!

DDR3 Script Aid – Usage Overview

(Continued)

- Step 3 (continued): Input System Information

i.Mx Part	i.Mx6Q
Bus Width	i.Mx6Q
Density per chip select (Gb)	i.Mx6D
Number of Chip Selects used	i.Mx6DL
	i.Mx6S

Bus Width	64
Density per chip select (Gb)	16
Number of Chip Selects used	32
	64

Density per chip select (Gb)	8
Number of Chip Selects used	2
Total DRAM Density (Gb)	4
DRAM Clock Freq (MHz)	8
	16
	32

Number of Chip Selects used	1
Total DRAM Density (Gb)	1
	2

DRAM Clock Freq (MHz)	528
DRAM Clock Cycle Time (ns)	400
	528

Address Mirror (for CS1)	Disable
SI Configuration	Enable
	Disable

System Information	
i.Mx Part	i.Mx6Q
Bus Width	64
Density per chip select (Gb)	8
Number of Chip Selects used	1
Total DRAM Density (Gb)	8
DRAM Clock Freq (MHz)	528
DRAM Clock Cycle Time (ns)	1.894
Address Mirror (for CS1)	Disable

DDR3 Script Aid – Usage Overview

(Continued)

- Step 4: Input Signal Integrity Configuration

Generally speaking, drive strength (DSE) and ODT should match the characteristic impedance of transmission line. Actual test report of trace impedance should be delivered by PCB vendor.

For example, for a 45 ohm single ended trace DSE can select 40ohm or 48ohm. A 100ohm differential trace DSE of one pin of pair can also select 48ohm etc.

SI Configuration	
DRAM DSE Setting - DQ/DQM (ohm)	48
DRAM DSE Setting - ADDR/CMD/CTL (ohm)	48
DRAM DSE Setting - CK (ohm)	48
DRAM DSE Setting - DQS (ohm)	48
System ODT Setting (ohm)	60

DDR3 Script Aid – Usage Overview

(Continued)

- Step 4 (continued): Input Signal Integrity Configuration

DRAM DSE Setting - DQ/DQM (ohm)	48
DRAM DSE Setting - ADDR/CMD/CTL (ohm)	34
	40
DRAM DSE Setting - CK (ohm)	48
DRAM DSE Setting - DQS (ohm)	60
	80
System ODT Setting (ohm)	120
	240

System ODT Setting (ohm)	60
	17
	20
	24
	30
	40
	60
	120
	Disable

SI Configuration	
DRAM DSE Setting - DQ/DQM (ohm)	48
DRAM DSE Setting - ADDR/CMD/CTL (ohm)	48
DRAM DSE Setting - CK (ohm)	48
DRAM DSE Setting - DQS (ohm)	48
System ODT Setting (ohm)	60

DDR3 Script Aid – Usage Overview

(Continued)

```

1 #=====
2 #init script for i.Mx6Q DDR3
3 #=====
4 mem      0x00000000      0xFFFFFFFF noverify
5 #=====
6 # Disable WDOG
7 #=====
8 mem set  0x020bc0c 16      0x30
9
10 #=====
11 # Enable all clocks (they are disabled by ROM code)
12 #=====
13 mem set  0x020c406 32      0xffffffff
14 mem set  0x020c406 32      0xffffffff
15 mem set  0x020c407 32      0xffffffff
16 mem set  0x020c407 32      0xffffffff
17 mem set  0x020c407 32      0xffffffff
18 mem set  0x020c407 32      0xffffffff
19 mem set  0x020c408 32      0xffffffff
20 mem set  0x020c408 32      0xffffffff
21
22 #=====
23 # IOMUX
24 #=====
25 #DDR IO TYPE:
26 mem set  0x020e07f 32      0x000C00c # IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE
27 mem set  0x020e07f 32      0x0000000 # IOMUXC_SW_PAD_CTL_GRP_DDRPKE
28
29 #CLOCK:
30 mem set  0x020e05f 32      0x0000002 # IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCLK_0
31 mem set  0x020e05f 32      0x0000002 # IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCLK_1
32

```

Step5: Review output

- DRAM initialization automatically generated per template
- Values in yellow are automatically updated from the “Register Configuration” tab
- No user input required in this tab



DDR3 Script Aid – Usage Overview

(Continued)

```
97 # For target board, may need to run write leveling calibration to fine tune these settings.
98 mem set      0x021b080c  32  0x00000000
99 mem set      0x021b0810  32  0x00000000
100 mem set     0x021b480c  32  0x00000000
101 mem set     0x021b4810  32  0x00000000
102
103 #Read DQS Gating calibration
104 mem set     0x021b083c  32  0x00000000 # MPDGCTRL0 PHY0
105 mem set     0x021b0840  32  0x00000000 # MPDGCTRL1 PHY0
106 mem set     0x021b483c  32  0x00000000 # MPDGCTRL0 PHY1
107 mem set     0x021b4840  32  0x00000000 # MPDGCTRL1 PHY1
108
109 #Read calibration
110 mem set     0x021b0848  32  0x40404040 # MPRDDLCTL PHY0
111 mem set     0x021b4848  32  0x40404040 # MPRDDLCTL PHY1
112
113 #Write calibration
114 mem set     0x021b0850  32  0x40404040 # MPWRDLCTL PHY0
115 mem set     0x021b4850  32  0x40404040 # MPWRDLCTL PHY1
...
```

Step5 (continued) : Review output

- Items in red are placeholders until calibration is run.
- Update these values with the results from the DDR Stress Tester

Readme Register Configuration RealView .inc **DS-5.ds** Calibration

DDR3 Script Aid – Usage Overview (Continued)

```
H:\IMX\IMX61x\Tools & Boards\DRAM Stress Test\Init files\MX6Q_v1.6_+ARD_RevD_Results.inc - Notepad++
File Edit Search View Encoding Language Settings Macro Run Plugins Window ?
i.MX6_DCIC_Init.ds drivers-mxc-thermal-thermal.c Modem Options.txt i.MX6_DCIC_Init-3.ds init_Review notes.c MX6C
1 //=====
2 //init script for i.MX6Q DDR3 ARD
3 //=====
4 // Revision History
5 // v01
6
7 // 2-5-2015 LZ
8 // Added values from DDR Stress Test from ARD Quad Rev D
9 //=====
10
11 wait = on
12 //=====
13 // Disable WDOG
14 //=====
15 //setmem /16 0x020bc000 = 0x30
16
17 //=====
18 // Enable all clocks (they are disabled by ROM code)
19 //=====
20 setmem /32 0x020c4068 = 0xffffffff
21 setmem /32 0x020c406c = 0xffffffff
22 setmem /32 0x020c4070 = 0xffffffff
23 setmem /32 0x020c4074 = 0xffffffff
24 setmem /32 0x020c4078 = 0xffffffff
25 setmem /32 0x020c407c = 0xffffffff
26 setmem /32 0x020c4080 = 0xffffffff
27 setmem /32 0x020c4084 = 0xffffffff
28
29 //=====
30 // IOMUX
31 //=====
32 //DDR IO TYPE:
33 setmem /32 0x020e0798 = 0x00000000 // IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE
34 setmem /32 0x020e0758 = 0x00000000 // IOMUXC_SW_PAD_CTL_GRP_DDRPKE
35
36 //CLOCK:
37 setmem /32 0x020e0588 = 0x00000030 // IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCLK_0
38 setmem /32 0x020e0594 = 0x00000030 // IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCLK_1
39
40 //ADDRESS:
```

Step5 (continued) : Review output

- Copy the content of the tab to a text file

Now we are ready to run the DDR Stress Tester!



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DRAM Stress Test – Overview and History

- Took years to develop, constantly evolving to catch elusive DRAM failures
- Compilation of various DRAM sub tests
 - Each sub test contains various data patterns/methods to stress the DRAM interface
 - Started with a few tests using memcpy and various data patterns (1's and 0's; A's and 5's; pseudo-random, etc)
 - Each new SoC/board presented new DRAM challenges/issues
 - New tests were created to debug
 - Historically, each test was run one-by-one, took time
 - Tests were compiled together into one overall test
 - Each test now called sub-test, executed through a function call
 - Marked beginning of 'stress test', sub-tests run in a loop, overnight
 - Cache enabled – important, needed to mimic OS-type transactions; more stress
 - Increment DRAM frequency – method to stress interface accounting for variations in PVT
 - How much above frequency max is considered ample?
 - Historically 30MHz or more seemed good
 - Useful for gathering statistical data; outliers may point to other issues

DRAM Stress Test – Overview and History

(Continued)

- Non-OS test to exercise DRAM interface
 - Non-OS: easier than OS to catch/debug DRAM failures
 - Used by factory as part of DRAM validation
 - Helps diagnose but doesn't fix DDR problems
- Purpose: Root out potential signal integrity issues due to inadequate board layout
 - Primarily uses sequential bursts of back-to-back data looking for simultaneous switching noise (SSN)
 - Validation vehicle that reports how robust DRAM interface is given current set of parameters (i.e. drive strength settings, timing parameters, board layout, etc)
- Runs from internal RAM
 - Device under test is DRAM itself, don't execute out of same memory being tested
 - Download to IRAM via JTAG debugger tools (RVD, Lauterbach, Macraigor)
 - Now available in a USB version.
- FAE's are able to provide tailored code if necessary.
 - Any debugger that supports specific SoC ARM core and elf should work
 - Freescale is not responsible to test every debugger or debug it if doesn't work on other debuggers

DRAM Stress Test – Overview and History

(Continued)

- Once DRAM stress test passes with ample margin, are we guaranteed the OS will never fail due to DRAM issues?
 - High degree of confidence DRAM robust enough, but...
 - OS is still the most stressful, particularly an OS stress test like Bonnie++
 - Recommend to run any OS stress tests to double check
 - Currently Supported SoC:
 - MX28, MX508, MX51, MX53, MX6DQ, MX6DL, MX6SL, MX6SX, MX7D
 - No plans to back port to older legacy processors
 - Issues encountered as some only have 16KB of IRAM
- Challenges
 - Test becoming too big to fit inside IRAM (128KB becoming a limiting factor)
 - When new sub-tests are created, no plan in place to back port to older processors

DRAM Stress Test – How to Run

Debugger Setup

- Stress test outputs `.elf`; can be run from various debuggers
 - Debuggers necessary for new SoC bring up; highly useful for new board bring up
 - Debuggers don't rely on bootloaders or on anything running
 - Simply having a debugger connect means the SoC is powered up and running
 - Debuggers allow user to quickly test fundamental DRAM init
 - Open a debugger memory window to perform simple write-read-verify
 - There are less expensive debugger options than ARM (like Macraigor)
 - May give up some functionality, but good enough to download and run stress test
- To run from a debugger
 - Run DRAM init (`.inc`, `.ds`, `.cmm`, `.mac`)
 - Refer to DRAM Script Aid/Register Programming Aid tool
 - Load and run the `.elf` file

DRAM Stress Test – Classic Version

Serial Port Setup

- DRAM Stress Test uses serial port output (UART) for user interaction
- Terminal program needed on the Host PC
 - Host PC: Tera Term or Hyperterminal
 - Ensure the correct COM port usage
 - Set up:

```
BAUD RATE - 115200
DATA - 8 bit
PARITY- none
STOP - 1bit
FLOW CONTROL - none
```
- Once test runs, look for output messages on the terminal
 - Various run control options
 - DRAM density to test, frequency range, etc

DRAM Stress Test – USB Version

- DDR Stress Tester uses USB for user interaction
 - Makes use of *.bin file output.
 - Need all in the same windows folder:
 - USB executable file (DDR_Stress_Tester)
 - *.bin file generated from source code (ddr-stress-test-<TGT>.bin)
 - *.inc script file (from Register Programming Aid)
 - Enter at the command prompt:
 - DDR_STRESS_TESTER -t <tgt> -df <prog_aid> -usb
 - DDR_STRESS_TESTER -h (Help Menu)
 - Allowable targets are the i.MX6x Family
 - Test runs from Windows command prompt just like Serial UART Terminal.

DRAM Stress Test – USB Version

```
Administrator: C:\Windows\System32\cmd.exe - DDR_Stress_Tester -t mx6x -df MX6Q_v1.5_SD.inc
Copyright (c) 2009 Microsoft Corporation. All rights reserved.

C:\Windows\System32>h:

H:\>cd binary2

H:\binary2>DDR_Stress_Tester -t mx6x -df MX6Q_v1.5_SD.inc
MX6DQ opened.
HAB_TYPE: DEVELOP
Image loading...
download Image to IRAM OK

Re-open MX6x device.
Running DDR test..., press "ESC" key to exit.

*****
  DDR Stress Test (1.0.3) for MX6DQ
  Build: Jun 25 2014, 12:09:21
  Freescale Semiconductor, Inc.
*****

=====DDR configuration=====
BOOT_CFG3[5-4]: 0x00, Single DDR channel.
DDR type is DDR3
Data width: 64, bank num: 8
Row size: 14, col size: 10
Chip select CSD0 is used
Density per chip select: 1024MB
=====

What ARM core speed would you like to run?
Type 0 for 650MHz, 1 for 800MHz, 2 for 1GHz, 3 for 1.2GHz
  ARM set to 800MHz

Please select the DDR density per chip select (in bytes) on the board
Type 0 for 2GB; 1 for 1GB; 2 for 512MB; 3 for 256MB; 4 for 128MB; 5 for 64MB; 6
for 32MB
For maximum supported density (4GB), we can only access up to 3.75GB. Type 9 to
select this
```



DRAM Stress Test – GUI Version (V2.10)

- The new Community Tool has a GUI interface to the Stress Test.
- The Script Aid (Excel) tool is still required to configure and generate the script.

The screenshot shows the 'Freescale DDR Stress Tester' application window. The interface includes several configuration sections:

- Configuration:** TARGET (MX6DQ), ARM Speed (800MHz), Verify DCD Address (checked), DDR Density (512MB), DDR CS (0), and DDR channel (0). A 'Download' button is present.
- Script Management:** A 'Load Init Script' button and a text field containing the path 'H:\I.MX\IMX61x\Tools & Boards\DS5\ARD_MX6Q_DDR3_init_v1.ds'.
- DDR Calibration:** A text field for 'DDR Freq(MHz)' set to 528, with 'DDR Calibration' and 'Save Result' buttons.
- DDR Stress Test:** An 'Over Night Test' checkbox (unchecked), 'Start Freq(MHz)' (450), and 'End Freq(MHz)' (528) fields, with 'DDR Stress Test' and 'Save Result' buttons.

The main output area displays the following text:

```
ARM Clock set to 800MHz
-----
DDR configuration
BOOT_CFG3[5-4]: 0x00. Single DDR channel.
DDR type is DDR3
Data width: 32, bank num: 8
Row size: 14, col size: 10
No chip select is enabled
Density per chip select: 512MB
-----
Current Temperature: 40
-----
DDR Stress Test Iteration 1
```


Are We There Yet?

- The script is configured for our hardware, the DDR Stress test is running, can we start testing DDR on our board now?
- Nope. We still need to calibrate for our hardware.
- Luckily the DDR Stress Test and the i.MX6 can provide the required calibration data.

Agenda

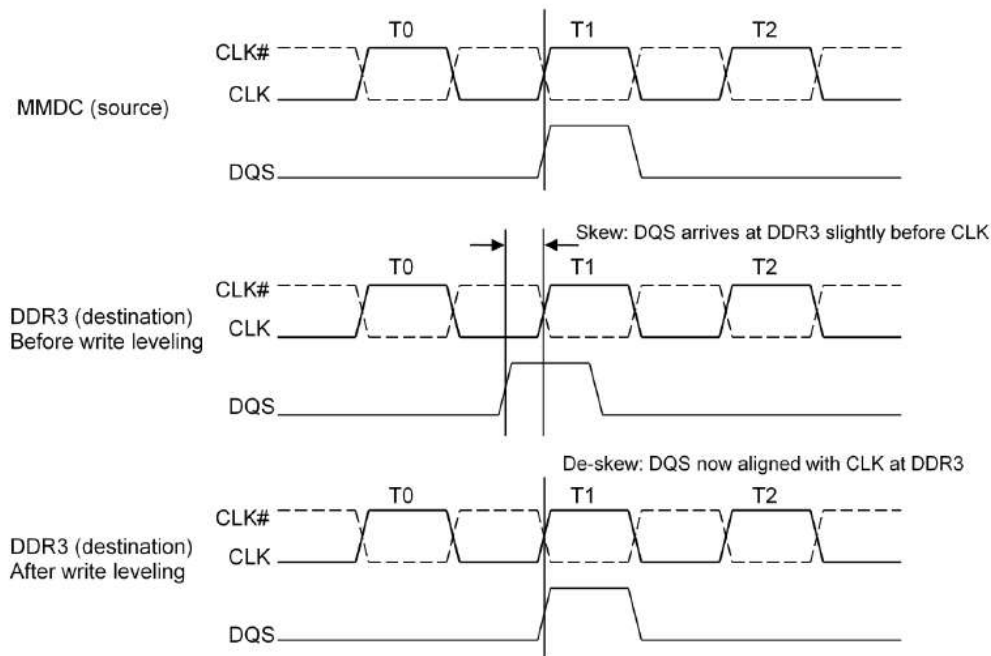
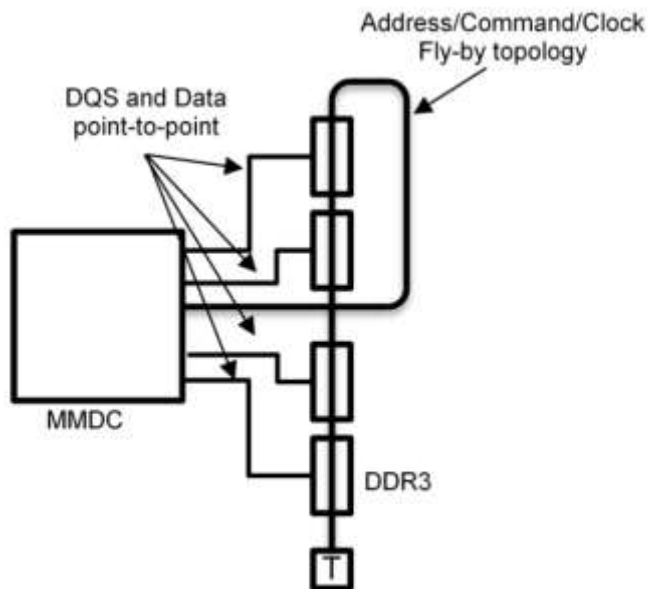
- Board bring-up: where DRAM bring-up fits in
 - Introduce the tools used for DRAM bring-up
- DDR3 Script Aid/DRAM Register Programming Aid
 - Introduction/Overview
 - Walkthrough
- DRAM Stress Test
 - Introduction/Overview
 - How to run; deep dive into sub-tests
- DRAM Calibration Overview
- Board Design Considerations

DRAM Calibration in the DRAM Stress Test

- MX6 MMDC Calibration App Note (AN4467): highly recommended reading to understand calibration concepts
- MX6 series DRAM controller (MMDC) features HW supported calibration methods:
 - Read DQS Gating calibration
 - Read DQS delay calibration
 - Write DQS delay calibration
 - Write-leveling calibration
- Previous i.MX SoC did not have this support in HW (with the exception of MX53)
 - That doesn't mean someone didn't come along and write their own type of SW calibration code for previous parts
- ZQ calibration is something simply enabled, no user interaction
 - Exception is MX508 where this requires a manual SW ZQ calibration routine
 - This routine is part of the MX508 DRAM Stress Test
 - This routine was obtained directly from design/validation and re-used in stress test

DRAM Calibration Conceptual Overview

Write Leveling Calibration



From the MX6DQ register programming aid example

These are for write leveling calibration, which is needed for fly-by board layout topology	MPWLDECTRL0 PHY0	0x021b080c	0x001F001F
	MPWLDECTRL1 PHY0	0x021b0810	0x001F001F
	MPWLDECTRL0 PHY1	0x021b480c	0x00440044
	MPWLDECTRL1 PHY1	0x021b4810	0x00440044

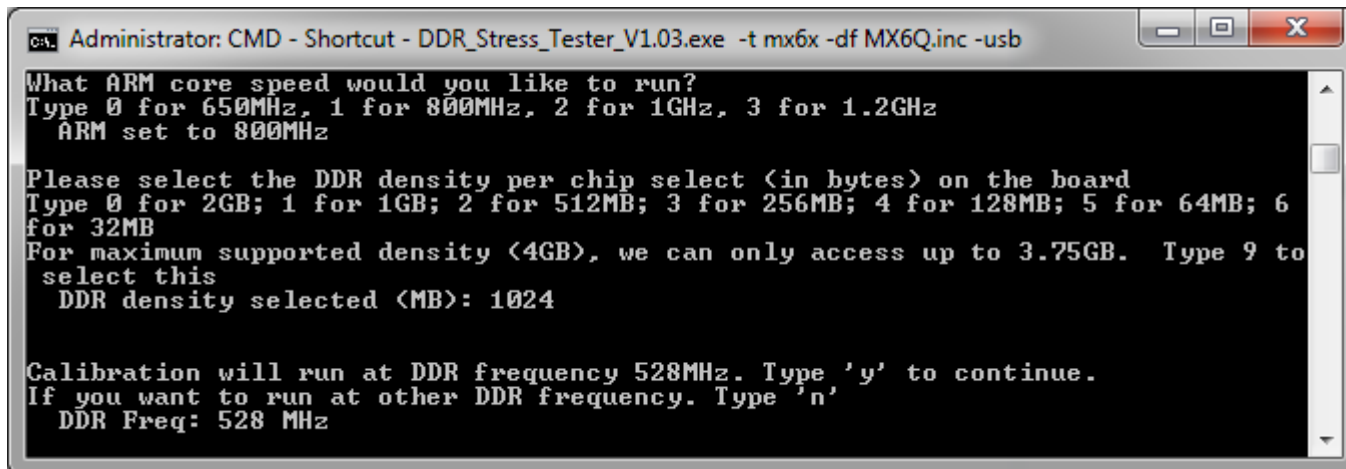
Values from validation board. For Sabre boards, which is routed point-to-point, can set all values to 0x1F.

- Compensates for CLK-to-DQS skew incurred from fly-by topology
 - Point-to-point memory layouts don't need this
 - Point-to-point memory layouts normally don't use terminations, like FSL development boards
- Relevant to DDR3 memories only (not supported with LPDDR2)
- Write Leveling Calibration code in MX6 DRAM Stress Test



DRAM Stress Test – Calibration Routines

- The DDR Stress test can be used to determine Write Leveling Parameters
- To run stress test, need *.inc file from Register programming Aid.
- When test first starts up, answer preliminary questions:
 - What core speed would you like to use?
 - What DDR density would you like to use?
 - Anything less than physically available memory is acceptable.
 - What DDR Frequency would you like to use?



```
Administrator: CMD - Shortcut - DDR_Stress_Tester_V1.03.exe -t mx6x -df MX6Q.inc -usb
What ARM core speed would you like to run?
Type 0 for 650MHz, 1 for 800MHz, 2 for 1GHz, 3 for 1.2GHz
  ARM set to 800MHz

Please select the DDR density per chip select (in bytes) on the board
Type 0 for 2GB; 1 for 1GB; 2 for 512MB; 3 for 256MB; 4 for 128MB; 5 for 64MB; 6
for 32MB
For maximum supported density (4GB), we can only access up to 3.75GB. Type 9 to
select this
  DDR density selected (MB): 1024

Calibration will run at DDR frequency 528MHz. Type 'y' to continue.
If you want to run at other DDR frequency. Type 'n'
  DDR Freq: 528 MHz
```

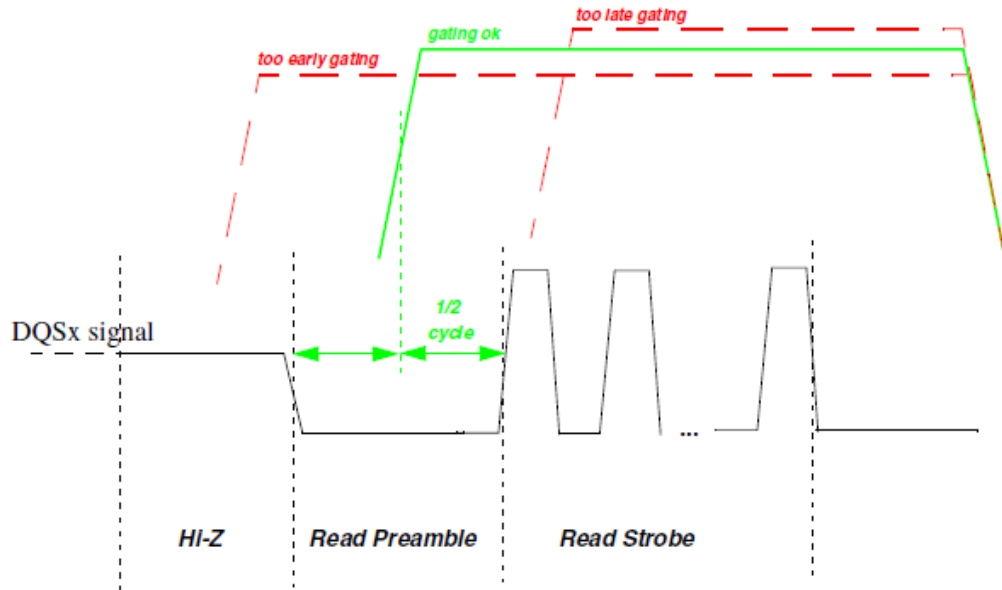
DRAM Stress Test – Calibration Routines

- The next question from the DDR Stress test is:
- Do you want to run the Write Leveling Calibration. Press 'y'
- The test will ask you to enter the four digit Mode Register 1 setting that you used in your initialization script.
- Once the MR1 setting is entered, the Stress Test will complete the Write Leveling Calibration Routine and report back the calibration values.
- Note that the GUI Version of the Stress Test handles the MR1 setting automatically.

```
Administrator: CMD - Shortcut - DDR_Stress_Tester_V1.03.exe -t mx6x -df MX6Q.inc -usb
Would you like to run the write leveling calibration? <y/n>
Please enter the MR1 value on the initialization script
This will be re-programmed into MR1 after write leveling calibration
Enter as a 4-digit HEX value, example 0004, then hit enter
0004 You have entered: 0x0004
Start write leveling calibration
Write leveling calibration completed
MMD0_MPWLDECTRL0 ch0 after write level cal: 0x00280023
MMD0_MPWLDECTRL1 ch0 after write level cal: 0x002F002A
MMD0_MPWLDECTRL0 ch1 after write level cal: 0x001B0028
MMD0_MPWLDECTRL1 ch1 after write level cal: 0x00140028
Would you like to run the DQS gating, read/write delay calibration? <y/n>
```

DRAM Calibration Conceptual Overview

Read DQS Gating Calibration



From the MX6DQ register programming aid example

These parameters are determined after running calibration. The parameters provided here are from Freescale's development board and will work as initial values. Update these values after running calibration.	MPDGCTRL0 PHY0	0x021b083c	0x434b0350
	MPDGCTRL1 PHY0	0x021b0840	0x034c0359
	MPDGCTRL0 PHY1	0x021b483c	0x434b0350
	MPDGCTRL1 PHY1	0x021b4840	0x03650348
	MPRDDLCTL PHY0	0x021b0848	0x4436383b
	MPRDDLCTL PHY1	0x021b4848	0x39393341
	MPWRDLCTL PHY0	0x021b0850	0x35373933
	MPWRDLCTL PHY1	0x021b4850	0x48254a36

- Not a JEDEC standard; controls i.MX internal DQS gate timing parameters
- Mechanism for our DRAM controllers to correctly sample incoming read DQS signal
- Relevant to DDR3 memories only (not supported with LPDDR2)
- Calibration code in MX6 and MX53 DRAM Stress Test

DRAM Stress Test – Calibration Routines

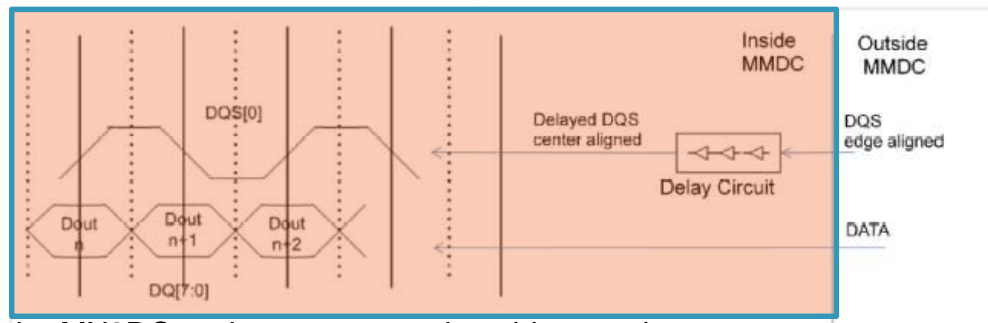
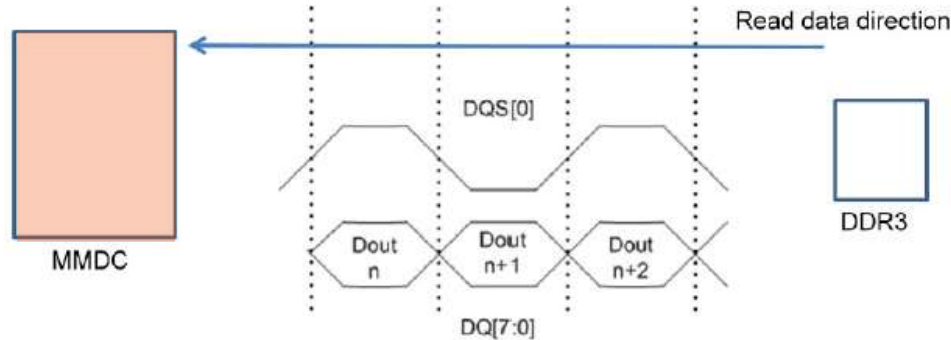
- The DQS Gating, Read/Write delay calibration tests are next.
- Would you like to run the DQS gating, read/write delay calibration tests:
Press 'y'
- Test will automatically run and provide results when finished:

```
Administrator: CMD - Shortcut - DDR_Stress_Tester_V1.03.exe -t mx6x -df MX6Q.inc -usb
Would you like to run the DQS gating, read/write delay calibration? (y/n)
Starting DQS gating calibration...
.....
BYTE 0:
  Start:      HC=0x01 ABS=0x00
  End:        HC=0x04 ABS=0x30
  Mean:       HC=0x02 ABS=0x57
  End-0.5*tCK: HC=0x03 ABS=0x30
  Final:      HC=0x03 ABS=0x30
BYTE 1:
  Start:      HC=0x02 ABS=0x0C
  End:        HC=0x04 ABS=0x18
  Mean:       HC=0x03 ABS=0x12
  End-0.5*tCK: HC=0x03 ABS=0x18
  Final:      HC=0x03 ABS=0x18
BYTE 2:
  Start:      HC=0x02 ABS=0x0C
  End:        HC=0x04 ABS=0x0C
  Mean:       HC=0x03 ABS=0x0C
  End-0.5*tCK: HC=0x03 ABS=0x0C
  Final:      HC=0x03 ABS=0x0C
BYTE 3:
  Start:      HC=0x02 ABS=0x04
  End:        HC=0x04 ABS=0x14
  Mean:       HC=0x03 ABS=0x0C
  End-0.5*tCK: HC=0x03 ABS=0x14
  Final:      HC=0x03 ABS=0x14
BYTE 4:
  Start:      HC=0x02 ABS=0x10
  End:        HC=0x04 ABS=0x24
  Mean:       HC=0x03 ABS=0x1A
  End-0.5*tCK: HC=0x03 ABS=0x24
  Final:      HC=0x03 ABS=0x24
BYTE 5:
  Start:      HC=0x02 ABS=0x0C
  End:        HC=0x04 ABS=0x10
  Mean:       HC=0x03 ABS=0x0E
  End-0.5*tCK: HC=0x03 ABS=0x10
  Final:      HC=0x03 ABS=0x10
BYTE 6:
  Start:      HC=0x00 ABS=0x48
  End:        HC=0x03 ABS=0x54
  Mean:       HC=0x02 ABS=0x0E
  End-0.5*tCK: HC=0x02 ABS=0x54
  Final:      HC=0x02 ABS=0x54
BYTE 7:
  Start:      HC=0x02 ABS=0x0C
  End:        HC=0x04 ABS=0x14
  Mean:       HC=0x03 ABS=0x10
  End-0.5*tCK: HC=0x03 ABS=0x14
  Final:      HC=0x03 ABS=0x14
DQS calibration MMDC0 MPDGCTRL0 = 0x43180330, MPDGCTRL1 = 0x0314030C
DQS calibration MMDC1 MPDGCTRL0 = 0x43100324, MPDGCTRL1 = 0x03140254
```



DRAM Calibration Conceptual Overview

Read DQS Delay Calibration (Continued)



From the MX6DQ register programming aid example

These parameters are determined after running calibration. The parameters provided here are from Freescale's development board and will work as initial values. Update these values after running calibration.	MPDGCTRL0 PHY0	0x021b083c	0x434b0350
	MPDGCTRL1 PHY0	0x021b0840	0x034c0359
	MPDGCTRL0 PHY1	0x021b483c	0x434b0350
	MPDGCTRL1 PHY1	0x021b4840	0x03650348
	MPRDDCTL PHY0	0x021b0848	0x4436383b
	MPRDDCTL PHY1	0x021b4848	0x39393341
	MPWRDLCTL PHY0	0x021b0850	0x35373933
	MPWRDLCTL PHY1	0x021b4850	0x48254a36

- Used to adjust read-DQS within read-data byte
- Relevant to DDR3 and LPDDR2 memories
- Calibration code in MX6 and MX53 DRAM Stress Test

DRAM Stress Test – Calibration Routines

- The Read calibration test is run begins next.
- “Waterfall” display shows visual of delay settings that allow for correct data readings.
 - Correct return marked with a ‘0’
- Test finds center of valid window and reports result at bottom.

```
Administrator: CMD - Shortcut - DDR_Stress_Tester_V1.03.exe -t mx6x ...
Note: Array result[] holds the DRAM test result of each byte.
0: test pass. 1: test fail
4 bits represent the result of 1 byte.
result 00000001:byte 0 fail.
result 00000011:byte 0, 1 fail.

Starting Read calibration...

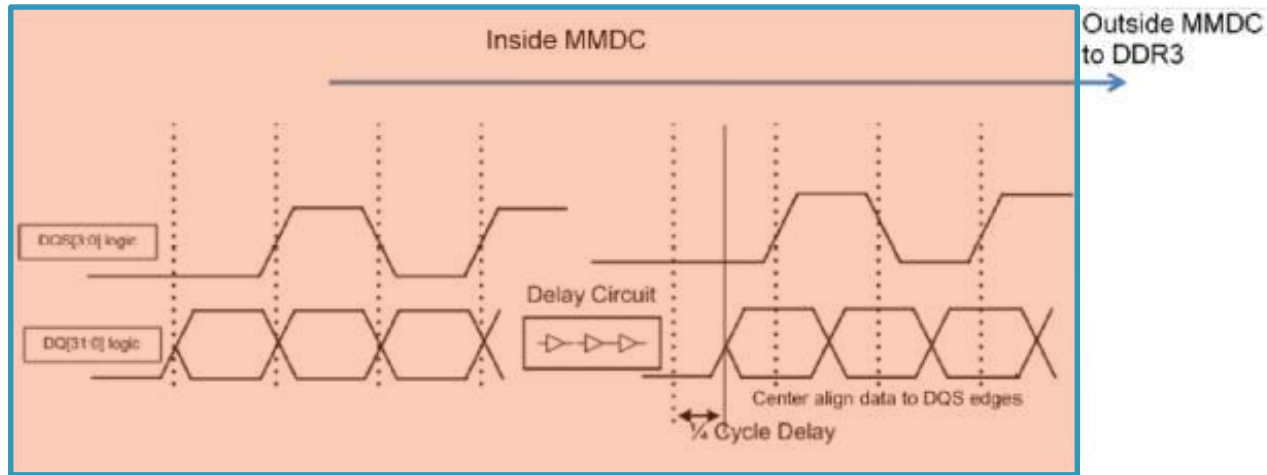
ABS_OFFSET=0x00000000 result[00]=0x11111111
ABS_OFFSET=0x04040404 result[01]=0x11111111
ABS_OFFSET=0x08080808 result[02]=0x11111111
ABS_OFFSET=0x0C0C0C0C result[03]=0x11011111
ABS_OFFSET=0x10101010 result[04]=0x11011011
ABS_OFFSET=0x14141414 result[05]=0x11011011
ABS_OFFSET=0x18181818 result[06]=0x00011000
ABS_OFFSET=0x1C1C1C1C result[07]=0x00011000
ABS_OFFSET=0x20202020 result[08]=0x00000000
ABS_OFFSET=0x24242424 result[09]=0x00000000
ABS_OFFSET=0x28282828 result[0A]=0x00000000
ABS_OFFSET=0x2C2C2C2C result[0B]=0x00000000
ABS_OFFSET=0x30303030 result[0C]=0x00000000
ABS_OFFSET=0x34343434 result[0D]=0x00000000
ABS_OFFSET=0x38383838 result[0E]=0x00000000
ABS_OFFSET=0x3C3C3C3C result[0F]=0x00000000
ABS_OFFSET=0x40404040 result[10]=0x00000000
ABS_OFFSET=0x44444444 result[11]=0x00000000
ABS_OFFSET=0x48484848 result[12]=0x00000000
ABS_OFFSET=0x4C4C4C4C result[13]=0x00000000
ABS_OFFSET=0x50505050 result[14]=0x00000000
ABS_OFFSET=0x54545454 result[15]=0x00000000
ABS_OFFSET=0x58585858 result[16]=0x00000000
ABS_OFFSET=0x5C5C5C5C result[17]=0x00100000
ABS_OFFSET=0x60606060 result[18]=0x01100000
ABS_OFFSET=0x64646464 result[19]=0x11100110
ABS_OFFSET=0x68686868 result[1A]=0x11110111
ABS_OFFSET=0x6C6C6C6C result[1B]=0x11110111
ABS_OFFSET=0x70707070 result[1C]=0x11111111
ABS_OFFSET=0x74747474 result[1D]=0x11111111
ABS_OFFSET=0x78787878 result[1E]=0x11111111
ABS_OFFSET=0x7C7C7C7C result[1F]=0x11111111

MMDC0 MPRDDLCTL = 0x46383C3E, MMDC1 MPRDDLCTL = 0x3C3A3242
```



DRAM Calibration Conceptual Overview

Write DQS Delay Calibration



From the MX6DQ register programming aid example

These parameters are determined after running calibration. The parameters provided here are from Freescale's development board and will work as initial values. Update these values after running calibration.	MPDGCTRL0 PHY0	0x021b083c	0x434b0350
	MPDGCTRL1 PHY0	0x021b0840	0x034c0359
	MPDGCTRL0 PHY1	0x021b483c	0x434b0350
	MPDGCTRL1 PHY1	0x021b4840	0x03650348
	MPRDDCTL PHY0	0x021b0848	0x4436383b
	MPRDDCTL PHY1	0x021b4848	0x39393341
	MPWRDLCTL PHY0	0x021b0850	0x35373933
	MPWRDLCTL PHY1	0x021b4850	0x48254a36

- Used to center output write-DQS within write-data byte
- Relevant to DDR3 and LPDDR2 memories
- Calibration code in MX6 and MX53 DRAM Stress Test

DRAM Stress Test – Calibration Routines

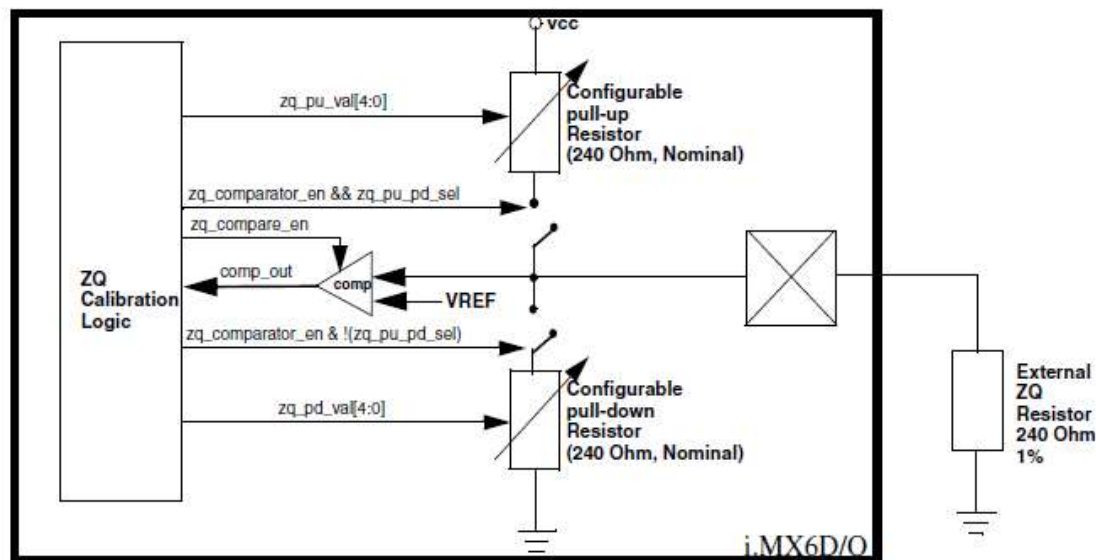
- The Write calibration test is run last.
- Test uses the same display as for the Read calibration test.
- Test finds center of valid window and reports result at bottom.

```
Administrator: CMD - Shortcut - DDR_Stress_Tester_V1.03.exe -t mx6x -...
MMDC0 MPRDDLCTL = 0x46383C3E, MMDC1 MPRDDLCTL = 0x3C3A3242
Starting Write calibration...
ABS_OFFSET=0x00000000 result[00]=0x11111111
ABS_OFFSET=0x04040404 result[01]=0x10111111
ABS_OFFSET=0x08080808 result[02]=0x10111111
ABS_OFFSET=0x0C0C0C0C result[03]=0x10101111
ABS_OFFSET=0x10101010 result[04]=0x10100110
ABS_OFFSET=0x14141414 result[05]=0x10100010
ABS_OFFSET=0x18181818 result[06]=0x00100010
ABS_OFFSET=0x1C1C1C1C result[07]=0x00000000
ABS_OFFSET=0x20202020 result[08]=0x00000000
ABS_OFFSET=0x24242424 result[09]=0x00000000
ABS_OFFSET=0x28282828 result[0A]=0x00000000
ABS_OFFSET=0x2C2C2C2C result[0B]=0x00000000
ABS_OFFSET=0x30303030 result[0C]=0x00000000
ABS_OFFSET=0x34343434 result[0D]=0x00000000
ABS_OFFSET=0x38383838 result[0E]=0x00000000
ABS_OFFSET=0x3C3C3C3C result[0F]=0x00000000
ABS_OFFSET=0x40404040 result[10]=0x00000000
ABS_OFFSET=0x44444444 result[11]=0x00000000
ABS_OFFSET=0x48484848 result[12]=0x00000000
ABS_OFFSET=0x4C4C4C4C result[13]=0x00000000
ABS_OFFSET=0x50505050 result[14]=0x00000000
ABS_OFFSET=0x54545454 result[15]=0x00000000
ABS_OFFSET=0x58585858 result[16]=0x00000000
ABS_OFFSET=0x5C5C5C5C result[17]=0x00000000
ABS_OFFSET=0x60606060 result[18]=0x01001000
ABS_OFFSET=0x64646464 result[19]=0x01001000
ABS_OFFSET=0x68686868 result[1A]=0x11011000
ABS_OFFSET=0x6C6C6C6C result[1B]=0x11011100
ABS_OFFSET=0x70707070 result[1C]=0x11111110
ABS_OFFSET=0x74747474 result[1D]=0x11111111
ABS_OFFSET=0x78787878 result[1E]=0x11111111
ABS_OFFSET=0x7C7C7C7C result[1F]=0x11111111
MMDC0 MPWRDLCTL = 0x363E4440, MMDC1 MPWRDLCTL = 0x3E304438
```



DRAM Calibration Conceptual Overview

ZQ Calibration



- Feature of both i.MX* and DRAM (DDR3 and LPDDR2)
- Used to calibrate the pull-up/pull-down resistors of DRAM IO pads (tighter control of pad impedance)
- ZQ calibration occurs automatically, simply just need to enable it
 - Except on MX508, there's a SW routine to do this (in stress test)

* Only i.MX parts that support DDR3 and/or LPDDR2: MX6, MX53, MX508

Calibration is complete, now what?

Plug the calibration results into the Script and save it.
No need to rerun the calibration tests.

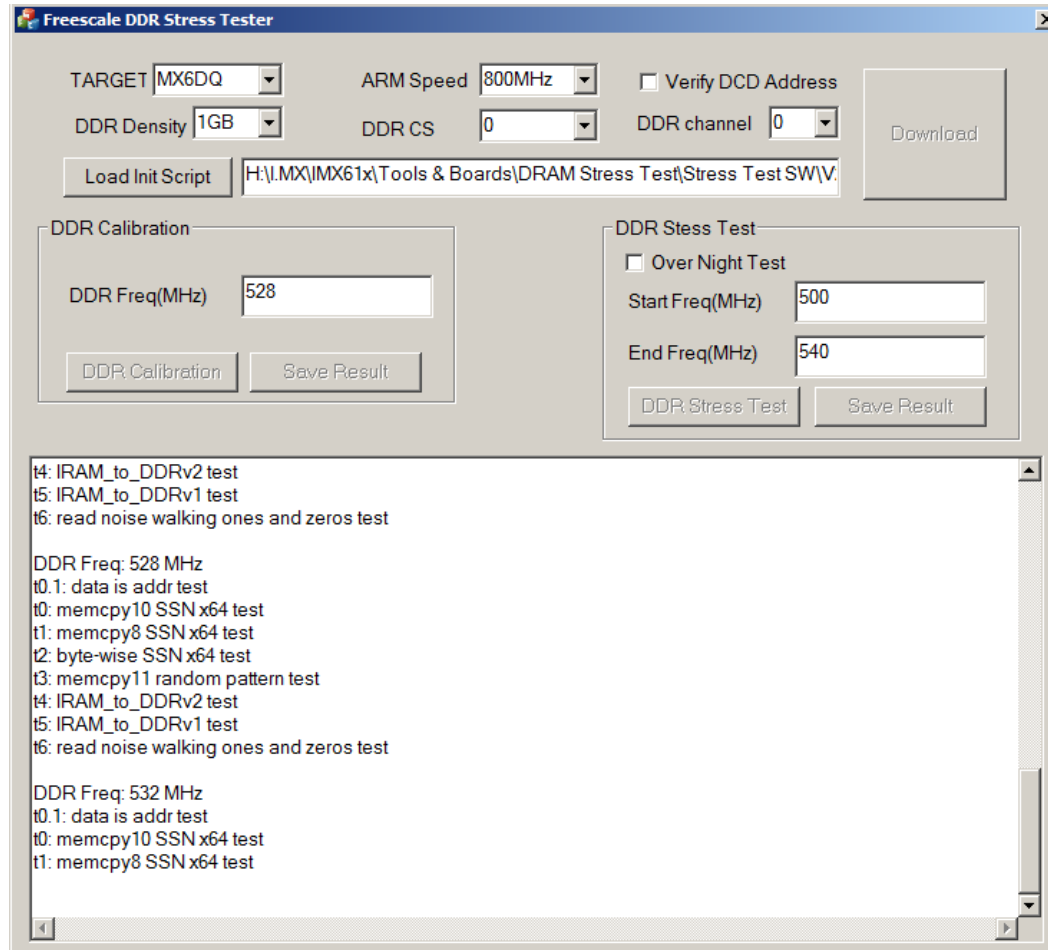
```
97 # For target board, may need to run write leveling calibration to fine tune these settings.
98 mem set 0x021b080c 32 0x00000000
99 mem set 0x021b0810 32 0x00000000
100 mem set 0x021b480c 32 0x00000000
101 mem set 0x021b4810 32 0x00000000
102
103 #Read DQS Gating calibration
104 mem set 0x021b083c 32 0x00000000 # MPDGCTRL0 PHY0
105 mem set 0x021b0840 32 0x00000000 # MPDGCTRL1 PHY0
106 mem set 0x021b483c 32 0x00000000 # MPDGCTRL0 PHY1
107 mem set 0x021b4840 32 0x00000000 # MPDGCTRL1 PHY1
108
109 #Read calibration
110 mem set 0x021b0848 32 0x40404040 # MPRDDLCTL PHY0
111 mem set 0x021b4848 32 0x40404040 # MPRDDLCTL PHY1
112
113 #Write calibration
114 mem set 0x021b0850 32 0x40404040 # MPWRDLCTL PHY0
115 mem set 0x021b4850 32 0x40404040 # MPWRDLCTL PHY1
...
```

Note: Power cycle the hardware in between loading scripts and new DDR configuration values.

```
• MMDC registers updated from calibration
• Write leveling calibration
• MMDC_MPWLDECTRL0 ch0 (0x021b080c) = 0x0021001D
• MMDC_MPWLDECTRL1 ch0 (0x021b0810) = 0x00290022
• MMDC_MPWLDECTRL0 ch1 (0x021b480c) = 0x0016002B
• MMDC_MPWLDECTRL1 ch1 (0x021b4810) = 0x000F0022
• Read DQS Gating calibration
• MPDGCTRL0 PHY0 (0x021b083c) = 0x433C034C
• MPDGCTRL1 PHY0 (0x021b0840) = 0x03380328
• MPDGCTRL0 PHY1 (0x021b483c) = 0x433C0350
• MPDGCTRL1 PHY1 (0x021b4840) = 0x03380304
• Read calibration
• MPRDDLCTL PHY0 (0x021b0848) = 0x4234383E
• MPRDDLCTL PHY1 (0x021b4848) = 0x38363242
• Write calibration
• MPWRDLCTL PHY0 (0x021b0850) = 0x32363E3A
• MPWRDLCTL PHY1 (0x021b4850) = 0x3C304038
```

Running the DRAM Stress Test

- Now we are ready to run the DDR Stress Test.



DRAM Stress Test – Interpreting DRAM Failures

- Failures observed may help narrow down a root cause; following are some pointers:
- **Bit wise failures**
 - Normally indicates one or more data lines experiencing glitch due to signal integrity issues (too slow rise/fall time, or too fast rise and fall time attributing to ringing)
 - Varying temperature is one method to narrow down the root cause
 - If cooling down the part causes more failures, then it is likely the drive strength is too high causing more overshoots and undershoots
 - If heating up the part causes more failures, then the drive strength is too low and the signals may not rise/fall fast enough
 - Playing around with drive strengths often help (start with i.MX side and then try DRAM side)
- **Byte wise failures**
 - This is usually indicative of a problem with the DQS signals: too slow a rise/fall time, there is a glitch, or over/under shoots (signal integrity issues)
 - Temperature testing (see bit-wise failures) to assist in narrowing down the issue with the DQS signal
 - Playing around with drive strengths help; also try playing around with DQS to data timing
- **Entire word is wrong or random**
 - This may indicate something more catastrophic either in the logic of the DRAM controller, or some issue with address and/or command signals
 - Could be a problem with board layout
 - Try playing around with DRAM controller's timings like 'RALAT'

DRAM Stress Test – Interpreting DRAM Failures

(Continued)




- Keep in mind that these are only pointers to help diagnose DRAM related memory failures. In the past, DRAM failures were attributed to:
 - Poor board layout resulting in simultaneous switching noise (SSN) causing glitches.
 - Inadequate IO PAD design - often the IO PAD has poorly controlled impedance (either too high or too low a drive strength). This can be easily proven when observing a data signal or DQS signal being sourced by the DRAM memory (read access) or by the SoC (write access). One will often times observe that the DRAM memory provides a much cleaner waveform than that of the SoC.
 - Internal package issues (poor routing of power/ground signals, not providing proper ground returns, ground bounce, etc.)
 - DRAM controller logic bugs, often found in corner use cases where an internal bus master causes a transaction or series of subsequent transactions that were not anticipated or verified during the design process
 - Jitter on the SDCLK lines due to poor PLL design, or noise induced on the clock source itself (outside of the SoC from an external crystal or oscillator).
 - For LPDDR2, make sure i.MX IOMUX has pull down enabled for DQS signals
- Always remember to double-check DRAM initialization (DRAM register programming aid)

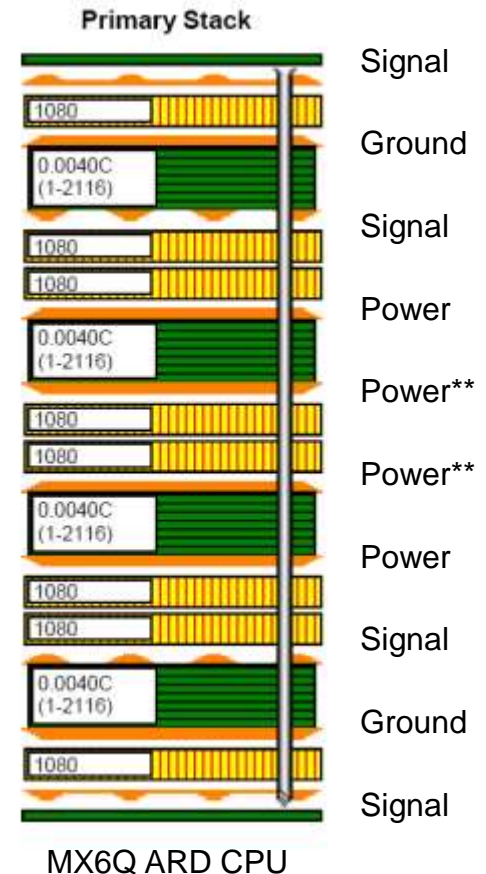
Agenda

- Board bring-up: where DRAM bring-up fits in
 - Introduce the tools used for DRAM bring-up
- DDR3 Script Aid/DRAM Register Programming Aid
 - Introduction/Overview
 - Walkthrough
- DRAM Stress Test
 - Introduction/Overview
 - How to run; deep dive into sub-tests
- DRAM Calibration Overview
- Board Design Considerations

8-Layer Board Stack-up

- Board stack-up critical for high-speed signal quality.
- Impedances must be pre-planned.
- High-speed signals must have a reference plane on an adjacent layer to minimize cross-talk.
- FSL Reference design = Isola 370HR
- Power** - additional power plane to support MX6Q to MX6Solo power options only.

Impedance Type	Layer	Design	Actual	Pitch	Plane	Target	Tol (ohms)
1  Surface MS	L1	0.00470	0.0045	-	-	50	5.0
	-	-	-	-	L2		
2  EC Microstrip	L1	0.00370	0.0038	0.0090	-	90	9.0
	-	0.00370	0.0038	-	L2		
3  EC Microstrip	L1	0.00450	0.00325	0.0100	-	100	10.0
	-	0.00450	0.00325	-	L2		



DDR Routing 1

- Swapping DDR3 Data lines within bytes facilitates routing
 - **Write Leveling** – lowest order bit within byte lane must remain on lowest order bit of byte lane
 - For example D0, D8, D16, ... fixed, other data lines free to swap within byte lane
 - JEDEC DDR3 memory restriction.
- No restrictions for complete byte lane swapping
 - DQS and DQM must follow lanes

DDR Routing 2

- Data re-assignment facilitates routing
 - **Data re-assigned within byte group**
 - **Byte Groups can be reassigned**

i.MX Contact	Memory Contact
DRAM_D0	DQ8
DRAM_D1	DQ15
DRAM_D2	DQ10
etc	etc
DRAM_D7	DQ9
SDQS0	DQS1
DQM0	DM1

← Lowest order bit

DDR Routing 3

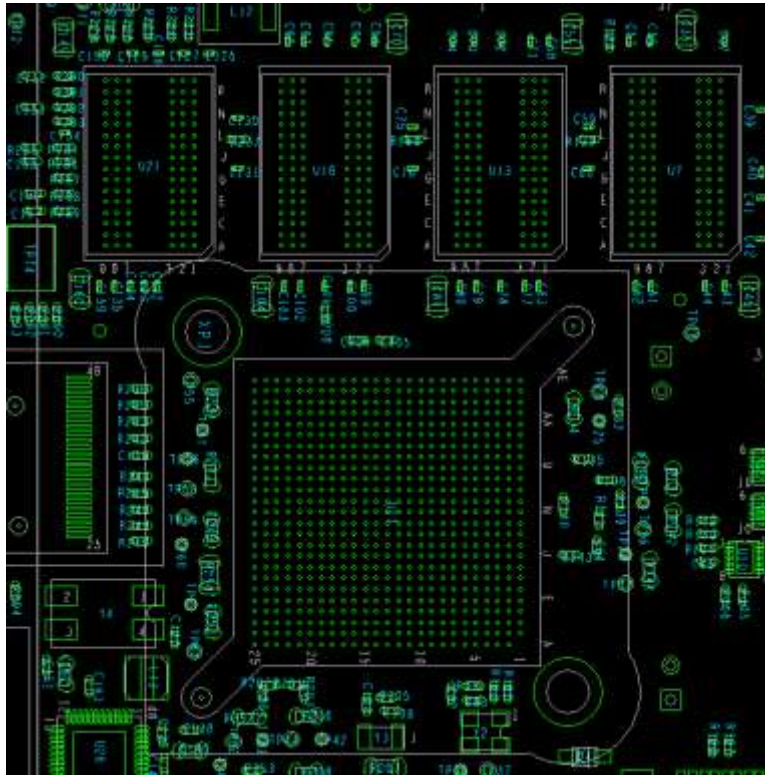
DDR (64-bit) routing configurations can be routed as:

- *“T” configurations*
 - Termination resistors not required
 - Accomplished with short routing lengths and on-chip drive strength control
 - Design limited to one chip select (4 x16 DDR's)
 - DDR3, 2 GBytes using latest memories (4 GBytes coming)
- *“Fly-by” configuration*
 - MX6 DDR controller provides Address mirroring when using 2 chip selects. Aids routing for memories on both sides of board.
 - Bus termination resistors required
 - Proven design method, easy to simulate

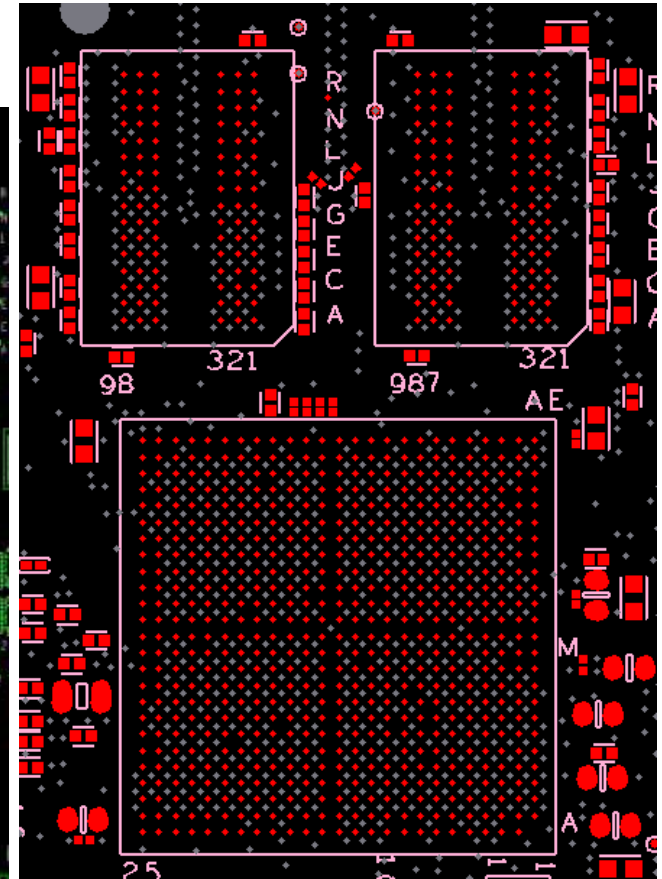
DDR Routing 4

- Prototype boards should plan for DDR signal breakout boards from Agilent or other.
 - Allows probing signal quality
 - Alternate – Remove one memory to probe bus

MX6Q DDR3
“Fly-by”
Configuration



MX6Q DDR3 “T” Configuration



Fly-By Topology vs. T Route

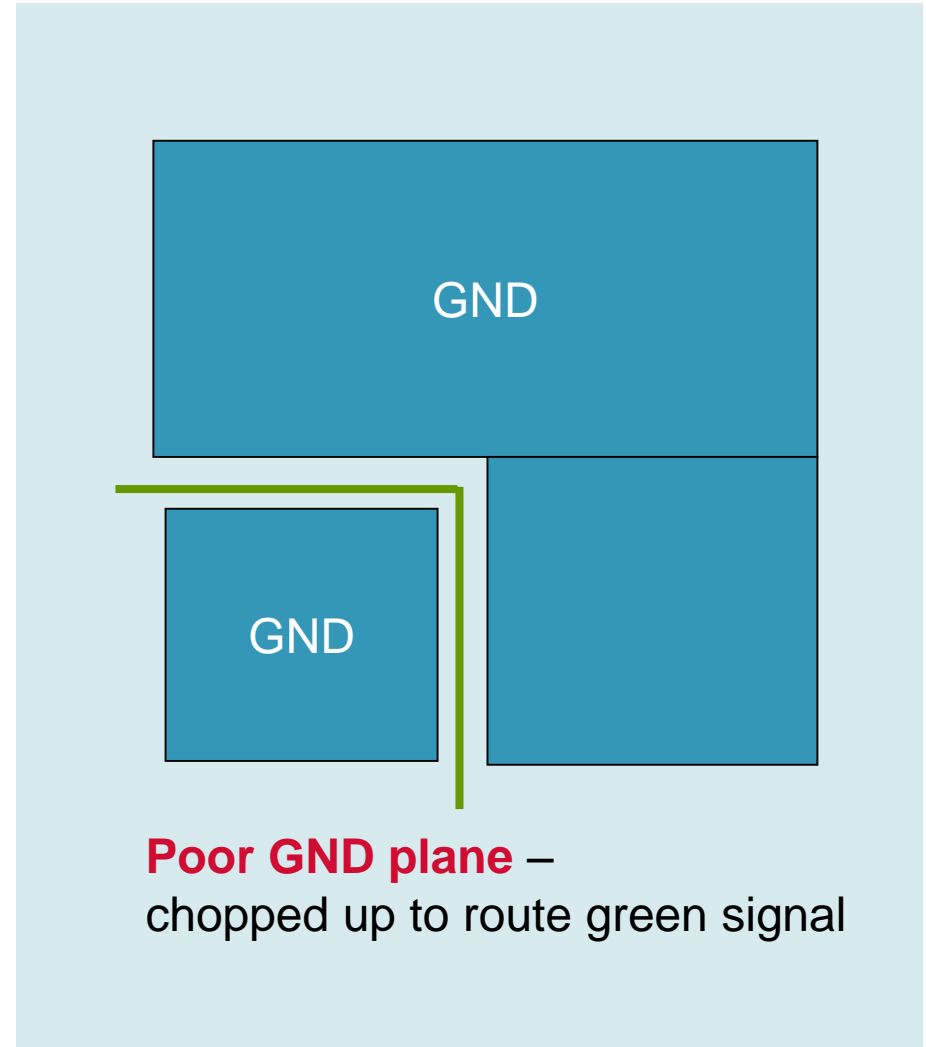
- Fly-By Topology Advantages:
 - Easier to route
 - Less chance for reflection in Address and Command traces.
 - Parallel termination resistors go at end of traces.
 - Reduced cross-talk at the pads
- T Route Advantages:
 - Less power consumption
 - Traces not pulled up to VREF.
 - Better performance.
 - Don't lose extra clock cycle to reads and writes.

Layout considerations for high-speed signals

- High-speed signals must not cross reference plane gaps
- Avoid creating slots, voids, and splits in reference planes. Review via voids to ensure they do not create splits (space out vias).
- Clocks or Strobes on same layer need at least 2.5x spacing from adjacent trace (2.5x height from reference plane) to control cross-talk.
- All Synchronous modules should have bus length matching and relative clock length control.
 - CLK should be longer than the longest signal in the Data/Addr/Control group (+5 mils)
- Many web resources

Power Grid Potential Errors

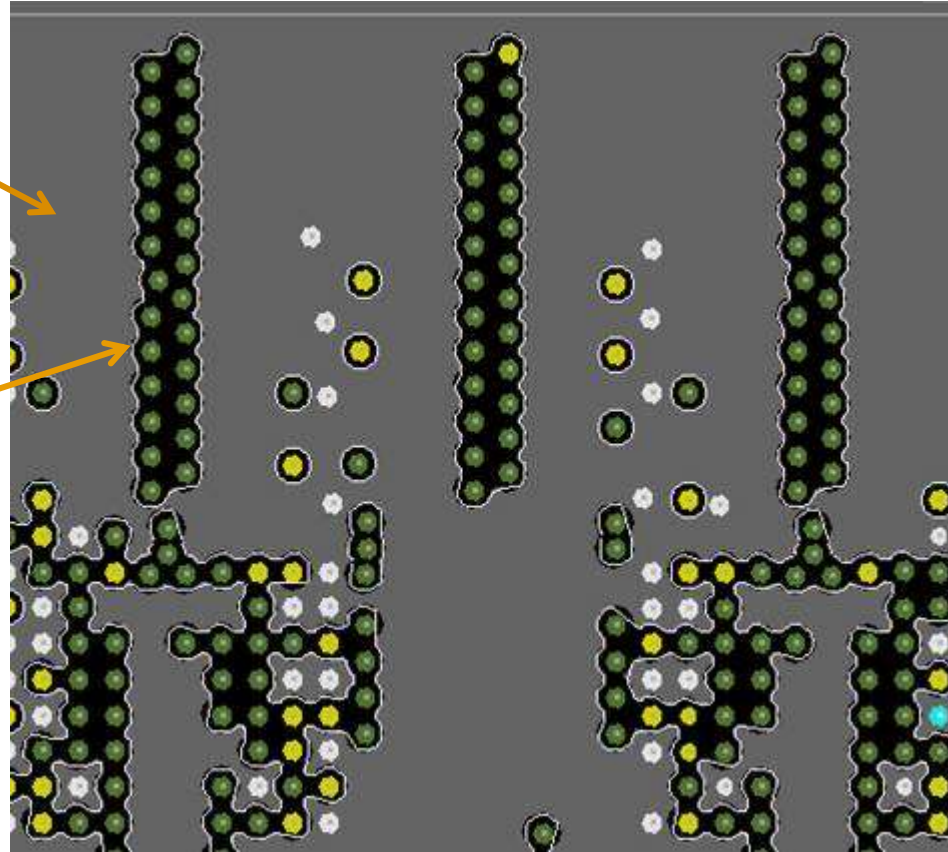
- Chopping up planes reduces effectiveness



DRAM GND Plane – Poor Layout

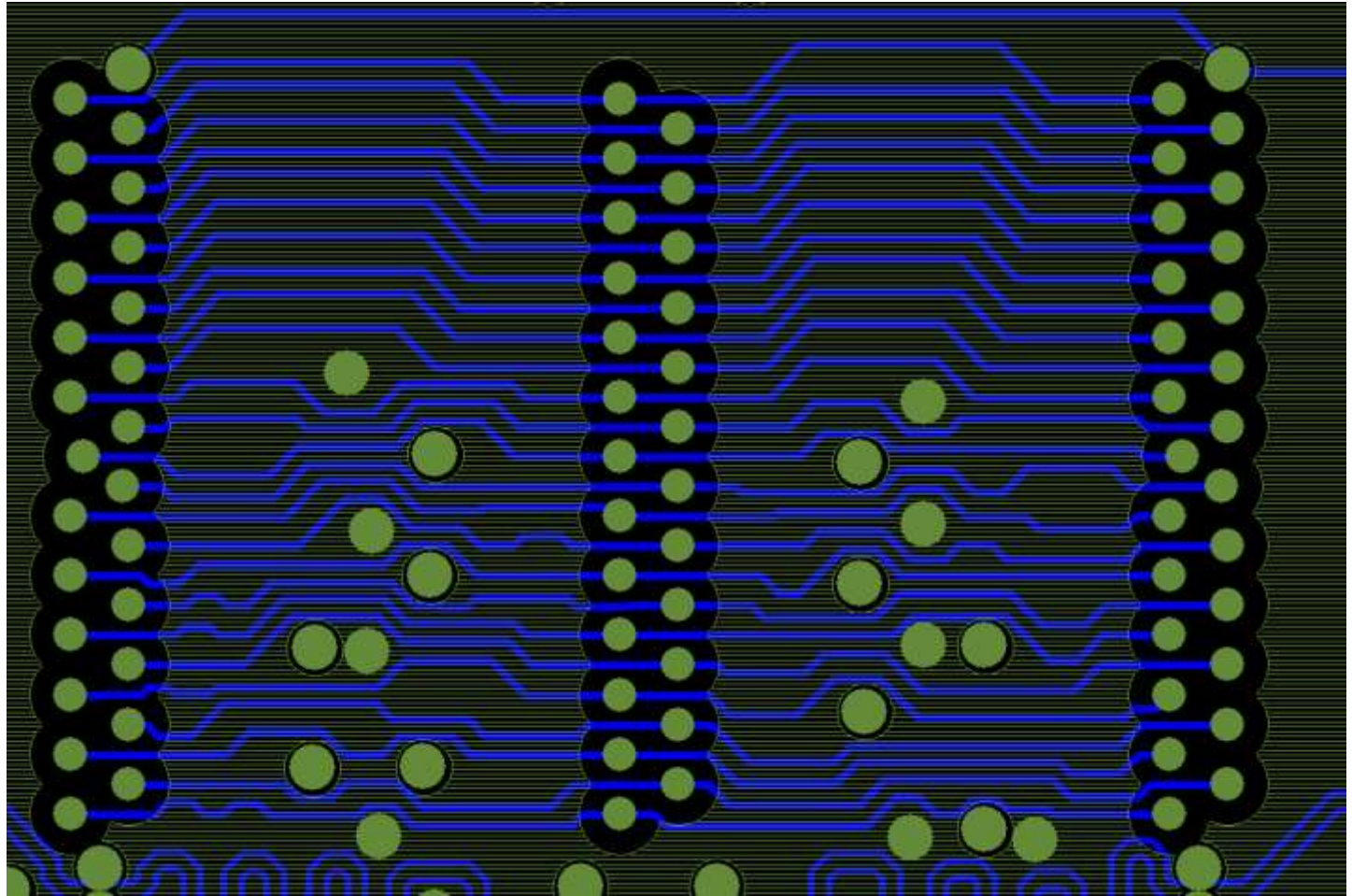
Gray = copper

Black = no copper



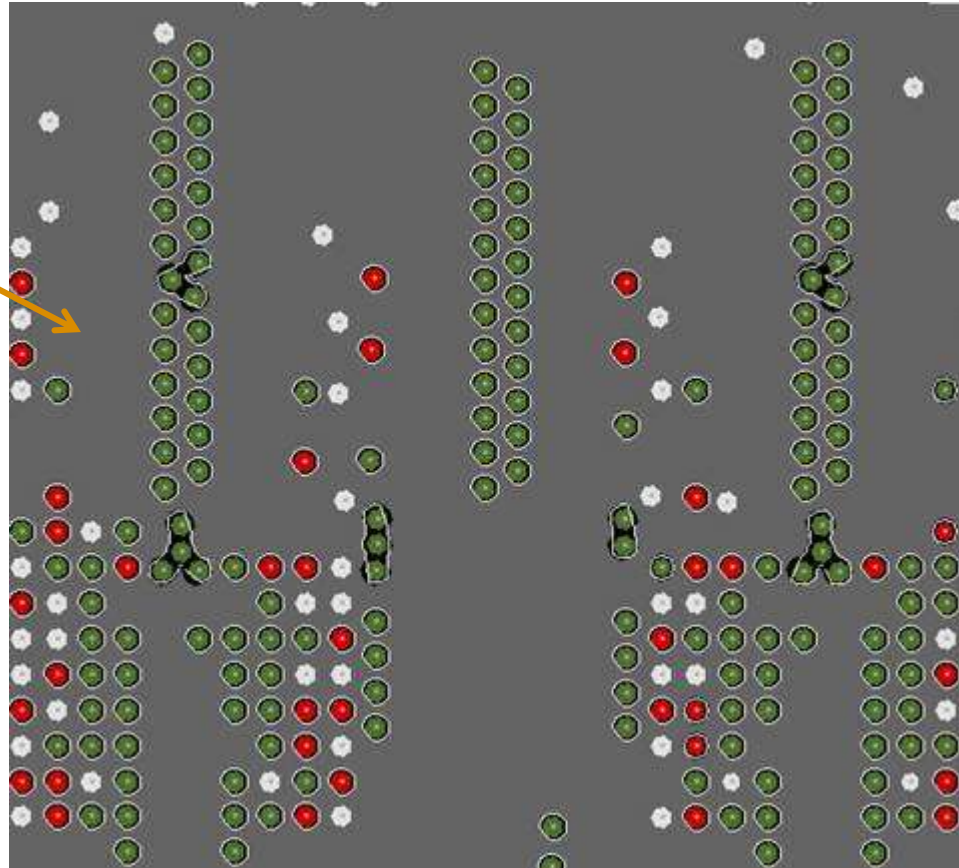
GND Plane of Previous Slide – Poor Layout Detail

- Vias too close together
- Horizontal current flow blockage



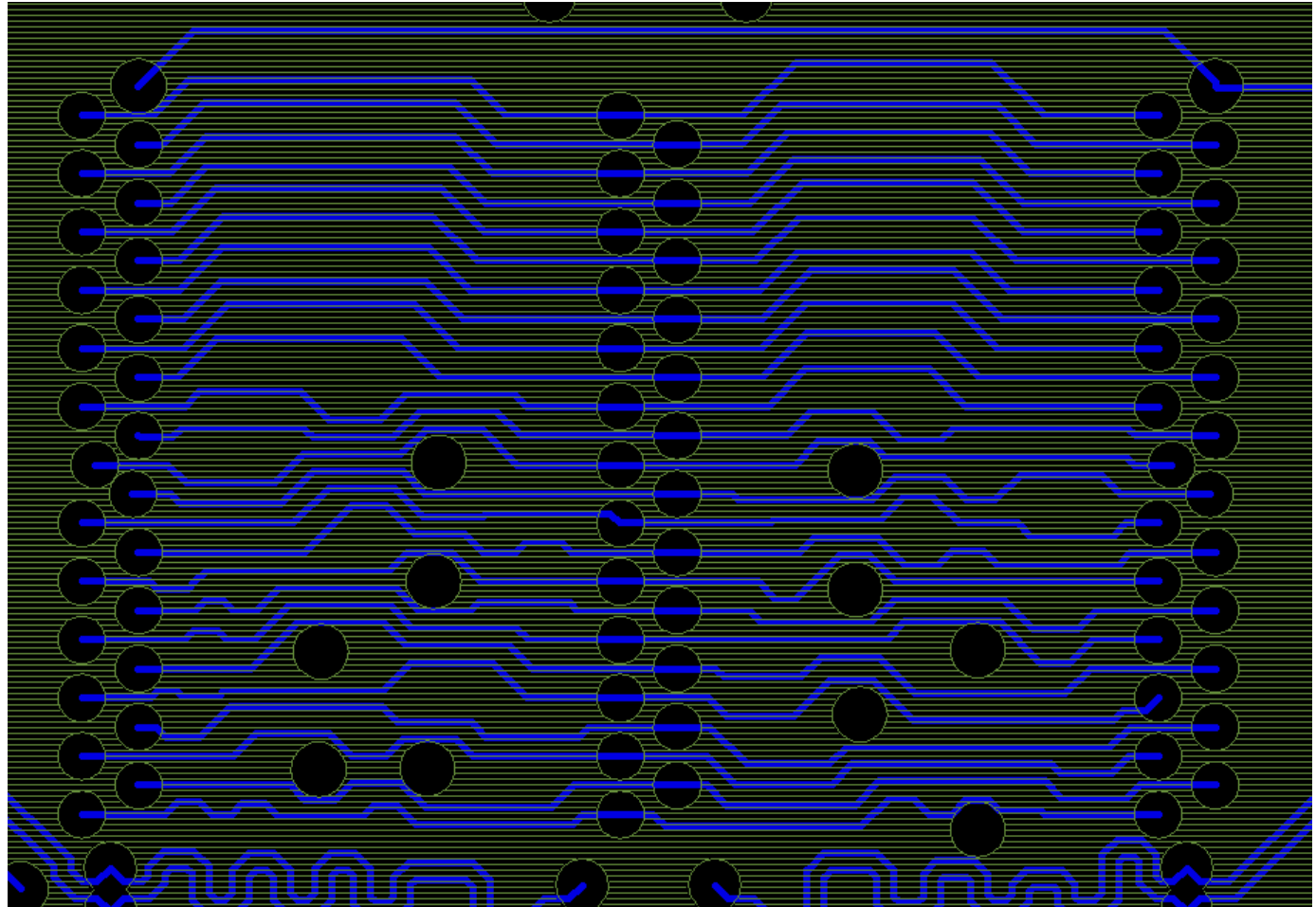
GND Plane - Good Layout

Gray = copper



GND Plane of Previous Slide – Good Layout Detail

- Vias spaced apart
- Facilitates horizontal current flow



High-Speed Signal Impedance

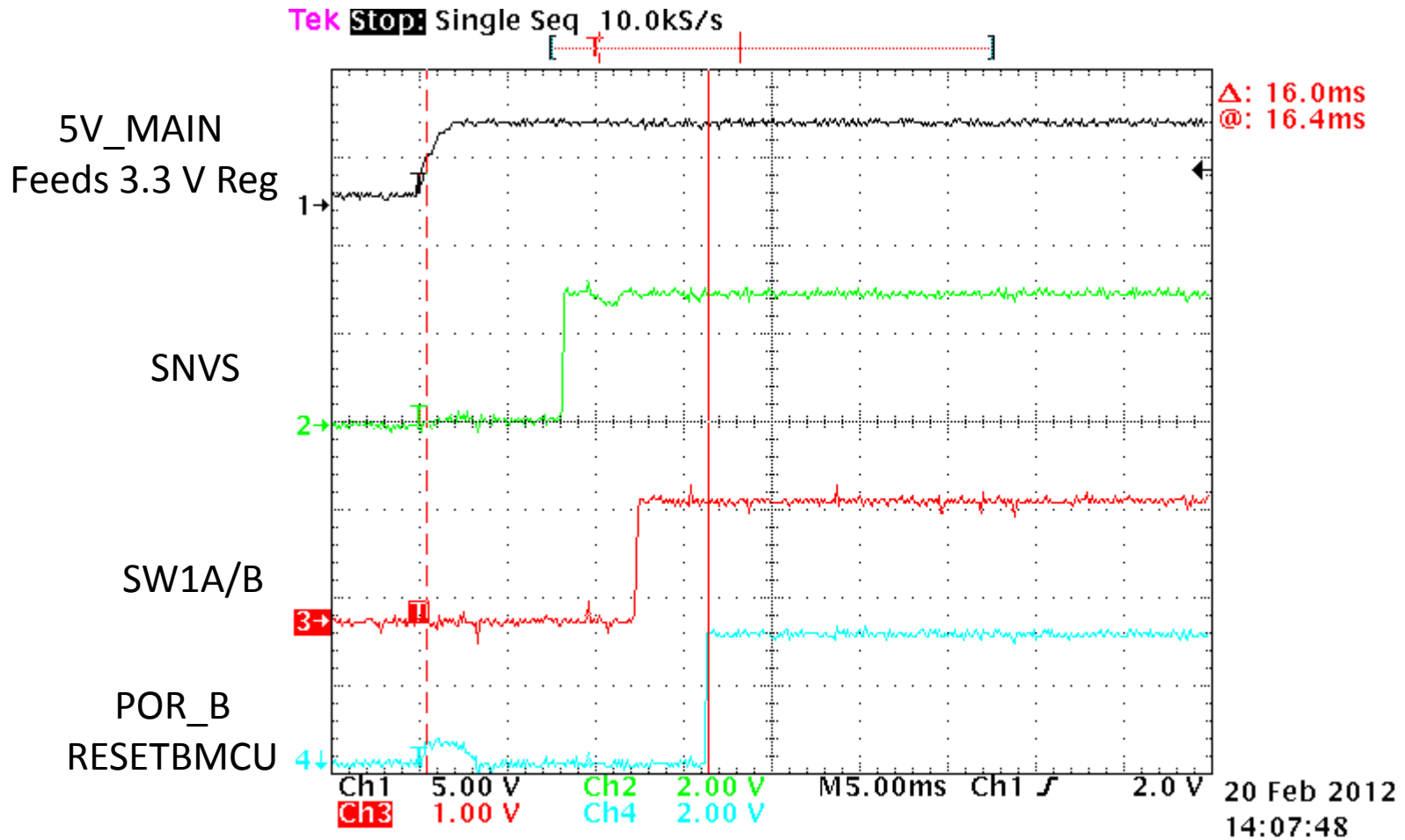
Signal Group	Impedance	Layout Tolerance (+/-)
All signals, unless specified	50 Ohm SE	2%
USB Diff signals	90 Ohm Diff	2%
Diff signals: LVDS, SATA, HDMI, DDR, PCIE, MIPI (CSI & DSI), MLB, Phy IC to Ethernet Connector	100 Ohm Diff (85 ohm PCI)	2%

Bring-Up: Power – Example Voltage Report

Board Name: _____ Serial #: _____ Data Collected by: _____ Date: _____

Source	Net Name	Expected (V)	Measured (V)	Measured Point	Comment
Main	5V0	5.0	5.103	C5.1	
3.3 V discrete reg	3V3_DELAYED	3.35	3.334	SH1	Requires LDO3 to enable
PMIC Switcher 1	VDDARM	1.375	1.377	SH2	
PMIC Switcher 2	VDDSOC	1.375	1.376	SH3	
PMIC Switcher 3	1V5_DDR	1.5	1.501	SH4	
PMIC LDO1	1V8	1.8	1.802	TP9	
PMIC LDO2	2V5	2.5	0.3	TP5	
VREFDDR	0V75_REFDDR	0.75	0.751	C8.1	50% of 1V5_DDR
Coin Cell	3V0_STBY	3.0	3.006	TP1	
MX6	VDDARM_CAP	1.1	1.114	C6.1	
MX6	VDDHIGH_CAP	2.5	2.515	SH5	
MX6	VDDSNVS_CAP	1.0	1.016	TP2	

Bring-Up: Power-Up Sequence



Summary

- Overview of tools used by the factory to optimize and debug DRAM interface
 - Excel spread sheet based register programming aid
 - DRAM stress test using open source compiler
- DRAM Calibration app note available from Freescale
 - Introduction of DRAM calibration concepts
- Case study of DRAM debug efforts



Links to Useful DRAM Documents

- JEDEC

DDR3 Specification:

<http://www.jedec.org/sites/default/files/docs/JESD79-3E.pdf>

DDR3L Amendment:

http://www.jedec.org/sites/default/files/docs/JESD79-3-1_1.pdf

LPDDR3 Specification:

<http://www.jedec.org/sites/default/files/docs/JESD209-3.pdf>

WideIO SDR Specification:

<http://www.jedec.org/sites/default/files/docs/JESD229.pdf>

LPDDR2 Specification:

<http://www.jedec.org/sites/default/files/docs/JESD209-2E.pdf>

- Micron Documentation

DRAM Support Site:

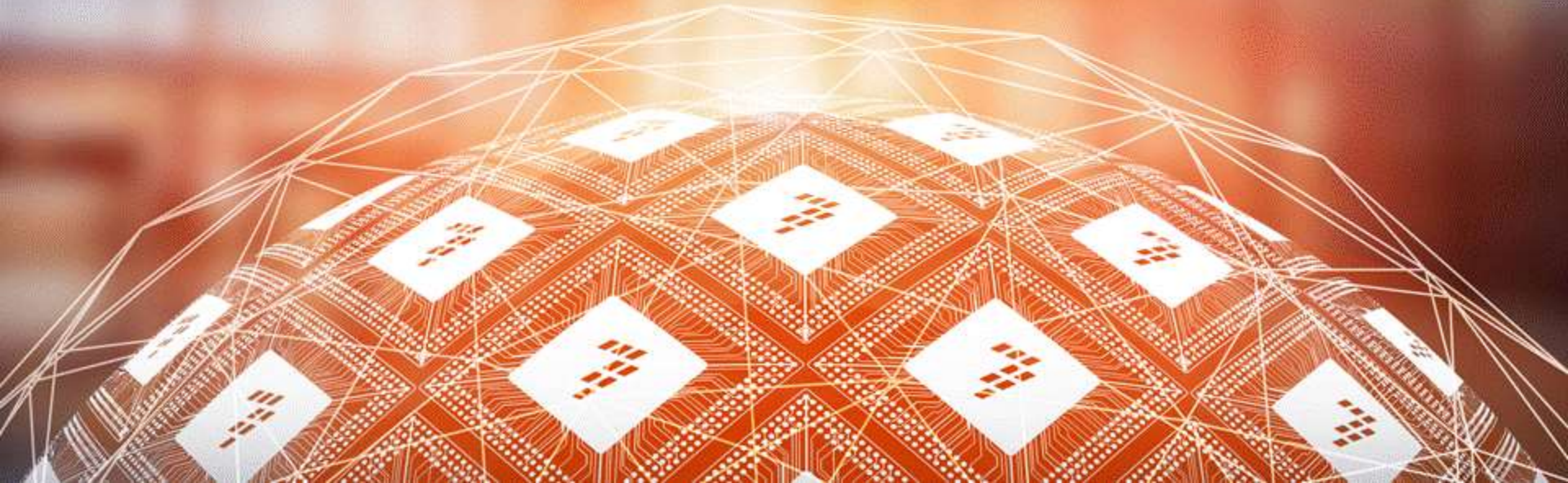
http://www.micron.com/products/dram/ddr3-sdram#documentation_support

References

- FTF Session **FTF-ENT-F0039** *Designing Transmission Lines in High-Speed Printed Circuit Boards: Preventing Potential Problems*
 - Go to freescale.com → Freescale Technology Forum, Training, tools, ... → FTF Americas → Technical Sessions Library → FTF-ENT-F0039
- *Books recommended from the session:*
 - *Right the First Time: A Practical Handbook on High Speed PCB and System Design, Volumes I & II, Lee W. Ritchey. Speeding Edge, ISBN 0-9741936-0-7*
 - *Signal and Power Integrity Simplified (2nd Edition), Eric Bogatin. Prentice Hall, ISBN 0-13-703502-0*
 - *High Speed Digital Design: A Handbook of Black Magic, Howard W. Johnson & Martin Graham. Prentice Hall, ISBN 0-13-395724-1*

DRAM Register Programming Aid Walkthrough.

- MX6DQ DDR3 Example
(based on DDR3 validation board)



DRAM Register Programming Aid - Walkthrough

Instructions

Shaded cells may require updating per the DRAM memory data sheet parameters. Certain registers should not need to be modified by the user. If a register is not provided then it is assumed this parameter is not to be changed per the provided initialization script. Certain registers are provided though they may be noted as recommended to not change.

For Sabre boards with CS1 not populated, set this to 1

Legend

On Register Configuration Tab, this color indicates the bitfields that would commonly require updating.	
On Register Configuration Tab, this color indicates the bitfields that may be updated, but should typically not require it.	
On Register Configuration Tab, this color indicates the bitfields that are updated automatically from setting provided in the "Device Information" table or other cells, and should not be changed manually	Automatically Updated Setting
On Register Configuration Tab, an unshaded cell means that the value should remain as is and should not be modified. In these cases, the settings are provided for completeness.	
On other tabs, this color indicates the cells that are affected by changes on the Register Configuration tab.	

Device Information	
Memory type:	DDR3
Manufacturer:	Micron
Memory part number:	MT41J128M16HA-15E
Density of each DDR3 device (Gb):	2
Number of DRAM devices per chip select	4
Density per chip select (Gb) ¹ :	8
Number of Chip Selects used ²	2
Total DRAM density (Gb)	16
Number of ROW Addresses ²	14
Number of COLUMN Addresses ²	10
Number of BANKS ²	8
Bus Width (input 16, 32, or 64 bits) ²	64
Clock Cycle Freq (MHz) ³	533
Clock Cycle Time (ns)	1.876

User inputs clock speed "Clock Cycle (ns)" will change accordingly, value used throughout tool

Revision History

- 0.9 - Fixed issue with SDCKE0/1 IOMUX programming (DSE set in CTLDS)
- 0.8 - Made calibration values update-able in the Register Configuration tab to easily update the values in the RealView .inc file tab
- 0.7 - added DDR_SEL field to DRAM_RESET pad, changed MR1 write (needed to align with DDR_SEL field set to 11).
- 0.6 - added power savings features to align with validation scripts
- 0.5 - added MPODCTRL register programming option
- 0.4 - updated tMOD field: In DDR3 mode this field should be set to max (tMRD,tMOD).
- 0.3 - fixed DDR_4_BANK description
- 0.2 - grammatical corrections
- 0.1 - initial

1. Important: it is necessary to populate this field with the density in Gbits as it is used later in the CS0_END calculation. This field is calculated from the previous two fields. The user can also simply type in the total density as well in this field.
2. Important, these fields need to be filled out correctly as these values are used later in this tool for register settings.
3. Even though i.MX6Q runs at 528MHz, set timings according to 533MHz to allow for a little more margin

Pull down menu for DSE

From the ref manual

000	DISABLED — Output driver disabled.
001	240OHM — 240 Ohm
010	120OHM — 120 Ohm
011	80OHM — 80 Ohm
100	60OHM — 60 Ohm
101	48OHM — 48 Ohm
110	40OHM — 40 Ohm
111	34OHM — 34 Ohm

DRAM Pad Name	Field (i.e. DSE)	Binary Setting	bit setting within register	Notes	Pad Register value (HEX)
SDQS[7:0]	DSE	111	00000038	000: output driver disabled 001: Weakest ... 111: Strongest	IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS[7:0] 0x020e05a8 0x020e05b0 0x020e0524 0x020e051c 0x020e0518 0x020e050c 0x020e05b8 0x020e05c0
DQM[7:0]	DDR_INPUT	0	00000000	0: CMOS mode (recommended) 1: Differential input mode	IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM[7:0] 0x020e05ac 0x020e05b4 0x020e0528 0x020e0520 0x020e0514 0x020e0510 0x020e05bc 0x020e05c4
	DSE	111	00000030	000: output driver disabled 001: Weakest ... 111: Strongest	



DRAM Register Programming Aid - Walkthrough

SDCLK_0, SDCLK_1	DDR_INPUT	0	00000000	0: CMOS mode (recommended) 1: Differential input mode	IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCLK_0	0x020e0588	0x00000030
	DSE	110	00000030	000: output driver disabled 001: Weakest ... 111: Strongest	IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCLK_1	0x020e0594	
DRAM_RESET	DDR_SEL	11	000C0000	DDR Select Field Select one out of next values for pad: DRAM_RESET. 00 Reserved 01 Reserved 10 LPDDR2 mode (240 Ohm driver unit calibration, 240, 120, 80, 60, 48, 40, 32 Ohm drive strengths at 1.2V) 11 DDR3 mode (240 Ohm driver unit calibration, 240, 120, 80, 60, 48, 40, 32 Ohm drive strengths at 1.5V)	IOMUXC_SW_PAD_CTL_PAD_DRAM_RESET	0x020e057c	0x000C0030
	DSE	110	00000030	0: CMOS mode (recommended) 1: Differential input mode 000: output driver disabled 001: Weakest ... 111: Strongest			
SDCKE0, SDCKE1 (DSE (drive strength) configured in CTLDS)	DDR_INPUT	0	00000000	0: CMOS mode (recommended) 1: Differential input mode	IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCKE0	0x020e0590	0x00003000
	HYS	0	00000000	0: Hysteresis disable (recommended) 1: Hysteresis enable			
	PUS	0	00000000	Pull Up / Down Config. Field 00: 100K Ohm Pull Down (recommended) 01: 47K Ohm Pull Up 10: 100K Ohm Pull Up 11: 22K Ohm Pull Up	IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCKE1	0x020e0598	
	PUE	1	00002000	Pull / Keep Select Field 0: Keeper			
	PKE	1	00001000	Pull / Keep Enable Field 0: Pull/Keeper Disabled 1: Pull/Keeper Enabled (recommended)			
	ODT	000	00000000	On Die Termination Field 000: off (recommended) 001 120 Ohm ODT ... 110 20 Ohm ODT 111 RESERVED			
SDODT0, SDODT1	DDR_INPUT	0	00000000	0: CMOS mode (recommended) 1: Differential input mode	IOMUXC_SW_PAD_CTL_PAD_DRAM_SDODT0	0x020e059c	0x00003030
	HYS	0	00000000	0: Hysteresis disable (recommended) 1: Hysteresis enable			
	PUS	0	00000000	Pull Up / Down Config. Field 00: 100K Ohm Pull Down (recommended) 01: 47K Ohm Pull Up 10: 100K Ohm Pull Up 11: 22K Ohm Pull Up	IOMUXC_SW_PAD_CTL_PAD_DRAM_SDODT1	0x020e05a0	
	PUE	1	00002000	Pull / Keep Select Field 0: Keeper			
	PKE	1	00001000	Pull / Keep Enable Field 0: Pull/Keeper Disabled 1: Pull/Keeper Enabled (recommended)			
	ODT	000	00000000	On Die Termination Field 000: off (recommended) 001 120 Ohm ODT ... 110 20 Ohm ODT 111 RESERVED			
	DSE	110	00000030	000: output driver disabled 001: Weakest ... 111: Strongest			

Continuation of "IOMUX part" of DRAM Register Programming aid

Note, for Sabre boards with only one CS populated, we found we can reduce all DRAM IO DSE to 101



DRAM Register Programming Aid - Walkthrough

Continuation of "IOMUX part" of
DRAM Register Programming aid

Many IO's are grouped together

B0DS, B1DS, B2DS, B3DS, B4DS, B5DS, B6DS, B7DS (DRAM data byte groups)	DSE	110	00000030	000: output driver disabled 001: Weakest ... 111: Strongest	IOMUXC_SW_PAD_CTL_PAD_ DRAM_B[7:0]DS	0x020e0784 0x020e0788 0x020e0794 0x020e079c 0x020e07a0 0x020e07a4 0x020e07a8 0x020e0748	0x00000030
ADDSDS (DRAM Address pads A[15:0] and SDBA[2:0])	DSE	110	00000030	000: output driver disabled 001: Weakest ... 111: Strongest	IOMUXC_SW_PAD_CTL_PAD_ DRAM_ADDSDS	0x020e074c	0x00000030
CTLDS (DRAM Control pads CS0, CS1, SDBA2, SDCKE0, SDCKE1, SDWE)	DSE	110	00000030	000: output driver disabled 001: Weakest ... 111: Strongest	IOMUXC_SW_PAD_CTL_GRP_ CTLDS	0x020e078c	0x00000030
DDRMODE_CTL	DDR_INPUT	1	00020000	DDR / CMOS Input Mode Field Select one out of next values for group: DDRMODE_CTL (Pads: DRAM_SDQS0 DRAM_SDQS1 DRAM_SDQS2 DRAM_SDQS3 DRAM_SDQS4 DRAM_SDQS5 DRAM_SDQS6 DRAM_SDQS7). 0: CMOS input type 1: Differential input mode (recommended)	IOMUXC_SW_PAD_CTL_GRP_ DDRMODE_CTL	0x020e0750	0x00020000
DDRMODE	DDR_INPUT	1	00020000	DDR / CMOS Input Mode Field Select one out of next values for group: DDRMODE (Pads: DRAM_D[63:0]). 0: CMOS input type 1: Differential input mode (recommended)	IOMUXC_SW_PAD_CTL_GRP_ DDRMODE	0x020e0774	0x00020000
DDR_TYPE	DDR_SEL	11	000C0000	DDR Select Field Select one out of next values for group: DDR_TYPE for all DDR address, data, and control pads 00: reserved 01: reserved 10: LPDDR2 mode (240Ohm driver unit calibration, 240, 120, 80, 60, 48, 40, 34 Ohm drive strengths) at 1.2V power 11: DDR3 mode (240Ohm driver unit calibration, 240, 120, 80, 60, 48, 40, 34 Ohm drive strengths) at 1.5V power (required for DDR3)	IOMUXC_SW_PAD_CTL_GRP_ DDR_TYPE	0x020e0798	0x000C0000
DDRPKE	PKE	0	00000000	Pull / Keep Enable Field for DDR pads 0: Pull/Keeper Disabled (recommended) 1: Pull/Keeper Enabled	IOMUXC_SW_PAD_CTL_GRP_ DDRPKE	0x020e0758	0x00000000



DRAM Register Programming Aid - Walkthrough

For Sabre boards with CS1 not populated, we need to clear this bit (SDE_1)

MMDC Control Parameter	N/A	control bit setting (decimal)	bit setting within register	Notes	Register name	Register address	Register value (HEX)
SDE_0	-	1	80000000	SDE_0: Enable Chip Select 0, set to 0 (disable) or 1 (enable)	MDCTL	0x021B0000	0xC31A0000
SDE_1	-	1	40000000	SDE_1: Enable Chip Select 1, set to 0 (disable) or 1 (enable)			
ROW	-	3	03000000	ROW: number of ROW addresses. NOTE: this value is taken from the Device Information table above. Modify this value only in the table above.			
COL	-	1	00100000	COL number of Column addresses. NOTE: : this value is taken from the Device Information table above. Modify this value only in the table above.			
BL	-	1	00080000	BL: Burst length. For DDR3, set to 1 for burst length 8.			
DSIZ	-	2	00020000	DSIZ: Data bus size. Note: this value is taken from the Device Information table above. Modify this value only in the table above.			

These are automatically updated from previous parameter settings

MMDC timing parameter (DDR device timing parameter)	value from DDR data sheet (ns)	Clock Cycle or Binary Setting	bit setting within register	Notes	Register name	Register address (HEX)	Register value (HEX)
tCKE	5.625	3	00020000	tCKE - KE minimum pulse width. Obtain this value from DDR3 data sheet.	MDPDC	0x021B0004	0x00020036
tCKSRX	10	6	00000030	tCKSRX - This field determines the amount of clock cycles before self-refresh exit. Obtain this value from DDR3 data sheet.			
tCKSRE	10	6	00000006	tCKSRE - This field determines the amount of clock cycles before self-refresh entry. Obtain this value from DDR3 data sheet.			
PWDT_1	-	5	00005000	Power Down Timer - Chip Select 1. Freescale validation determined a value of 5 was the most optimal. For systems with only one chip select with devices on CS0, these bits don't apply, but keeping them set will allow backwards compatibility with systems with two chip selects.			
PWDT_0	-	5	00000500	Power Down Timer - Chip Select 0. Freescale validation determined a value of 5 was the most optimal.			
BOTH_CS_PD	-	1	00000040	Parallel power down entry to both chip selects. Leave this set so that both chip selects will enter power down together. For systems with only one chip select, this bit doesn't apply, but keeping it set will allow backwards compatibility with systems with two chip selects.			

There are two separate settings, first for initialization, the second enables power savings, it gets placed at end of initialization

JEDEC standard timing parameters, obtain value from DDR3 data sheet

For Sabre boards with CS1 not populated, we can keep these parameters untouched as they have no adverse affect and will minimize differences between init scripts

DRAM Register Programming Aid - Walkthrough

tAOFPD	2	2	08000000	tAOFPD - This field determines the time between termination circuit starts to turn off the ODT resistance till termination has reached high impedance. Obtain this value from DDR3 data sheet.	MDOTC	0x021B0008	0x09444040
tAONPD	2	2	01000000	tAONPD - This field determines the time between termination circuit gets out of high impedance and begins to turn on till ODT resistance are fully on. Obtain this value from DDR3 data sheet.			
tANPD	-	5	00400000	tANPD - Asynchronous ODT to power down entry delay. In DDR3 should be set to tCWL-1. Obtain this value from DDR3 data sheet. This is also calculated from MDCGFG1[tCWL].			
tAXPD	-	5	00040000	tAXPD - Asynchronous ODT to power down exit delay. In DDR3 should be set to tCWL-1. Obtain this value from DDR3 data sheet. This is also calculated from MDCGFG1[tCWL].			
tODTLon	-	4	00004000	tODTLon - This field determines the delay between ODT signal and the associated RTT, where according to JEDEC standard it equals WL(write latency) - 2. Therefore, the value that is configured to tODTLon field should correspond the value that is configured to MDCGFG1[tCWL]. Obtain this value from DDR3 data sheet. This is also calculated from MDCGFG1[tCWL].			
tODT_idle_off	-	4	00000040	memory ODT off. Obtain this value from DDR3 data sheet. Usually just tCWL-2.	MDCFG0	0x021B000C	0x555A7975
tRFC	160	86	55000000	tRFC - Refresh command to Active or Refresh command time. Obtain this value from DDR3 data sheet.			
tXS	170	91	005A0000	tXS - Exit self refresh to non READ command. Obtain this value from DDR3 data sheet.			
tXP	6	4	00006000	tXP - Exit power down with DLL-on to any valid command. Obtain this value from DDR3 data sheet.			
tXPDLL	24	13	00001800	tXPDLL - Exit precharge power down with DLL frozen to commands requiring DLL. Obtain this value from DDR3 data sheet.			
tFAW	45	24	00000170	tFAW - Four Active Window (all banks). Obtain this value from DDR3 data sheet.			
tCL	13.5	8	00000005	tCL - CAS Read Latency. Obtain this value from DDR3 data sheet.			

These are automatically updated from other parameter settings

JEDEC standard timing parameters, obtain value from DDR3 data sheet

DRAM Register Programming Aid - Walkthrough

JEDEC standard timing parameters, obtain value from DDR3 data sheet

tRCD	13.5	8		tRP - Precharge command period (same bank). Obtain this value from DDR3 data sheet.	MDCFG1	0x021B0010	0xFF538F64
tRP	13.5	8	1C000000	tRC - Active to Active or Refresh command period (same bank). Obtain this value from DDR3 data sheet.			
tRC	49.5	27	03400000	tRAS - Active to Precharge command period (same bank). Obtain this value from DDR3 data sheet.			
tRAS	36	20	00130000	tRPA - Precharge-all command period. Obtain this value from DDR3 data sheet.			
tRPA	-	1	00008000	tWR - WRITE recovery time (same bank). Obtain this value from DDR3 data sheet.			
tWR	15	8	00000E00	tMRD - Mode Register Set command cycle (all banks). Obtain this value from DDR3 data sheet. In DDR3 mode this field should be set to max (tMRD,tMOD).			
tMRD	-	12	00000160	tCWL - CAS Write Latency. Obtain this value from DDR3 data sheet.			
tCWL	-	6	00000004	tDLLK - DLL locking time. 512			
tDLLK	-	512	01FF0000	tRTP - Internal READ command period (same bank). Obtain this value from DDR3 data sheet.			
tRTP	7.5	4	000000C0	tWTR - Internal WRITE to READ recovery time (same bank). Obtain this value from DDR3 data sheet.			
tWTR	7.5	4	00000018	tRRD - Active to Active command period (same bank). Obtain this value from DDR3 data sheet.			
tRRD	6	4	00000003	tXPR - Obtain this value from DDR3 data sheet.			
tXPR	170	91	005A0000	SDE_to_RST			
SDE_to_RST	-	13	00000E00	RST_to_CKE			
RST_to_CKE	-	32	00000021				

MMDC pin	Chip select 0 pin	Chip select 1 pin
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5
A7	A7	A8
A8	A8	A7
B0	B0	B1
B1	B1	B0

MMDC Control Parameter	N/A	control bit setting (decimal)	bit setting within register				
CALIB_PER_CS	-	0	00000000	CALIB_PER_CS: determines which chip select the associated calibration is targeted to. Set to 0 for CS0 or 1 for CS1. Note if both chip selects are populated, recommend to set to 0.	MDMISC	0x021B0018	0x00081740
ADDR_MIRROR	-	1	00080000	ADDR_MIRROR: for DDR3, address bits in the following pairs [A3,A4], [A5,A6], [A7,A8], [B0,B1] are swapped from the MMDC to CS1 to aid in routing of the DDR device on CS1. As DDR devices on CS1 are placed on the opposite side of the board from CS0, swapping these signals aids in the board routing. If the board enables this feature and routes these signals accordingly, then set this bit. Otherwise, this bit should be cleared.			
LHD	-	0	00000000	LHD: Latency hiding disable. Recommend to clear this bit to enable latency hiding and improve performance.			
WALAT	-	0	00000000	WALAT: Write Additional latency. Recommend to clear these bits. Proper board design should ensure that the DDR3 devices are placed close enough to the MMDC to ensure that the shew between CLK and DQS is less than 1 cycle.			
BI_ON	-	1	00001000	BI_ON: Bank Interleaving On. Recommend to set this bit to enable bank interleaving; improves performance.			
LPDDR2_S2	-	0	00000000	Set to 0; not applicable to DDR3.			
MIF3_MODE	-	3	00000600	MIF3_MODE: Command prediction working mode; set to 0x3 for optimal performance.			
RALAT	-	5	00000140	RALAT: Read Additional Latency. Set to 0x5 for optimal performance.			
DDR_4_BANK	-	0	00000000	DDR_4_BANK: set to 0 for 8 banks, 1 for 4 banks. NOTE: this value is taken from the Device Information table above. Modify this value only in the table above.			
DDR_TYPE	-	0	00000000	DDR3 mode - set to 0. Do not change.			
LPDDR2_2CH	-	0	00000000	Set to 0; not applicable to DDR3.			
RST	-	0	00000000	Set to 0 for normal operation.			

Needs to align with board layout
Sabre boards don't populate CS1, so clear this bit

If any WL calibration parameter >0x20, should set WALAT = 1.

Because this is a dedicated DDR3 programming aid, these values are pre-set and not to be changed



DRAM Register Programming Aid - Walkthrough

MMDC Parameter	Calculated End Address (starting at offset 0x10000000)	control bit setting (decimal)	bit setting within register	Notes	Register name	Register address	Register value (HEX)
CS0_END	0x50000000	39	00000027	Note: DO NOT change the values directly in these cells, instead, program the Density of each DDR device and number of devices in the cells at the top of the page. End Address is calculated from cells above: Density of each DDR device multiplies by the number of devices per chip select, then add offset of 256MB. Note that the total DDR density on CS0 is offset by 0x1000000, which is the starting address of the CS0 memory region. Hence the CS0_END is the sum of the DDR density on CS0 with offset 0x10000000.	MDASP	0x021B0040	0x00000027

MMDC Control Parameter	N/A	control bit setting (decimal)	bit setting within register	Notes	Register name	Register address	Register value (HEX)
------------------------	-----	-------------------------------	-----------------------------	-------	---------------	------------------	----------------------

ODT3_INT_RES	-	1	00020000	On chip ODT byte3 resistor - This field determines the Rtt_Nom of the on chip ODT byte3 resistor during read accesses. For x64 configuration, this applies to byte 7 with register address at 0x021B4818. 000 Rtt_Nom Disabled. 001 Rtt_Nom 120 Ohm/75 Ohm 010 Rtt_Nom 60 Ohm/150 Ohm (default setting for FSL boards) 011 Rtt_Nom 40 Ohm/50 Ohm 100 Rtt_Nom 30 Ohm/37.5 Ohm 101 Rtt_Nom 24 Ohm/30 Ohm 110 Rtt_Nom 20 Ohm/25 Ohm 111 Rtt_Nom 17 Ohm/21 Ohm	MPODCTRL	0x021B0818 0x021B4818	0x00011117
ODT2_INT_RES	-	1	00002000	On chip ODT byte2 resistor - This field determines the Rtt_Nom of the on chip ODT byte2 resistor during read accesses. For x64 configuration, this applies to byte 6 with register address at 0x021B4818.			
ODT1_INT_RES	-	1	00000200	On chip ODT byte1 resistor - This field determines the Rtt_Nom of the on chip ODT byte1 resistor during read accesses. For x64 configuration, this applies to byte 5 with register address at 0x021B4818.			
ODT0_INT_RES	-	1	00000020	On chip ODT byte0 resistor - This field determines the Rtt_Nom of the on chip ODT byte0 resistor during read accesses. For x64 configuration, this applies to byte 4 with register address at 0x021B4818.			
ODT_RD_ACT_EN	-	0	00000000	Active read CS ODT enable. The bit determines if ODT pin of the active CS will be asserted during read accesses. 0 Active CS ODT pin is disabled during read access. 1 Active CS ODT pin is enabled during read access. This is generally not set for Freescale boards			
ODT_RD_PAS_EN	-	1	00000004	Inactive read CS ODT enable. The bit determines if ODT pin of the inactive CS will be asserted during read accesses. 0 Inactive CS ODT pin is disabled during read accesses to other CS. 1 Inactive CS ODT pin is enabled during read accesses to other CS. For Freescale boards with devices on both chip selects, this bit is generally set as the board layout considers termination applied for the non-active chip select device. For boards with a device on only one chip select, this bit can be cleared, however, leaving it set should not cause any issues.			
ODT_WR_ACT_EN	-	1	00000002	Active write CS ODT enable. The bit determines if ODT pin of the active CS will be asserted during write accesses. 0 Active CS ODT pin is disabled during write access. 1 Active CS ODT pin is enabled during write access. For Freescale boards with devices on both chip selects, this bit is generally set. In some cases, the board may be designed to account for the termination of only the other (passive) device during writes, hence this bit can be cleared. However, even in such a case, leaving it set does not cause any issues. For boards with only one chip select populated, it is recommended to set this bit. Hence, by default, this bit remains set.			
ODT_WR_PAS_EN	-	1	00000001	Inactive write CS ODT enable. The bit determines if ODT pin of the inactive CS will be asserted during write accesses. 0 Inactive CS ODT pin is disabled during write accesses to other CS. 1 Inactive CS ODT pin is enabled during write accesses to other CS. For Freescale boards with devices on both chip selects, this bit is generally set as the board layout considers termination applied for the non-active chip select device. For boards with a device on only one chip select, this bit can be cleared, however, leaving it set should not cause any issues.			

This gets calculated from the "density parameter per chip select "(cell C21). You can click on the cells to see the following formulas:
 ="0x"&DEC2HEX(((C21*1024*1024*1024)/8+ 256*1024*1024), 8)
 =(((C19*C20*1024*1024*1024)/8+ 256*1024*1024)/(32*1024*1024))-1)

More details of this in the next slide



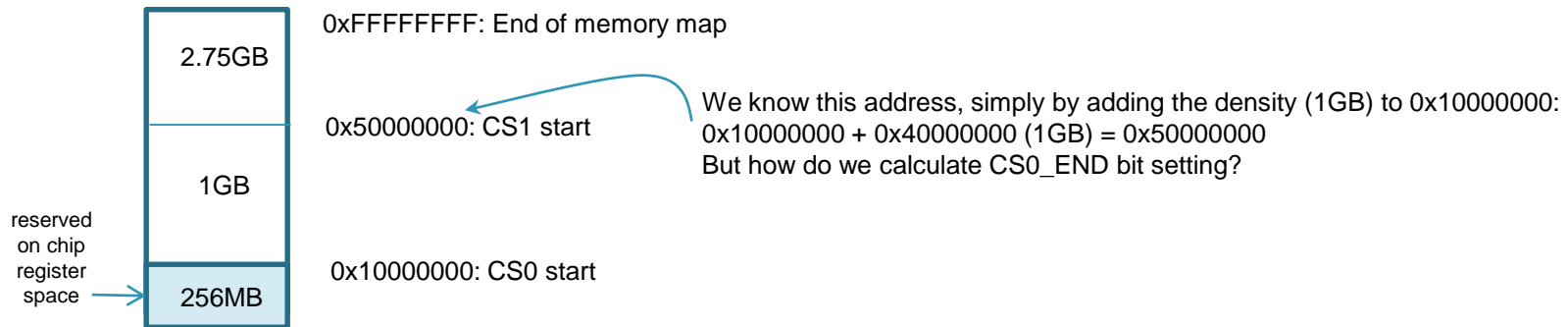
DRAM Register Programming Aid - Walkthrough

- **MDASP: CS0_END** defines the absolute last address associated with CS0 with increments of 256Mb (32MB)

CS0_END bit settings:

Register bit setting
0000000 - 256Mb (32MB)
0000001 - 512Mb
0000010 - 768Mb
.
0011111 - 8Gb (1GB)
0111111 - 16Gb (2GB)
1111111 - 32Gb (4GB)

- Note, these offsets *start* from address 0x0, in general CS0 starts at 0x10000000; these are not offsets from 0x10000000!
- So, a CS0_END setting of 0000000 means that CS0 ends at 0x02000000 (before it begins).. Yeah, this setting is meaningless
 - Actually, any setting from 0000000 to 0000111 is meaningless (0000111 is 256MB (2Gb) which is 0x10000000)
 - Example, assume there is 1GB (8Gbits) of DDR3 memory on CS0



To calculate CS0_END setting, first remember this is the absolute address starting from 0x0.
Next, as seen in the figure above, calculate the end address of CS0 by adding the DRAM density to 0x10000000.
Now that we have the end (absolute) address, take this value and divide by 256MB (32MB) then subtract 1 (since CS0_END = 0 starts at 256Mb).

Taking the example above, density = 1GB, so CS0 end is $0x10000000 + 0x40000000 = 0x50000000$
 $(0x50000000 / 0x2000000) - 1 = 39$ decimal (or 0x27) (or 0100111)

Generically: $[(0x10000000 + \text{density_MB}) / 0x2000000] - 1 = \text{CS0_END setting}$

32MB = 0x2000000

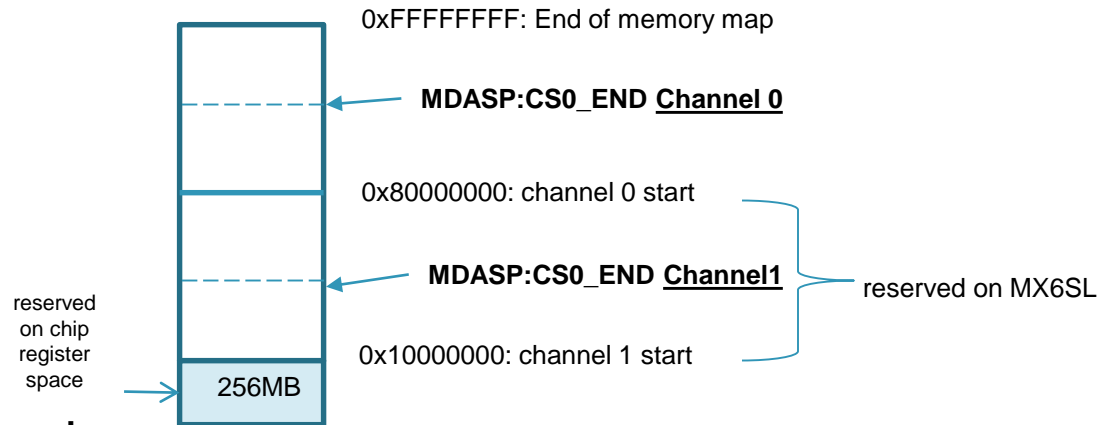
DRAM Register Programming Aid - Walkthrough

- **DDR mapping to MMDC controller ports**
 - Section 2.3 of the Reference Manual
 - Specifies the DDR setting used by the Network Interconnect Bus System
 - Must be set correctly for the AXI bus (or buses) to work with the MMDCs.
 - Allowed values:
 - '00 Fixed memory Map for use with DDR3 memory (Default)
 - '01 Fixed memory Map for use with LPDDR2 memory
 - '10 Interleaved memory Map for use with 2-channel LPDDR2 memory.
- **Can be set by customer in one of two ways:**
 - BTCFG3[5:4] pins EIM_A20 (bit4), EIM_A21 (bit5)
 - Blow internal OTP fuses for BTCFG3[5:4]
 - Un-documented register 0x00B00000 allows Freescale to override external settings.
- **Interleaving is done internal to the NIC-301 controller**
 - Memory enters MMDC already addressed for 2-channel mode, except:
 - Channel 0 starts at 0x88000000
 - Channel 1 starts at 0x08000000

DRAM Register Programming Aid - Walkthrough

- **MDASP: CS0_END 2-channel LPDDR2: “Fixed Mode”**

- Each channel has a set starting address
 - Channel 0: 0x80000000
 - Channel 1: 0x10000000
- You can use a 1-channel LPDDR2 device, need to pick a channel (channel 0 is most common choice)
 - MX6SL (aka Megrez) only has channel 0, so MMDC DRAM memory space starts at 0x80000000
- For MX6DQ (Arik) and MX6DL (Rigel), there are two MDASP:CS0_END, one for each LPDDR2 channel



- **Calculate CS0_END for each channel**

- Channel 0: $[(0x80000000 + \text{density_MB}) / 0x2000000] - 1$

Example1: 2 chip select, each with 512MB, $CS0_END = [(0x80000000 + 0x20000000) / 0x2000000] - 1 = 0x4F$

Example2: 2 chip select, each with 256MB, $CS0_END = [(0x80000000 + 0x10000000) / 0x2000000] - 1 = 0x47$

- Channel 1: $[(0x10000000 + \text{density_MB}) / 0x2000000] - 1$ (not for MX6SL)

Example1: 2 chip select, each with 512MB, $CS0_END = [(0x10000000 + 0x20000000) / 0x2000000] - 1 = 0x17$

Example2: 2 chip select, each with 256MB, $CS0_END = [(0x10000000 + 0x10000000) / 0x2000000] - 1 = 0xF$

DRAM Register Programming Aid - Walkthrough

- **MDASP: CS0_END 2-channel LPDDR2: “Interleaved Mode”**

- **Slightly different.**

- Each channel has a set starting address

- Channel 0: 0x88000000
- Channel 1: 0x08000000

- **Calculate CS0_END for each channel**

- Channel 0: $[(0x88000000 + \text{density_MB}) / 0x2000000] - 1$

Example1: 2 chip select, each with 512MB, CS0_END=[(0x88000000+0x20000000)/0x2000000]-1=0x53

Example2: 2 chip select, each with 256MB, CS0_END=[(0x88000000+0x10000000)/0x2000000]-1=0x4B

- Channel 1: $[(0x08000000 + \text{density_MB}) / 0x2000000] - 1$

Example1: 2 chip select, each with 512MB, CS0_END=[(0x08000000+0x20000000)/0x2000000]-1=0x13

Example2: 2 chip select, each with 256MB, CS0_END=[(0x08000000+0x10000000)/0x2000000]-1=0xB

DRAM Register Programming Aid - Walkthrough

DDR3 MR2 Parameter or MMDC MDCSR Parameter	N/A	control bit setting (decimal)	bit setting within register	Notes	Register name	Register address	Register value (HEX)			
MR2: RTT	-	2	04000000	Dynamic ODT (RTT(WR)). 00-disabled; 01-RZQ/4; 10-RZQ/2; 11-reserved (RZQ=240ohm)	MDCSR	0x021B001C	0x04088032			
MR2: SRT	-	0	00000000	SRT: Self refresh temperature, set to 0 for normal operation						
MR2: ASR	-	0	00000000	ASR: Auto self refresh, set to 0 for normal operation						
MR2: CWL	-	6	00080000	CAS Write Latency. This value is taken from the MMDC tCWL parameter setting above. Do not modify this bit as it is automatically programmed.						
CON_REQ	-	1	00008000	Configuration request - set to 1 for this operation.						
WL_EN	-	0	00000000	Set to 0; not applicable to mode register programming.						
CMD	-	3	00000030	CMD: set to 0x3 for load mode register command.						
CMD_CS	-	0	00000000	Determines which chip select command is targeted to.						
CMD_BA	-	2	00000002	CMD_BA - set to 0x2 for MR2						
DDR3 MR3 Parameter or MMDC MDCSR Parameter	N/A	control bit setting (decimal)	bit setting within register	Notes				Register name	Register address	Register value (HEX)
MR3: MPR	-	0	00000000	MPR enable - set to 0 for normal operation	MDCSR	0x021B001C	0x00008033			
MR3: MPR_RF	-	0	00000000	Set to 0 for normal operation						
CON_REQ	-	1	00008000	Configuration request - set to 1 for this operation.						
WL_EN	-	0	00000000	Set to 0; not applicable to mode register programming.						
CMD	-	3	00000030	CMD: set to 0x3 for load mode register command.						
CMD_CS	-	0	00000000	Determines which chip select command is targeted to.						
CMD_BA	-	3	00000003	CMD_BA - set to 0x3 for MR3						
DDR3 MR1 Parameter or MMDC MDCSR Parameter	N/A	control bit setting (decimal)	bit setting within register	Notes				Register name	Register address	Register value (HEX)
MR1: Q Off	-	0	00000000	Set to 0 for normal operation	MDCSR	0x021B001C	0x00048031			
MR1: TDQS	-	0	00000000	Termination data strobe (TDQS) is a function of the x8 DDR3 SDRAM configuration; set to 0 for x16 and x32 memories						
MR1: RTT (M9)	-	0	00000000	On-die termination (ODT) resistance RTT. 000-disabled; 001-RZQ/4; 010-RZQ/2; 011-RZQ/6; 100-RZQ/12; 101-RZQ/8; 110&111-reserved (RZQ=240ohm)						
MR1: RTT (M2)	-	1	00040000							
MR1: WL	-	0	00000000	Write leveling enable - set to 0 for normal operation						
MR1: ODS (M5)	-	0	00000000	Output Drive Strength: 00-RZQ/6 (40ohm); 01-RZQ/7 (34ohm); 10&11-reserved						
MR1: ODS (M1)	-	0	00000000							
MR1: AL	-	0	00000000	AL: Additive Latency, set to 0						
MR1: DLL	-	0	00000000	DLL Enable - set to 0						
CON_REQ	-	1	00008000	Configuration request - set to 1 for this operation.						
WL_EN	-	0	00000000	Set to 0; not applicable to mode register programming.						
CMD	-	3	00000030	CMD: set to 0x3 for load mode register command.						
CMD_CS	-	0	00000000	Determines which chip select command is targeted to.						
CMD_BA	-	1	00000001	CMD_BA - set to 0x1 for MR1						
DDR3 MR0 Parameter or MMDC MDCSR Parameter	N/A	control bit setting (decimal)	bit setting within register	Notes				Register name	Register address	Register value (HEX)
MR0: PD	-	0	00000000	Precharge power-down (PD) - set to 0 for normal operation				MDCSR	0x021B001C	0x09408030
MR0: WR	-	4	08000000	Write recovery. 000-16; 001-5; 010-6; 011-7; 100-8; 101-10; 110-12; 111-14. Make sure to match MMDC tWR.						
MR0: DLL	-	1	01000000	DLL reset - set to 1 to reset DLL; self clearing						
MR0: BT	-	0	00000000	Burst type: set to 0						
MR0: CL (M6)	-	1	00400000							
MR0: CL (M5)	-	0	00000000	CAS latency: 0010-5; 0100-6; 0110-7; 1000-8; 1010-9; 1100-10; 1110-11; 0001-12; 0011-13. Make sure to match CAS to MMDC						
MR0: CL (M4)	-	0	00000000							
MR0: CL (M2)	-	0	00000000	tCL						
MR0: BL	-	0	00000000	Burst length - set to 00 for fixed 8 burst length						
CON_REQ	-	1	00008000	Configuration request - set to 1 for this operation.						
WL_EN	-	0	00000000	Set to 0; not applicable to mode register programming.						
CMD	-	3	00000030	CMD: set to 0x3 for load mode register command.						
CMD_CS	-	0	00000000	Determines which chip select command is targeted to.						
CMD_BA	-	0	00000000	CMD_BA - set to 0x0 for MR0						

Mode Register #



DRAM Register Programming Aid - Walkthrough

if CS1 populated							
DDR3 MR2 Parameter or MMDC MDSCR Parameter	N/A	control bit setting (decimal)	bit setting within register	Notes	Register name	Register address	Register value (HEX)
MR2: RTT	-	2	04000000	Dynamic ODT (RTT(WR)). 00-disable; 01-RZQ/4; 10-RZQ/2; 11-reserved (RZQ=240ohm)	MDSCR	0x021B001C	0x0408803A
MR2: SRT	-	0	00000000	SRT: Self refresh temperature, set to 0 for normal operation			
MR2: ASR	-	0	00000000	ASR: Auto self refresh, set to 0 for normal operation			
MR2: CWL	-	6	00080000	CAS Write Latency. This value is taken from the MMDC tCWL parameter setting above. Do not modify this bit as it is automatically programmed.			
CON_REQ	-	1	00008000	Configuration request - set to 1 for this operation.			
WL_EN	-	0	00000000	Set to 0; not applicable to mode register programming.			
CMD	-	3	00000030	CMD: set to 0x3 for load mode register command.			
CMD_CS	-	1	00000008	Determines which chip select command is targeted to.			
CMD_BA	-	2	00000002	CMD_BA - set to 0x2 for MR2			
DDR3 MR3 Parameter or MMDC MDSCR Parameter	N/A	control bit setting (decimal)	bit setting within register	Notes			



Rest of CS1 mode register programming is exactly the same as CS0

- If board doesn't populate CS1, can still perform mode register writes to CS1 even though nothing there, but preferably...
- Other option, remove CS1 mode register writes in "RealView .inc file" tab:

```
// Mode register writes
setmem /32 0x021b001c = 0x04088032 // MMDC0_MDSCR, MR2 write, CS0
setmem /32 0x021b001c = 0x00008033 // MMDC0_MDSCR, MR3 write, CS0
setmem /32 0x021b001c = 0x00048031 // MMDC0_MDSCR, MR1 write, CS0
setmem /32 0x021b001c = 0x09408030 // MMDC0_MDSCR, MR0 write, CS0
setmem /32 0x021b001c = 0x04008040 // MMDC0_MDSCR, ZQ calibration command sent to device on CS0

setmem /32 0x021b001c = 0x0408803A // MMDC0_MDSCR, MR2 write, CS1
setmem /32 0x021b001c = 0x0000803B // MMDC0_MDSCR, MR3 write, CS1
setmem /32 0x021b001c = 0x00048039 // MMDC0_MDSCR, MR1 write, CS1
setmem /32 0x021b001c = 0x09408038 // MMDC0_MDSCR, MR0 write, CS1
setmem /32 0x021b001c = 0x04008048 // MMDC0_MDSCR, ZQ calibration command sent to device on CS1

setmem /32 0x021b0020 = 0x00005800 // MMDC0_MDREF
setmem /32 0x021b0818 = 0x00022227 // DDR_PHY_P0_MPODCTRL
setmem /32 0x021b4818 = 0x00022227 // DDR_PHY_P1_MPODCTRL
```



DRAM Register Programming Aid - Walkthrough

The final configurable parameters in the Register Configuration tab – calibration values

	Register name	Register address	Register value (HEX)	
<p>These parameters are determined after running calibration. The parameters provided here are from Freescale's development board and will work as initial values. Update these values after running calibration.</p>	MPDGCTRL0 PHY0	0x021b083c	0x434b0350	Read DQS gating
	MPDGCTRL1 PHY0	0x021b0840	0x034c0359	
	MPDGCTRL0 PHY1	0x021b483c	0x434b0350	Read delay line: read DQS-to-DQ delay
	MPDGCTRL1 PHY1	0x021b4840	0x03650348	
	MPRDDCTL PHY0	0x021b0848	0x4436383b	Write delay line: write DQS-to-DQ delay
	MPRDDCTL PHY1	0x021b4848	0x39393341	
	MPWRDLCTL PHY0	0x021b0850	0x35373933	Write leveling
	MPWRDLCTL PHY1	0x021b4850	0x48254a36	
<p>These are for write leveling calibration, which is needed for fly-by board layout topology</p>	MPWLDECTRL0 PHY0	0x021b080c	0x001F001F	
	MPWLDECTRL1 PHY0	0x021b0810	0x001F001F	
	MPWLDECTRL0 PHY1	0x021b480c	0x00440044	
	MPWLDECTRL1 PHY1	0x021b4810	0x00440044	

If you run calibration, then you can update these values with the values found in calibration

more on calibration later ...



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