S32 DDR Tools Suite

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NXP | SECURE CONNECTIONS FOR A SMARTER WORLD

Agenda

- Industry Trends
- Basic DDR SDRAM Structure
- Next Generation of DDR Subsystems
- S32 DDR Tool

Industry Trends

Industry Trend

- DDR4 DRAM pricing is lower or same as DDR3\3L. The pricing crossover occurred around Q4 of 2015. Similarly, LPDDR4 is expected to crossover LPDDR3 in 2018.

- Production DDR4 DRAM, DIMMs and LPDDR4 are available from most DRAM vendors.

- The first NXP device with DDR4 support, T104x product, taped out in Q42013.The LS1043A also supports DDR4. Nearly 4 years of product experience with DDR4.
  - Many current and all future QorIQ products including T1, LS1, and LS2 products will support DDR4.

- The first NXP device with LPDDR4 support is the i.MX8 Family.

DDR3, DDR4 and LPDDR – Major Vendors

Supported by all major memory vendors

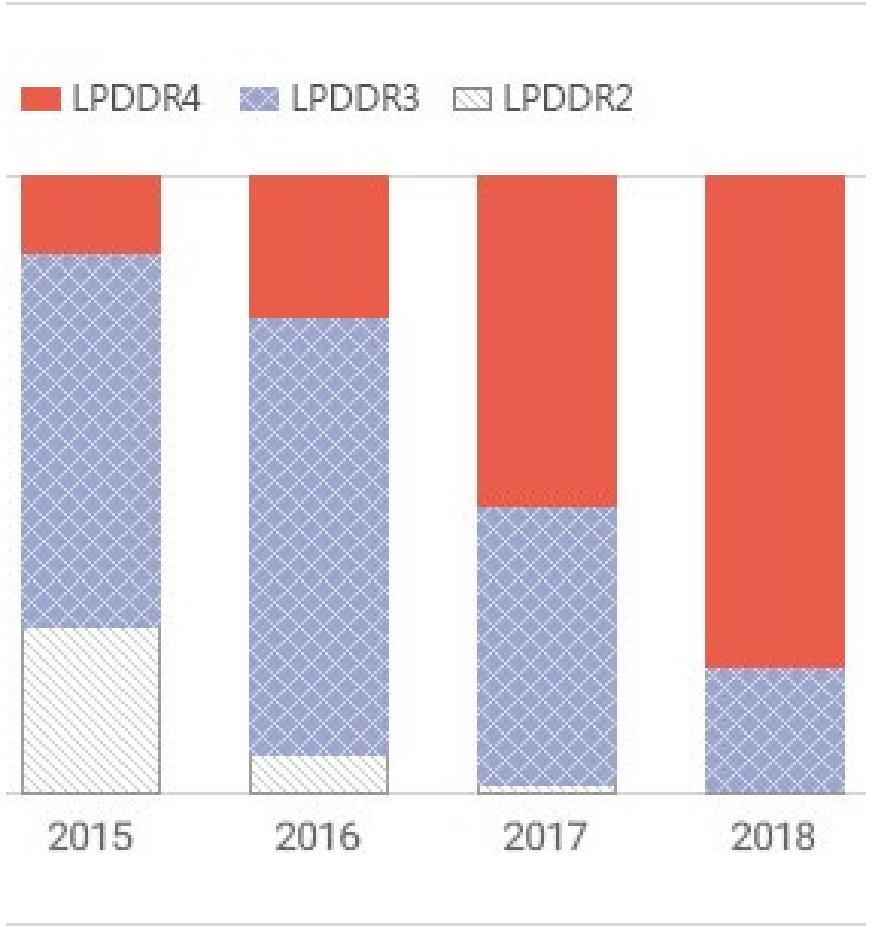
winbond

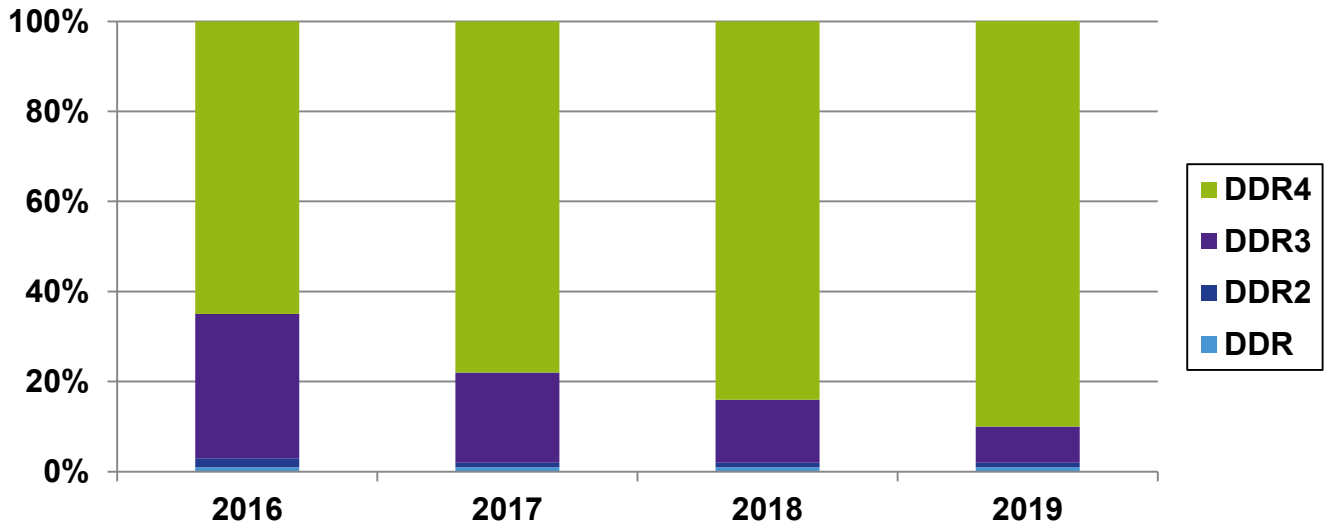
Etron 鈺創科技
Etron Technology, Inc.

ProMOS TECHNOLOGIES

Powerchip 力晶科技

DRAM Migration Roadmap





	2016	2017	2018	2019
DDR	1%	1%	1%	1%
DDR2	2%	1%	1%	1%
DDR3	32%	20%	14%	8%
DDR4	65%	78%	84%	91%

DDR3/DDR3L/DDR4 Power Saving

- DDR3 DRAM provides 20% power savings over DDR2
- DDR3L DRAM provides 10% power savings over DDR3
- DDR4 DRAM provides 37% power savings over DDR3L

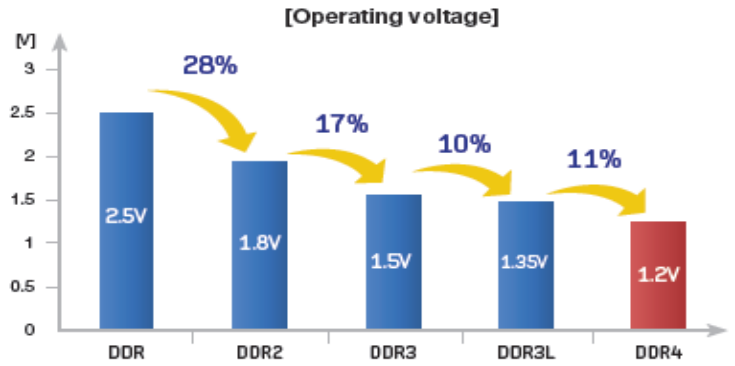


Figure 4. Reduced operating voltage requirements of DDR4 compared to DDR3L

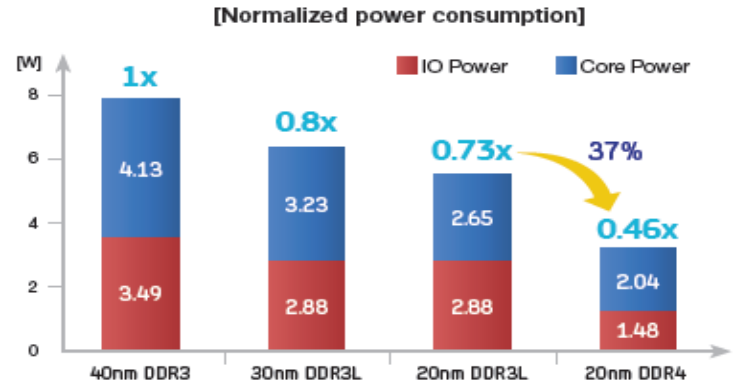


Figure 5. Reduced normalized power consumption requirements of DDR4 compared to DDR3L

SAMSUNG

LPDDR2/LPDDR3/LPDDR4 Power Saving

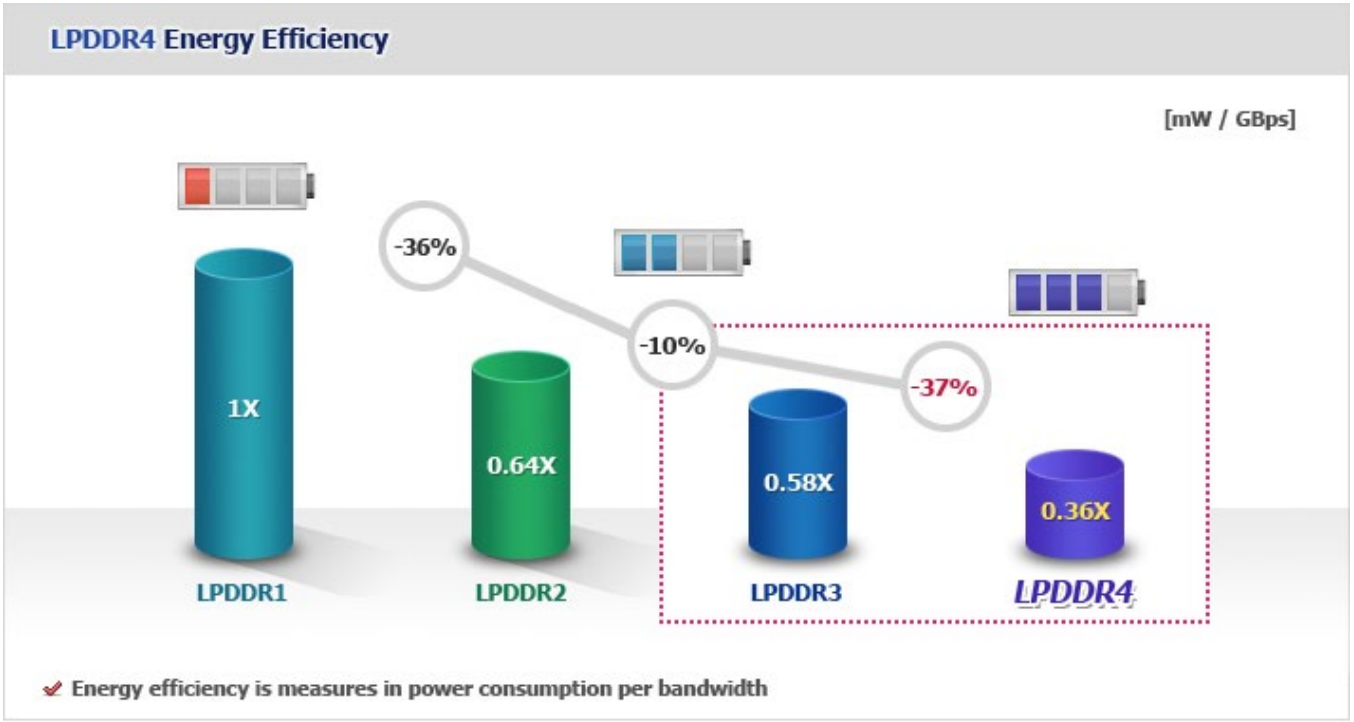
- LPDDR2 DRAM provides 36% power savings over LPDDR1
- LPDDR3 DRAM provides 10% power savings over LPDDR2
- PLDDR4 DRAM provides 37% power savings over LPDDR3

Reductions in operating voltage – LPDDR

1.8V (LPSDR, LPDDR)

1.2V (LPDDR2, LPDDR3)

1.1V, 0.6V (**LPDDR4**/LPDDR4X)



*Source : SEC

DDR SDRAM Highlights and Comparison

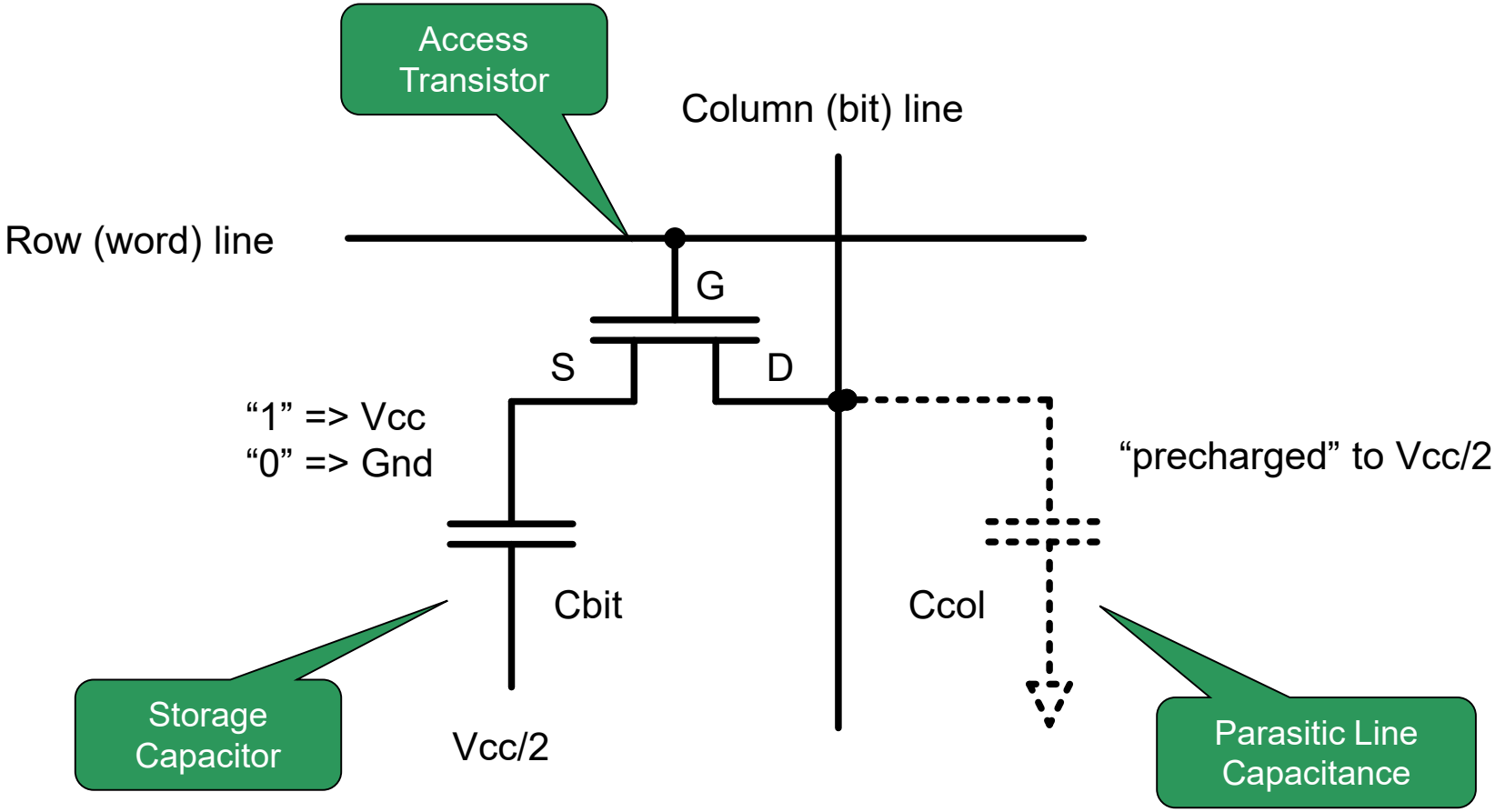
Feature/Category	DDR3	DDR4	LPDDR4
Package	BGA only	BGA only	BGA. PoP, Bare Die
Densities	512Mb -8Gb	2Gb -16Gb	2Gb to 16Gb per channel
Data Bus Organization	x4, x8, x16	x4, x8, x16	x32, (2 channels, x16), x64 (4 channels, x16)
Voltage	DDR3L:1.35V Core & I/O DDR3: 1.5V Core & I/O	1.2V Core 1.2V I/O, also 2.5V external VPP	LPDDR4: 1.1V, 1.8V Core & I/O LPDDR4X: 0.6V
Data I/O CMD, ADDR I/O	Center Tab Termination (CTT) CTT	Pseudo Open Drain (POD) CTT	LVSTL Programable voltage swing
Internal Memory Banks	8	16 for x4/x8 (2 BG), 8 for x16	8 per channel
Data Rate	DDR3/3L: up to2133/1866 MT/s	1600–3200 MT/s	1600-3200 MT/s (possible 4266 MT/s)
VREF	VREFCA & VREFDQ external	VREFCA external VREFDQ internal	CA Vref Internally Generated, Command Bus Training
Data Strobes/Prefetch/Burst Length/Burst Type	Differential/8-bits/BC4, BL8/ Fixed, OTF	Same as DDR3	BL16, BL32

DDR SDRAM Highlights and Comparison (Cont'd)

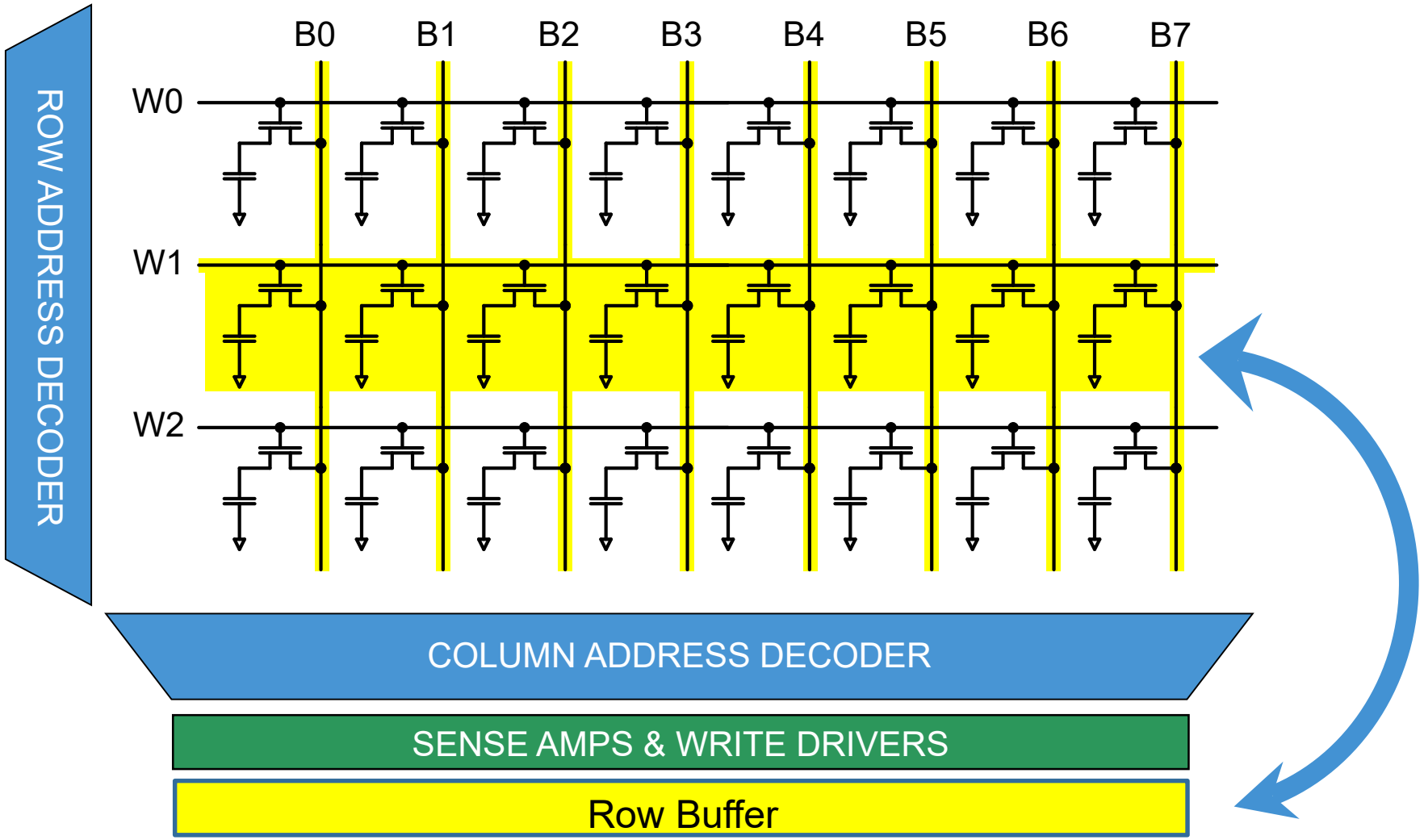
Feature/Category	DDR3	DDR4	LPDDR4
CRC Data Bus & C/A Parity	No	Yes	No
Connectivity test (TEN pin)	No	Yes	No
Bank Grouping	No	Yes	No
Data Bus Inversion	No	Yes	Yes
Write Leveling / ZQ / Reset	Yes	Yes	Yes
ACT_n new pin & command	No	Yes	No
Low power auto self-refresh	No	Yes	Yes
VREFDQ calibration	No	Yes	Yes

Basic DDR SDRAM Structure

Single Transistor Memory Cell

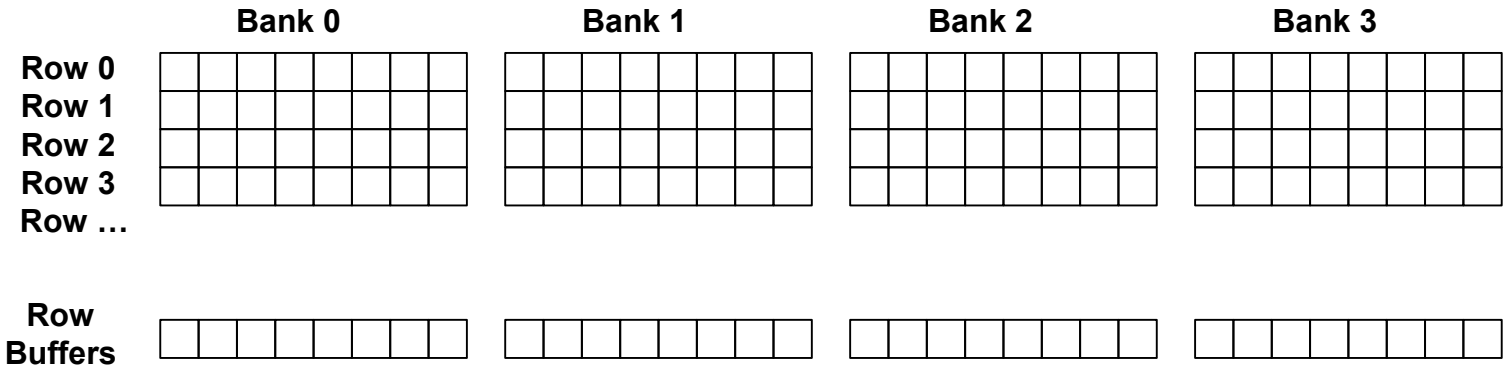


Memory Arrays



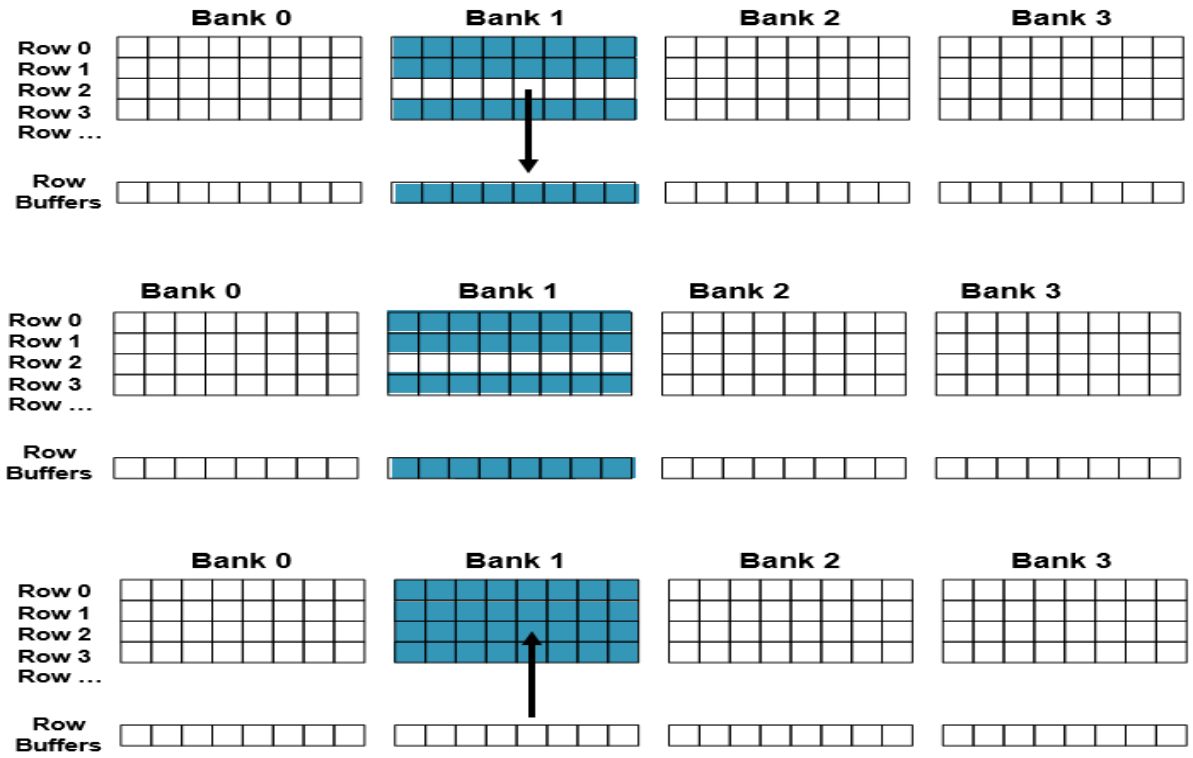
Internal Memory Banks

- Multiple arrays organized into banks
- Multiple banks per memory device
  - DDR3 – 8 banks, and 3 bank address (BA) bits
  - DDR4 – 16 banks with 4 banks in each of 4 sub bank groups
  - Can have one active row in each bank at any given time
- Concurrency
  - Can be opening or closing a row in one bank while accessing another bank



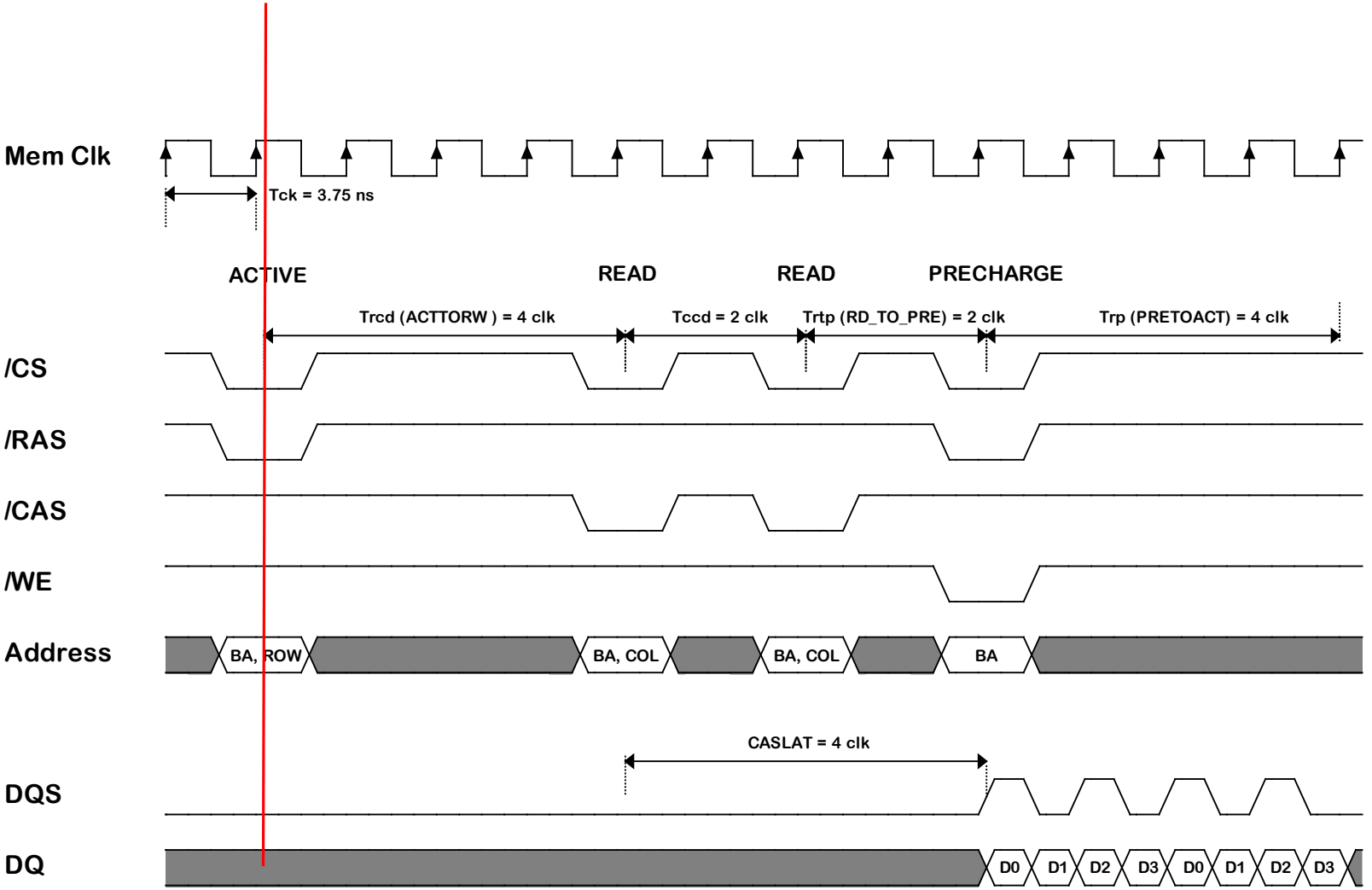
Memory Access

- A requested row is activated and made accessible through the bank's row buffers
- read and/or write are issued to the active row in the row buffers
- The row is precharged and is no longer accessible through the bank's row buffers



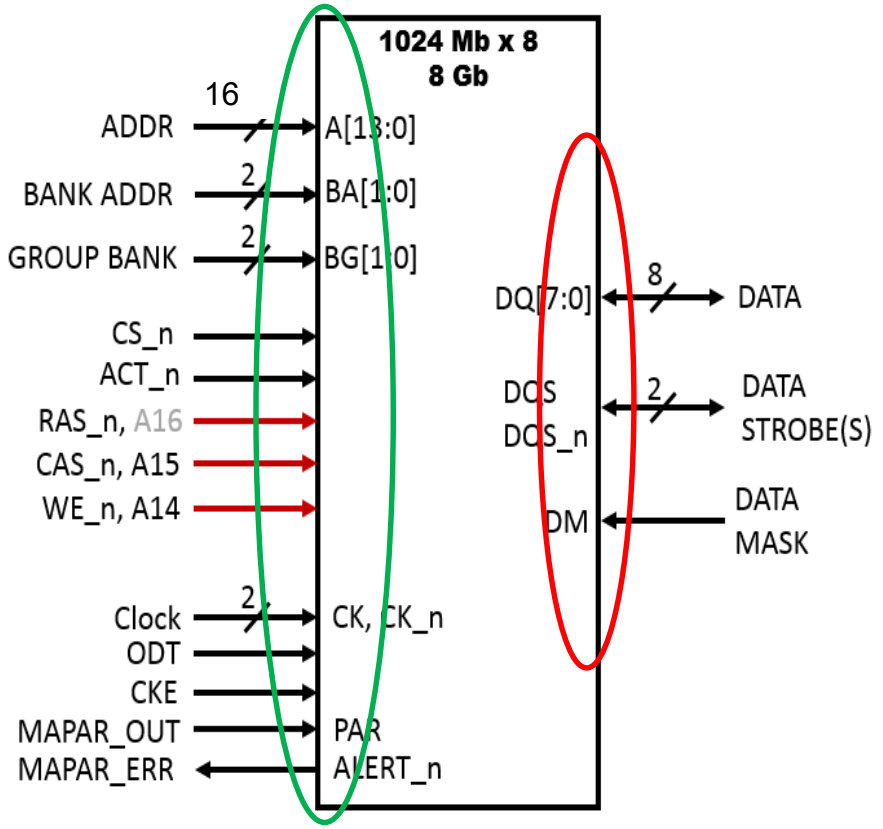
Example: DDR4-2133
Open Page = 2.133Gb/s maximum bandwidth
Closed Page = 199Mb/s maximum bandwidth
10x performance advantage to read and write from an open page

DDR2-533 Read Timing Example



Example – 8Gb DDR4 SDRAM

- Micron MT40A1G8
- 1024M x 8 (64M x 8 x 16 banks)
- 8 Gb total
- 16-bit row address
  - 64K rows
- 10-bit column address
  - 1K bits/row (1KB in x8 data with DRAM)
- 2-bit group and 2-bit bank address
- DATA bus: DQ, DQS, /DQS, DM (DBI)
- ADD bus: A, BA, GB, ACT, /CS, /RAS, /CAS, /WE, ODT, CKE, CK, /CK, PAR, /ALERT



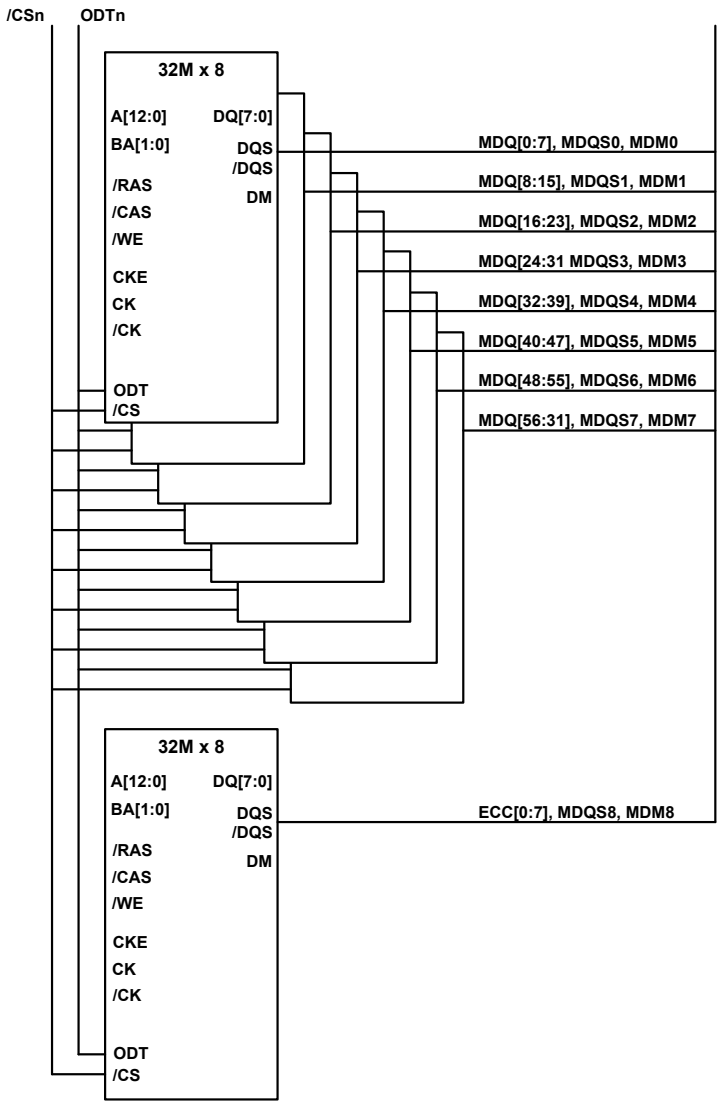
ADD bus DATA bus

Example – DDR4 UDIMM

- Micron MTA9ASF51272AZ
- 9 each 512M x 8 DRAM devices
- 512M x 72 overall
- 4 GB total, single “rank”
- 9 “byte lanes”

Two Signal Bus

- 1- Address, command, control, and clock signals are shared among all 9 DRAM devices
- 2- Data, strobe, data mask not shared



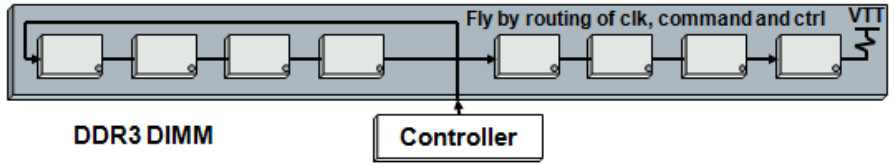
DRAM Module Type

UDIMM: Unbuffered Desktop standard

MiniDIMM:
Computing and Networking

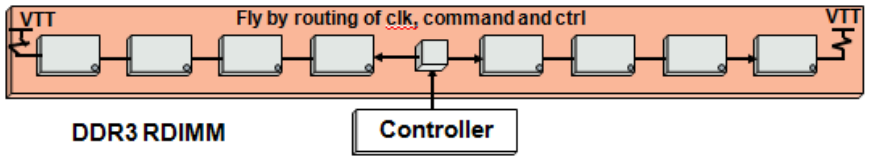
SODIMM: Notebook standard

VLP MiniDIMM:
Computing and Networking



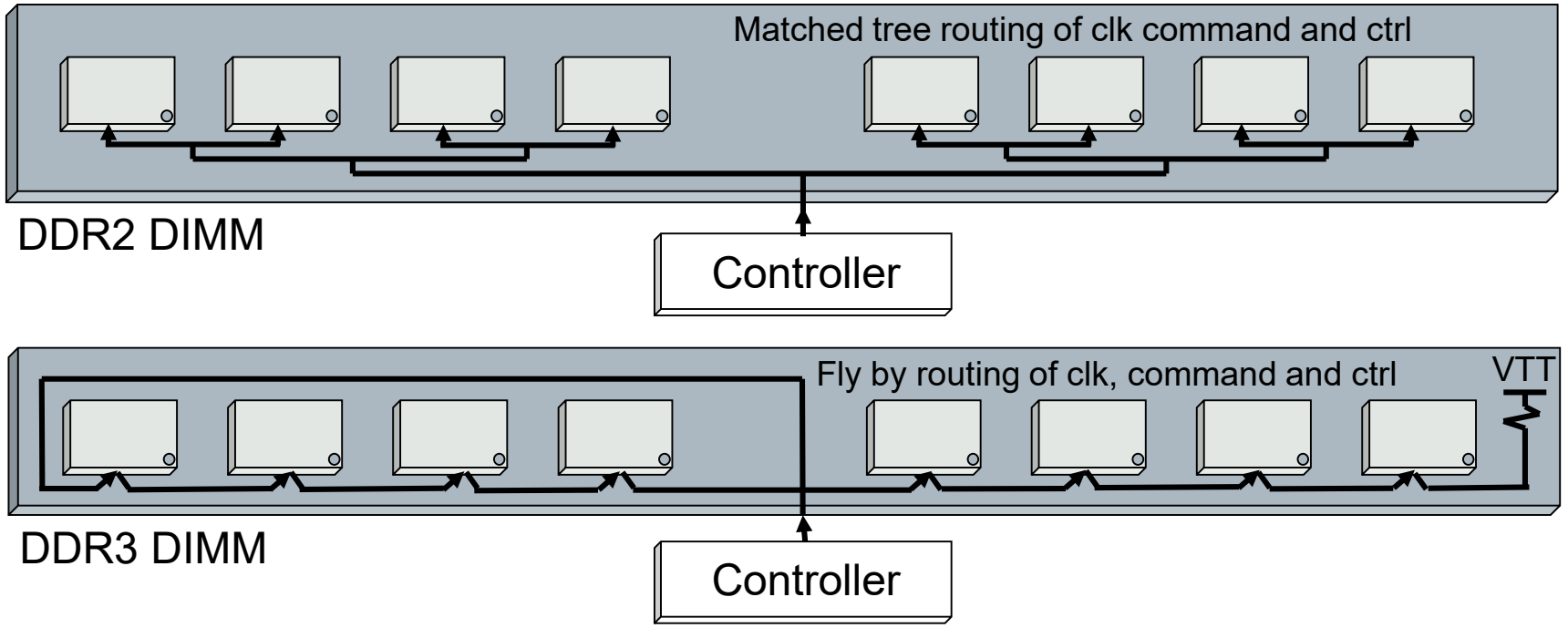
RDIMM: Registered Server standard

VLP RDIMM: Very Low Profile
Computing and Networking



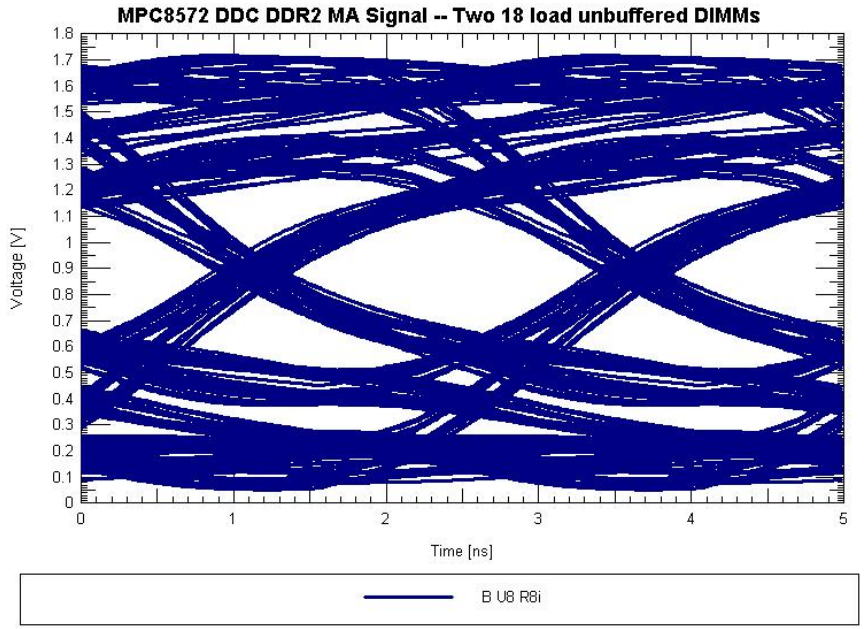
Fly-By Routing Topology

- Introduction of “fly-by” architecture
  - Address, command, control & clocks
  - Data bus (not illustrated below) remains unchanged, ie, direct 1-to-1 connection between the Controller bus lanes and the individual DDR devices.
  - Improved signal integrity…enabling higher speeds
  - On module termination

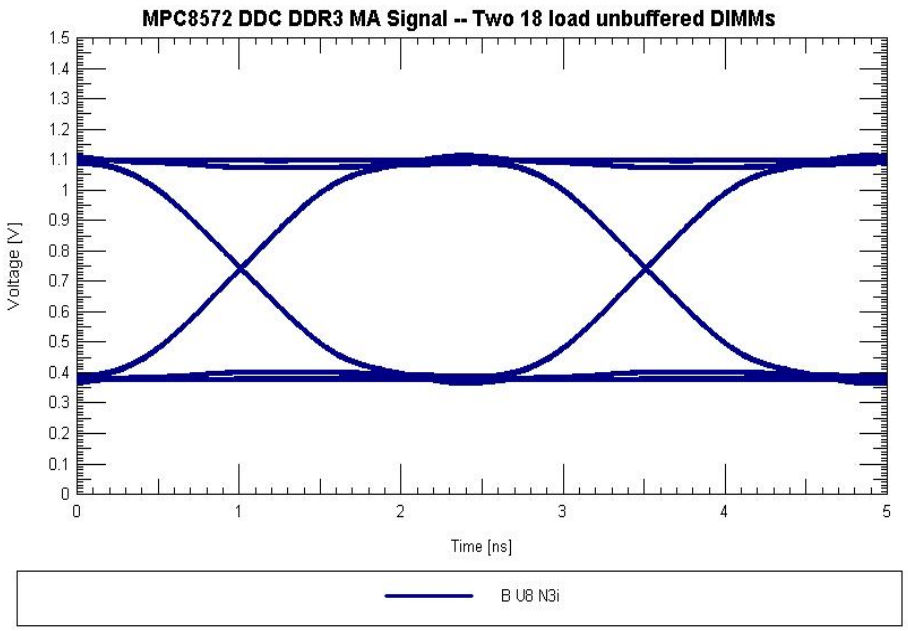


Fly-By Routing Improved SI

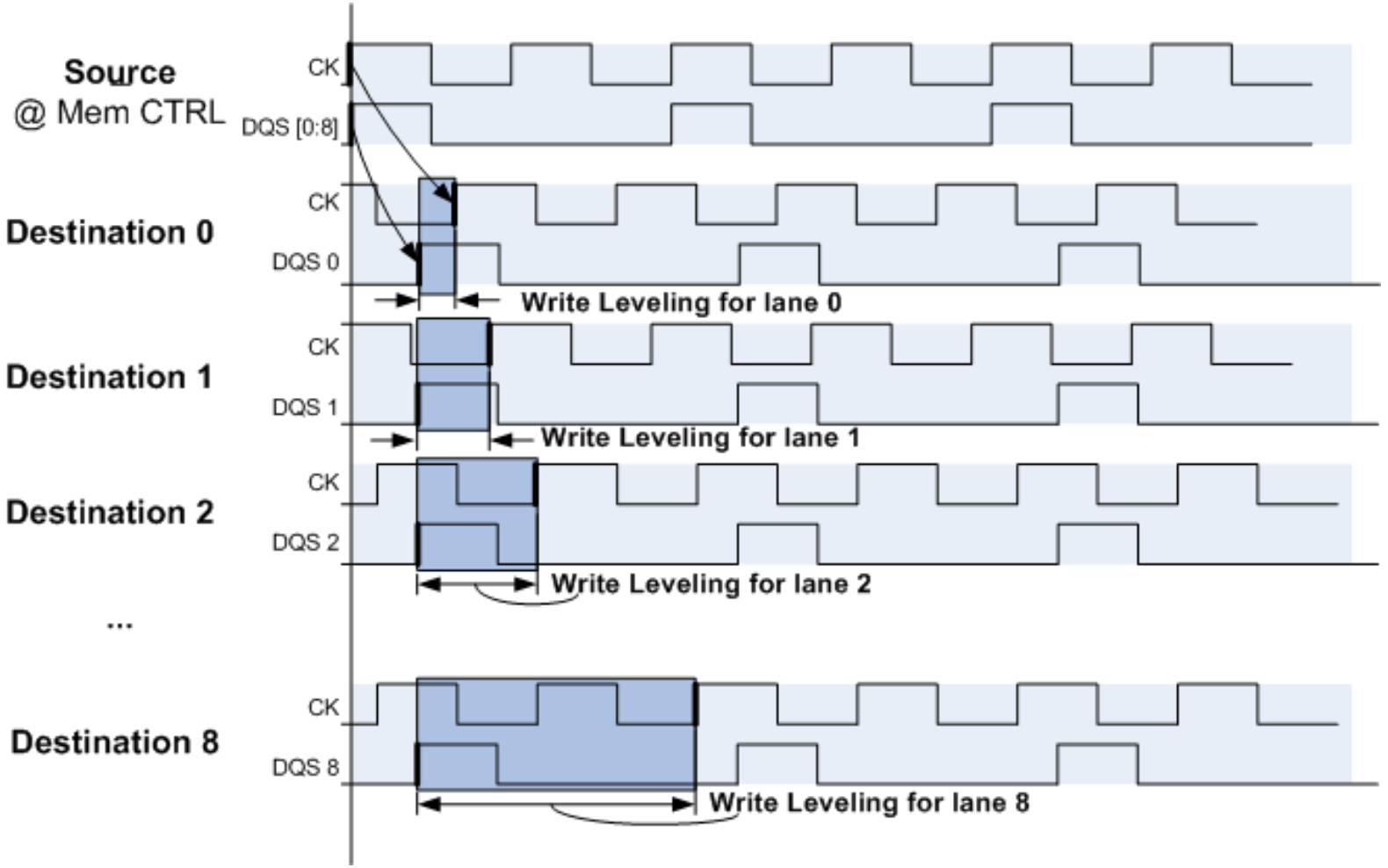
DDR2 Matched Tree Routing



DDR3 Fly By Routing

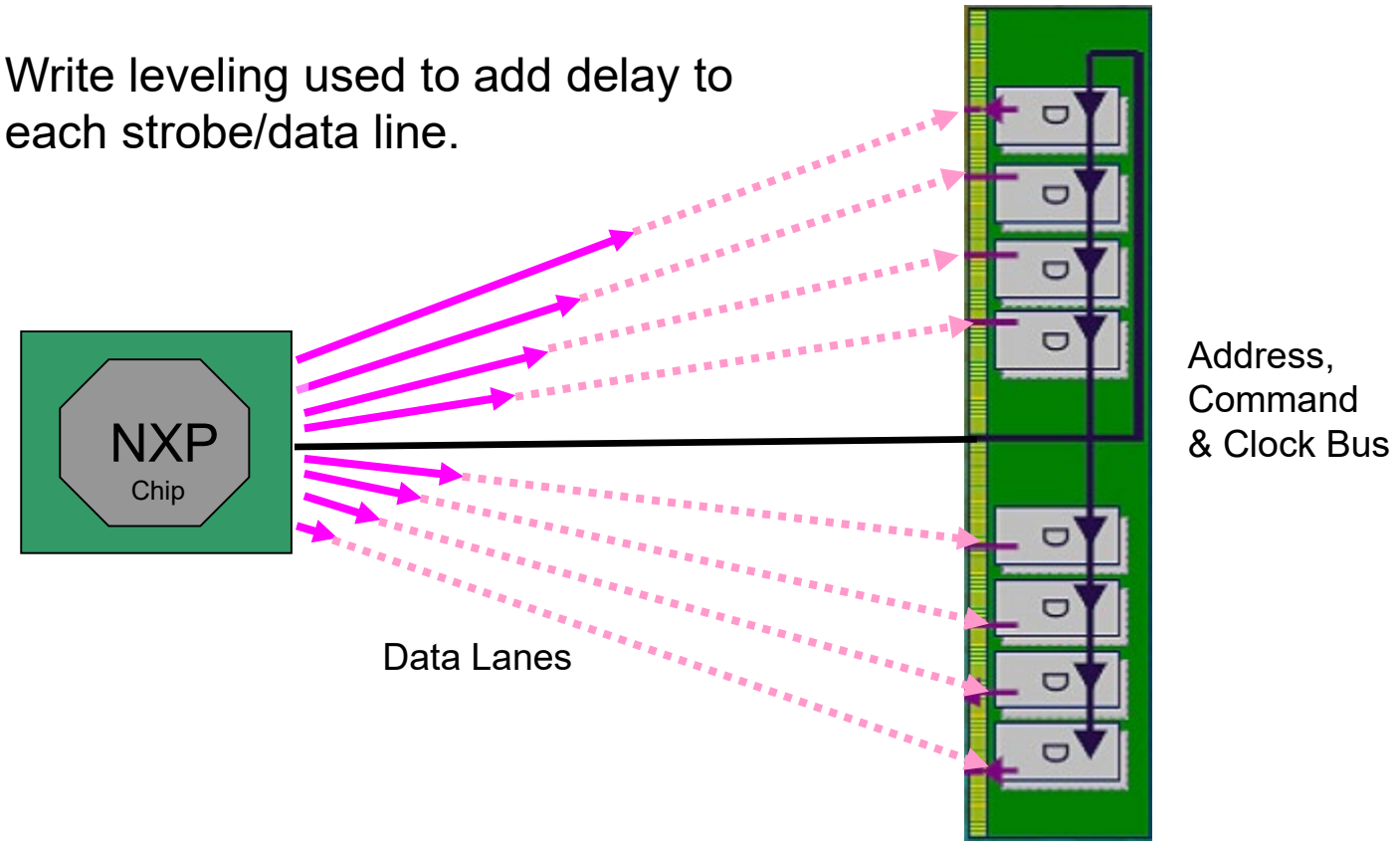


What Is Write Leveling?



Write Adjustment

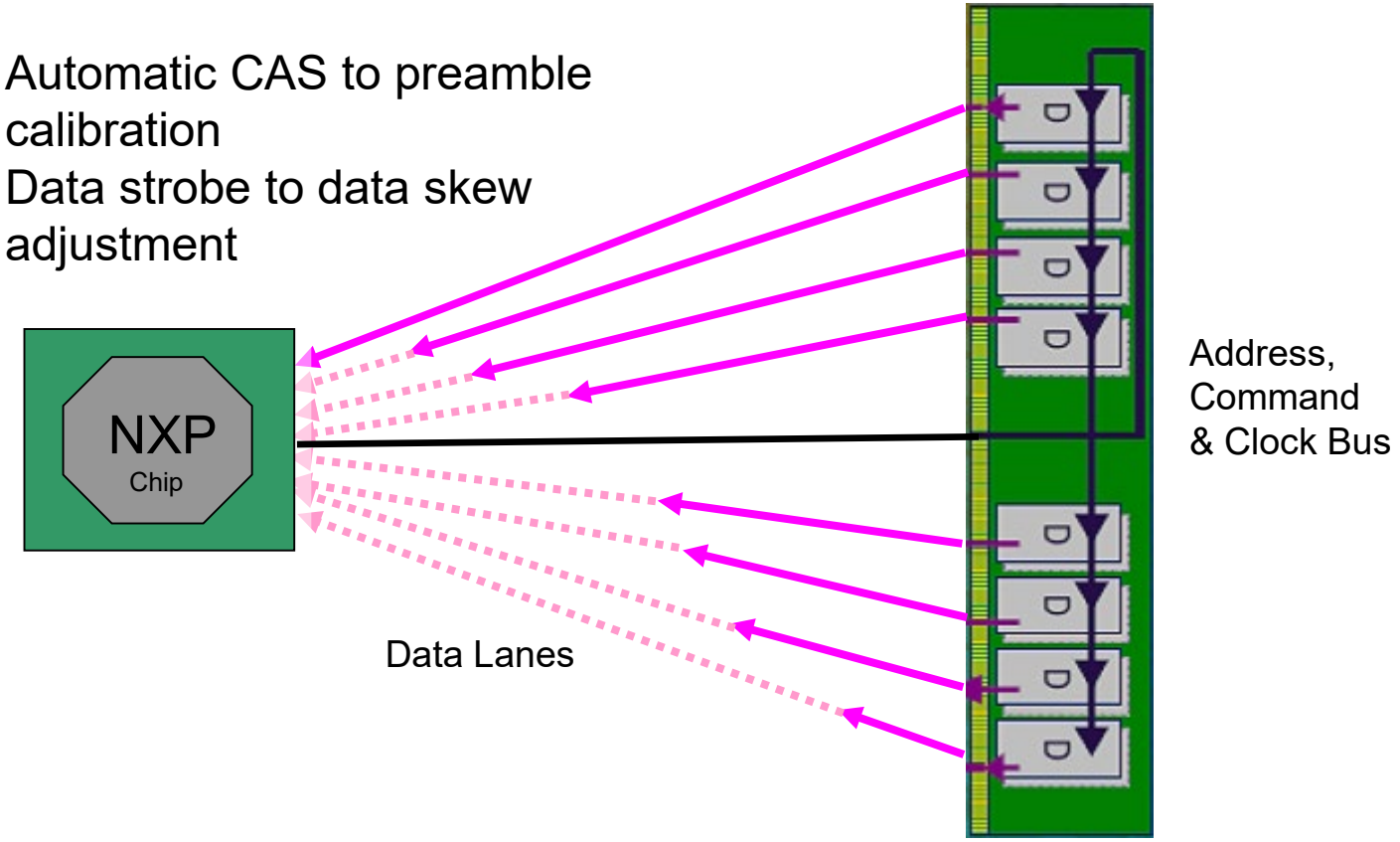
- Write leveling used to add delay to each strobe/data line.



Write leveling sequence during the initialization process will determine the appropriate delays to each data byte lane and add this delay for every write cycle.

Read Adjustment

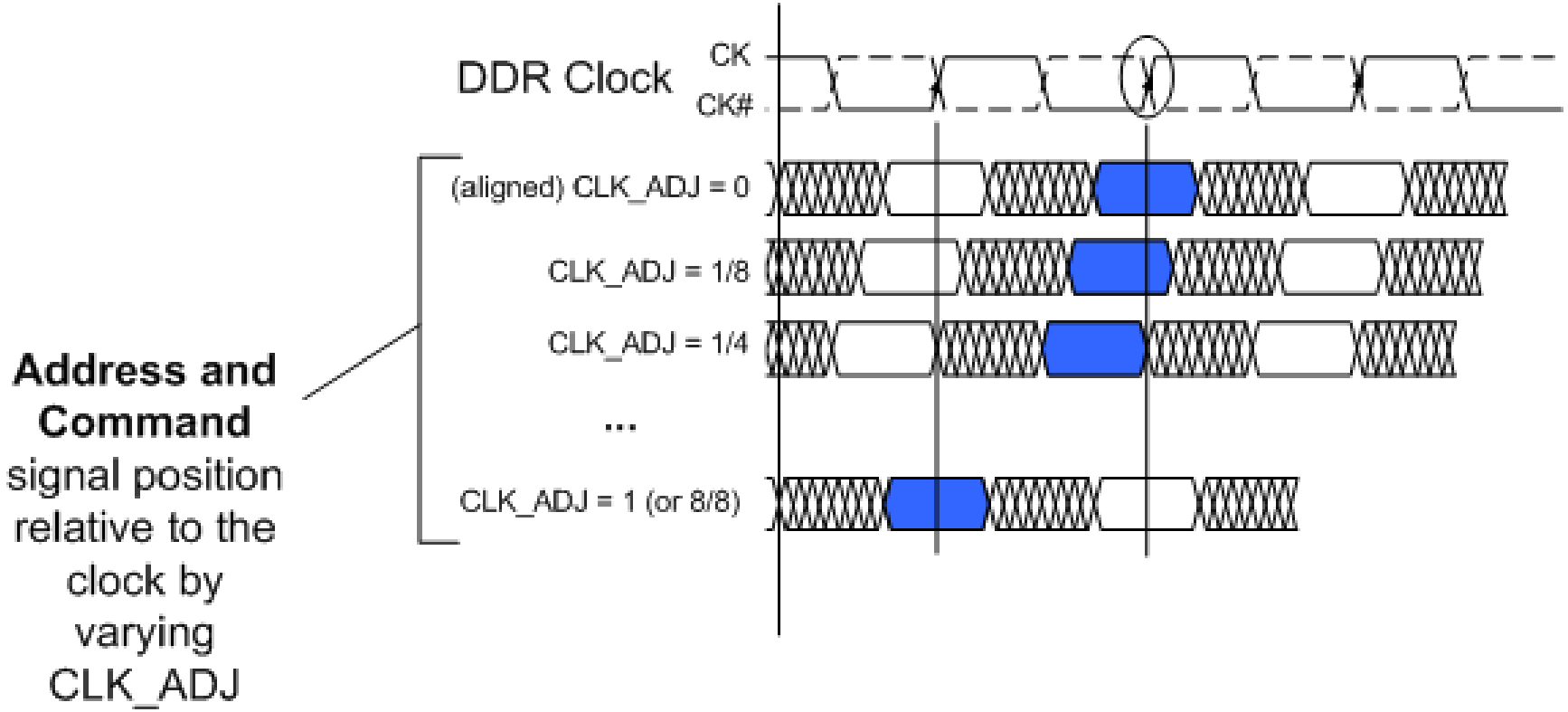
- Automatic CAS to preamble calibration
- Data strobe to data skew adjustment



Auto CPO will provide the expected arrival time of preamble for each strobe line of each byte lane during the read cycle to adjust for the delays cased by the fly-by topology.

CLK_ADJ – Clock Adjust

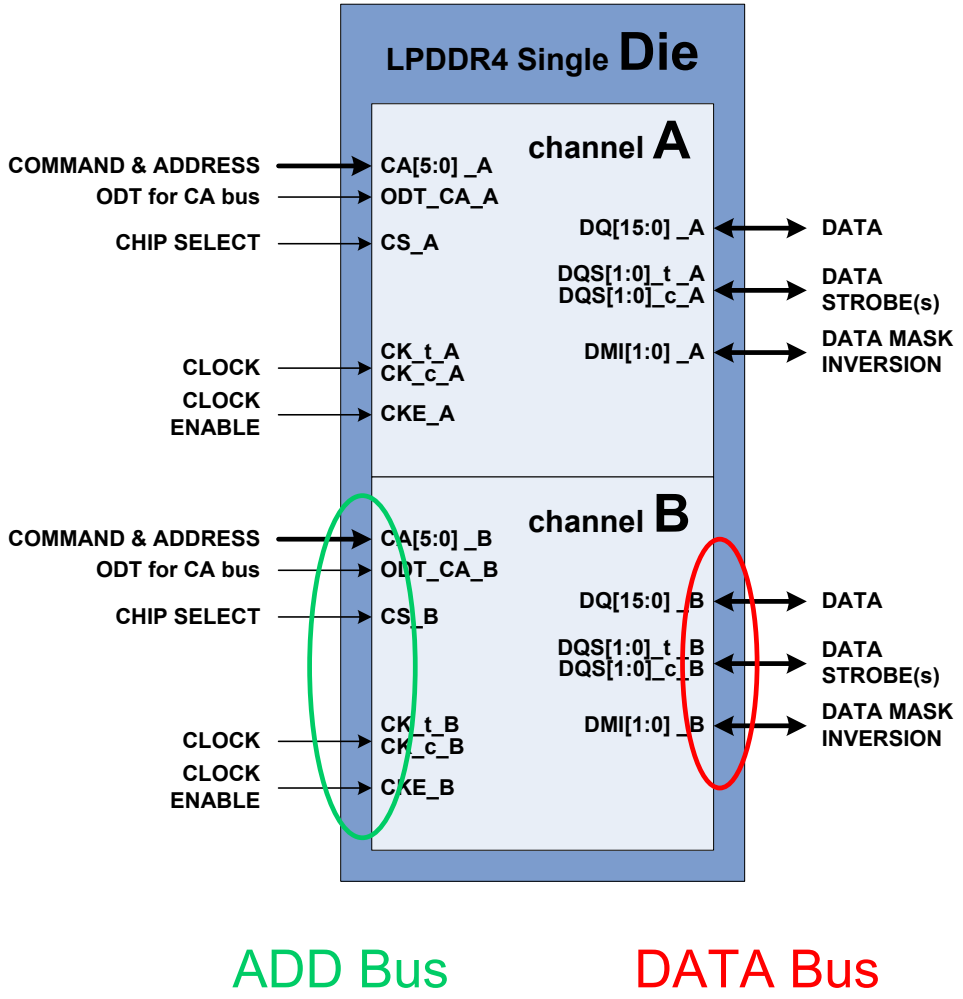
- CLK_ADJ defines the timing of the address and command signals relative to the DDR clock.



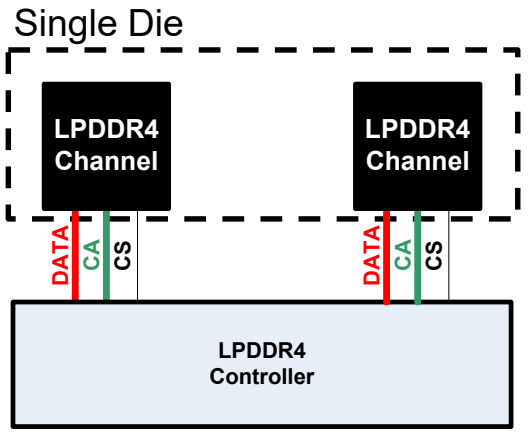
Example – Generic LPDDR4 SDRAM

- 2 Channels per die
- 1, 2 or 4 Die per package
- 8 Banks per channel
- 2Gb to 16Gb Density range per channel

- DATA bus: DQ, DQS_t, DQS_c, DMI
- ADD bus: CA, OTD_CA, CS, CKE, CK_t, CK_c

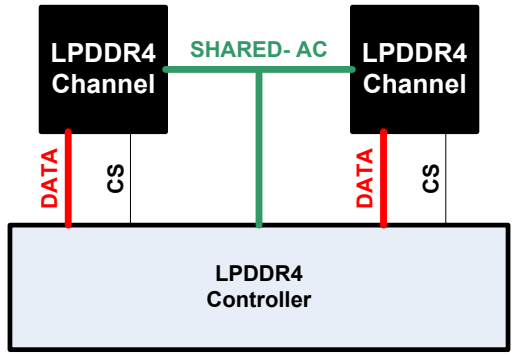


Example – LPDDR4 Arrangements – Single Die (2 Channels)



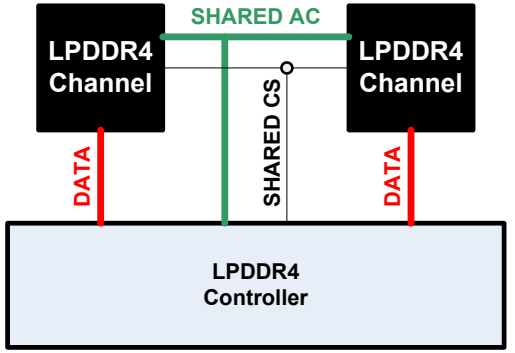
Multi-Channel

CA Pins: 12
DQ Pins: 32
CS Pins: 2
Banks: 16
Fetch (bytes): 32



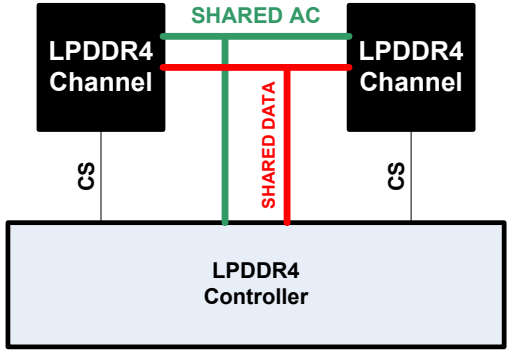
Shared-AC

CA Pins: 6
DQ Pins: 32
CS Pins: 2
Banks: 16
Fetch(bytes): 32/64



DDR/Parallel

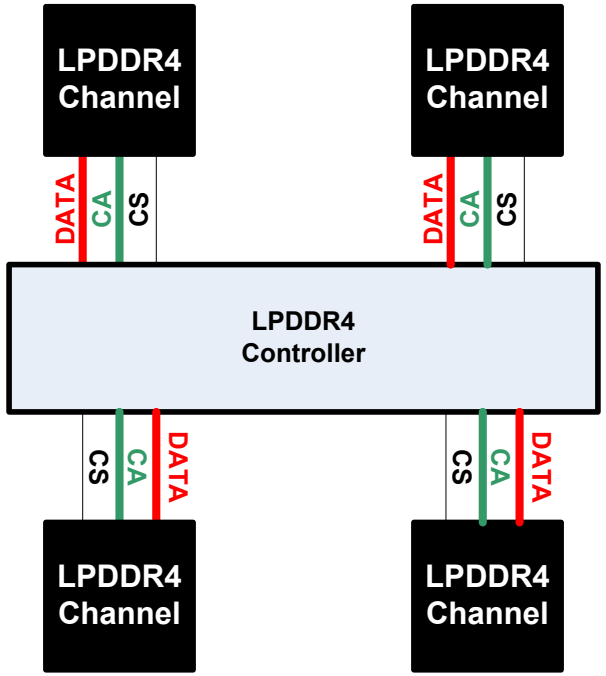
CA Pins: 6
DQ Pins: 32
CS Pins: 1
Banks: 8
Fetch(bytes): 64



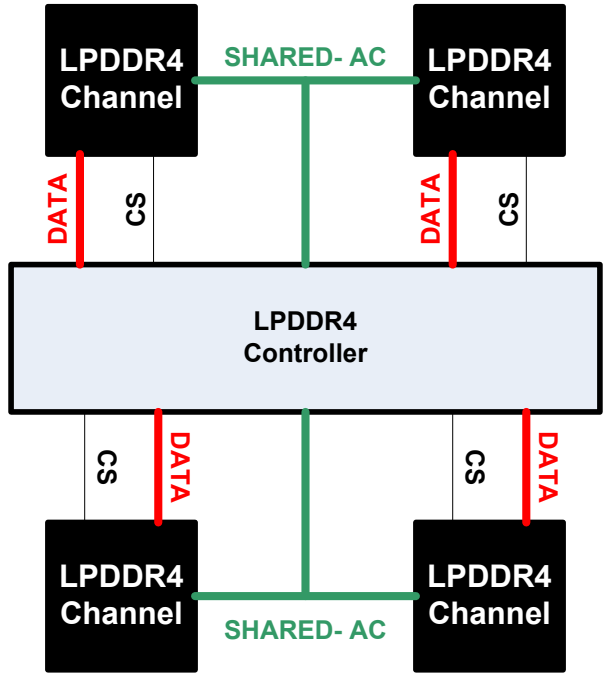
Multi-Rank/Serial

CA Pins: 6
DQ Pins: 16
CS Pins: 2
Banks: 8
Fetch(bytes): 32

Example – LPDDR4 Arrangements – 2 Die (4 Channels)

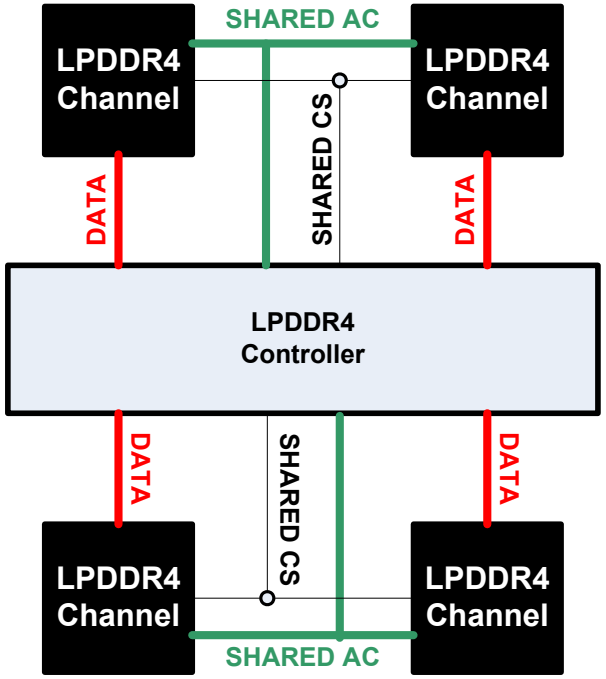


Multi-Channel

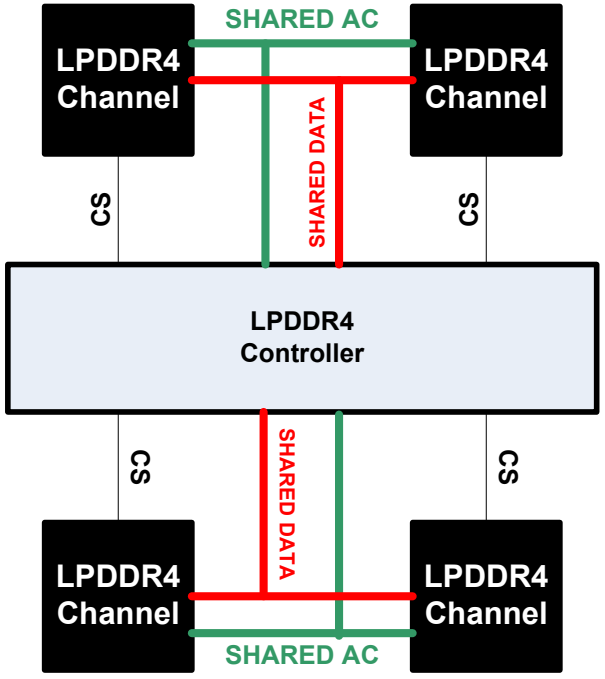


Shared-AC

Example – LPDDR4 Arrangements – 2 Die (4 Channels) Cont'd

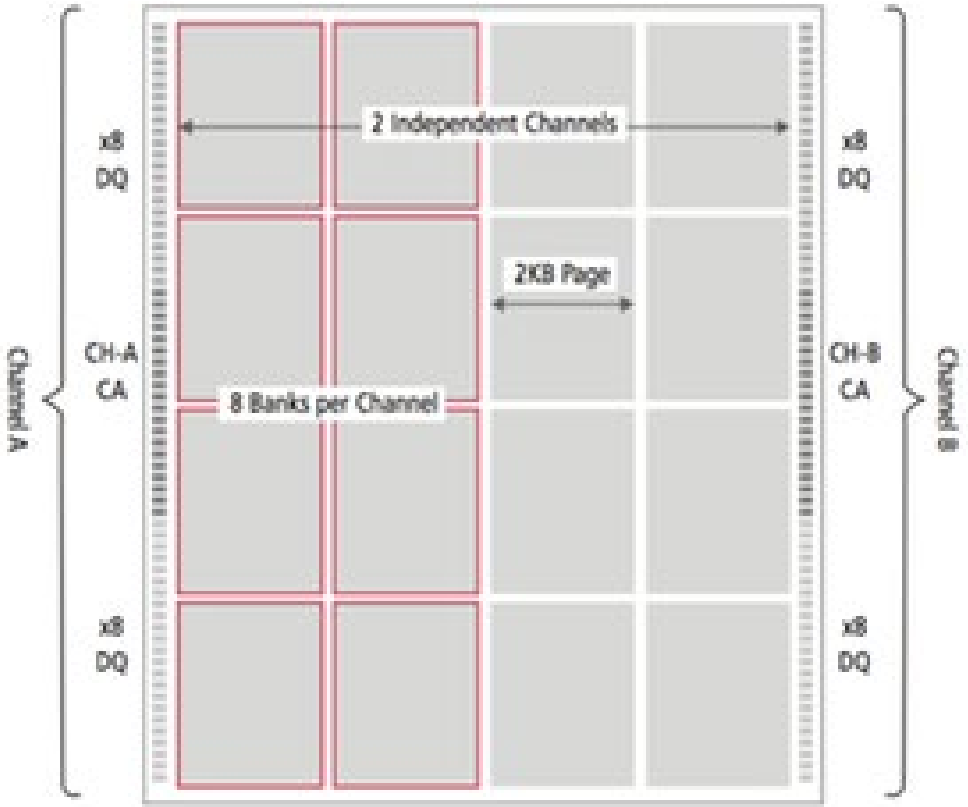


DDR/Parallel

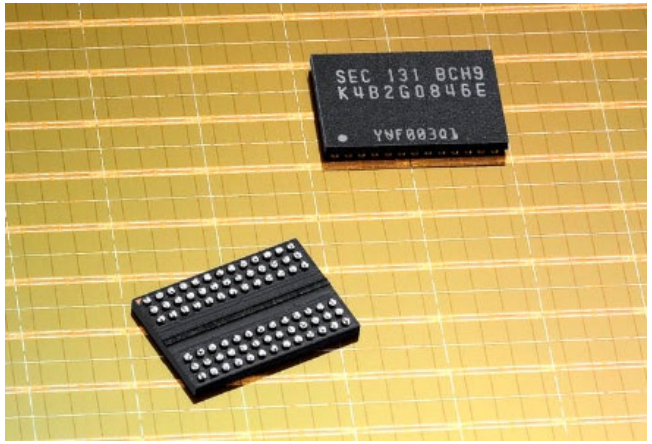


Multi-Rank/Serial

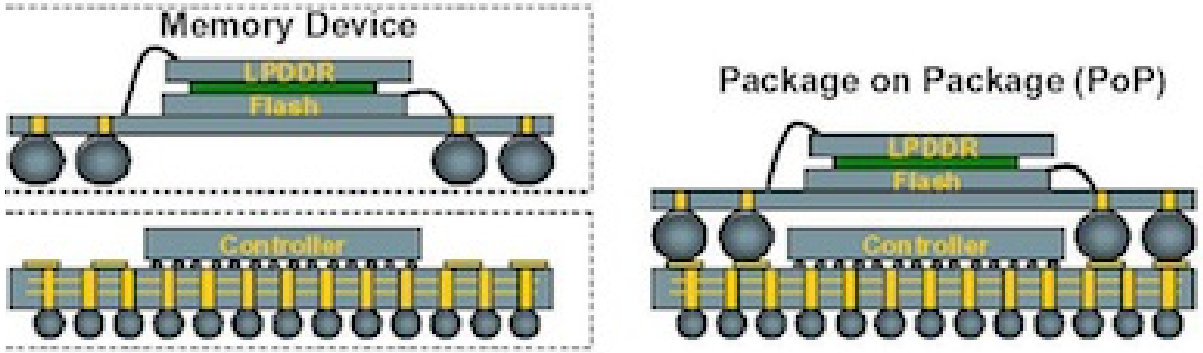
LPDDR4 Package



LPDDR4 Die Layout



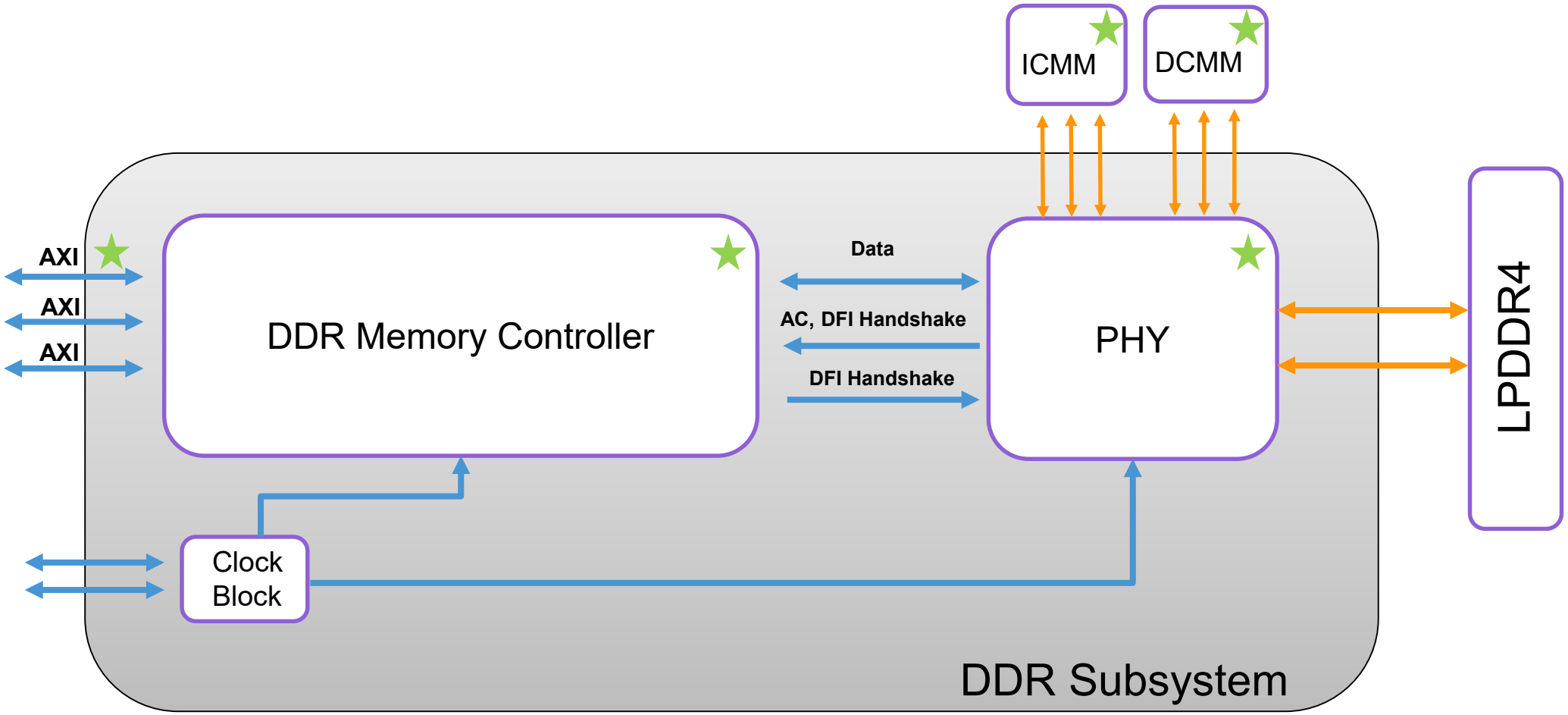
Micron LPDDR4



FLASH & LPDDR in PoP configuration

Next Generation of DDR Subsystems

Overview



★Configured by S32 DDR Tool

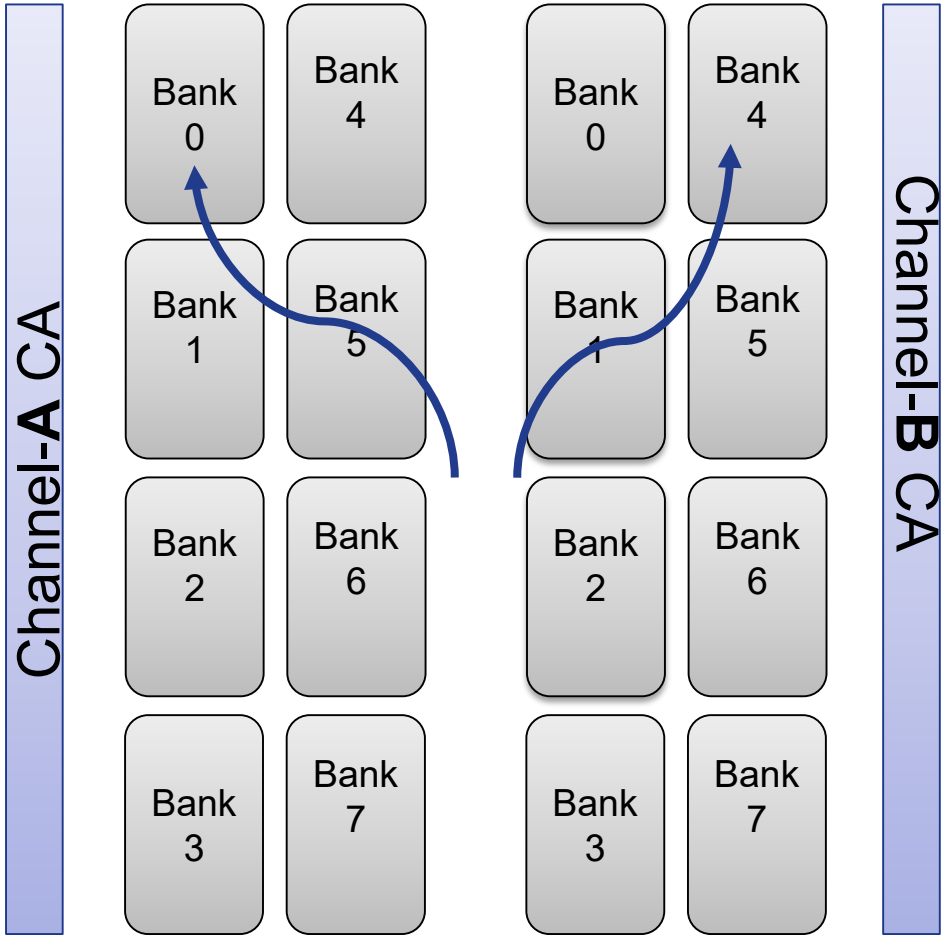
DDR Controller

- Support for LPDDR4, DDR4 and DDR3
- Address collision handling
- Quality of service (QoS)
- ECC scrubber
- Low power operation -software controlled
- Address map
- Error injection through software (ECC data poisoning)
- ZQ calibration

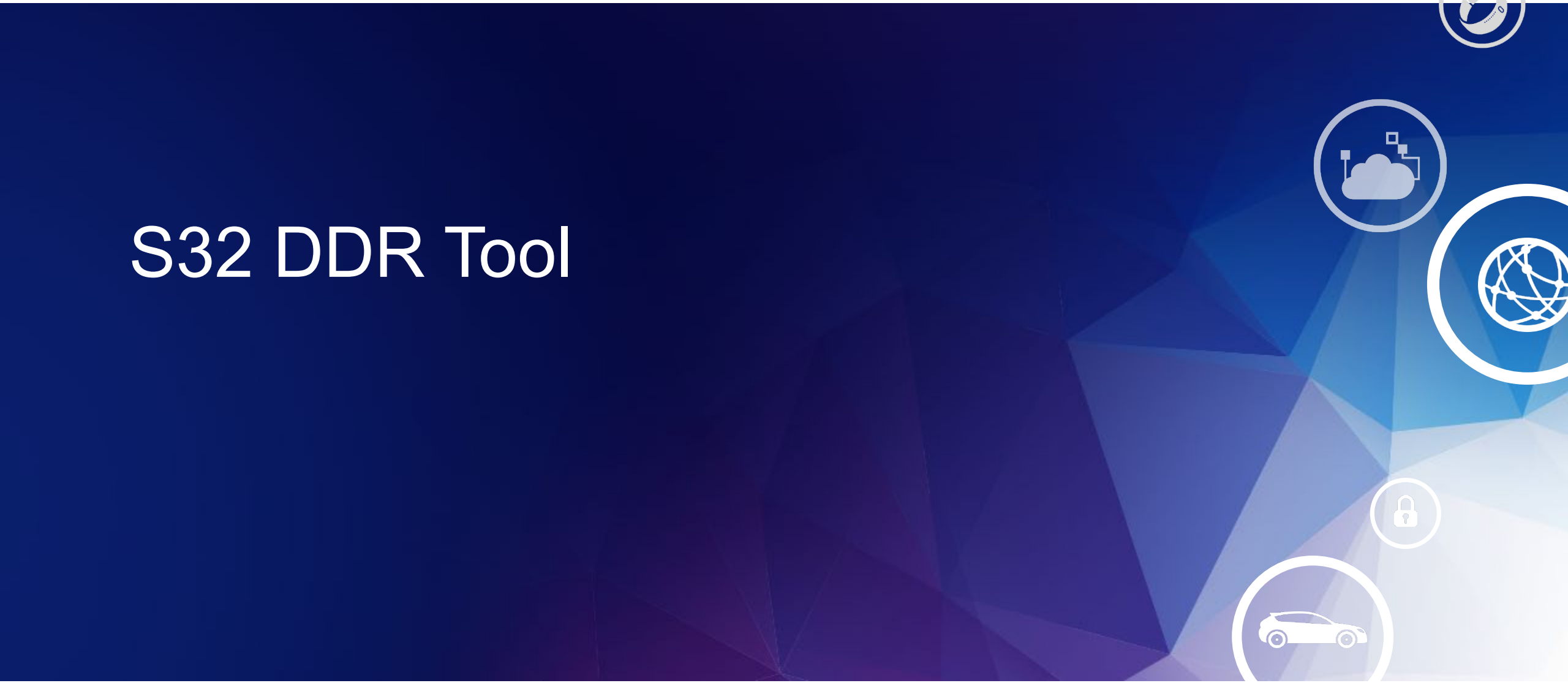
PHY

- Support 8-bit and 16-bit DDR3 and DDR4 DRAM devices.
- Support 16-bit per channel LPDDR4 DRAM devices.
- PHY independent, firmware-based training using an embedded calibration processors.

- Three inactive idle states:
  - DFI_LP Mode: most clocks and delay lines gated
  - PHY Inactive: leakage only
  - PHY Retention: Core power removed, most I/Os powered down, SDRAMs held in self-refresh

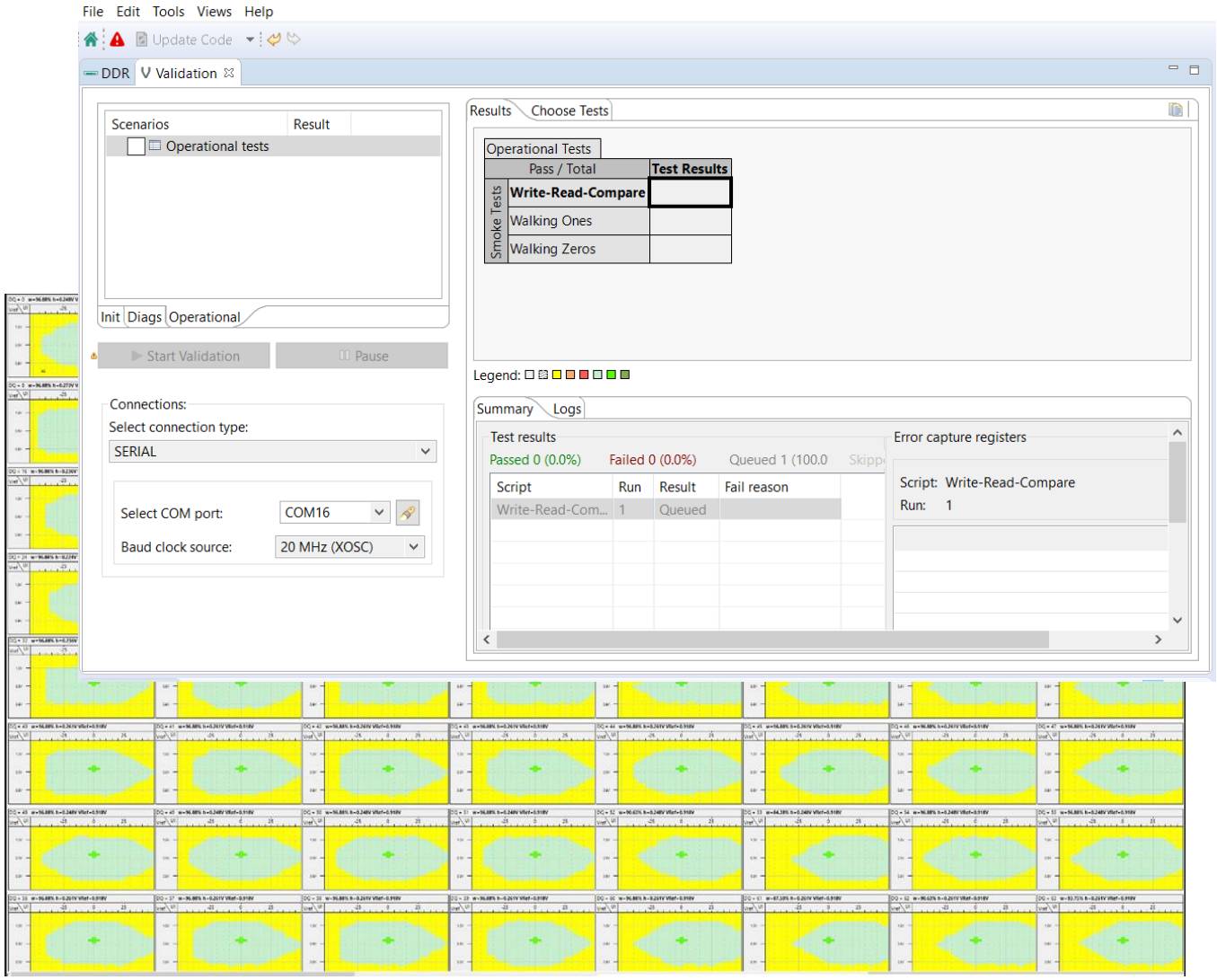


S32 DDR Tool



Overview

- S32 DDR Tool, Configuration and Validation
  - PHY Initialization
  - DDR Controller initialization
  - Various specialized tests, includes margin tests
  - Unified DDR Tool for multiple NXP parts
  - Support for LPDDR4
  - Serial download protocol
  - No debugger needed, uses UART communication



Initialization Steps

User Configuration	Configure DDRC	Write firmware parameters	Post training setup
Convert to DDRC Register values and PHY Parameters	Compute PHY Parameters	Execute the firmware	Enable AXI Ports
Upload DDR Tool target application	Configure AXI Ports	Get PHY messages	Run tests
Enable and configure DDR Clocks	Upload PHY firmware	Load PIE image	Generate Code

P2041RDB – DDRv Results

Determine the best WRLVL_START byte lanes values

Pass / Total		WRLVL_START								
		5/8 clocks	3/4 clocks	7/8 clocks	1 clocks	9/8 clocks	5/4 clocks	11/8 clocks	3/2 clocks	13/8 clocks
CLK_ADJ	**1/2 clocks**	3/3	3/3							
	5/8 clocks									
	3/4 clocks									

Determine the best clock adjust value

CLK_ADJ								
0	1/8	1/4	3/8	1/2	5/8	3/4	7/8	1
0/3	3/3	3/3	3/3	3/3	3/3	3/3	0/3	0/3

Determine WRLVL margin per byte lane

Pass / Total		**Lane 0**	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7
WRLVL_START	**1/8 clocks**	0/3	0/3	0/3	3/3	0/3	0/3	0/3	0/3
	1/4 clocks	0/3	3/3	0/3	3/3	0/3	0/3	0/3	0/3
	3/8 clocks	0/3	3/3	0/3	3/3	0/3	0/3	0/3	0/3
	1/2 clocks	3/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3
	5/8 clocks	3/3	3/3	3/3	3/3	0/3	3/3	0/3	0/3
	3/4 clocks	3/3	3/3	3/3	3/3	0/3	3/3	0/3	3/3
	7/8 clocks	3/3	3/3	3/3	3/3	0/3	3/3	3/3	3/3
	1 clocks	3/3	3/3	3/3	0/3	3/3	3/3	3/3	3/3
	9/8 clocks	3/3	3/3	3/3	0/3	3/3	3/3	3/3	3/3
	5/4 clocks	2/3	0/3	3/3	0/3	3/3	3/3	3/3	3/3
	11/8 clocks	0/3	0/3	3/3	0/3	3/3	3/3	3/3	3/3
	3/2 clocks	0/3	0/3	0/3	0/3	3/3	3/3	3/3	3/3
	13/8 clocks	0/3	0/3	0/3	0/3	3/3	0/3	3/3	3/3
	7/4 clocks	0/3	0/3	0/3	0/3	3/3	0/3	3/3	0/3
	15/8 clocks	0/3	0/3	0/3	0/3	3/3	0/3	0/3	0/3
	2 clocks	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
	17/8 clocks	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
	9/4 clocks	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
	19/8 clocks	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
	5/2 clocks	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3

T1040RDB – DDRv Results

Determine the best WRLVL_START byte lanes values

Pass / Total		WRLVL_START								
		5/8 clocks	3/4 clocks	7/8 clocks	1 clocks	9/8 clocks	5/4 clocks	11/8 clocks	3/2 clocks	13/8 clocks
CLK_ADJ	**1/2 clocks**	3/3	3/3							
	5/8 clocks									
	3/4 clocks									

Determine the best clock adjust value

CLK_ADJ																
0	1/16	1/8	3/16	1/4	5/16	3/8	7/16	1/2	9/16	5/8	11/16	3/4	13/16	7/8	15/16	1
0/3	3/3	3/3	3/3	3/3	3/3	3/3	3/3	3/3	3/3	3/3	3/3	3/3	3/3	3/3	0/3	0/3

Determine WRLVL margin per byte lane

Pass / Total		Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7	Lane 8 (ECC)
WRLVL_START	**1/8 clocks**	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
	1/4 clocks	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
	3/8 clocks	3/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
	1/2 clocks	3/3	3/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
	5/8 clocks	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3	0/3
	3/4 clocks	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3	0/3
	7/8 clocks	3/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3
	1 clocks	3/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	3/3
	9/8 clocks	3/3	3/3	3/3	3/3	3/3	0/3	0/3	0/3	3/3
	5/4 clocks	3/3	3/3	3/3	3/3	3/3	3/3	0/3	0/3	3/3
	11/8 clocks	0/3	3/3	3/3	3/3	3/3	3/3	3/3	0/3	3/3
	3/2 clocks	0/3	0/3	3/3	3/3	3/3	3/3	3/3	0/3	3/3
	13/8 clocks	0/3	0/3	0/3	3/3	3/3	3/3	3/3	3/3	3/3
	7/4 clocks	0/3	0/3	0/3	3/3	3/3	3/3	3/3	3/3	3/3
	15/8 clocks	0/3	0/3	0/3	0/3	3/3	3/3	3/3	3/3	3/3
	2 clocks	0/3	0/3	0/3	0/3	3/3	3/3	3/3	3/3	0/3
	17/8 clocks	0/3	0/3	0/3	0/3	3/3	3/3	3/3	3/3	0/3
	9/4 clocks	0/3	0/3	0/3	0/3	0/3	0/3	3/3	3/3	0/3
	19/8 clocks	0/3	0/3	0/3	0/3	0/3	0/3	0/3	3/3	0/3
	5/2 clocks	0/3	0/3	0/3	0/3	0/3	0/3	0/3	3/3	0/3

P5040 Customer Board – DDRv Results

Determine the best WRLVL_START byte lanes values

Pass / Total		WRLVL_START								
		5/8 clocks	3/4 clocks	7/8 clocks	1 clocks	9/8 clocks	5/4 clocks	11/8 clocks	3/2 clocks	13/8 clocks
CLK_ADJ	**1/2 clocks**	3/3	3/3							
	5/8 clocks									
	3/4 clocks									

Determine the best clock adjust value

CLK_ADJ								
0	1/8	1/4	3/8	1/2	5/8	3/4	7/8	1
0/3	3/3	3/3	3/3	3/3	3/3	3/3	3/3	0/3

Determine WRLVL margin per byte lane

Pass / Total		**Lane 0**	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7	Lane 8 (ECC)
WRLVL_START	**1/8 clocks**	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
	1/4 clocks	3/3	3/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
	3/8 clocks	3/3	3/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
	1/2 clocks	3/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3
	5/8 clocks	3/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3
	3/4 clocks	3/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	3/3
	7/8 clocks	3/3	3/3	3/3	3/3	3/3	3/3	3/3	0/3	3/3
	1 clocks	3/3	3/3	3/3	3/3	3/3	3/3	3/3	3/3	3/3
	9/8 clocks	3/3	3/3	3/3	3/3	3/3	3/3	3/3	3/3	3/3
	5/4 clocks	0/3	0/3	3/3	3/3	3/3	3/3	3/3	3/3	3/3
	11/8 clocks	0/3	0/3	3/3	3/3	3/3	3/3	3/3	3/3	3/3
	3/2 clocks	0/3	0/3	0/3	0/3	3/3	3/3	3/3	3/3	3/3
	13/8 clocks	0/3	0/3	0/3	0/3	3/3	3/3	3/3	3/3	3/3
	7/4 clocks	0/3	0/3	0/3	0/3	3/3	3/3	3/3	3/3	0/3
	15/8 clocks	0/3	0/3	0/3	0/3	0/3	0/3	0/3	3/3	0/3
	2 clocks	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
	17/8 clocks	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
	9/4 clocks	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
	19/8 clocks	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
	5/2 clocks	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3

SECURE CONNECTIONS
FOR A SMARTER WORLD