

# S32 Configuration Tools Supporting the Next-Generation of S32 Products

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October 2019 | Session #AMF-AUT-T3842



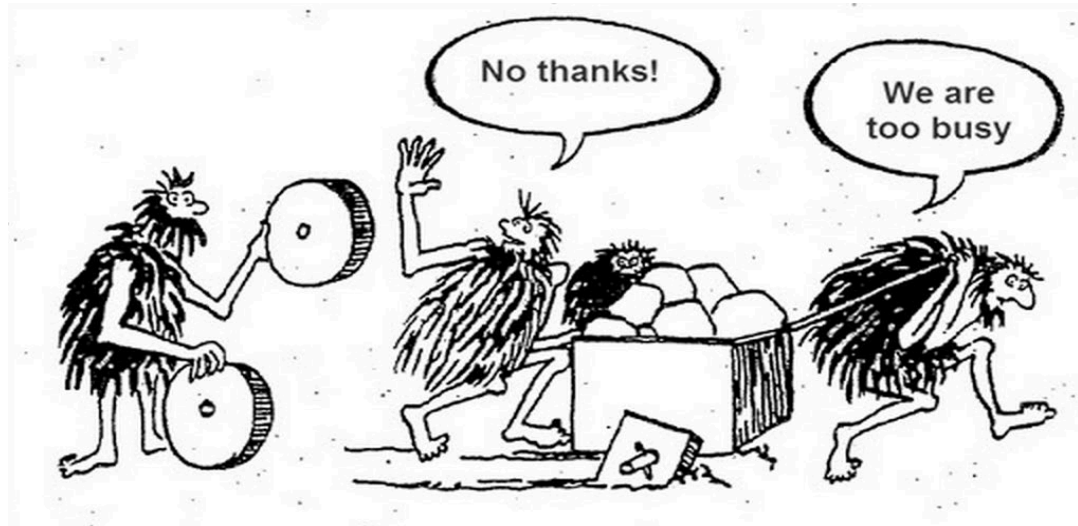
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# Agenda

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- Short Description of **S32 Configuration Tools Suite**
- **Pins Tool** – Correct and Fast Pins Routing
- **Clocks Tool** – Friendly Visual Clock Tree Configuration
- **Peripherals Tool** – Simple SDK Configuration
- **Device Configuration Data Tool** – Quick Peripheral Configuration
- **Image Vector Tool** – Intuitive Image Vector Table Definition

WITH



WITHOUT

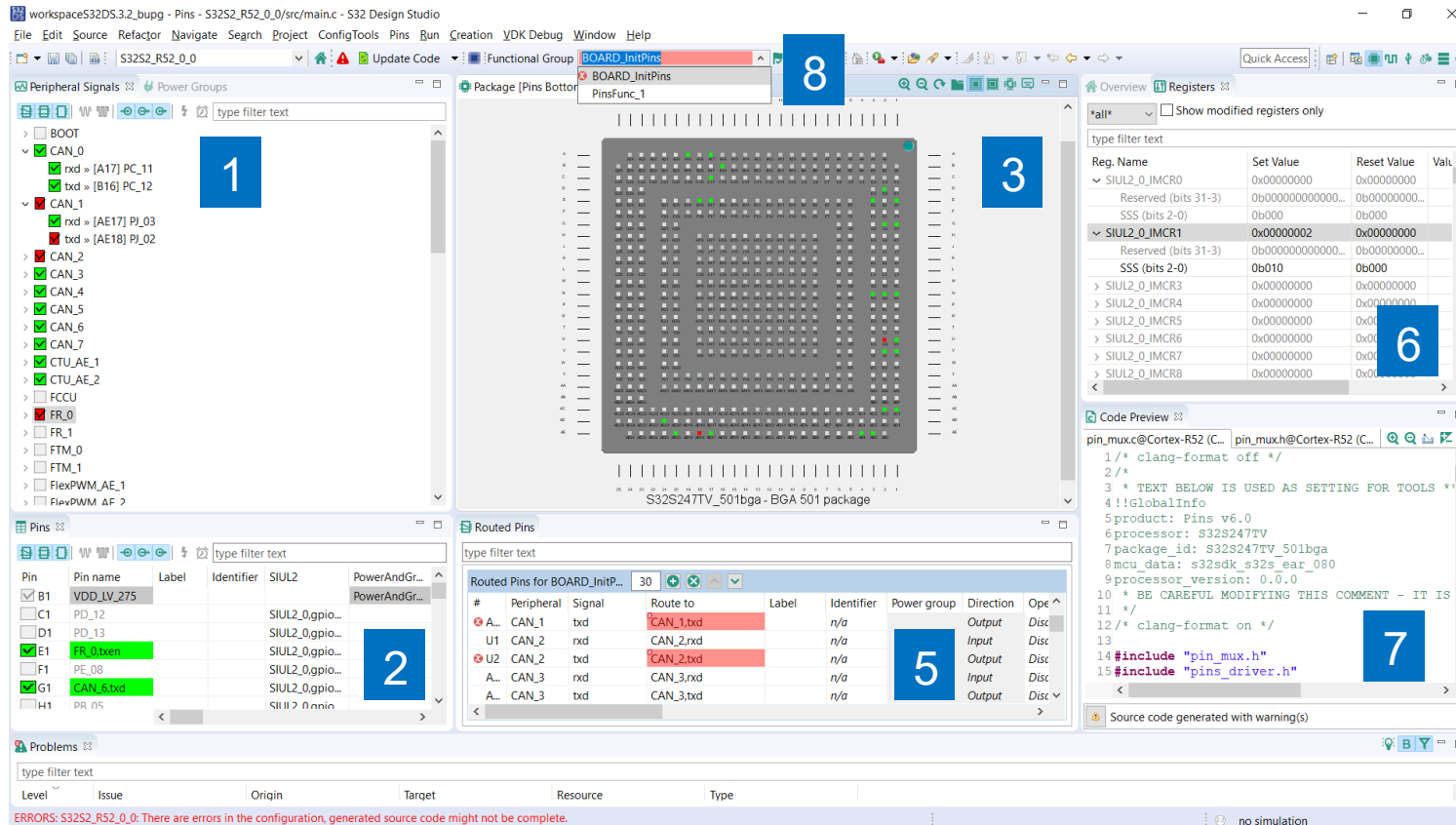
## S32 Configuration Tool

Quick **GUI based Configuration** and **Code Generation** for AMP parts/platforms.

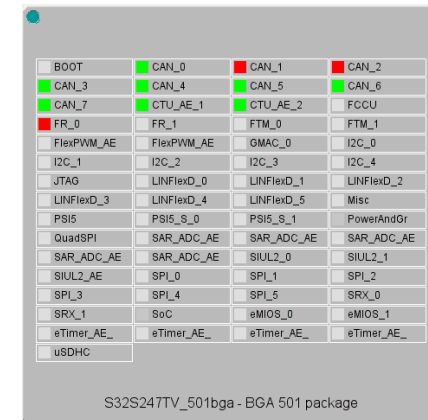
- ✓ Read and digest documentation to understand part capabilities: RM, DS, Schematics, SDK API
- ✓ Figure out correct types & values for all parameters used
- ✓ Manual integration of SDK drivers in S32DS projects

# Pins Tool Features Summary

Caption showing Pins Tool for S32xxx – BGA501 package



- Quick configuration of pins from:
  1. Peripherals View
  2. Pins View
  3. Package View
  4. Resource View



- Setting allowed properties for each pin (5)
- Validation of pins selection (5)
- Support & help for managing conflicts (5)
- Registers modified information (6)
- Configuration C - Code Generation (7)
- Multiple Configuration Support (8)
- Predefined board configurations
- Power Groups Highlight

# Setting Pin Electrical Characteristics

workspaceS32DS.3.2\_bupg - Pins - S32S2\_R52\_0\_0/src/main.c - S32 Design Studio

File Edit Source Refactor Navigate Search Project ConfigTools Pins Run Creation VDK Debug Window Help

S32S2\_R52\_0\_0 Update Code Functional Group BOARD\_InitPins

Routed Pins

type filter text

Routed Pins for BOARD\_InitP... 30

#	Peripheral	Signal	Route to	Label	Identifier	Power group	Direction	Open Drain	Slew Rate Control	Slew Rate Enable	Pull Select	Pull Enable	Receiver Select	Safe Mode Control	Hysteresis
A...	CAN_0	rx	CAN_0,rx		n/a		Input	Disabled	Frequency 150~166Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	n/a
B...	CAN_0	tx	CAN_0,tx		n/a		Output	Disabled	Frequency 150~166Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	n/a
A...	CAN_1	rx	CAN_1,rx		n/a		Input	Disabled	Frequency 166~208Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	Disabled
A...	CAN_1	tx	CAN_1,tx		n/a		Output	Disabled	Frequency 166~208Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	Disabled
U1	CAN_2	rx	CAN_2,rx		n/a		Input	Disabled	Frequency 166~208Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	Disabled
U2	CAN_2	tx	CAN_2,tx		n/a		Output	Disabled	Frequency 166~208Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	Disabled
A...	CAN_3	rx	CAN_3,rx		n/a		Input	Disabled	Frequency 166~208Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	Disabled
A...	CAN_3	tx	CAN_3,tx		n/a		Output	Disabled	Frequency 166~208Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	Disabled
D2	CAN_4	tx	CAN_4,tx		n/a		Output	Disabled	Frequency 150~166Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	n/a
E3	CAN_4	rx	CAN_4,rx		n/a		Input	Disabled	Frequency 150~166Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	n/a
V2	CAN_5	tx	CAN_5,tx		n/a		Output	Disabled	Frequency 166~208Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	Disabled
V1	CAN_5	rx	CAN_5,rx		n/a		Input	Disabled	Frequency 166~208Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	Disabled
G1	CAN_6	tx	CAN_6,tx		n/a		Output	Disabled	Frequency 150~166Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	n/a
G2	CAN_6	rx	CAN_6,rx		n/a		Input	Disabled	Frequency 150~166Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	n/a
A...	CAN_7	tx			n/a		Output	Disabled	Frequency 150~166Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	n/a
A...	CAN_7	rx			n/a		Input	Disabled	Frequency 150~166Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	n/a
C...	CTU_AE_1	trigger_in, 0	[D2] PE_04		n/a		Input	Disabled	Frequency 150~166Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	n/a
C...	CTU_AE_1	trigger_out, 0	[AE18] PJ_02		n/a		Output	Disabled	Frequency 150~166Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	Disabled
E...	CTU_AE_2	trigger_out, 0	[U2] PJ_04		n/a		Output	Disabled	Frequency 150~166Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	Disabled
E...	CTU_AE_2	trigger_in, 0	[AC1] PL_07		n/a		Input	Disabled	Frequency 150~166Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	Disabled
E...	CTU_AE_2	trigger_in, 0	[AD7] PM_09		n/a		Input	Disabled	Frequency 150~166Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	Disabled
A...	FR_0	debug, 0	[AD9] PB_00		n/a		Output	Disabled	Frequency 166~208Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	Disabled
A...	FR_0	debug, 1	[AD2] PC_09		n/a		Output	Disabled	Frequency 166~208Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	Disabled
U2	FR_0	debug, 2	[B16] PC_12		n/a		Output	Disabled	Frequency 166~208Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	Disabled
U1	FR_0	debug, 3	[AE20] PD_05		n/a		Output	Disabled	Frequency 166~208Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	Disabled
N1	FR_0	rx, A	[G1] PE_10		n/a		Input	Disabled	Frequency 166~208Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	Disabled
A...	FR_0	rx, B	[G3] PE_12		n/a		Input	Disabled	Frequency 166~208Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	Disabled
N2	FR_0	tx, A	[N2] PL_04		n/a		Output	Disabled	Frequency 166~208Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	Disabled
A...	FR_0	tx, B	FR_0,tx		n/a		Output	Disabled	Frequency 166~208Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	Disabled
N3	FR_0	txen, A	FR_0,txen		n/a		Output	Disabled	Frequency 166~208Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	Disabled
E1	FR_0	txen, B	FR_0,txen		n/a		Output	Disabled	Frequency 150~166Mhz	n/a	Pulldown	Disabled	Differential vref based receiver	Disabled	n/a

General Purpose I/O 180:FlexRay Transmit;FlexRay Transmit;GMAC Pulse Per Second;RGMII Carrier Sense;RGMII Receive Error

Half drive strength with slew rate control

Half drive strength with slew rate control

Half drive strength with slew rate control

Pin is already routed to 'FR\_0' peripheral; to signal(s) 'FR\_0,tx,A'.

ERRORS: S32S2\_R52\_0\_0: There are errors in the configuration, generated source code might not be complete.

no simulation

- Note default availability of information regarding the Power Group domain for a pin.
- All fields are configurable and settings will be reflected into the generated configuration code.

# S32 Configuration Tools – Clock Tool Features Summary

The screenshot displays the S32 Configuration Tools interface with the following components and callouts:

- 1:** Clock Diagram View showing the clock tree structure with various PLLs, dividers, and outputs.
- 2:** Clocks Table showing the configuration of clock sources and outputs.
- 3:** Clock Outputs table listing outputs like ADC2\_0\_CLK, ADC2\_1\_CLK, and CLKOUT0\_CLK.
- 4:** Clock Sources table listing sources like ftm\_0\_ext\_ref and FXOSC source.
- 5:** Register configuration table for various PLLs and DFS registers.
- 6:** Code Preview showing the generated C code for clock configuration.
- 7:** Problems panel showing any configuration issues.
- 8:** Multiple Configurations Support, indicated by the '8' icon in the top toolbar.

- Quick configuration of clock from:
  1. Clock Diagram View (1)
  2. Clock Summary Table
    - Sources (2)
    - Outputs (3)
- Setting values for clock tree elements
  - PLLs
  - DFS
  - Dividers
  - Selectors
- Validation of selected choices (7)
- Support & help for managing conflicts (4)
- Registers modified information (5)
- Configuration C - Code Generation (6)
- Multiple Configurations Support (8)
  - Various power modes for example

# S32 Configuration Tools – Clock Tool Help & Support

**FTM0 external reference clock** [type:clock source, id: MC\_CGM\_0.ftm0\_ext\_ref, component: MC\_CGM\_0]

**TYPE:** Variable - The frequency can be adjusted in the range: (min=1 Hz, max=20 MHz)

**STATUS:** Element is disabled

**CONSTRANTS:** Output frequency must be in range: 1 Hz - 20 MHz

**VALUE:** Inactive

```

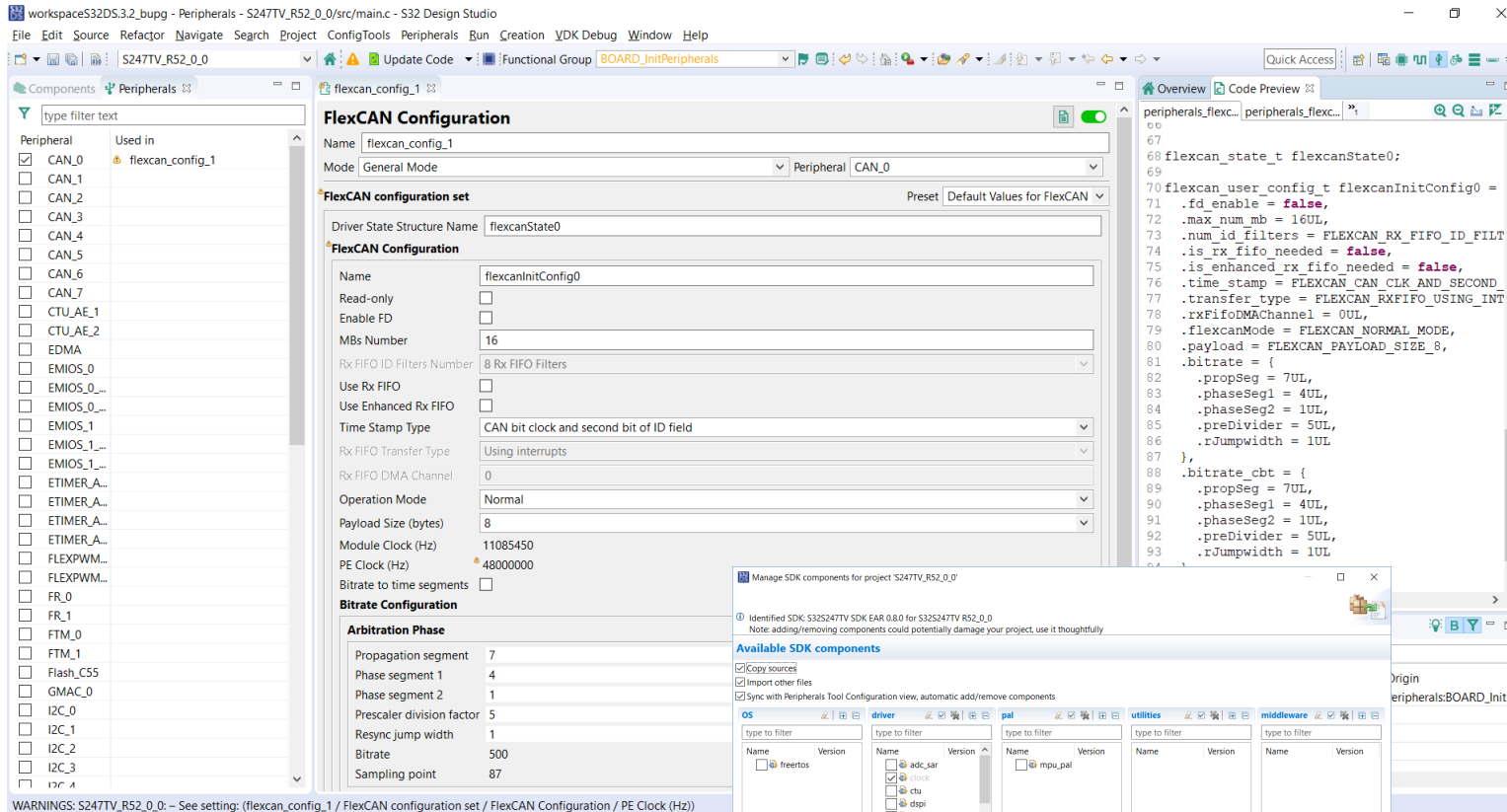
/* Important information:
 *
 * This script contains clock configuration
 * Support for SDK calls will be implemented
 */

/* TEXT BELOW IS USED AS SETTING FOR TOOLS ****
!!GlobalInfo
product: Clocks v4.0
processor: S32S247xxxx
package_id: S32S247
mcu_data: amp_sdk1_0
processor_version: 0.0.0
* BE CAREFUL MODIFYING THIS COMMENT - IT IS YA

#include "clock_config.h"
  
```

- Based on Silicon Datasheet and/or Silicon User Manual a suite of constrains are defined in the tool.
- Constrains are taken into account both to offer user's suggestion regarding ranges of values allowed for a certain configuration and for making the background checks once a selection is done.

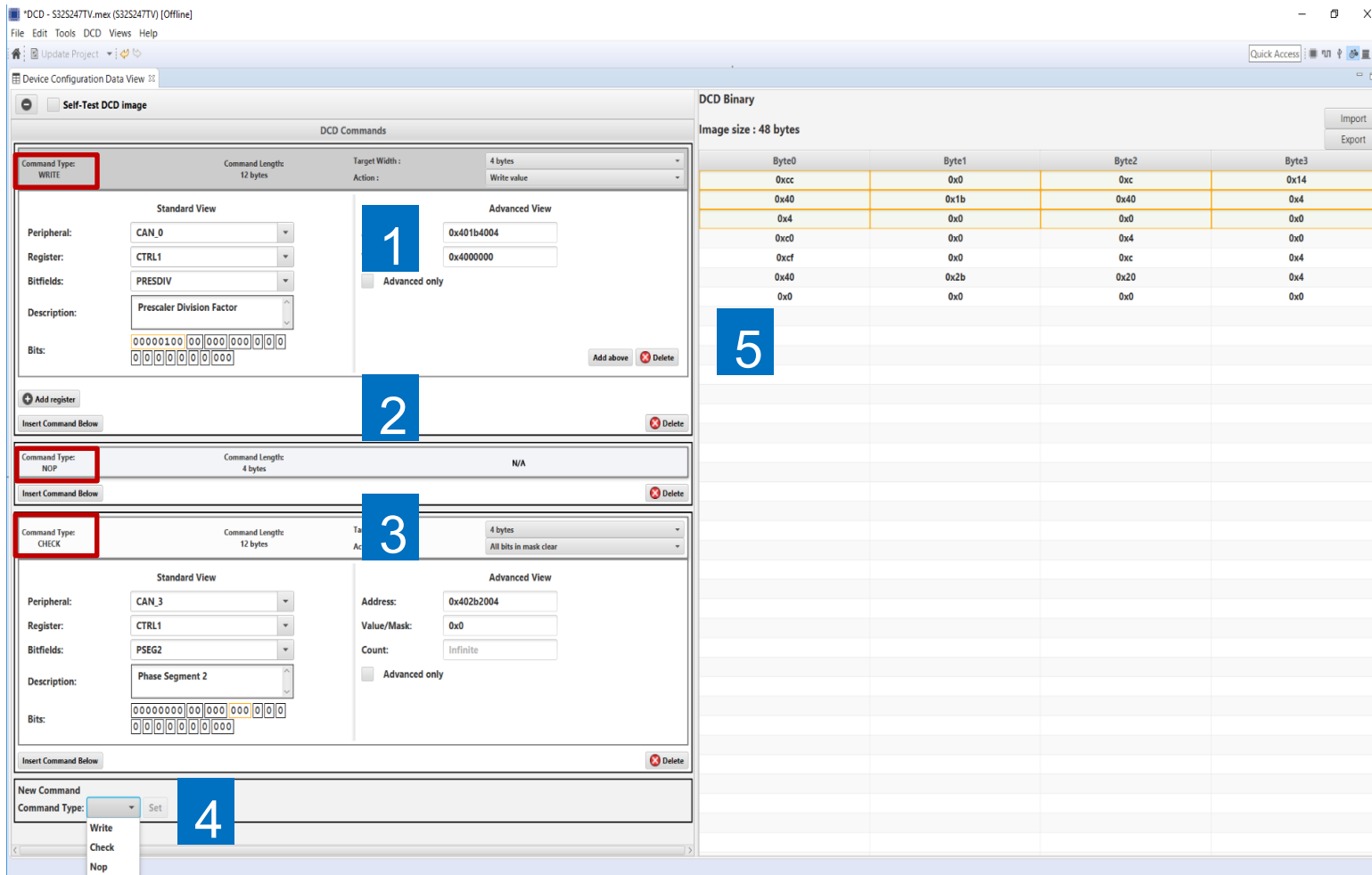
# S32 Configuration Tools – Peripheral Tool Features Summary



- Quick settings for all drivers
- Input and dependency verification engine
- Integration with S32 IDE Projects
- SDK Driver management
- Support for multiple configurations and driver versions.
- Integrated documentation for each driver
- C code generation
- Automatic mechanism to add/remove drivers



# S32 Configuration Tools – DCD Tool Features Summary



- DCD Tool used mainly to define SoC IP configurations prior to HSE Firmware boot-up or Application Boot Code execution.
- DCD Tool Supports following commands:
  - 1.WRITE – writes a memory area
  - 3.CHECK – checks a memory area
  - 2.NOP – introduces a wait
- DCD Tool generates a binary (5) which incorporates all the settings done.
- Main scenario flow:
  - Import an existing DCD binary image
  - Update it with graphical view
  - Save it and export it in binary or C format.

# S32 Configuration Tools – IVT Tool Features Summary

The screenshot displays the IVTView tool interface with several key features highlighted by blue boxes with numbers 1 through 5:

- 1:** Memory Layout view showing segments like IVT Image, DCD, DCD (backup), HSE, HSE (backup), and Application bootloaders.
- 2:** Automatic Align section in the Boot Configuration panel.
- 3:** Problems list at the bottom showing error messages about segment overlaps.
- 4:** Image Table section listing DCD, DCD (backup), HSE, HSE (backup), and Application bootloaders with their start addresses and sizes.
- 5:** Export Blob Image button in the Boot Configuration panel.

- Memory layout overview and segment overlapping detection. (1)
- Automatic memory segments alignment. Using a starting alignment address the tool will generate start address for all images. (2)
- Export in binary and C format.
- Validation of selected choices. (3)
- Table with the list of images. Size of the image can be automatically determine if the user provides full path of the file. (4)
- Generate Boot Blob image – complete image with all IVT nodes. (5)



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