A Novel Approach to Power Distribution: Building a Solid Foundation

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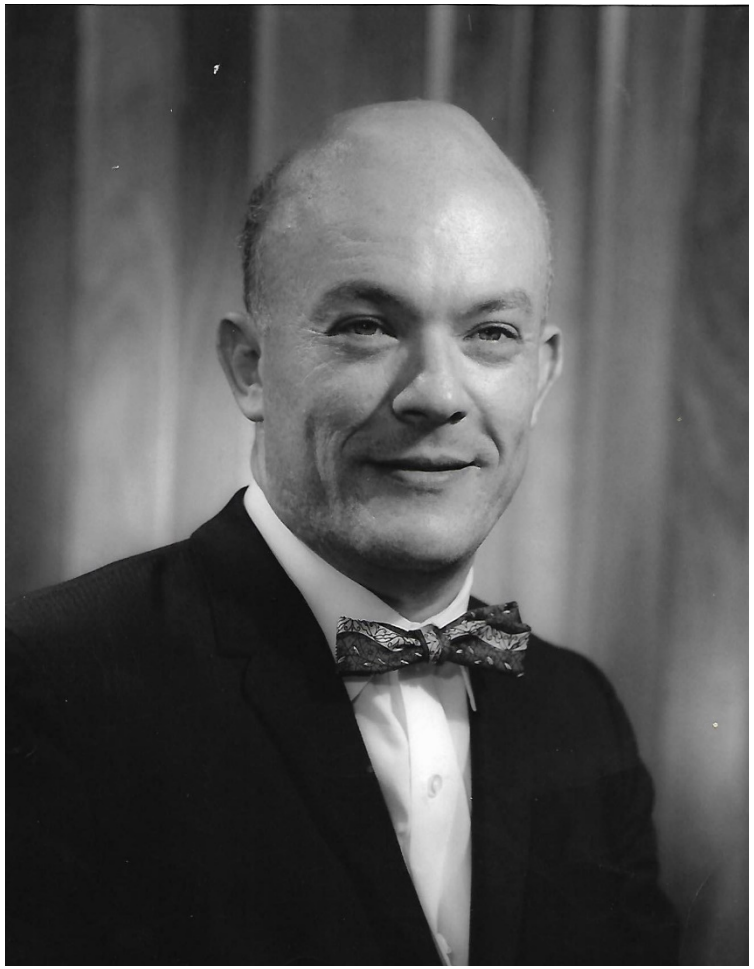
NXP | SECURE CONNECTIONS FOR A SMARTER WORLD

In memory of

Ralph Morrison

January 4, 1925-August 2, 2019

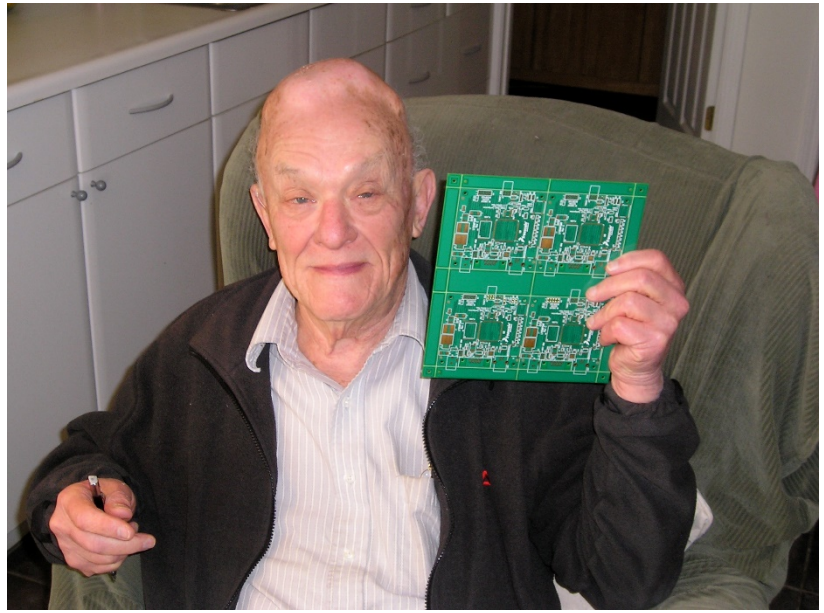


Ralph Morrison

January 4, 1925 - August 2, 2019

Books Published:

Grounding and Shielding in Instrumentation Wiley 1967 – (6th edition 2016)
DC Amplifiers in instrumentation - Wiley 1970
Instrumentation Fundamentals and Applications – Wiley 1984
Grounding and Shielding in Facilities - Wiley 1990
Noise and Other Interfering Signals - Wiley 1991
Solving Interference Problems in Electronics - Wiley 1995
The Fields of Electronics - Wiley 2002
Electricity - A Self Study Guide Wiley - August 2003
Electronics - A Self Study Guide Wiley - September 2003
Practical Electronics: A Self-Teaching Guide – Wiley 2008
The Fields of Electronics: Understanding Electronics Using Basic Physics – Wiley 2008
Digital Circuit Boards: Mach 1 GHz – Wiley 2012
Fast Circuit Boards: Energy Management – Wiley 2017



BS Physics 1949 California Institute of Technology
Pasadena, California

MS EE 1964 University of Southern California
Los Angeles, California

Born in Los Angeles of immigrant parents in 1925, Ralph Morrison grew up in the great depression of the 30s. Ralph was uncertain whether to follow a career in music or science. He was keenly interested in electricity and radio as a teenager. Drafted at age 18, Ralph served in the infantry in WW2 in Patton's 3rd Army. He then used the GI Bill to get a BS in Physics from Caltech. After beginning his professional career at Applied Physics Corporation in Pasadena, Ralph received an MS in EE from USC at night school. Ralph designed instrumentation amplifiers for aerospace and formed a new company called Dynamics Instrumentation and functioned as VP of engineering. Ralph wrote numerous articles on shielding that were excellent sales tools. This lead to writing his first book published by John Wiley in 1967. This book titled Grounding and Shielding has been rewritten every ten years and is now in its 6th Edition, selling over 2 million copies worldwide. He also wrote 12 other books on related topics.

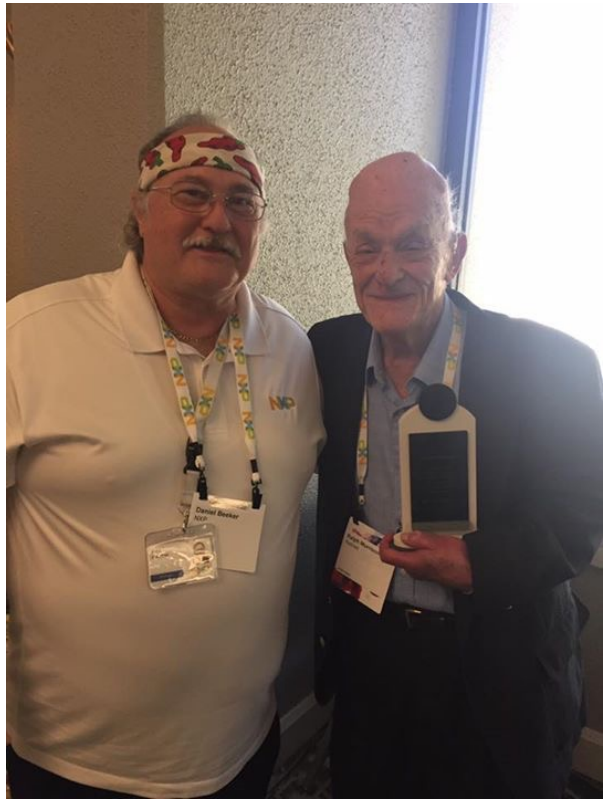
Ralph Morrison

January 4, 1925 - August 2, 2019

Music was a huge part of his life

Ralph Morrison

January 4, 1925 - August 2, 2019



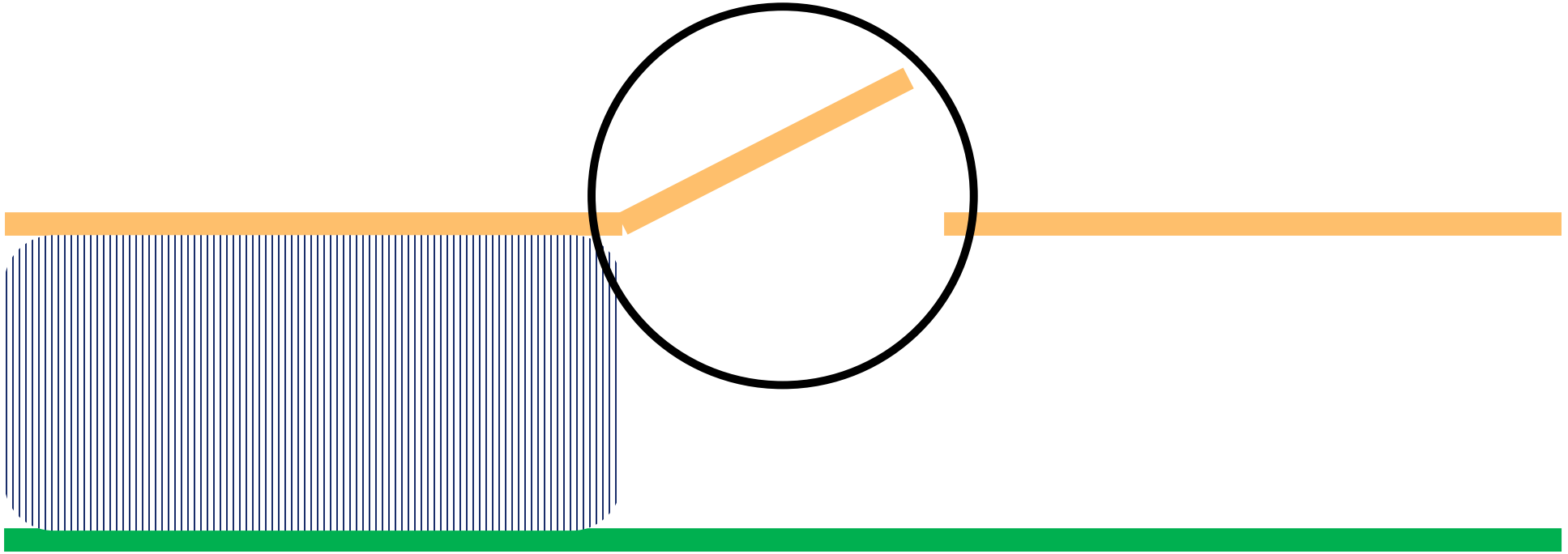
Lifetime Achievement Award from NXP

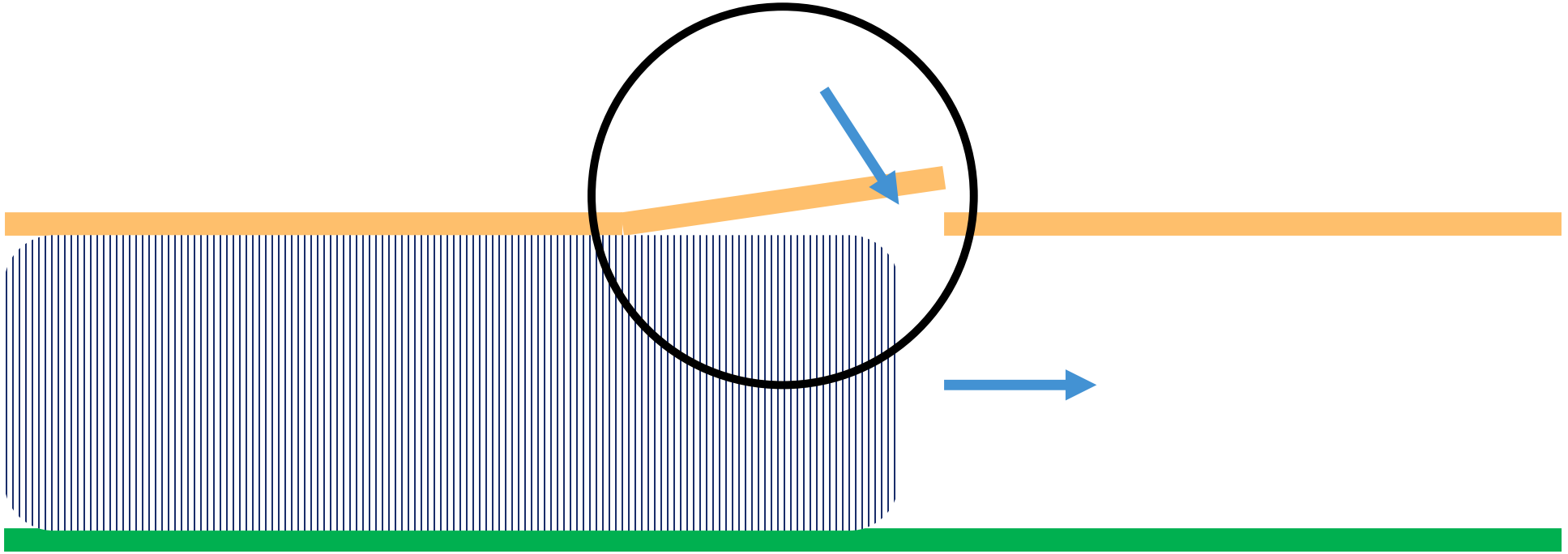
Disclaimer

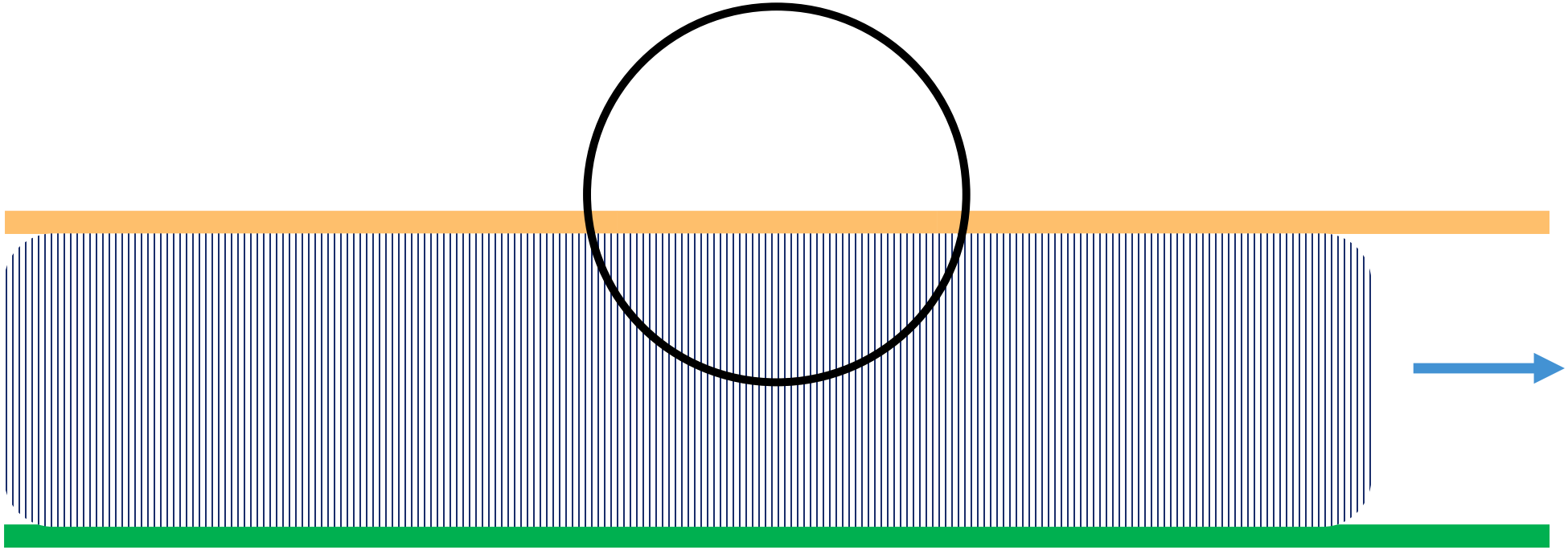
- If you have taken this class before, there are not many changes.
- I teach other classes that contain similar material.
- If you are like me, you need to hear this more than one time for it to begin to make sense.
- I WILL continually mention the need for understanding how fields behave in order to be able to use them effectively.
- I play the song over and over to brainwash you.

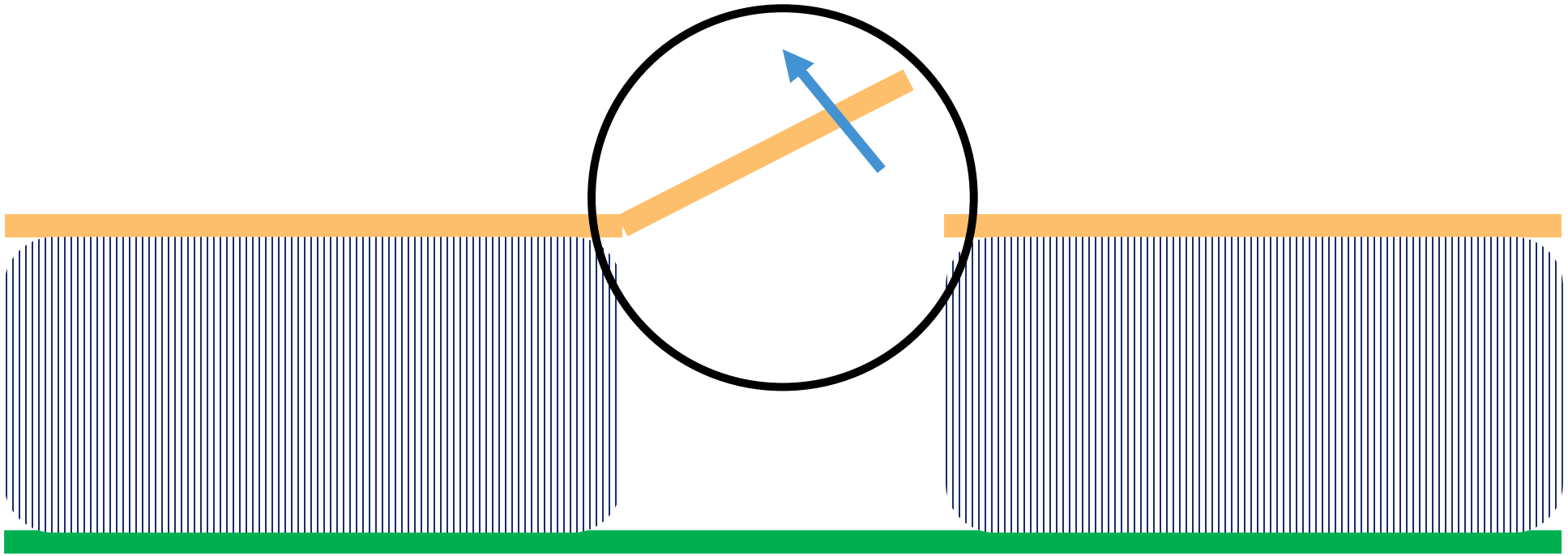
Agenda

- Changes on the Wind
- Foundation of Electronics
- Electromagnetic Field Behavior
- Power Supply Basics
- What's in the Waves
- Managing the Spaces
- Component Placement and Routing
- PCB Layout Considerations
- Test Results: Adding Ground Planes
- SMPS Circuit and Layout Analysis
- Closing Remarks and Reference Information









News Flash!

- We all are involved with developing products which generate, control and consume electromagnetic field energy.
- This is what we are taught:
  - Circuit theory pretends that electric energy is made up of electrons moving in the conductors.
  - Switches add conductors, and the current instantly starts to move in the loop.
  - The wires carry the energy, and the load instantly affects the flow of energy.

- Wrong!
  - Switches add new **spaces**, and the moving field carries the energy.
  - It takes time for the field energy to move into that **space**.
    - The moving field energy has no idea of what it is at the end of the new **space**.
  - Field energy moving through a **space** induces current flow in the conductors.
    - The magic here is the displacement current flowing through the dielectric at the wave front, completing the circuit.

Because You Know…

- It’s All About the Space!
  (not wires)

In Case You Already Forgot…

“All About the Space“ To the tune of Meghan Trainor’s “All about that Bass”. Copyright 2015 Daniel L. Beeker.
http://youtu.be/WglPHiZx4Gw

Because you know it’s all about the **space**
'Bout the **space**, not wires
It’s all about the **space**
'Bout the **space**, not wires
It’s all about the **space**
'Bout the **space**, not wires
It’s all about the **space**
'Bout the **space**... **space**... **space**... **space**

Yeah, it's pretty clear, you don’t believe it
But the wires just show, just show, where all the fields will fit
‘Cause all the energy only moves in the **space**
“Gotta put all the wires in all the right places”

I know your teacher said, it’s the conductor
We know that’s not the way, don’t listen to, the instructor
If you got fields a movin’, you got current flow
‘Cause it’s the movin’ fields that really make everything go

Yeah, your teachers they told you "don't worry about the field”
They said, “The math that they use isn’t something you wish to wield”.
You know that circuits are better, you just have to make them connect
So if that’s what you’re into, then you know what to expect

Because you know it’s all about the **space**
'Bout the **space**, not wires
It’s all about the **space**
'Bout the **space**, not wires
It’s all about the **space**

'Bout the **space**, not wires
It’s all about the **space**
'Bout the **space**...Hey!

I'm bringing physics back
Go 'head and tell them circuit fossils that
No, I'm just saying, I know you think they're right
But I'm here to tell you...
Physics tells us that it fields in **space** that’s really outta sight

I know your teacher said, it’s the conductor that holds the key
We know that’s not the way, you’ve gotta listen to me
If you got fields that are movin’, that makes all the current flow
So you gotta take all of this in, and lose all that you know

Because you know it’s all about the **space**
'Bout the **space**, not wires
It’s all about the **space**
'Bout the **space**, not wires
It’s all about the **space**
'Bout the **space**, not wires
It’s all about the **space**
'Bout the **space**...

Changes on the Wind

What Changes?

- Smaller device geometries and higher current switching capabilities have thrust us all into the world of RF, HF, UHF and microwave energy management
- Rise times on even the lowest tech devices now exhibit gigahertz impact
- These changes directly impact product functionality and reliability

What Changes?

- IC technology was described as % shrink from Integer Design Rules
  - Circuit-based approach usually was close enough
- IC technology now described in nanometers
  - Circuit-based approach completely falls apart
- EM field (physics) based approach essential
- EMC standards have changed
  - Lower frequency compliance requirements
  - Higher frequency compliance requirements
  - Lower emissions levels allowed
  - Greater immunity required
- The playing field and the equipment have changed!
- This really is a brand new game!

What Can We Do?

- The skills required are only taught in a few universities
  - Missouri University of Science and Technology (formerly the University of Missouri-Rolla) http://www.mst.edu/
  - Clemson University http://www.cvel.clemson.edu/emc
  - Grand Valley State University http://www.gvsu.edu
- Our sagest mentors may not be able to help
- Nearly every rule of thumb is wrong
- To gain the skills needed, you have to actively seek them
- Industry conferences
  - PCB West
  - IEEE EMC Society events
  - EMC Week
  - Embedded Systems Conferences
  - EMC Week
  - Classes held by your favorite silicon vendor ☺

What Can We Do?

About Me: Daniel Beeker

- 39+ years experience at Motorola/Freescale/NXP designing and working with microprocessor and microcontroller development systems
- 30+ years working with automotive customers in one of the most demanding embedded control environments
- Championing the cause for increased awareness of advanced design technologies
- Used to believe in black magic, but Ralph Morrison set me straight!
- Firmly entrenched in physics-based design philosophy

Foundation of Electronics

What is Electricity?

Is it volts and amperes …

or electric and magnetic fields?

What is Electricity?

- Fields are basic to all circuit operation
- Volts and amperes make things practical
  - We easily can measure volts and amperes
  - More difficult to measure “E” and “H” fields

(Slide compliments of Ralph Morrison, Consultant)

What is Electricity?

Fields do all of the work

- “Current flow” is an artifact caused by moving fields, in the conductors that bound them
  - This is a result of the fields interacting with the molecules in the conductor
  - This interaction consumes some of the field energy, hence a resulting voltage drop caused by this “resistance”
  - The conversion of field energy results in increased movement of the molecules (kinetic energy), hence is converted to “heat”!
  - The dielectric also consumes energy the same way, unless it is a vacuum.
  - Electromagnetic energy moves slower through a physical dielectric that through space because it must go around the molecules, increasing the distance it must travel, making it seem to go slower. The velocity of the waves is constant.

Heresy!!

- THAT is NOT what WE were taught.
- THAT is NOT the perspective we have used our entire careers.
- How dare you contradict my professors and my mentors?
- Didn’t what we are doing work for years?
- Don’t I just have to connect the pins and things will work?

- …Wait a minute, then why do we have so much trouble with signal integrity and EMC??
- Maybe there IS something we are missing…

Heresy!!

- Is the song still going through your heads?
- It is “All About the **Space**!!”
- Words to live by!!
- Now let’s see what we can learn so we can understand this mystery

Maxwell's Equations

$$\oint \mathbf{E} \cdot d\mathbf{A} = \frac{q_{enc}}{\varepsilon_0}$$

$$\oint \mathbf{B} \cdot d\mathbf{A} = 0$$

$$\oint \mathbf{E} \cdot d\mathbf{s} = -\frac{d\Phi_B}{dt}$$

$$\oint \mathbf{B} \cdot d\mathbf{s} = \mu_0 \varepsilon_0 \frac{d\Phi_E}{dt} + \mu_0 i_{enc}$$

(Slide compliments of http://www.physics.udel.edu/~watson/phys208/ending2.html)

Maxwell’s Equations

Maxwell *was* smart!

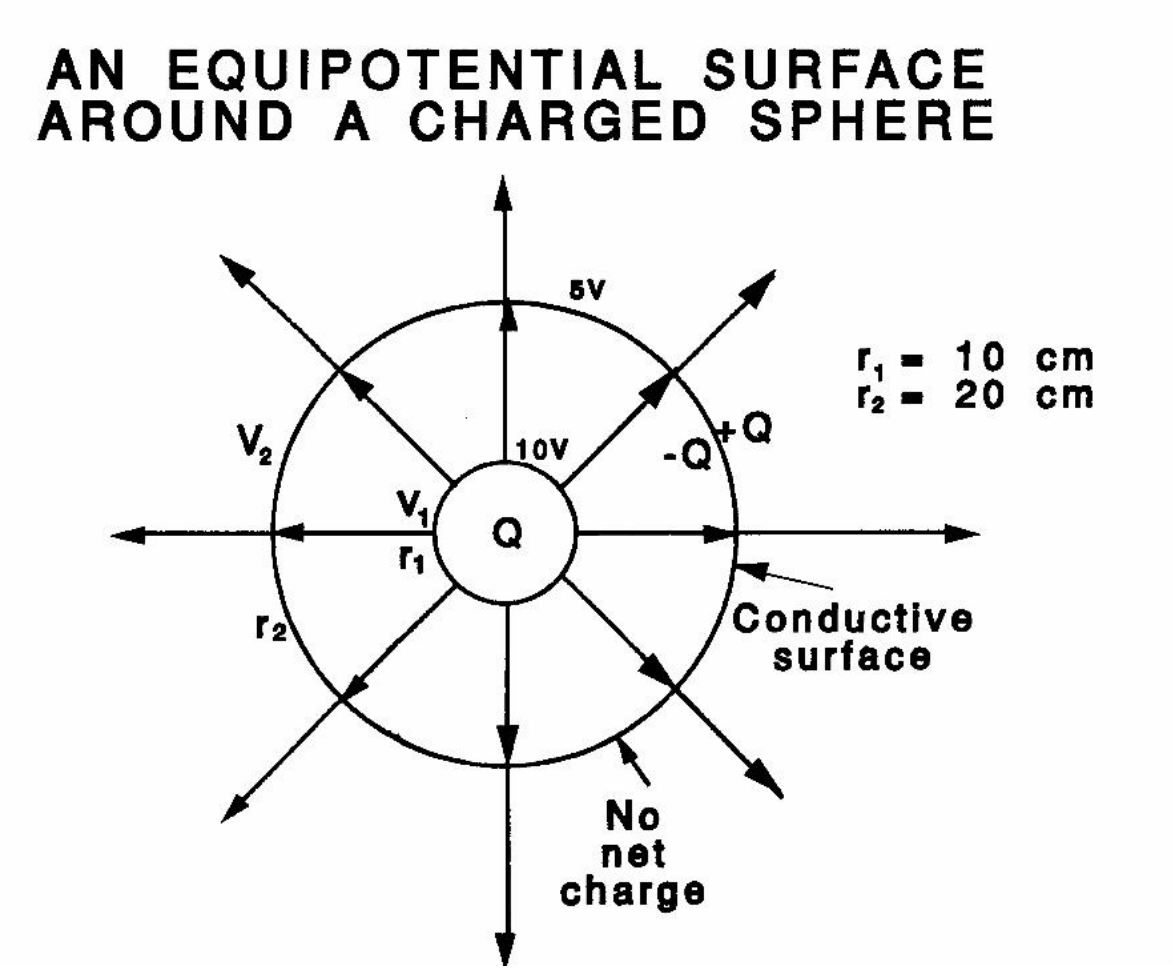
Heresy!!

- Maxwell's equations are all about the interaction between electric and magnetic fields

- There are not any electrons in them
  - No holes, either
  - If it were all about electrons moving, how would fields move through **space**???

Electromagnetic Field Behavior

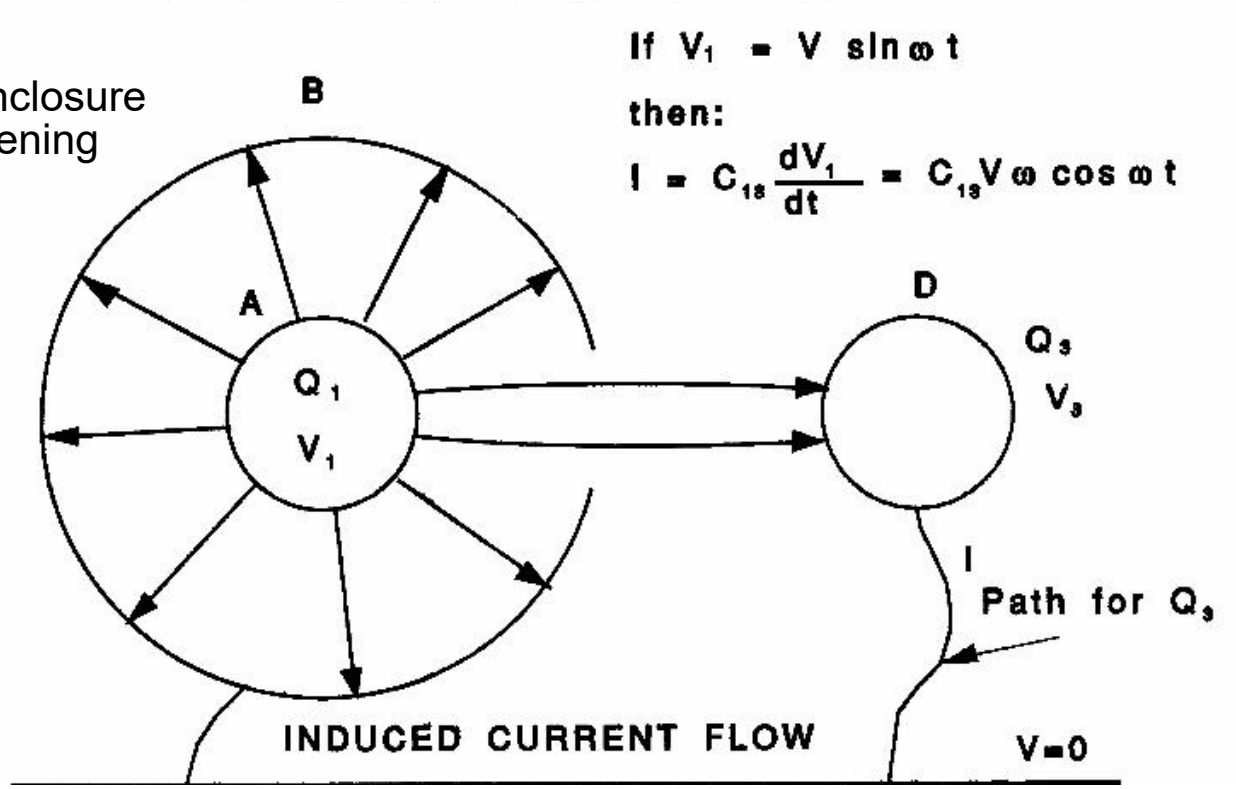
Contained Fields are Friendly!



(Slide compliments of Ralph Morrison, Consultant)

A Loose Field is Not a Friendly Field

A shielded enclosure with an opening

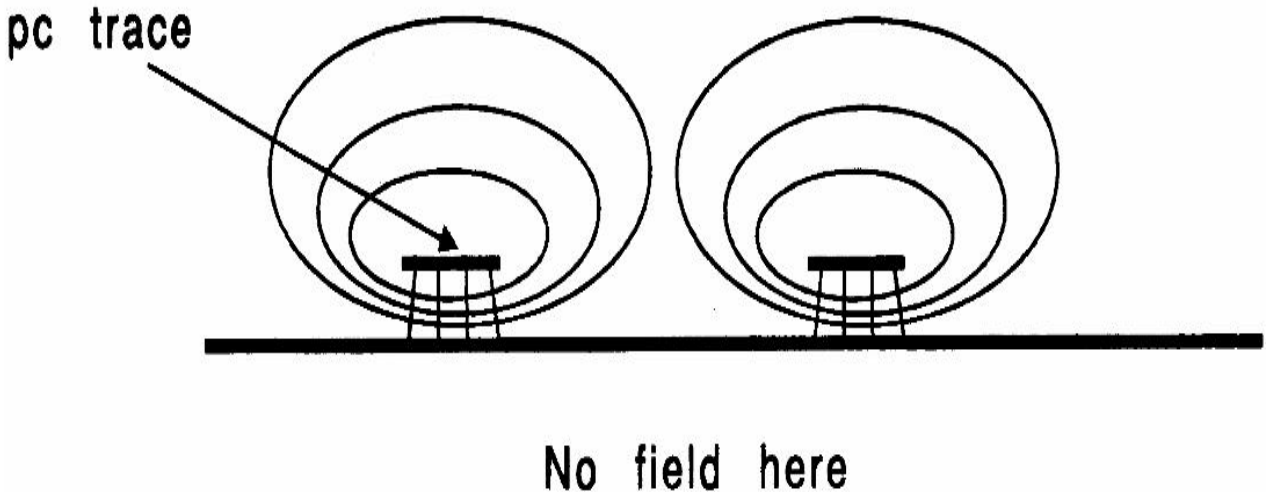


Field is not contained and looks for trouble

(Slide compliments of Ralph Morrison, Consultant)

Contained Fields are Friendly!

Fields concentrate under the traces and there is little crosstalk



Fields do not penetrate the plane

(Slide compliments of Ralph Morrison, Consultant)

Power Supply Basics

Energy Management

A capacitor is:

A conductor geometry that concentrates the storage of electric field energy

An inductor is:

A conductor geometry that concentrates the storage of magnetic field energy

In a capacitor:

Field energy is stored in the **space** between the plates

In an inductor:

Field energy is stored in the **space** around wires and in gaps

Think of capacitors as lakes between two rivers

Think of inductors as wire stretchers. They add travel time to the waves!

(Slide compliments of Ralph Morrison, Consultant)

Power Supply Transmission Line Properties

- In a good design:
  - Energy is available whenever there is a demand
  - The voltage source must be reasonably constant
  - Energy must be replaced after it is used or there will be logic (signal integrity) problems
  - This is called energy management
- Local sources of energy:
  - Decoupling capacitors
  - There is also energy available from ground/power plane capacitance
- New problem: It takes time to move this energy from storage to a load

(Slide compliments of Ralph Morrison, Consultant)

How Long Does It Take?

Wave velocity

- For traces on a circuit board $v = c/\varepsilon^{1/2}$
- Where “c” is the velocity of light and “ε” is the relative dielectric constant

v = 150 mm / ns or 6”/ns

All energy is moved by wave action!

- A drop in voltage sends a wave to get more energy
- Waves reflect at discontinuities (changes in the geometry of the **space**)
- A source of voltage is a discontinuity
- Each reflected wave can carry a limited amount of energy

(Slide compliments of Ralph Morrison, Consultant)

Getting 1 Ampere to Flow

What does this mean in my circuit board?

Initial power level in a 50 Ohm line

- 5 Ohm load and 5 V source
- I = 0.1 amperes or ½ watt

Now, how do I get 1 ampere (1 *coulomb* per second)?

Even if the line is only 1/16 inch long:

- It takes 10 ps for a wave to go 1/16 inch in FR4
- It takes 20 ps for a wave to make one round trip
- It takes 30 round trips to bring current level up to near one amp
- That is 600 ps, assuming zero rise time

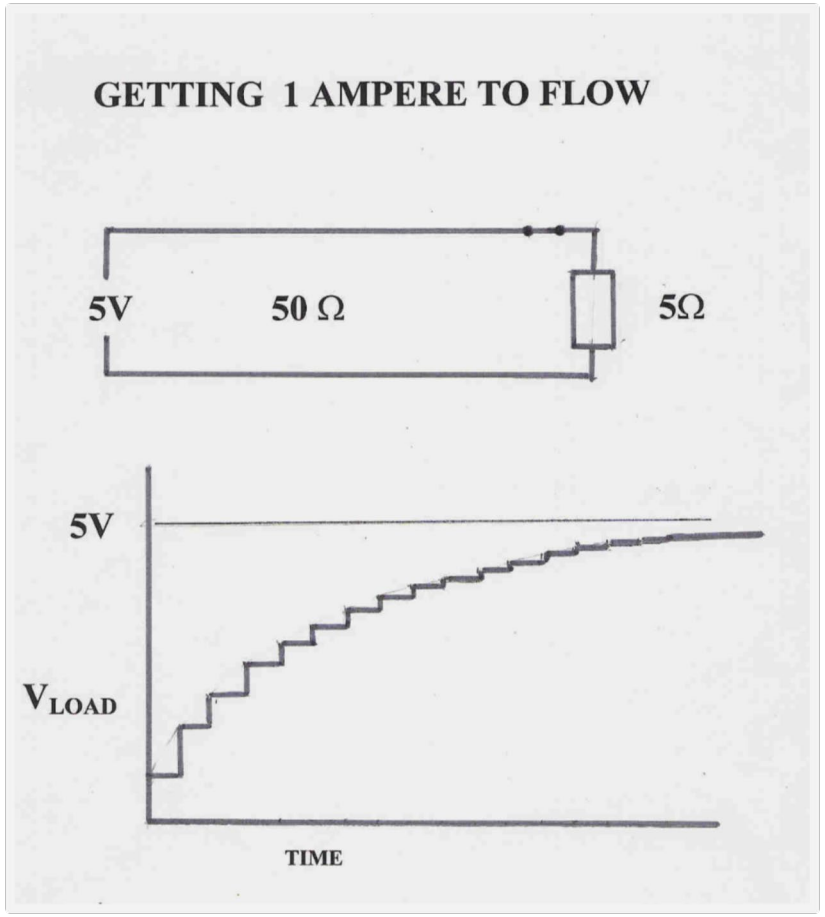
(Slide compliments of Ralph Morrison, Consultant)

Getting 1 Ampere to Flow

Note: This is not a curve, but a series of step functions.

The amplitude of the step is determined by the impedance of the transmission line.

The width of the step is determined by the length of the transmission line and a two way transition for the wave.



(Slide compliments of Ralph Morrison, Consultant)

Typical 1/16 Inch Connections

- Traces to capacitors
- Connections to IC dies
  - Lead frames and wire bonds
  - BGA interposers
- Traces to vias
- Vias to ground/power planes
- Remember, 1/16 inch is about 10 ps
  - Yes, you do care about picoseconds now!

(Slide compliments of Ralph Morrison, Consultant)

Transmission Lines

Capacitors are short transmission lines:

- Wave action is required to move energy in and out of a capacitor
- Don’t forget the connections to the capacitor!
- Self inductance does not properly tell the story of why it takes time to supply energy
- Circuit theory does not consider time delays
- See the previous diagram!

(Slide compliments of Ralph Morrison, Consultant)

What's in the Waves?

Energy Management

All energy is moved by wave action!

- When a switching element closes, the movement of the field energy into the new **space** results in a drop in the voltage (field density) of the power supply. The resulting field energy request (depletion wave) travels until this request is filled or it radiates.

The only way to reduce noise in a system is to reduce this distance and provide adequate sources of electromagnetic field energy.

Energy source hierarchy

- On-chip capacitance
- **Space** between the wire bonds
- Between layers of Substrate (BGA) or lead frame (QFP)
- Power planes if present
- Local bypass capacitors
- Field energy stored across the PCB structure
- Bulk storage capacitors
- Finally the power supply

We have to keep the field happy and contained as far up the food chain as we can, to reduce system noise.

(Slide compliments of Ralph Morrison, Consultant)

Energy Delivery From A Storage Device

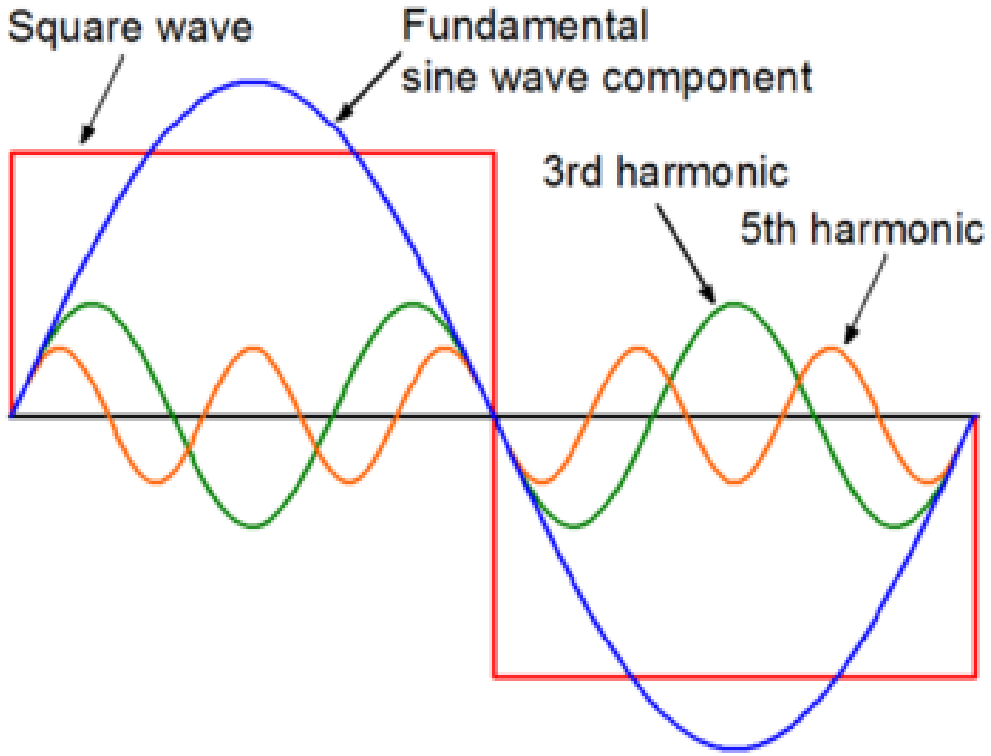
For energy to be delivered from a storage device:

- The wave requesting the energy (observed as a dip in the power supply caused by the switching event) has to travel to the source and back to the switch.

It’s a two-way trip!

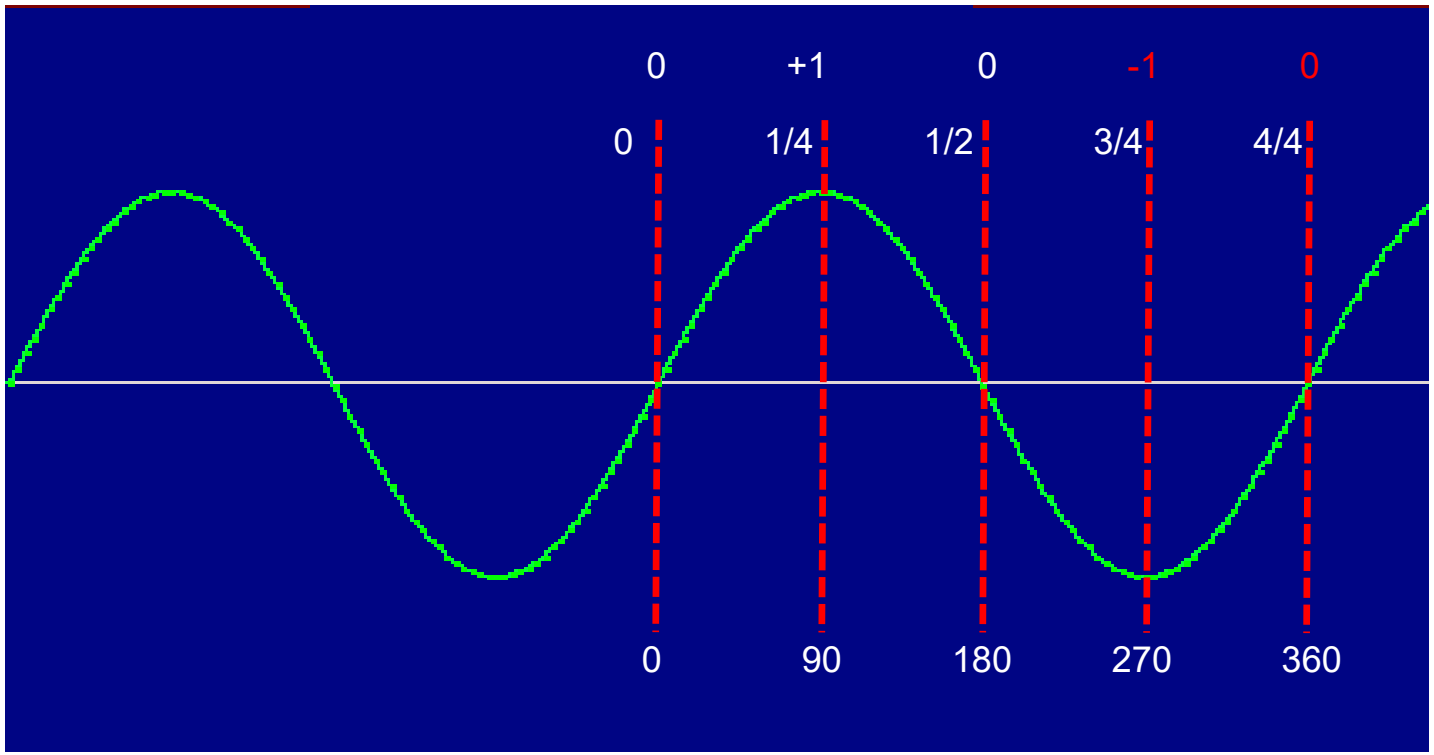
Digital Wave Perspective

- Square wave is made up of an infinite number of frequencies
- Design for the highest frequency the driver is capable of supporting



Analog Wave Perspective

- Seen as sine wave with positive and negative amplitude
- Rise time distance would be ¼ wavelength



Switching Frequency vs. Power Source

Frequency	1/20 Wave Length
5 MHz HMOS Rise time equivalent, 100 nanoseconds Rise time distance, 100 feet	4.92 feet Somewhere in the room
50 MHz (TTL Logic) UDR HCMOS Rise time equivalent, 10 nanoseconds Rise time distance, 10 feet	0.492 feet (5.9 inches) Somewhere on the board, should be routed as co-planar pairs
500 MHz (BiCMOS Logic) IDR HCMOS Rise time equivalent, 1 nanosecond Rise time distance, 1 foot	0.0492 feet (0.59 inches) Width of your finger, time to look at small geometry capacitors and power islands
5 GHz (GaAs Logic) 65 nm HCMOS Rise time equivalent, 100 picoseconds Rise time distance, 1.2 inches	0.00492 feet (0.059 in. or 1498.6 µm) In the package
50 GHz 32 nm HCMOS Rise time equivalent, 10 picoseconds Rise time distance, 0.12 inches	0.000492 feet (0.0059 in. or 149.86 µm) On the die

Switching Frequency vs. Power Source

- If the energy source is not inside the 1/20 wavelength distance, there will be radiated energy caused by the switching event (depletion wave).
- The job of the PCB designer is to minimize the amount of energy by managing the power delivery system for each type of switching event.
- As the geometry of the ICs we use continues to shrink, so does the area of effective power delivery.
- Well-defined power delivery transmission lines and small geometry, low impedance, field storage devices are essential.
- Even if they are outside of the “zone,” they can minimize the amount of radiated energy.

Fields are Friendly!

- Fields need to be carefully managed:
- Every connection must be treated as one conductor of a transmission line pair
- Field volumes (read “transmission line impedance”) must be carefully managed
- Each discontinuity (read “change in transmission line GEOMETRY”) results in reflections
- Each segment of this geometry must have enough field energy delivered to match the voltage (read “field density”) from the driver
- This all takes TIME

- Yes, this is now a four-dimensional geometric design problem

Energy and Logic Signals

- The transmission of a logic signal means that field energy is sent out on a transmission line
  - Logic drivers should be treated the same as any power source
- This is true even if the line is un-terminated
  - The driver does not know what is at the end of the transmission line
  - The driver only sees a short circuit until after a reflection occurs
- This energy must be transmitted to the receiver or lost in heat or radiation – it cannot be returned to the driver

Power Supply Connections

- Must be Well-Defined Transmission Lines
- Power traces MUST be one dielectric away from the return!
  - Adjacent to planar copper
  - Adjacent to ground trace
  - Any deviation from this WILL increase noise floor and radiated emissions, degrade signal integrity and decrease immunity

Field Storage Devices

- Energy storage component geometry and placement requirements are determined by the switching speed of the device
- The faster the switch, the more critical this becomes
- Do not expect behaviors from energy storage devices that are not possible

Field Storage Devices

- The frequency at which capacitors can respond to energy requirements is determined by their physical geometry and the connecting transmission line, not by their value

- Smaller capacitor packages respond faster because their terminals are closer together
  - More energy per wave cycle

- Devices which are closer to the switch respond faster because it takes less time to request and deliver energy

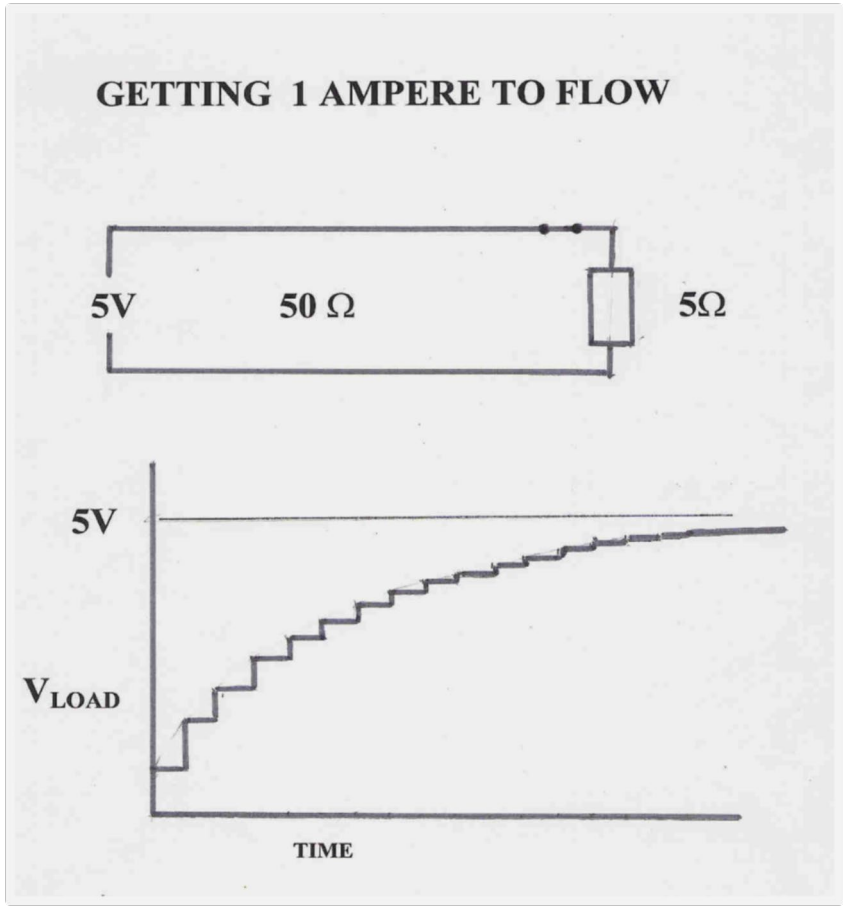
Field Storage Devices

- Total energy delivered by each wave is determined by the impedance of the capacitor structure (ESR) and the interconnecting structures

- The time it takes is determined by the distance from the switch and the length of the plate structure

Remember This Slide? Getting 1 Ampere to Flow

- Note: This is not a curve, but a series of step functions.
- The amplitude of the step is determined by the impedance of the transmission line.
- The width of the step is determined by the length of the transmission line and a two way transition for the wave.
- Note to self: this is exactly how a capacitor behaves!



(Slide compliments of Ralph Morrison, Consultant)

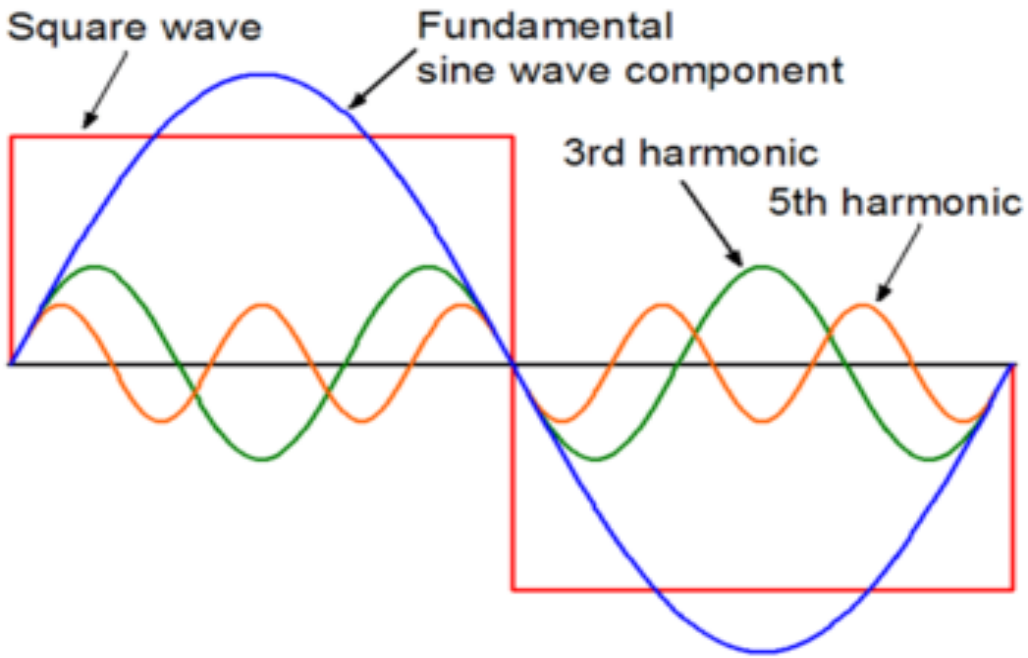
Managing the Spaces

Now for the Eureka Moment!

- Energy delivery from power supplies is a one way path!
- Each node in the power supply should be considered a discrete domain, with field energy traveling downstream from the power source to the switching device.
- The farther away from the switch, the longer it takes for the request for energy to be answered.

Now for the Eureka Moment!

- Switching waveform is made up of an infinite number of frequencies
- Design for the highest frequency the driver is capable of supporting



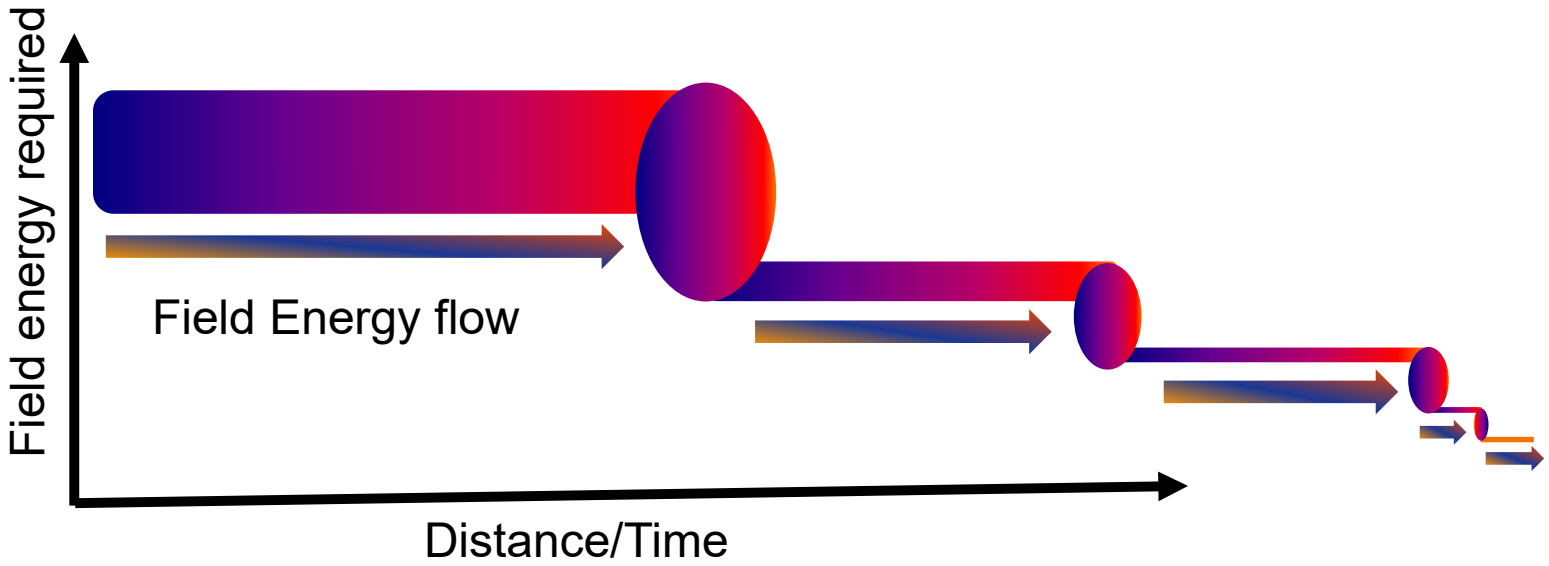
Now for the Eureka Moment!

- DO NOT ask for fast energy from a large package capacitor far away, and you will not be disappointed.

- Design the supply system to deliver different parts of the energy spectrum from matching structures.

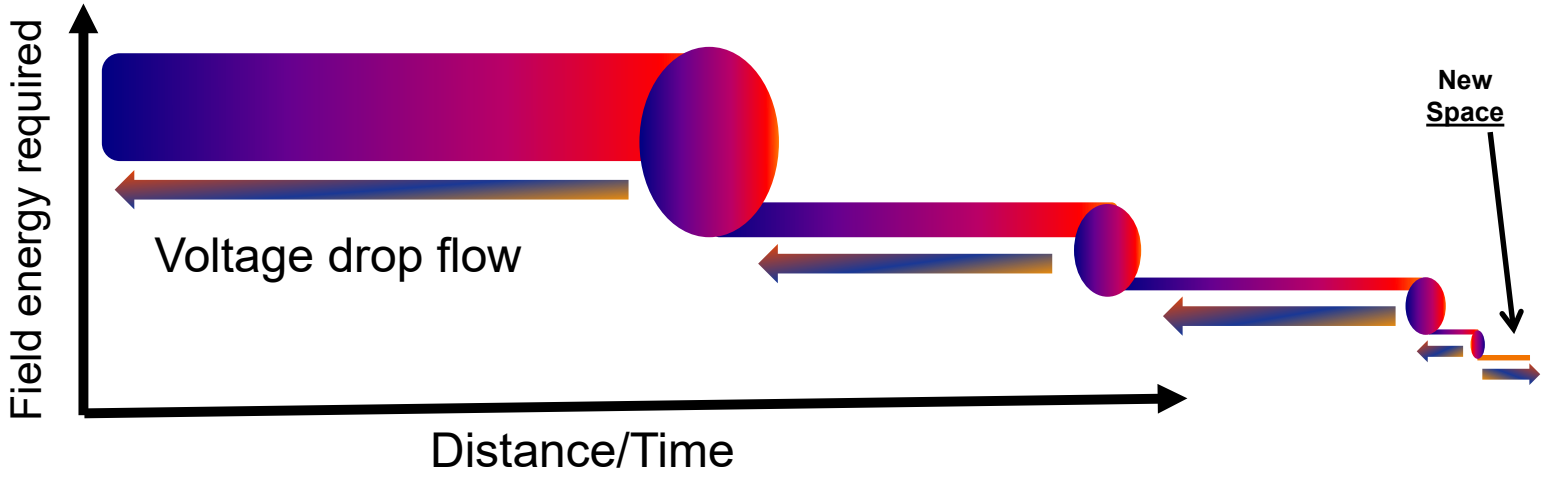
Now for the Eureka Moment!

- Imagine that you have water pipes of different sizes.
- The big pipes carry lots of water, but don't respond quickly to changes in the output.
- The little pipes don't carry much water, but respond quickly to changes in the output.
- The capacitors are like buckets for the water, they have to fill up before the water moves further down the pipe.
- The overall behavior is more like the loads are sucking the water, not that the source is pushing the water.
- Field energy is moving to the switch at the end to fill another **space** that is now connected when the switch is turned on.



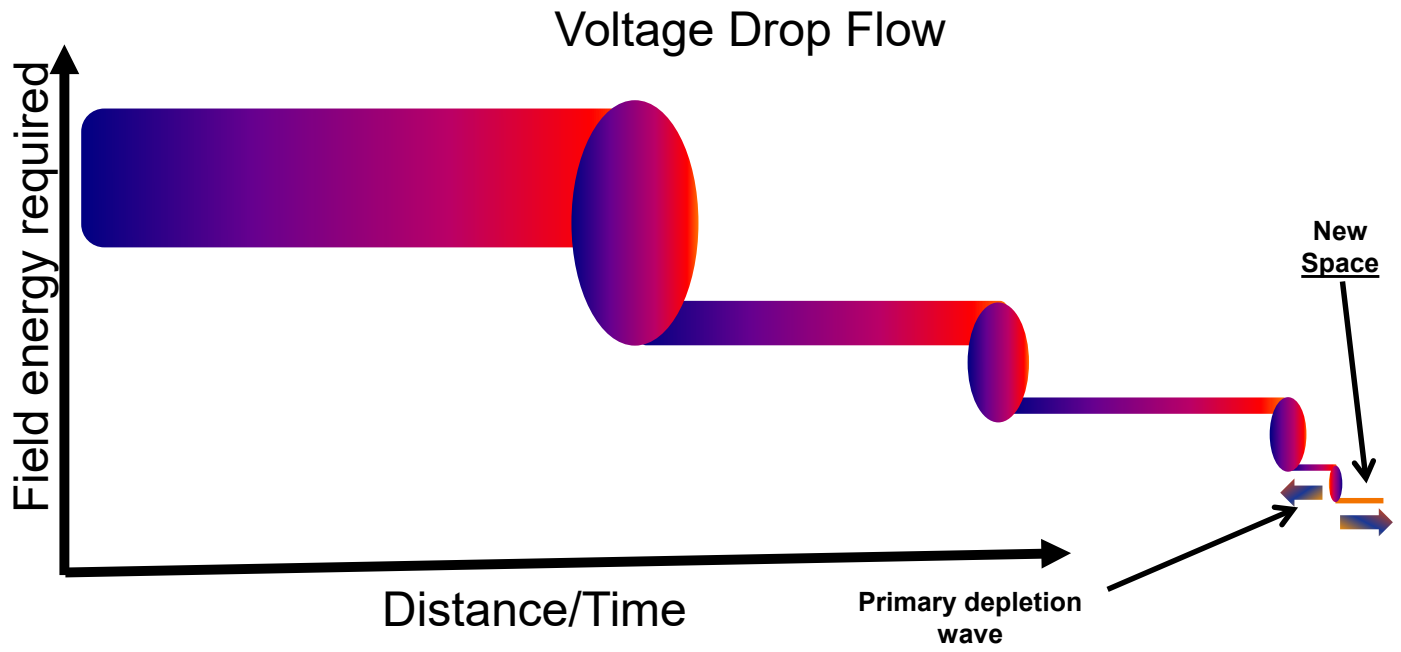
Now for the Eureka Moment!

- Yes! When you turn on a switch, you are adding a new **space** which has a different field density than the input to the switch.
- It takes time for the new **space** to fill with EM field energy, and it moves from the switch outward, inducing current flow in the conductors as it moves through the new **space**.
- Displacement current through the dielectric is what completes the circuit as the energy moves to fill the new **space**.
- The field density near the switch drops, as the energy moves into the new **space**.
- This causes a wave which travels upstream until it finds a discontinuity (change in transmission line geometry, or “impedance”) and reflects back with more field energy to replace that which moved into the new **space**.
- This process continues until either the switch is opened, or the new **space** has the same field density as the power supply.



Now for the Eureka Moment!

- Each reflection causes a drop in field density at the discontinuity, which in turn causes a new wave to move upstream to get more energy.
- The reflections from energy storage devices which are closer return faster. Reflections from discontinuities that are farther away take longer.
- This process continues until either the switch is opened, or the new **space** has the same field density as the power supply.



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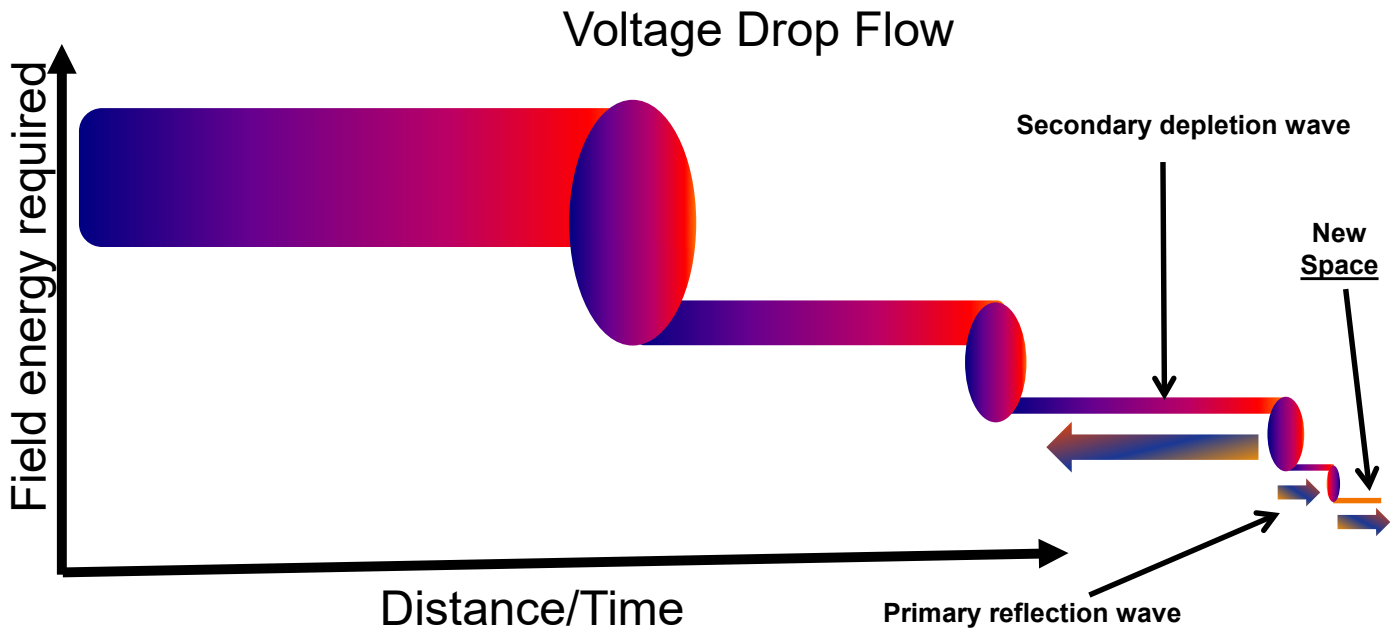
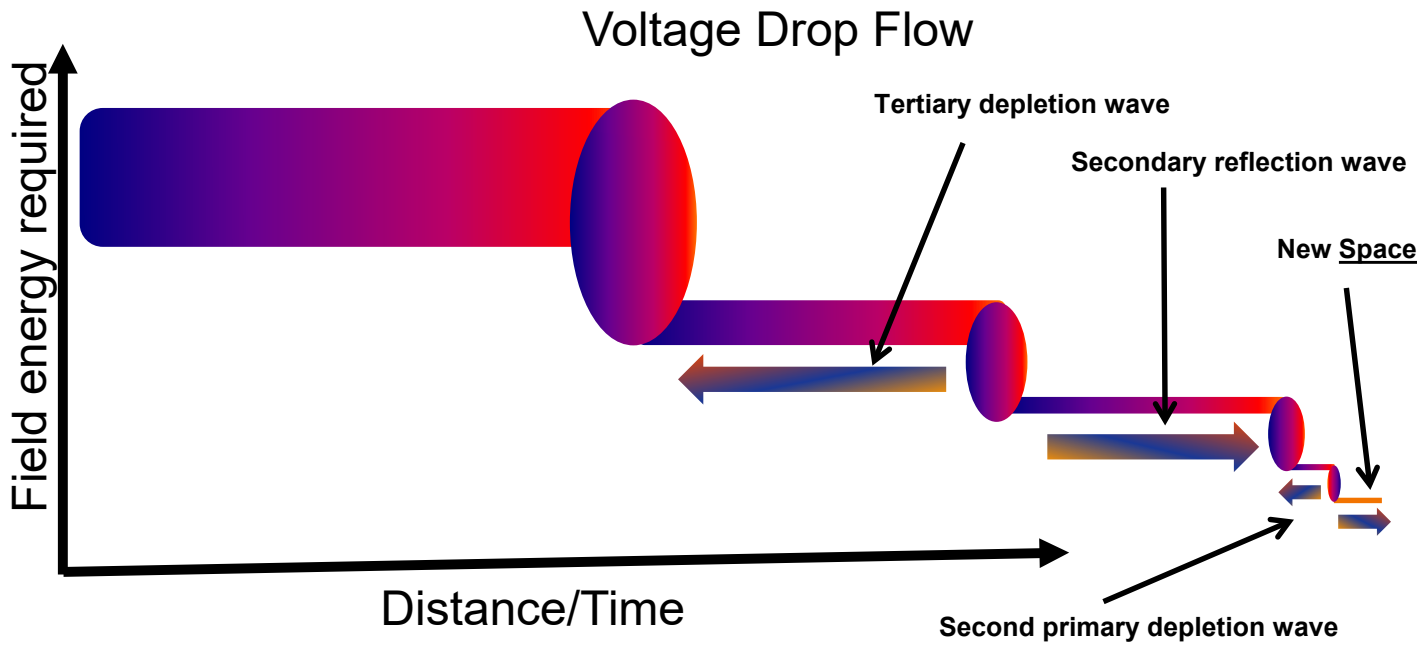
- Each reflection causes a drop in field density at the discontinuity, which in turn causes a new wave to move upstream to get more energy.
- The reflections from energy storage devices which are closer return faster. Reflections from discontinuities that are farther away take longer.
- This process continues until either the switch is opened, or the new **space** has the same field density as the power supply.



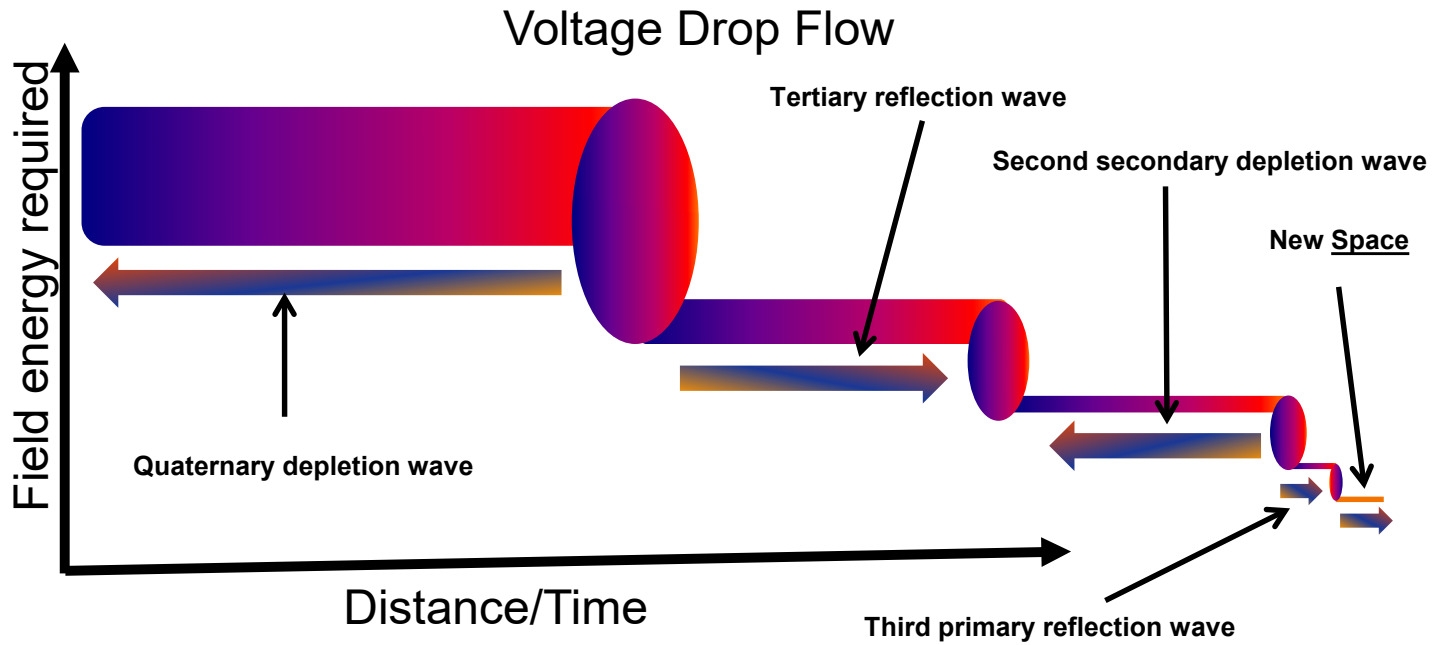
Now for the Eureka Moment!

- The charge storage devices upstream do not see any field depletion waves until many, many cycles occur at the switch point, because they are farther away!!
- Most system noise (radiated emission) is the result of too little energy stored close enough to the switch to keep the higher frequency depletion waves from finding a conductor that is long enough to be an antenna.
- This is determined by the switching speed of the driver.



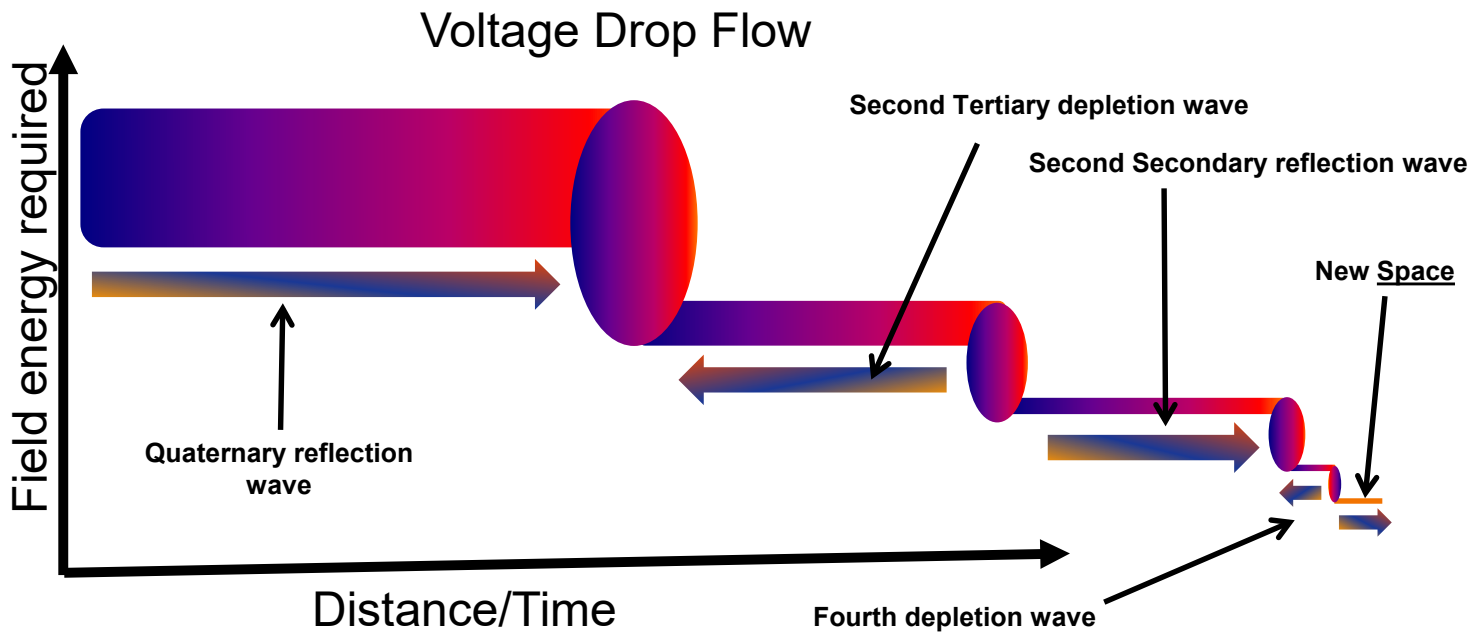
Now for the Eureka Moment!

- The goal of a good power supply design is to prevent this, and insure that the depletion/reflection cycles upstream have a slower and slower slope to the wave front
- The geometry of the transmission line and the energy storage device determine the cycle time and the amount of energy each wave contains.
- In most designs, the connections to the capacitor packages pose the largest discontinuities, because the connections are farther apart than the power supply transmission line conductors.



Now for the Eureka Moment!

- Proper power supply design results in depletion/reflection cycles with increasing cycle times and decreasing wave front slopes.
- This is driven by the distance between field storage devices and their package sizes.
- Proper power supply design results in a virtual steady state flow of field energy from the input power supply to the devices which consume the field energy.
- It is all about managing the movement of field energy through the **spaces**.



Now for the Eureka Moment!

- The goal is to create a network that basically allows for steady state delivery of energy, with each successive element only responsible for providing energy for the next downstream user.
- Remember this list?

Energy source hierarchy

- On-chip capacitance
- **Space** between the wire bonds
- Between layers of Substrate (BGA) or lead frame (QFP)
- Power planes if present
- Local bypass capacitors
- Field energy stored across the PCB structure
- Bulk storage capacitors
- Finally the power supply

Now for the Eureka Moment!

Each can supply energy determined by the **space** it contains and the **spaces** (transmission lines) between the elements

- On-chip capacitance (10s of fs)
  - Closest, supports the highest frequencies
- **Space** between the wire bonds (100s 0f fs)
  - Farther away, but still help to feed the on-chip capacitors
- Between layers of Substrate (BGA) or lead frame (QFP) (1s of ps)
  - Farther still, feeds the wire bond **spaces**
- Power/ground plane pairs, if present (10s of ps)
  - Power islands are best, used to collect the power pins and connect to the next element, feed the package
- Local bypass capacitors (10s of ps)
  - Small geometry (usually 0402), placed as close as possible, feed the power islands or package
- Field energy stored across the PCB structure (100s 0f ps)
  - Larger packages placed in the realm of the ICs, feed the local bypass devices
- Bulk storage capacitors (100s of ps)
  - Near the voltage regulator, feed the regional capacitors
- Finally the power supply (10s of ns)
  - Collects energy from the outside world and fills the bulk capacitors

Now for the Eureka Moment!

- In designs where there is not enough energy storage close to the switch, or the connections between the elements of the power distribution system are not one dielectric away from each other, the result will be switch coherent radiated emissions.
- The frequency of this noise is determined by the switching speed of the switch itself. The pulse recurrence time of the noise is driven by the distance between the discontinuities and the period of the switch toggle.
- Clock coherent switching noise results from inadequate energy delivery to the IC core.
- Bus coherent switching noise results from inadequate energy delivery to the address/data bus drivers.

Now for the Eureka Moment!

This will not work unless they are all transmission lines!!

- Must be Well-Defined Transmission Lines
- Power traces **MUST** be **ONE** dielectric away from the return!
  - Adjacent to planar ground copper
  - Adjacent to ground trace
  - Any deviation from this WILL increase noise floor and radiated emissions, degrade signal integrity and decrease immunity
- Important facts to remember
  - When a switch is closed, the new **space** becomes a power supply (the same behavior and rules apply)
  - When a switch is closed, all of the other **spaces** using the same source of energy will see the depletion waves

Now for the Eureka Moment!

- From all of this, we can see that most EMC issues result from starving the switches
- Correcting most EMC issues requires providing adequate energy from close enough sources to prevent the depletion waves from finding an antenna
- You prevent EMC issues by insuring the switches are properly fed, not by restricting the flow of energy

- One more point:
  - In a good power supply design, there is no need for ferrites, inductors, or filters, reducing system cost!

Managing the Plumbing

- The power distribution network must match the energy requirements for the system
  - Adequate Energy Storage Capacity
    - There has to be enough “capacitance” placed in the correct locations (per the previous discussion
  - Adequate Energy Transmission Capacity
    - The Plumbing MUST match the required “Coulombs per second”

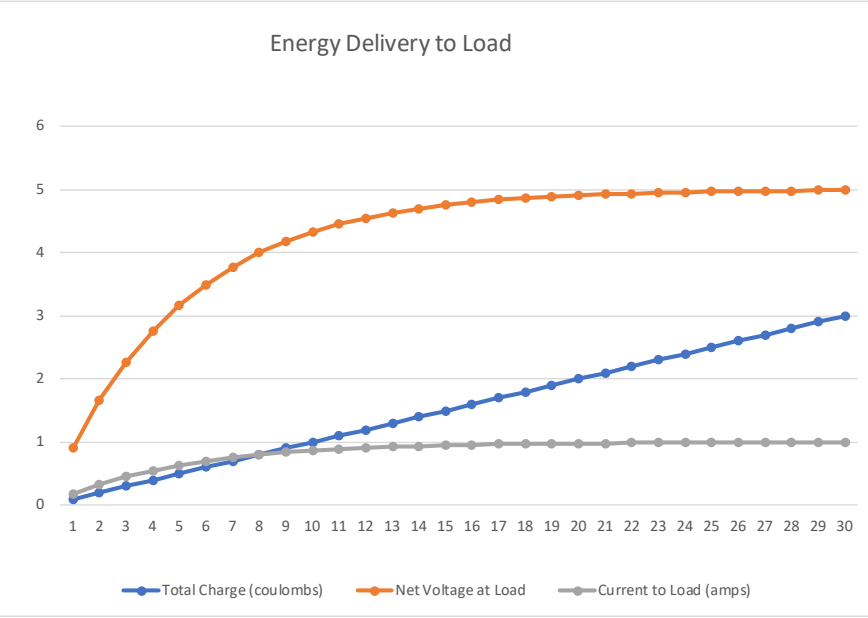
- The “load” package interface is usually the limiting factor
  - Analyze the device’s capability to transfer energy from the PCB to the Die
  - Design the PDN to exceed this limit

- Power supply nirvana is achieved!

Managing the Plumbing

- The power distribution network evaluation tool

Transmission Line Capabilities			
Assuming FR4 inner layers	6" per nS	Coulomb = 1A/sec	
= User Enty			
Signal or Supply Voltage		5	Volts
Transmission Line Impedance		50	Ohms
Transmission Line Length		1/16	inches
Load Resistance		5	Ohms
Number of transmission lines used		1	>/= 1



Energy Delivery to Load											
Wave Cycle	Charge Per Wave (coulombs)	Total Charge (coulombs)	Load (ohms)	Net Impedance (ohms)	Voltage Delta (volts)	2R/(R + Z)	Net Voltage at Load	Current to Load (amps)	Transmission Line Length (in)	Cycle Time (ps)	Elapsed Time (ps)
1	0.1	0.1	5	50	5.0000	0.9091	0.9091	0.1818	1/16	20.83	20.83
2	0.1	0.2	5	50	4.0909	0.7438	1.6529	0.3306	0.0625	20.83	41.67
3	0.1	0.3	5	50	3.3471	0.6086	2.2615	0.4523	0.0625	20.83	62.50
4	0.1	0.4	5	50	2.7385	0.4979	2.7594	0.5519	0.0625	20.83	83.33
5	0.1	0.5	5	50	2.2406	0.4074	3.1668	0.6334	0.0625	20.83	104.17
6	0.1	0.6	5	50	1.8332	0.3333	3.5001	0.7000	0.0625	20.83	125.00
7	0.1	0.7	5	50	1.4999	0.2727	3.7728	0.7546	0.0625	20.83	145.83
8	0.1	0.8	5	50	1.2272	0.2231	3.9959	0.7992	0.0625	20.83	166.67
9	0.1	0.9	5	50	1.0041	0.1826	4.1785	0.8357	0.0625	20.83	187.50
10	0.1	1	5	50	0.8215	0.1494	4.3278	0.8656	0.0625	20.83	208.33
11	0.1	1.1	5	50	0.6722	0.1222	4.4501	0.8900	0.0625	20.83	229.17
12	0.1	1.2	5	50	0.5499	0.1000	4.5500	0.9100	0.0625	20.83	250.00
13	0.1	1.3	5	50	0.4500	0.0818	4.6319	0.9264	0.0625	20.83	270.83
14	0.1	1.4	5	50	0.3681	0.0669	4.6988	0.9398	0.0625	20.83	291.67
15	0.1	1.5	5	50	0.3012	0.0548	4.7536	0.9507	0.0625	20.83	312.50
16	0.1	1.6	5	50	0.2464	0.0448	4.7984	0.9597	0.0625	20.83	333.33
17	0.1	1.7	5	50	0.2016	0.0367	4.8350	0.9670	0.0625	20.83	354.17
18	0.1	1.8	5	50	0.1650	0.0300	4.8650	0.9730	0.0625	20.83	375.00
19	0.1	1.9	5	50	0.1350	0.0245	4.8896	0.9779	0.0625	20.83	395.83
20	0.1	2	5	50	0.1104	0.0201	4.9096	0.9819	0.0625	20.83	416.67
21	0.1	2.1	5	50	0.0904	0.0164	4.9261	0.9852	0.0625	20.83	437.50
22	0.1	2.2	5	50	0.0739	0.0134	4.9395	0.9879	0.0625	20.83	458.33
23	0.1	2.3	5	50	0.0605	0.0110	4.9505	0.9901	0.0625	20.83	479.17
24	0.1	2.4	5	50	0.0495	0.0090	4.9595	0.9919	0.0625	20.83	500.00
25	0.1	2.5	5	50	0.0405	0.0074	4.9669	0.9934	0.0625	20.83	520.83
26	0.1	2.6	5	50	0.0331	0.0060	4.9729	0.9946	0.0625	20.83	541.67
27	0.1	2.7	5	50	0.0271	0.0049	4.9778	0.9956	0.0625	20.83	562.50
28	0.1	2.8	5	50	0.0222	0.0040	4.9819	0.9964	0.0625	20.83	583.33
29	0.1	2.9	5	50	0.0181	0.0033	4.9852	0.9970	0.0625	20.83	604.17
30	0.1	3	5	50	0.0148	0.0027	4.9879	0.9976	0.0625	20.83	625.00

Managing the Plumbing

- The power distribution network evaluation tool
  - Fill in the form to evaluate the capability of your network
  - Add more pipes if you don't move enough energy per wave cycle.
  - It's All About the Space!!

Transmission Line Capabilities				
Assuming FR4 inner layers	6" per nS		Coulomb = 1A/sec	
= **User Enty**				
Signal or Supply Voltage			**5**	**Volts**
Transmission Line Impedance			**50**	**Ohms**
Transmission Line Length			**1/16**	**inches**
Load Resistance			**5**	**Ohms**
Number of transmission lines used			**1**	**>/= 1**

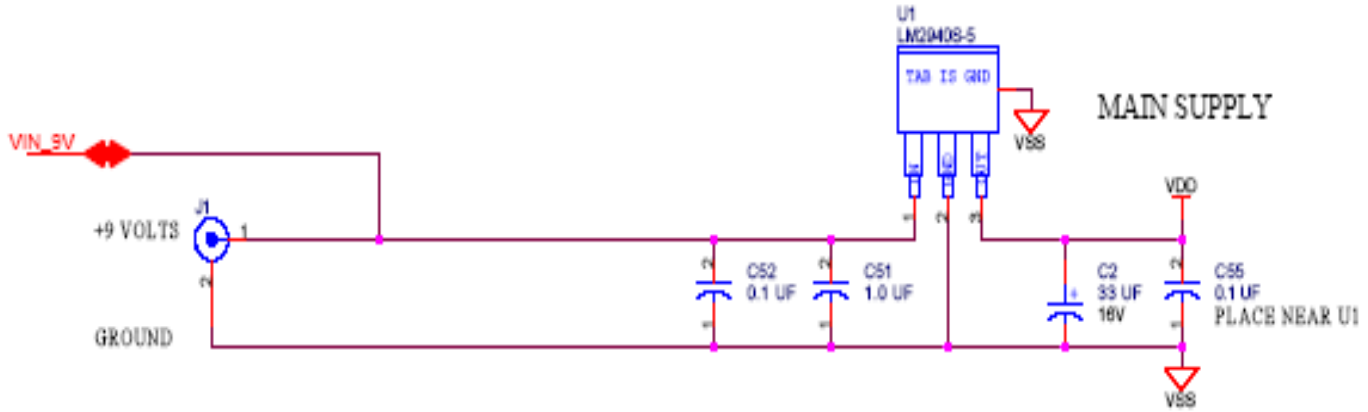
Component Placement and Routing

Where Do We Start?

- Board outline / usually pre-determined
  - Defined by previous product
  - Customer requirements
- Placement
- Pre-defined components / usually connectors
- Filter components / high priority, must be as close to the pins as allowed by manufacturing
- Power control / as close to connector involved as possible
- Voltage regulators
- Power switching devices

Power Supply Design Made Easy!

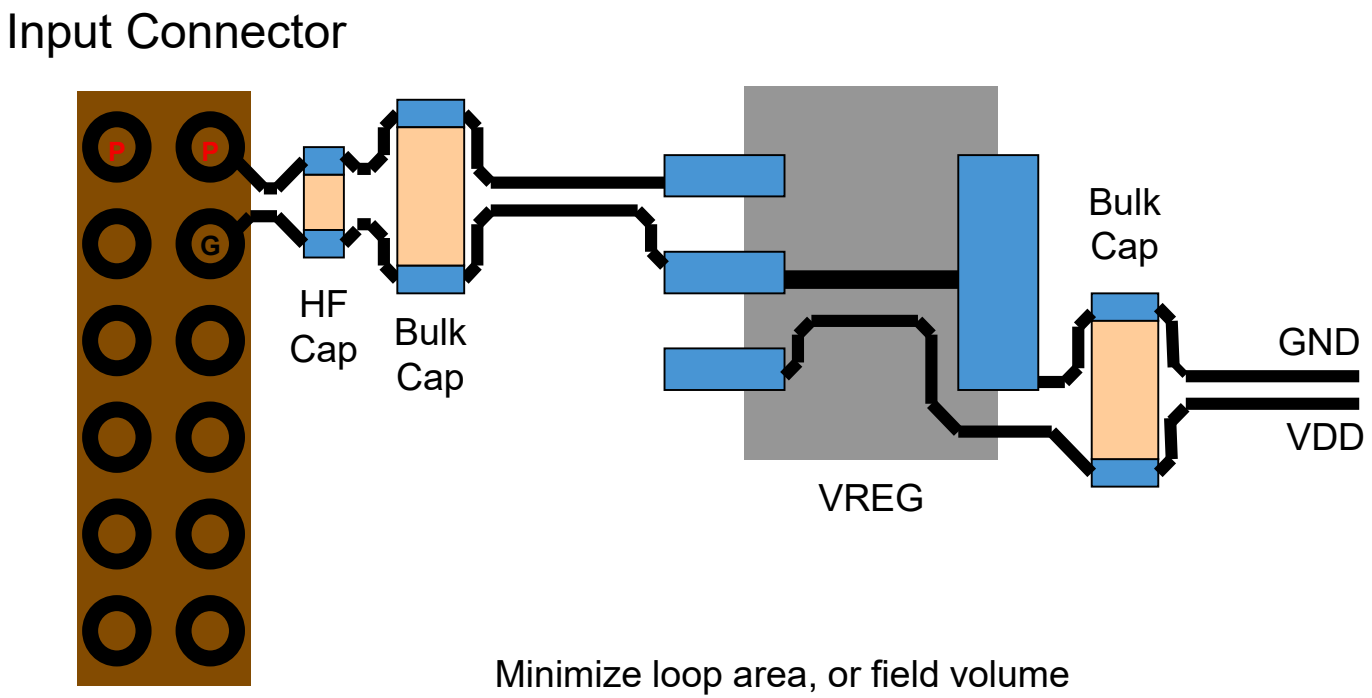
- Schematic must be evaluated during layout
  - Schematic is often lacking in order definition
  - Capacitors must be placed in the daisy chain in the correct order



PCB ~~signal~~ Transmission Line Routing

- The first and most important job is to route the power distribution network – it is the source of all of the electromagnetic energy you will be managing on the PCB
- On low layer count boards, with no dedicated ground plane, the power lines must be routed in pairs
  - Power and ground
  - Side by side
    - Trace width determined by current requirements
    - Spaced as close as manufacturing will allow them
  - Daisy chain from source to destination, connecting to each component, then finally to target devices
- Minimize the volume of the power transmission network

PCB ~~signal~~ Transmission Line Routing



Minimize loop area, or field volume

Energy flows from left to right, never the reverse!

PCB ~~signal~~ Transmission Line Routing

- Route power and ground traces as close as manufacturing allows
- Internal and customer separation requirements
- PCB fabrication limits for chosen supplier
  - Yes, you do need to know what the supplier can manufacture
  - Can have big impact on PCB cost
- Small changes in routing can have a large impact on performance
- Component placement is critical
  - Staying within lumped distance
    - Reduces component count
    - Reduces system cost
    - Improves EMC performance
    - Minimize the volume of the power transmission network

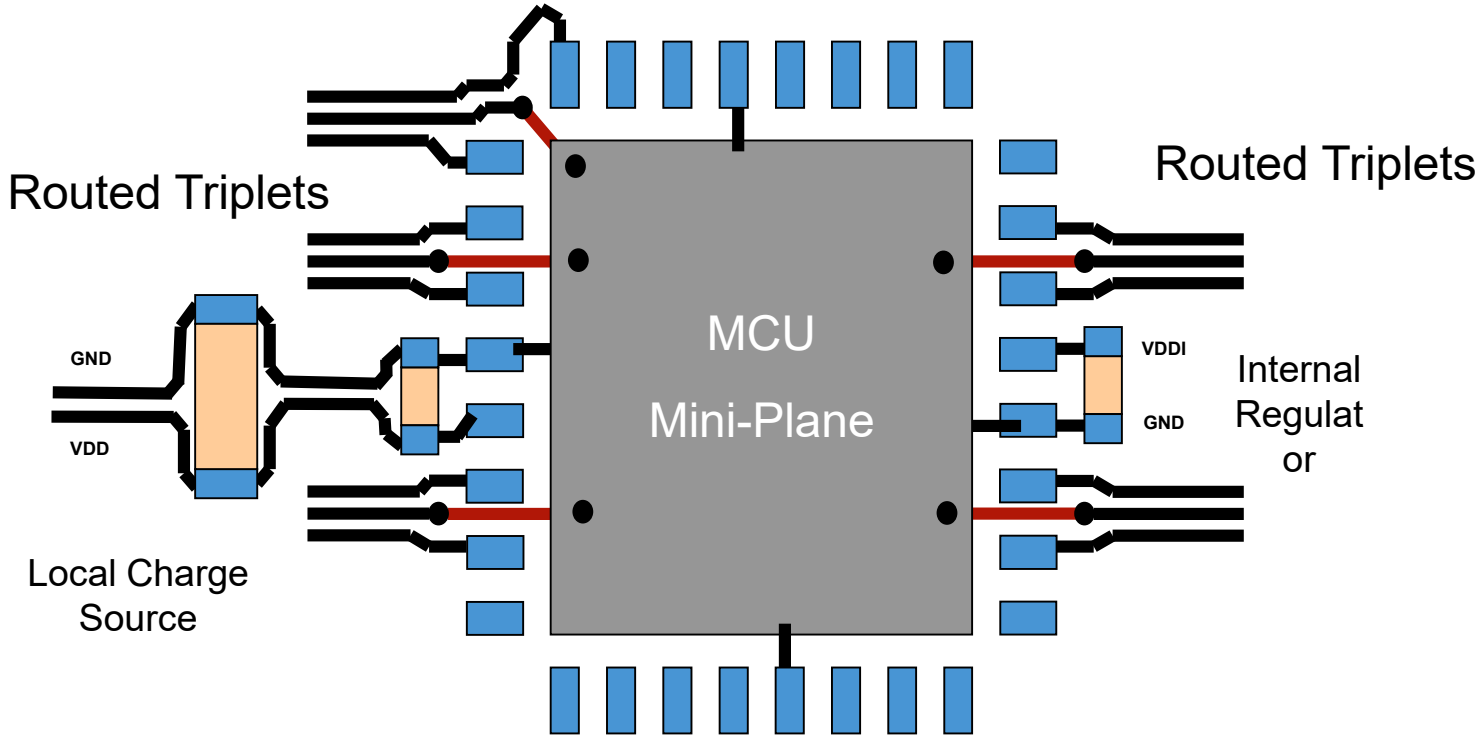
Power Supply Design Made Easy!

PCB power transmission line routing

- Power distribution component placement is critical
  - Supporting fast switches requires close placement
  - You MUST know how fast each device is switching
    - This determines the requirements of the power supply design
- Input storage devices at the connector must be large enough to support the energy needs of the devices connected to them
  - Wiring harnesses are too long to allow energy to be delivered quickly
  - Design each element of the power network to put a steady state demand on the field sources immediately upstream
  - As you get nearer to each switch group, provide progressively smaller structures that are physically closer

Power Supply Design Made Easy!

PCB signal transmission line routing



PCB Layout Considerations

Some New “Rules of Thumb"

PC Board Considerations

Flooding unused areas on the PCB layers with Ground:

- Properly implemented, will improve EMC performance
- Reduce cost by increasing PCB manufacturing yield
  - Less etch required, so less chemical is used
  - Balanced copper improves plating and
- Balanced copper improves final assembly yield
  - Reduced board warping

Remember to stitch the ground islands and planes together

- Minimum of two vias to ground copper above and below in the board stack
  - If this is not possible, try moving traces to allow two vias, or delete the island
- Try to make a pseudo-Faraday cage!

PC Board Considerations

- Use minimum trace widths and spacing for signal transmission lines
  - Refer to PCB fabricator's capabilities without a cost adder
  - Same thing goes for drill sizes and pad rings
- May be defined by either customer or internal requirements
- Wider traces for power supply transmission line pairs
- Provides maximum trace density

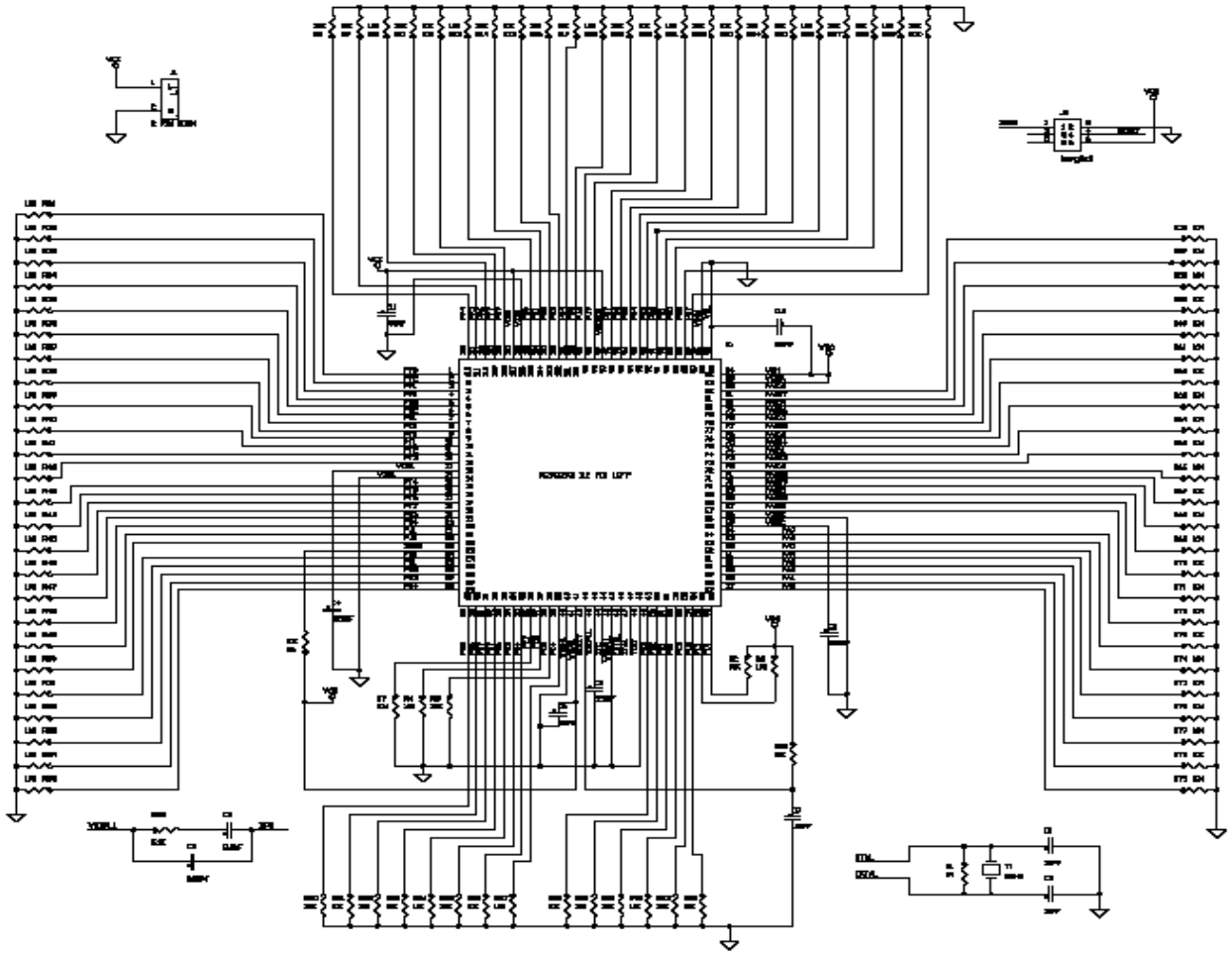
- Make room for all of those ground traces!

Test Results:
Adding Ground Planes

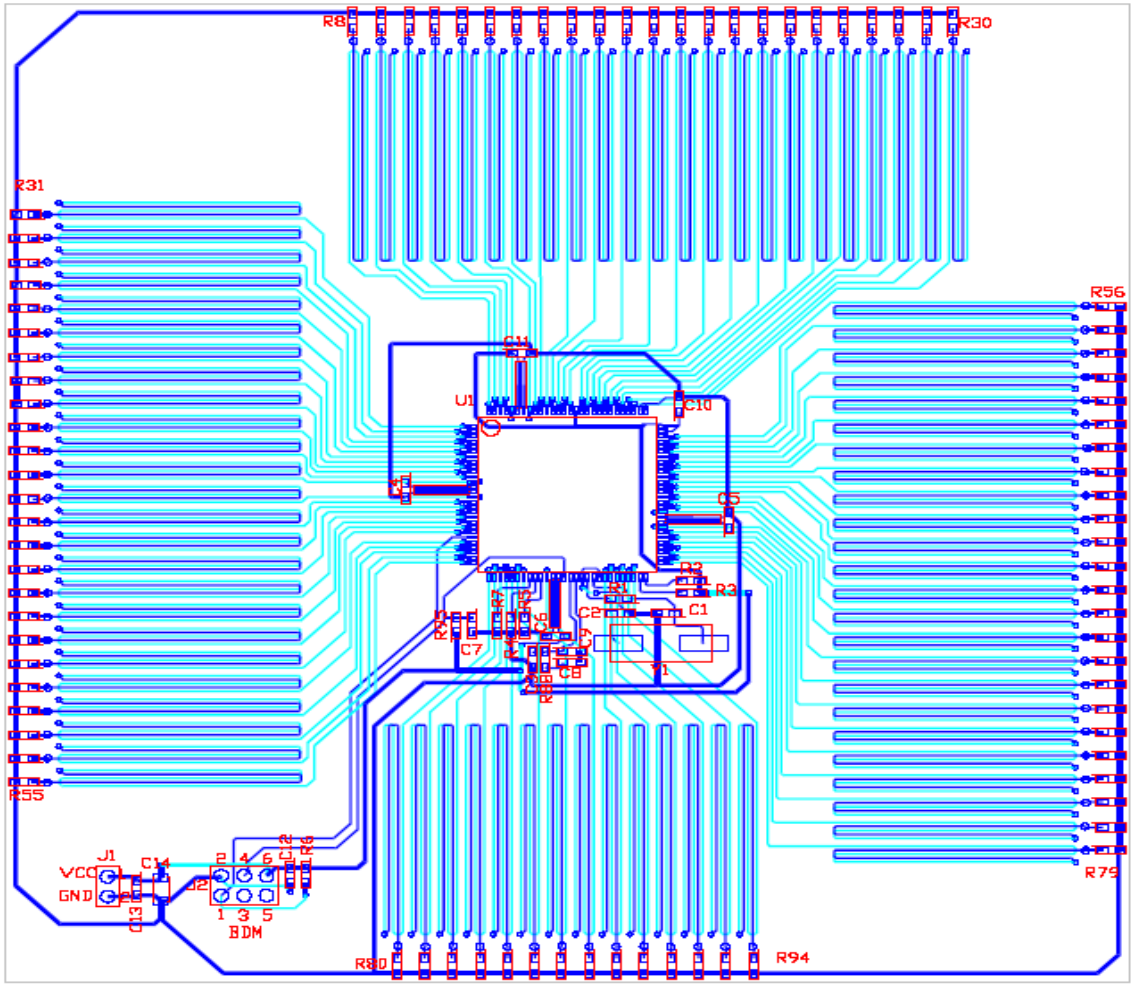
EMC Test Board

- EMC test board with no field control considered
- Two layers
- 112-pin MC9S12XD128 MCU
- All I/O lines routed to 10 K termination resistors using serpentine 6” traces
- All ground connections routed in “convenient” patterns
- Filter components placed “somewhere near”
- Line widths and spacing aimed for low cost FAB
- Software running at 40 MHz, toggling all I/O pins

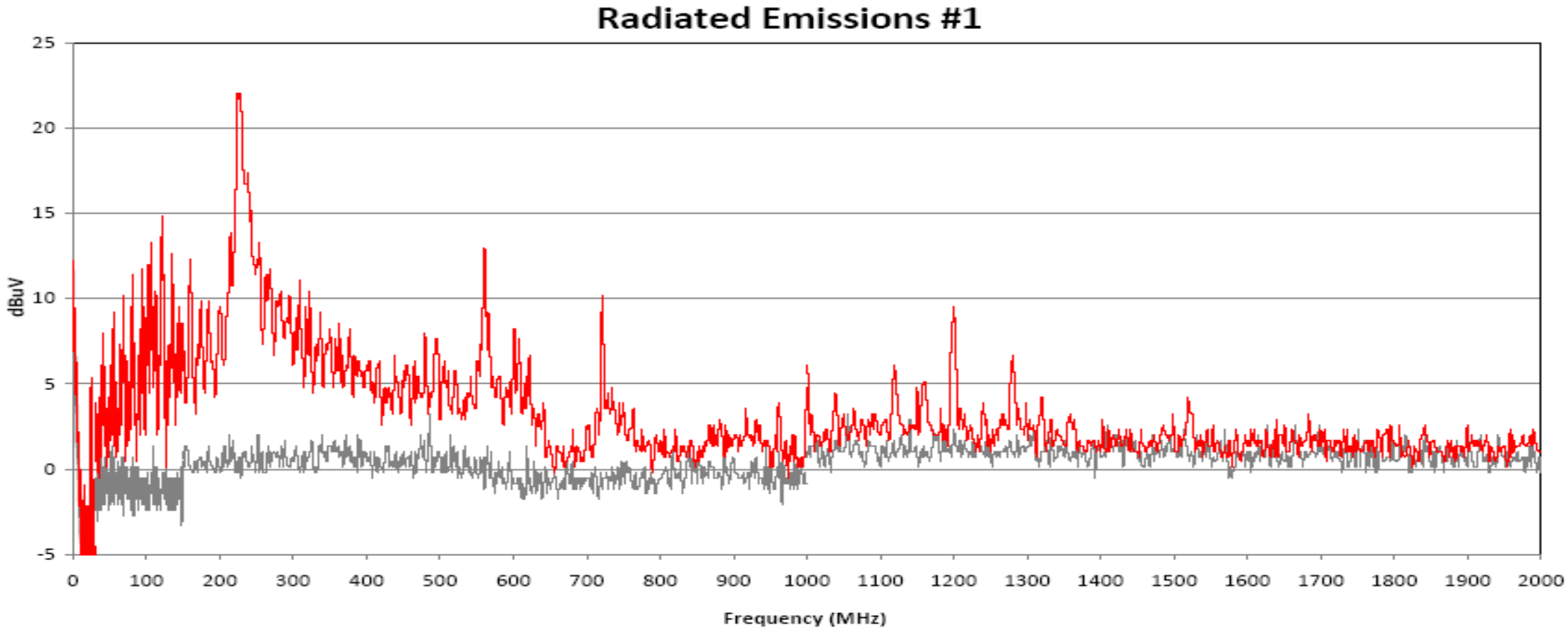
EMC Test Board Schematic



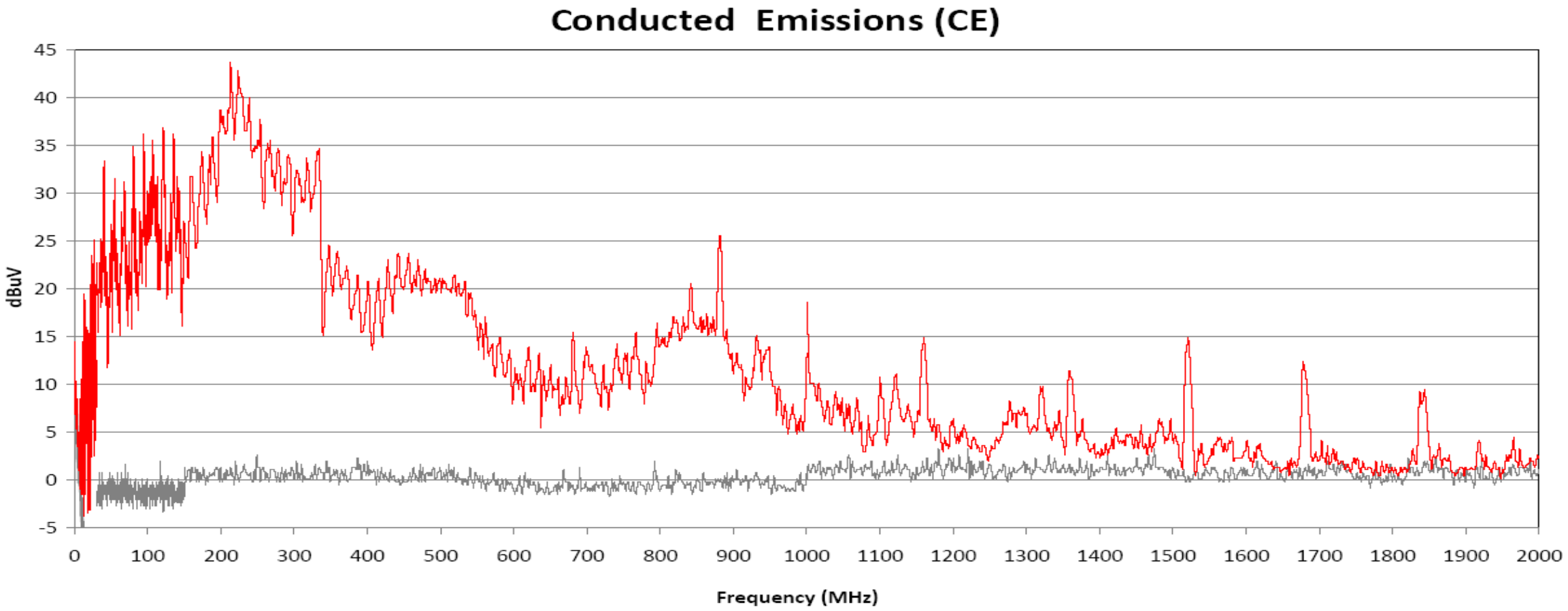
EMC Test Board Layout



Two-layer EMC Test Board Radiated Emissions



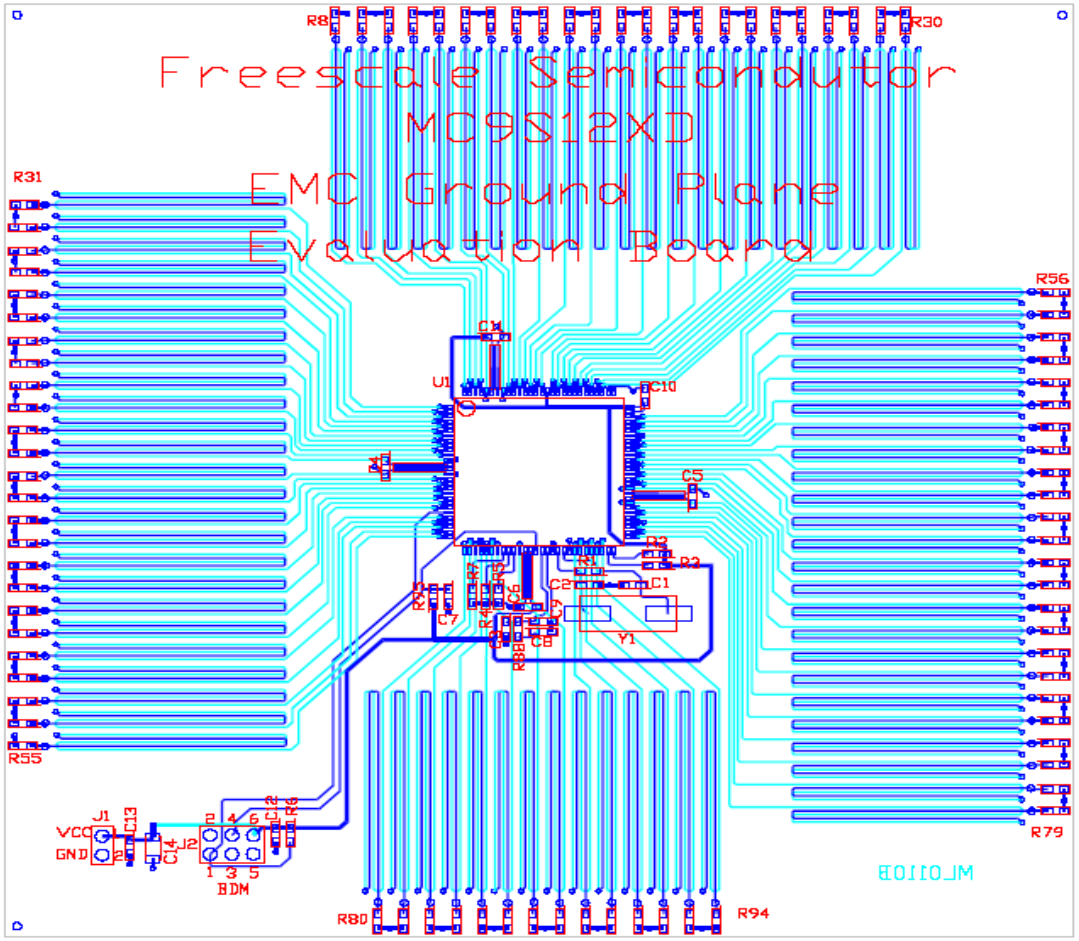
Two-layer EMC Test Board Conducted Emissions



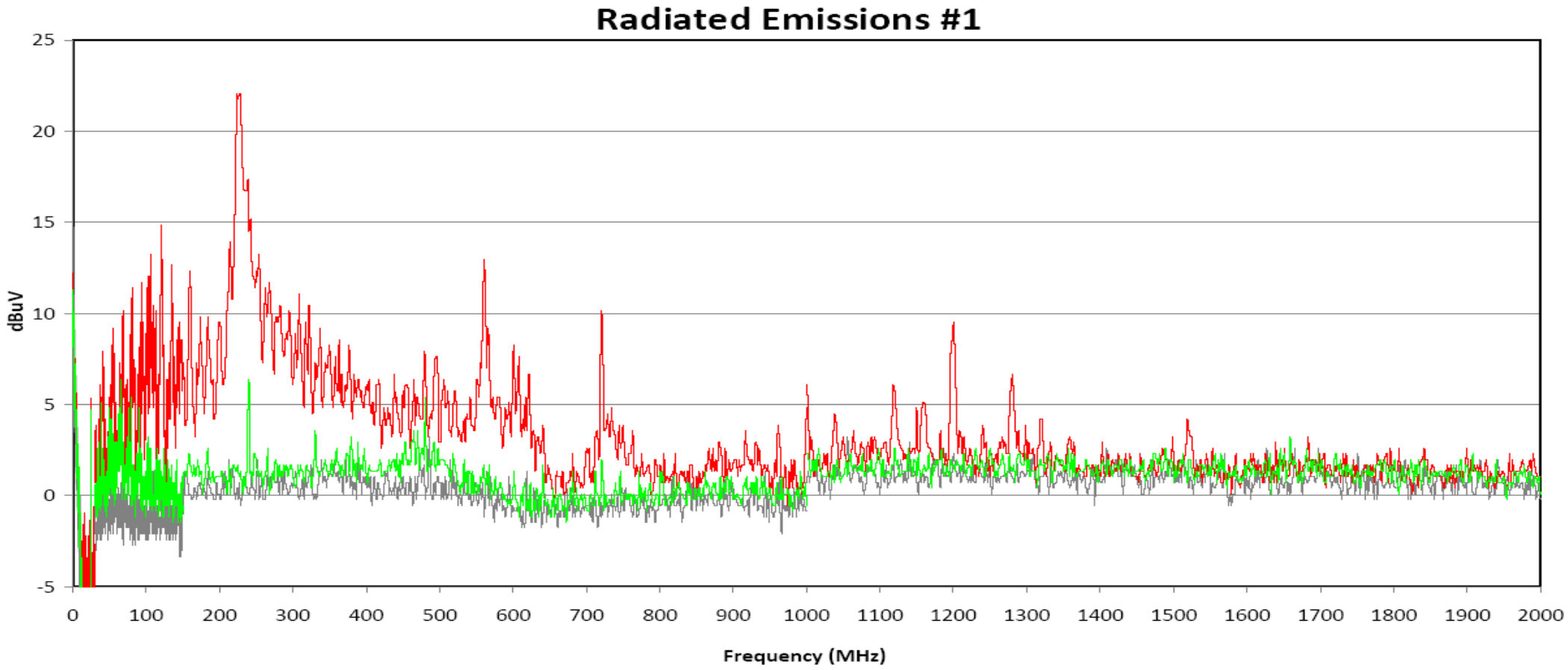
EMC Test Board, Rev 2

- EMC test board with tight field control considered
- Same schematic
- Four layers
- Core inserted with dedicated ground planes
- Outer layers exactly the same as 2 layer
- All ground connections made with via to ground planes
- Line widths and spacing aimed for low-cost FAB
- Same software

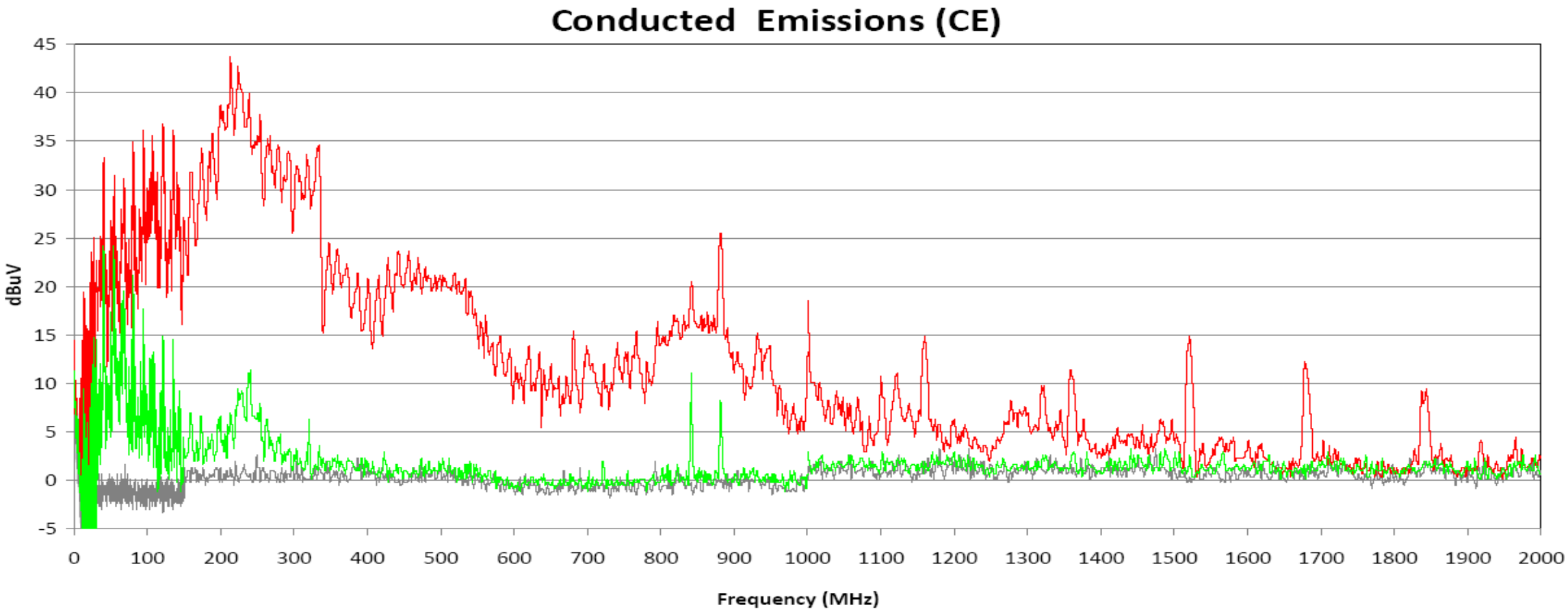
EMC Test Board Layout, Rev 2



2 vs. 4-layer EMC Test Board Radiated Emissions



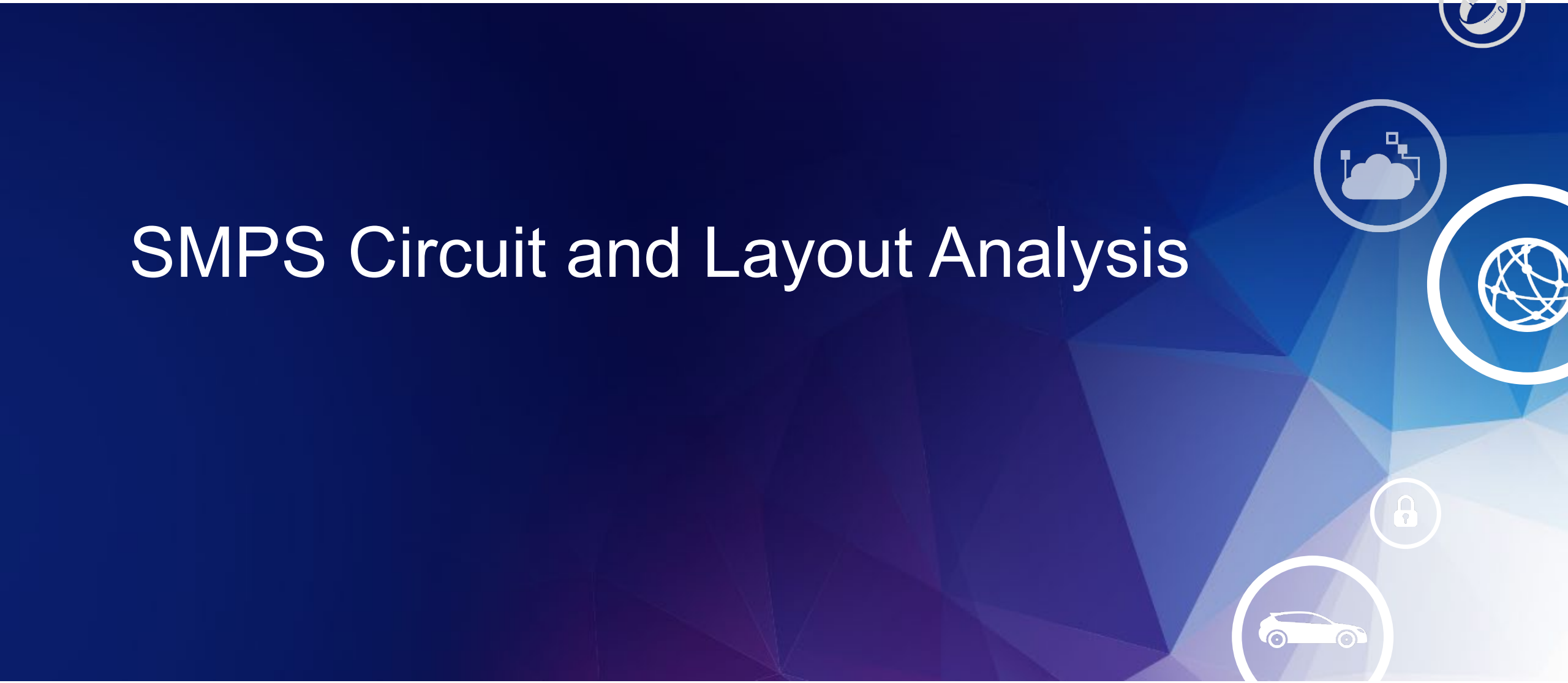
2 vs. 4-layer EMC Test Board Conducted Emissions



2 vs. 4-layer EMC Test Board Results

WOW! What would you do for 30 db?

SMPS Circuit and Layout Analysis



UJA1132 EMC Test Process

- Baseline design using NXP application notes and evaluation board design
- Conducted and Radiated Emissions tested at outside test lab
- Test environment and hardware constant
  - 1.9 M wiring harness connecting to 12 Volt 18 AH Battery

- Test various component choices and PCB layout versions
  - Single change for each version of the assembly
  - Measure Radiated and Conducted emissions for each version of the assembly
- Testing to be done at the same testing facility with the same setup for each board variation
- Compare test results to evaluate the EMC impact of component and layout changes
- Compare results with comparable devices which do not specify input inductors for EMC improvement
- Develop optimum component mix and layout for most cost effective implementation
  - Identify EMC performance and system cost impact resulting from each design version

UJA1132 EMC Test Environment

UJA1132 EMC Test Equipment RE

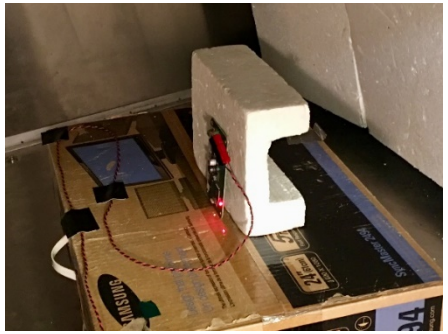
- Baseline design using NXP application notes and evaluation board design
- Conducted and Radiated Emissions tested at outside test lab
- Test environment and hardware constant
  - 1.9 M wiring harness connecting to 12 Volt 18 AH Battery

- Radiated Emission 150 KHz – 30 MHz (non-Standard Test)
  - EMCO 5311 GTEM
  - 1 Position corresponding to “y” above
  - HP 8546A Spectrum Analyzer (PA On, Attn.= 0 dB, BW 10 KHz)

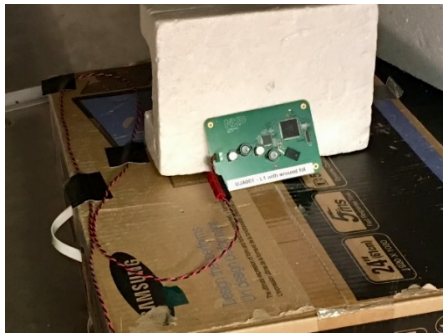
- Radiated Emission 30-1000 MHz (Standard Test)
  - EMCO 5311 GTEM
  - 3 Axis Correlation X, Y, Z
  - Mitec 40 dB Gain Preamplifier
  - HP E4407B Spectrum Analyzer
  - 100 KHz BW; Attenuator = 10 dB

X Axis

Y Axis

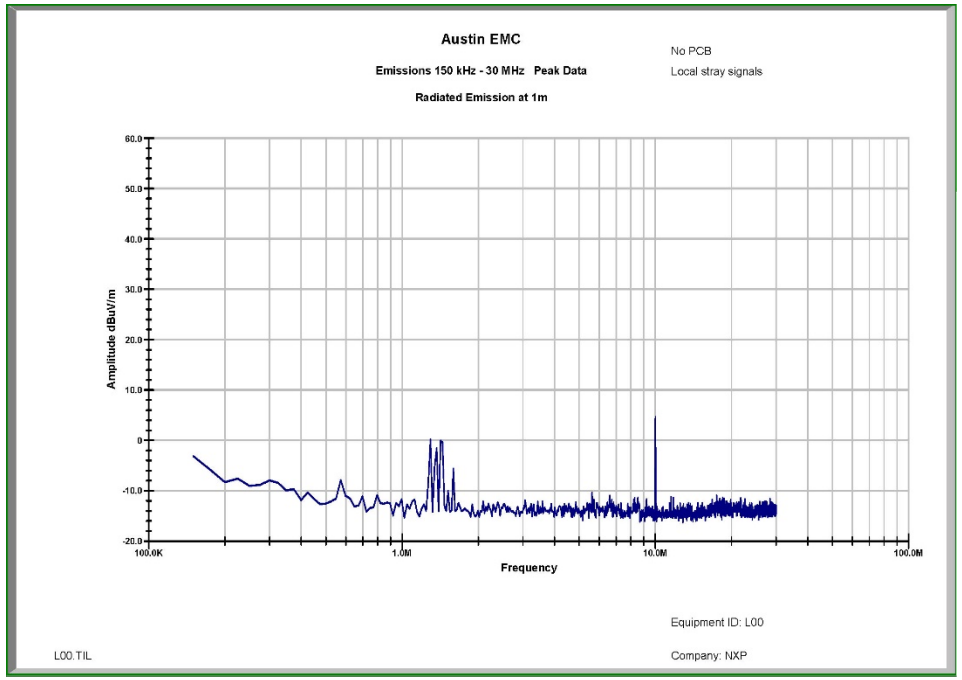


Z Axis

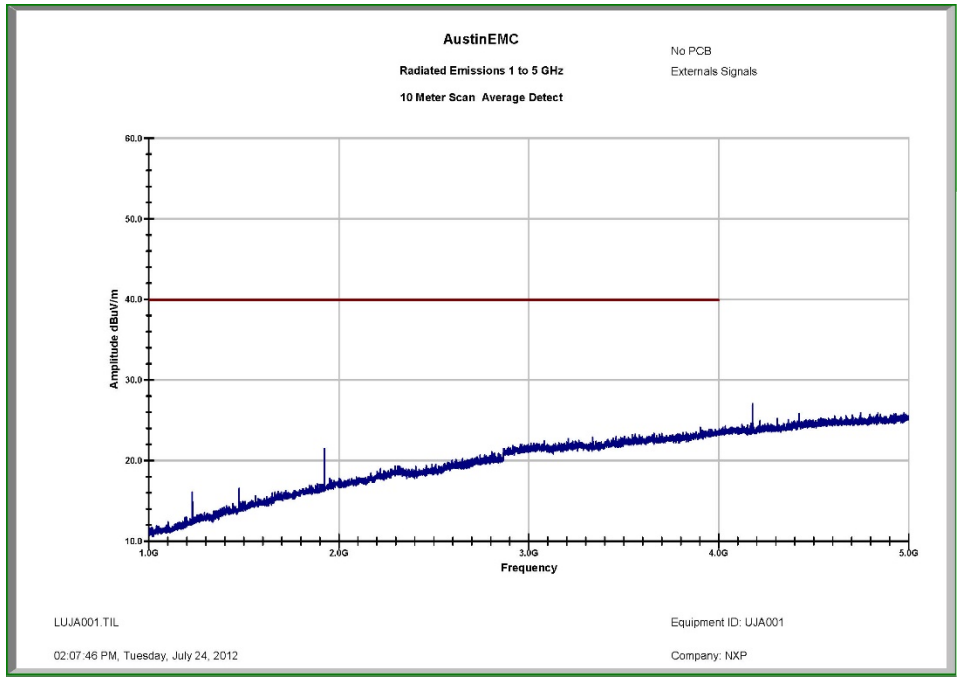


UJA1132 EMC Test Equipment RE

Chamber Low band RE ambient



Chamber Upper band RE ambient

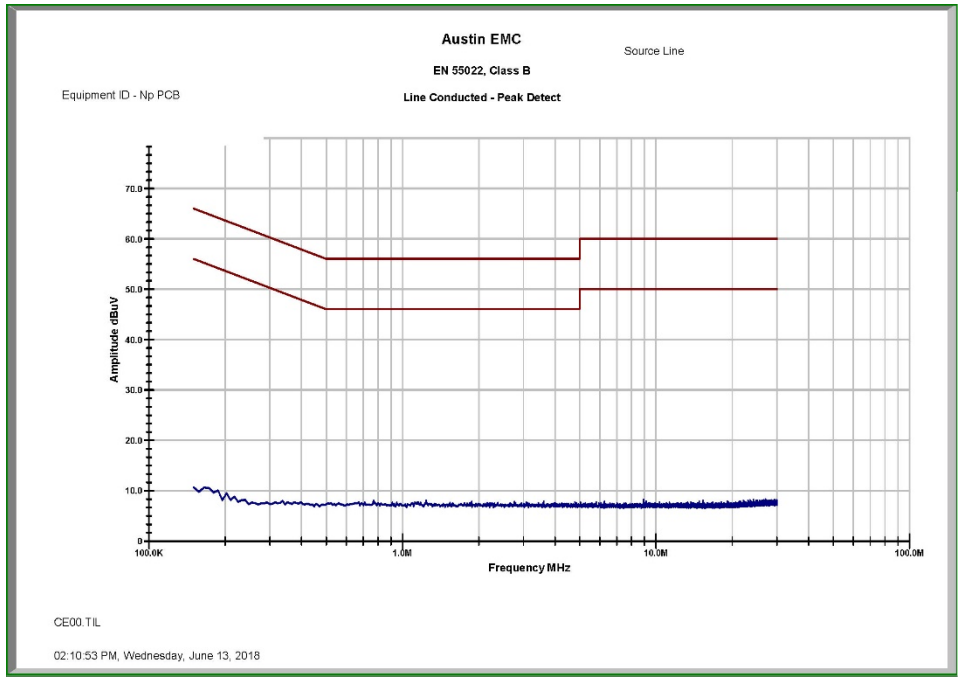


UJA1132 EMC Test Equipment CE

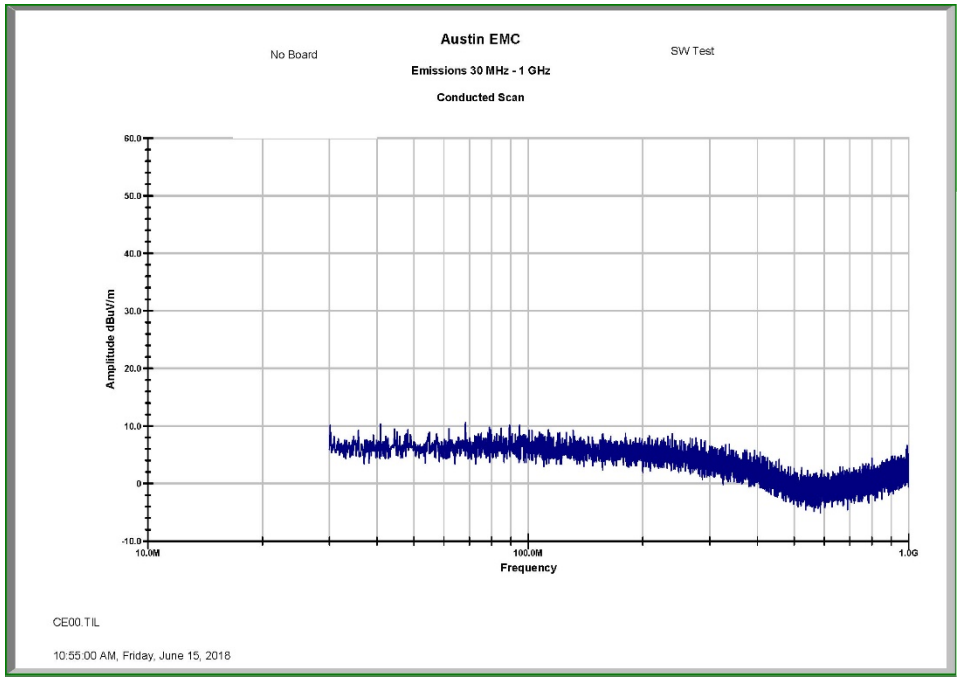
- Baseline design using NXP application notes and evaluation board design
- Conducted and Radiated Emissions tested at outside test lab
- Test environment and hardware constant
  - 1.9 M wiring harness connecting to 12 Volt 18 AH Battery
- Conducted Emission 150 kHz – 30 MHz (Standard Test)
  - Panashield Shielded Chamber 8’ X 10’ X 8.5’ H
  - Solar LISN 8012-50-R 24BNC (50 uH, 24 Amp)
  - HP 8546A Spectrum Analyzer (PA off, Attn.=10 dB, BW 10 KHz)
- Conducted Emission 30-MHz – 1000 MHz (non-Standard Test)
  - EMCO 5311 GTEM
  - Solar LISN 7225-1 (2 KHZ – 1 GHz, 10 Amps)
  - HP 8546A Spectrum Analyzer (PA On, BW 100 KHz, ATTN.=10 dB)

UJA1132 EMC Test Equipment CE

Chamber Low band CE ambient



Chamber Upper band CE ambient

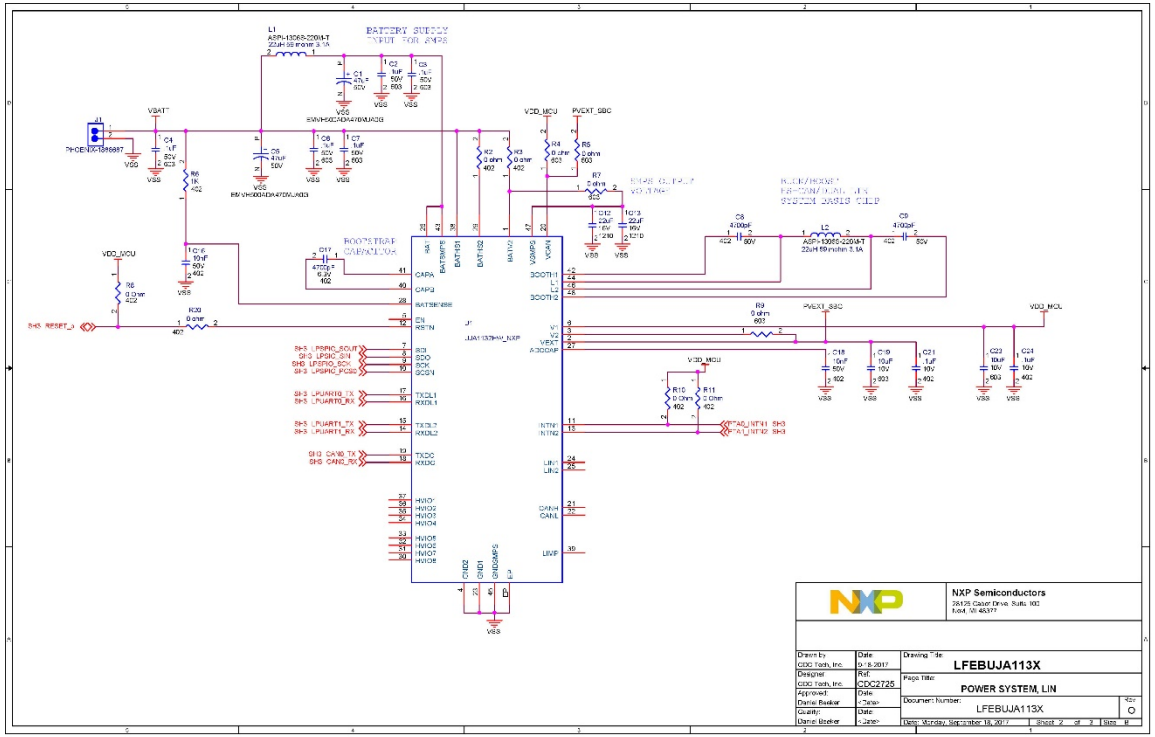


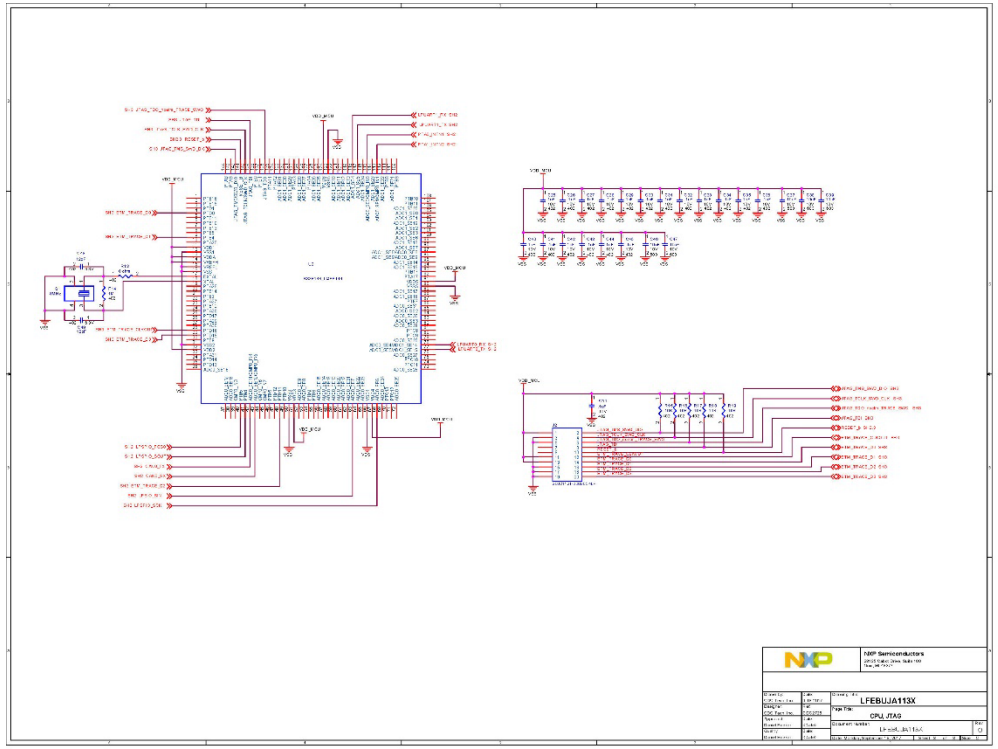
EMC Data for Baseline

Baseline design using PCB rev O

UJA1132 EMC Test Platform

- Baseline Design, PCB rev O schematic
- UJA1132HW SBC, PS32K148UAT0VLQT MCU with ETM debug interface
- Input EMC filter with two 47 µF Electrolytic capacitors and 22uH inductor

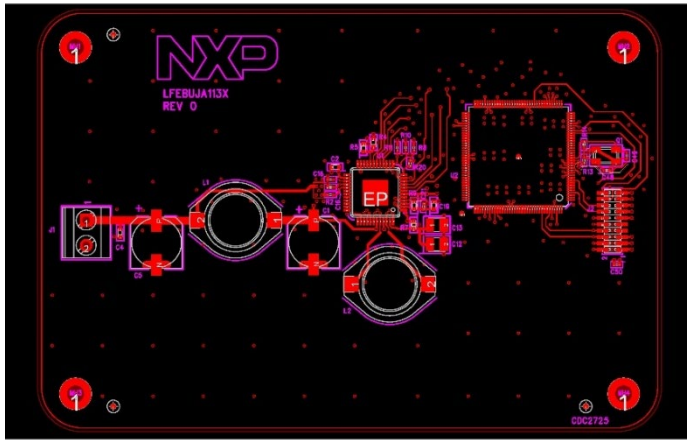




UJA1132 EMC Test Platform

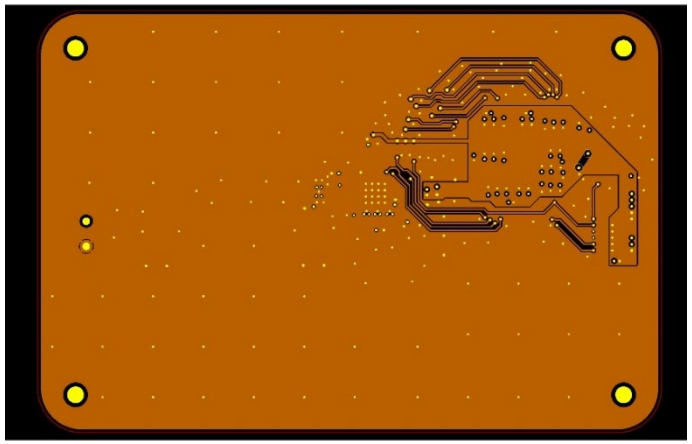
Baseline Design, PCB rev O PCB Layout

L1

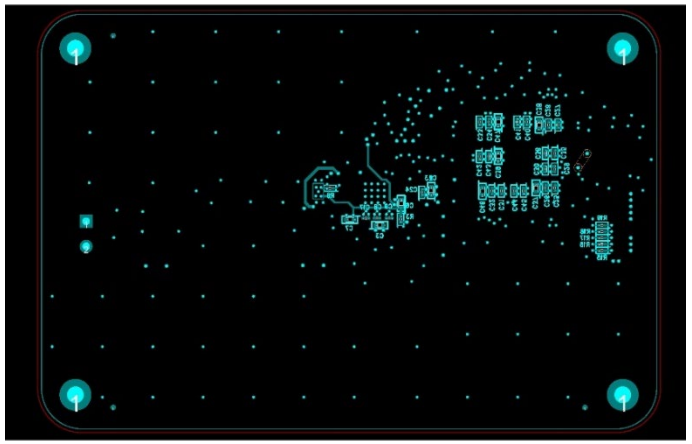


L3

L2



L4

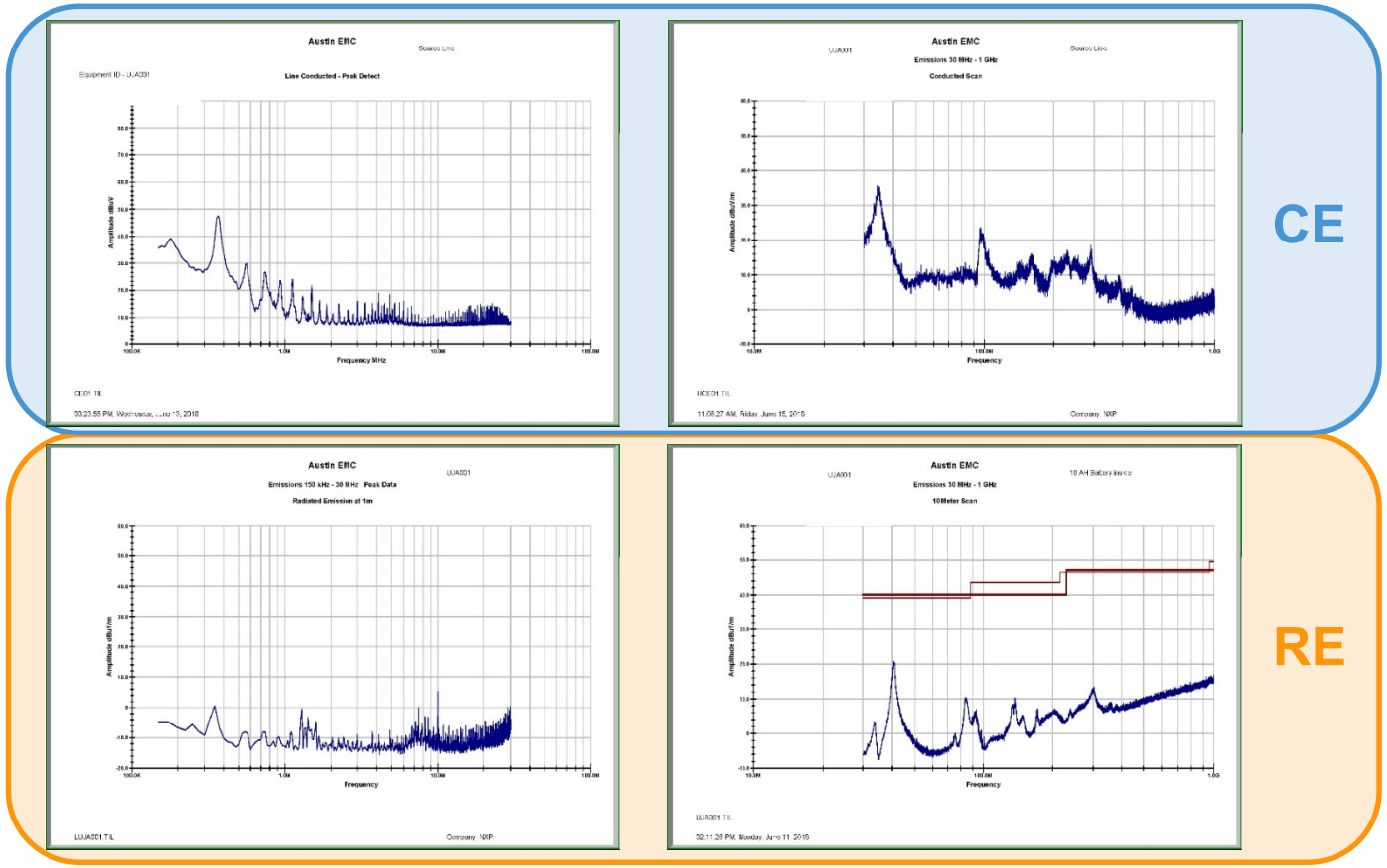


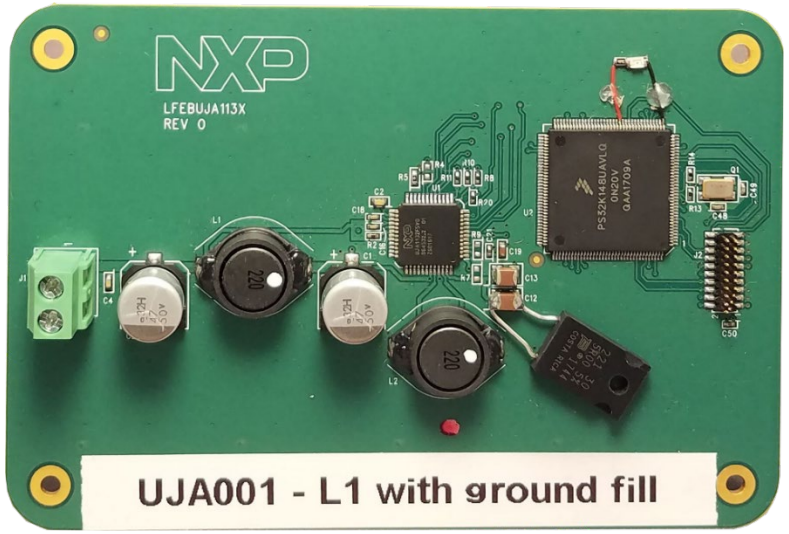
- Four layer PCB, Arduino Form factor
  - L1: Components, routing and ground flood
  - L2: Ground plane
  - L3: Power island, routing and ground flood
  - L4: Components, routing and ground flood
- VBATT using single dielectric between L1 trace and L2 ground plane
- Ground flood under discrete components where possible
- Extra components added to assembly:
  - 500 mA static load resistor
  - LED “MCU running” indicator

UJA1132 EMC Test Results

- Baseline Design, PCB rev O
- CE and RE peaks at 35 and 40 MHz

CE and RE peaks at PWM frequency, 375 KHz



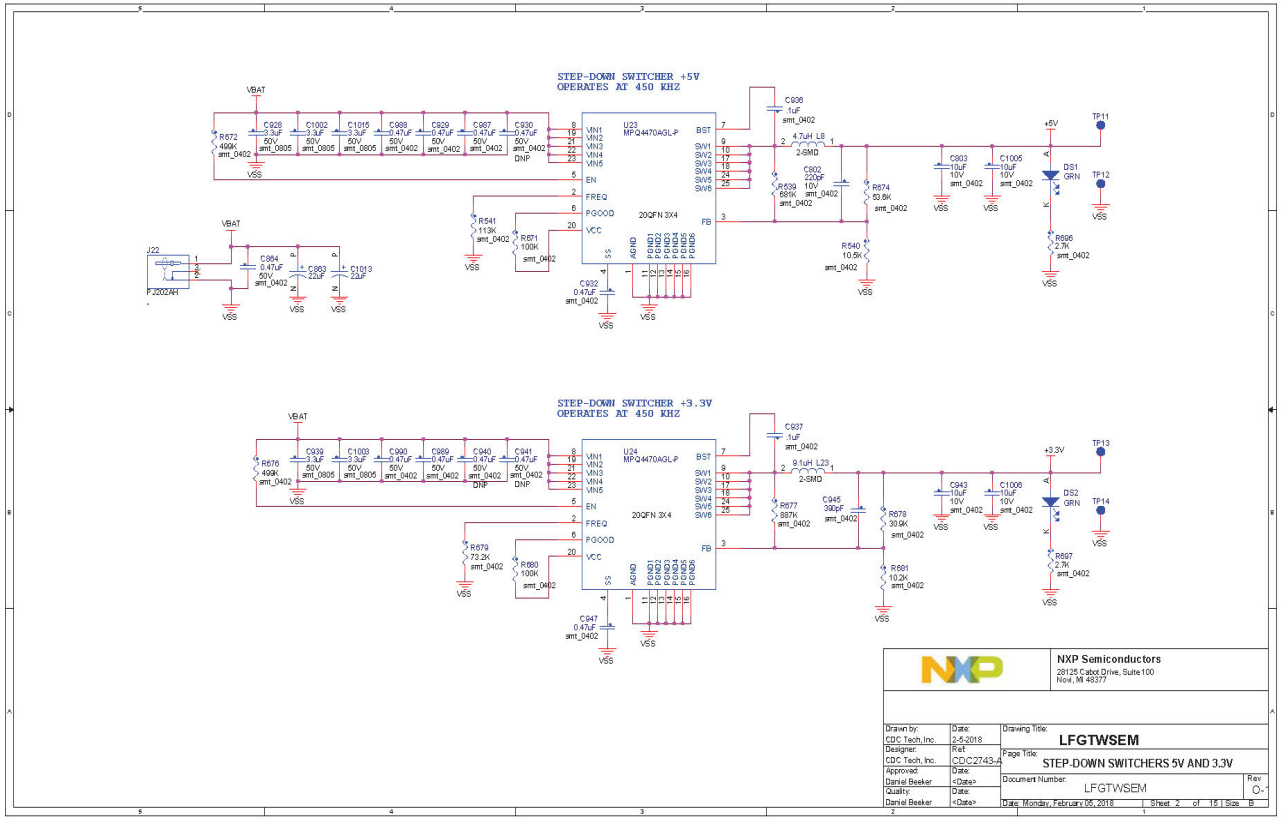


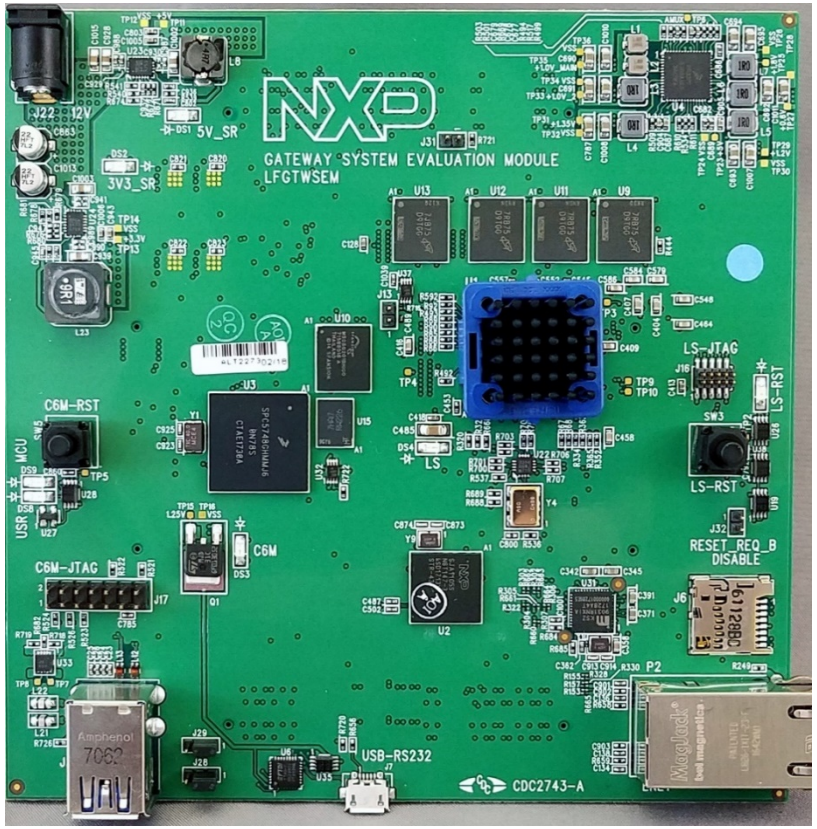
EMC Behavior vs Competitor ICs

Baseline design compared to assemblies with TI and MPS SMPS devices

LFGTWSEM Dual Chip Network Controller

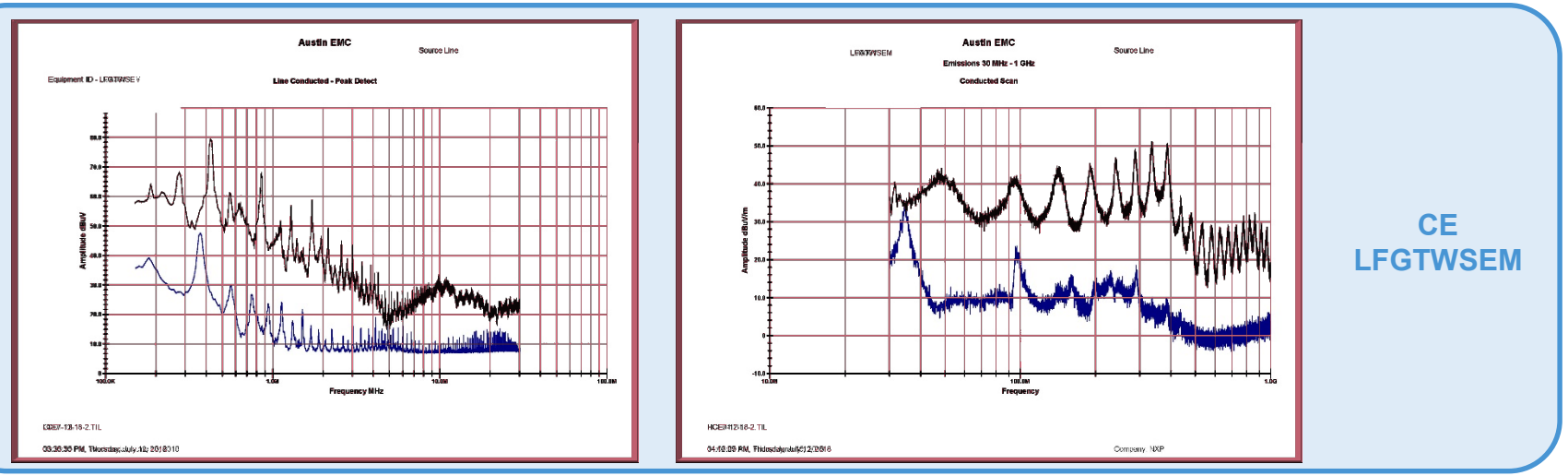
- Two Monolithic Power MPQ4470AGL-P SMPS, no input inductor
- LS1043AXE7QQB MPU @1 GHz, SJA1105SEL ethernet switch, SPC5748GHK0AMMJ6 MCU ethernet controller
- PC33PF8200A0ES PMIC, 4 GB DDR4, 18 layer PCB, 6 ground planes



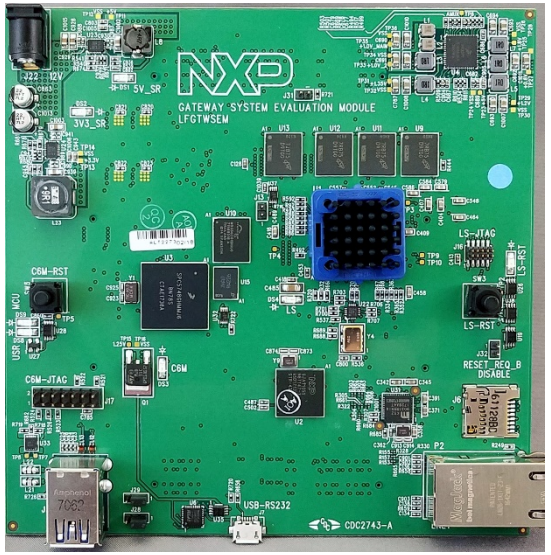


UJA1132 EMC Test Results

- Baseline Design, PCB rev O (in **BLUE**), LFGTWSEM (in **BLACK**) CE testing only
- LFGTWSEM 30 dBµV higher at switching frequency



CE
LFGTWSEM

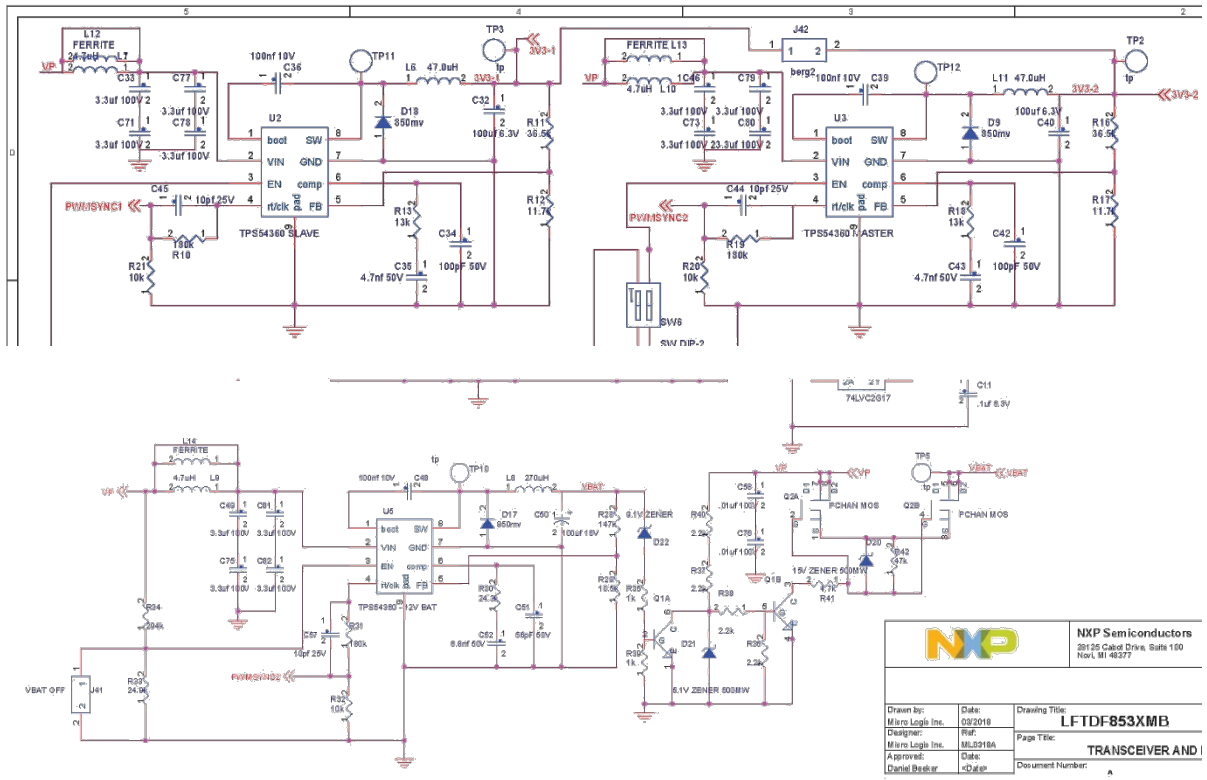


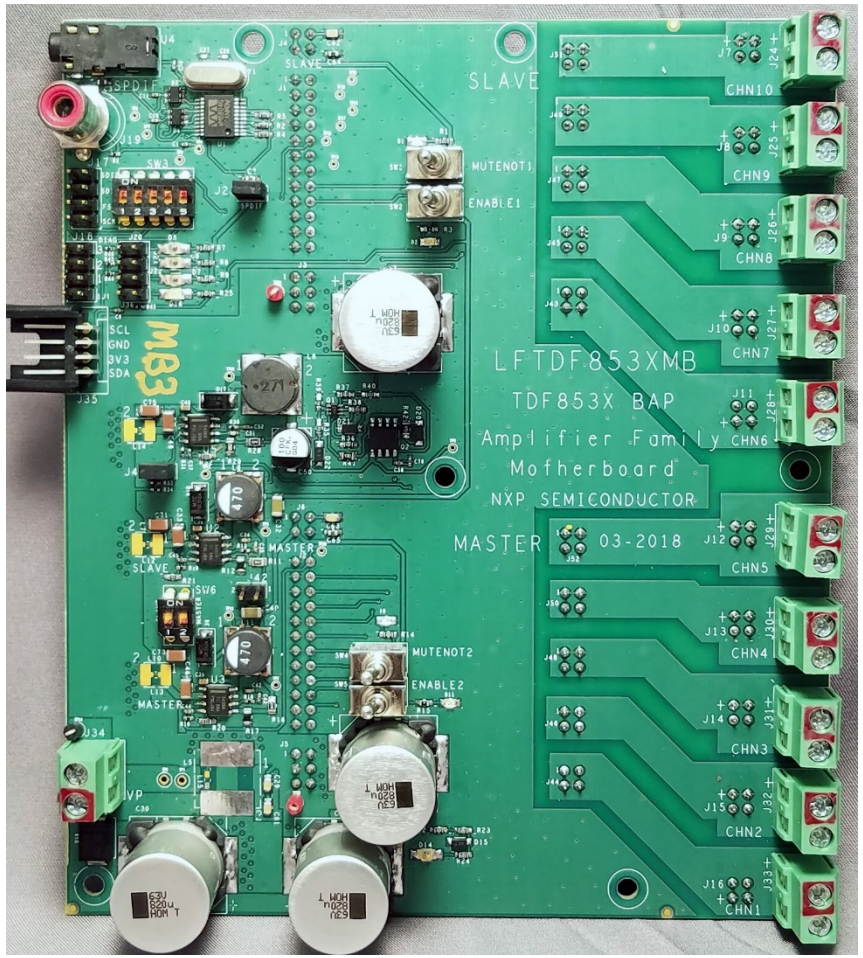
- Baseline Design, PCB rev O (in **BLUE**), LFGTWSEM (in **BLACK**)
- **LFGTWSEM certified for FCC CE and EU commercial sale**
- LFGTWSEM is 35 dBµV higher at the switching frequency of the PWM.
- LFGTWSEM is 30-40 dBµV higher over most of the upper band

LFTDF853XMB Digital Audio Motherboard

- Three Texas Instruments TPS54360 SMPS
- Four layer PCB, one ground plane

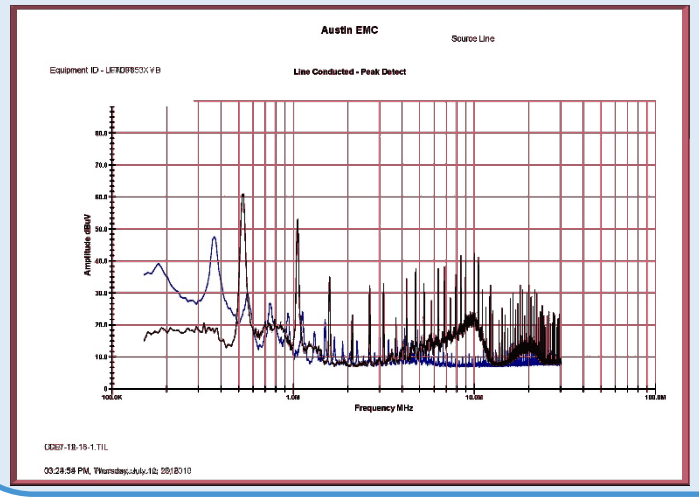
Input ferrites and inductors not populated

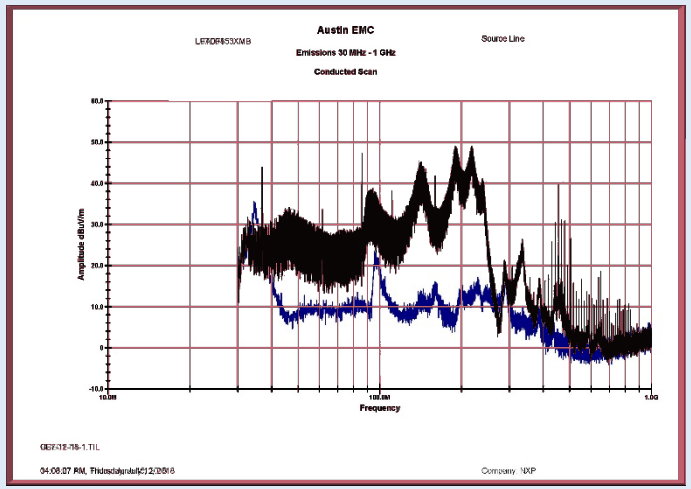




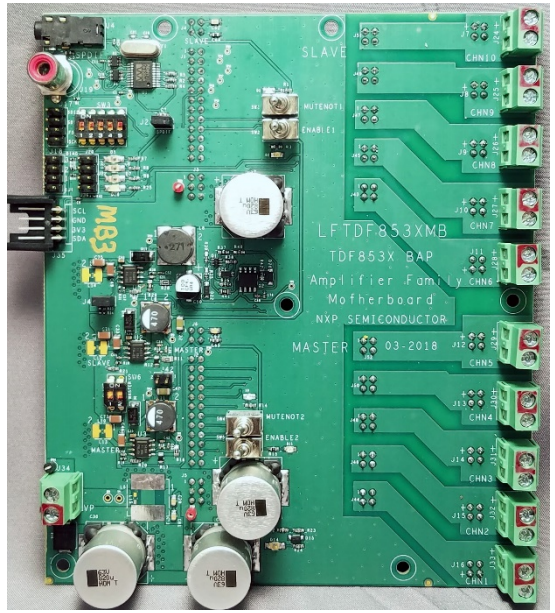
UJA1132 EMC Test Results

- Baseline Design, PCB rev O (in **BLUE**), LFTDF853XMB (in **BLACK**) CE testing only
- LFTDF853XMB 12 dBµV higher at switching frequency





CE
LFTDF853XMB



- Baseline Design, PCB rev O (in **BLUE**), LFTDF853XMB (in **BLACK**)
- LFTDF853XMB not yet certified for FCC CE and EU commercial sale
- LFTDF853XMB is 12 dBµV higher at the switching frequency of the PWM.
- LFTDF853XMB is 30 dBµV higher over most of the upper band

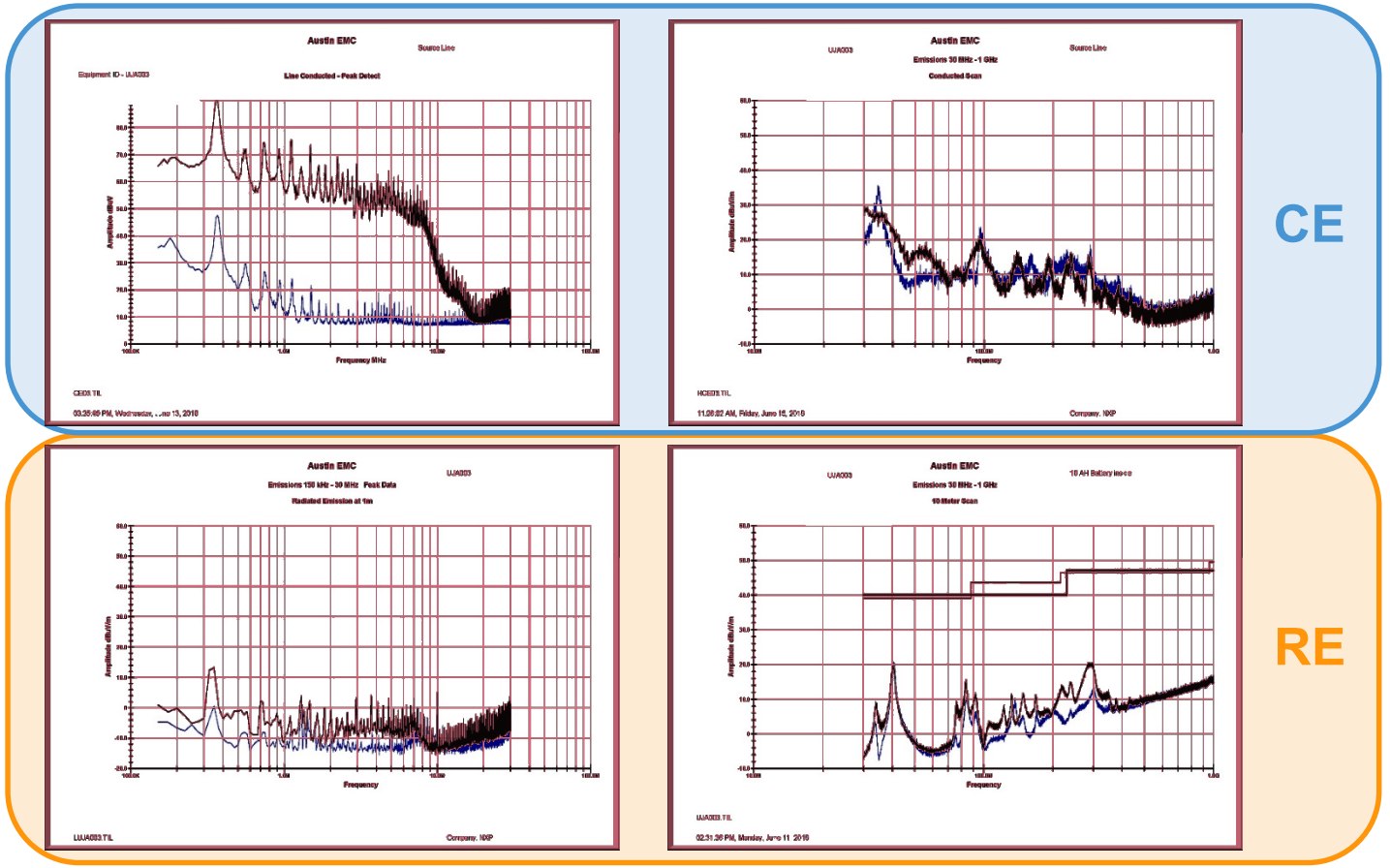
EMC Comparisons to Baseline

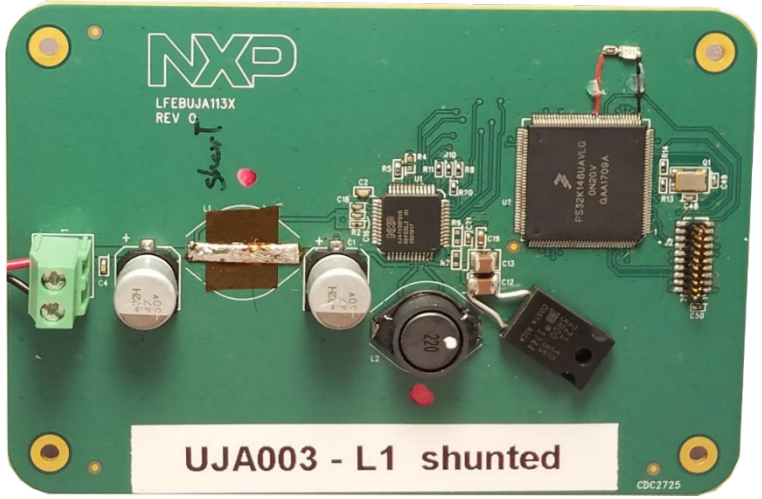
Baseline design compared to each successive revision of components using PCB

Rev O

UJA1132 EMC Test Results

- Baseline Design, Version 1 (in **BLUE**), Version 3 (in **BLACK**)
- Change from Version 2: L1 shunted
- CE 43 dBµV higher than baseline at ~375 KHz





Baseline Design, Version 1 vs Version 3

- Ground fill under L1 and L2 removed, L1 shunted

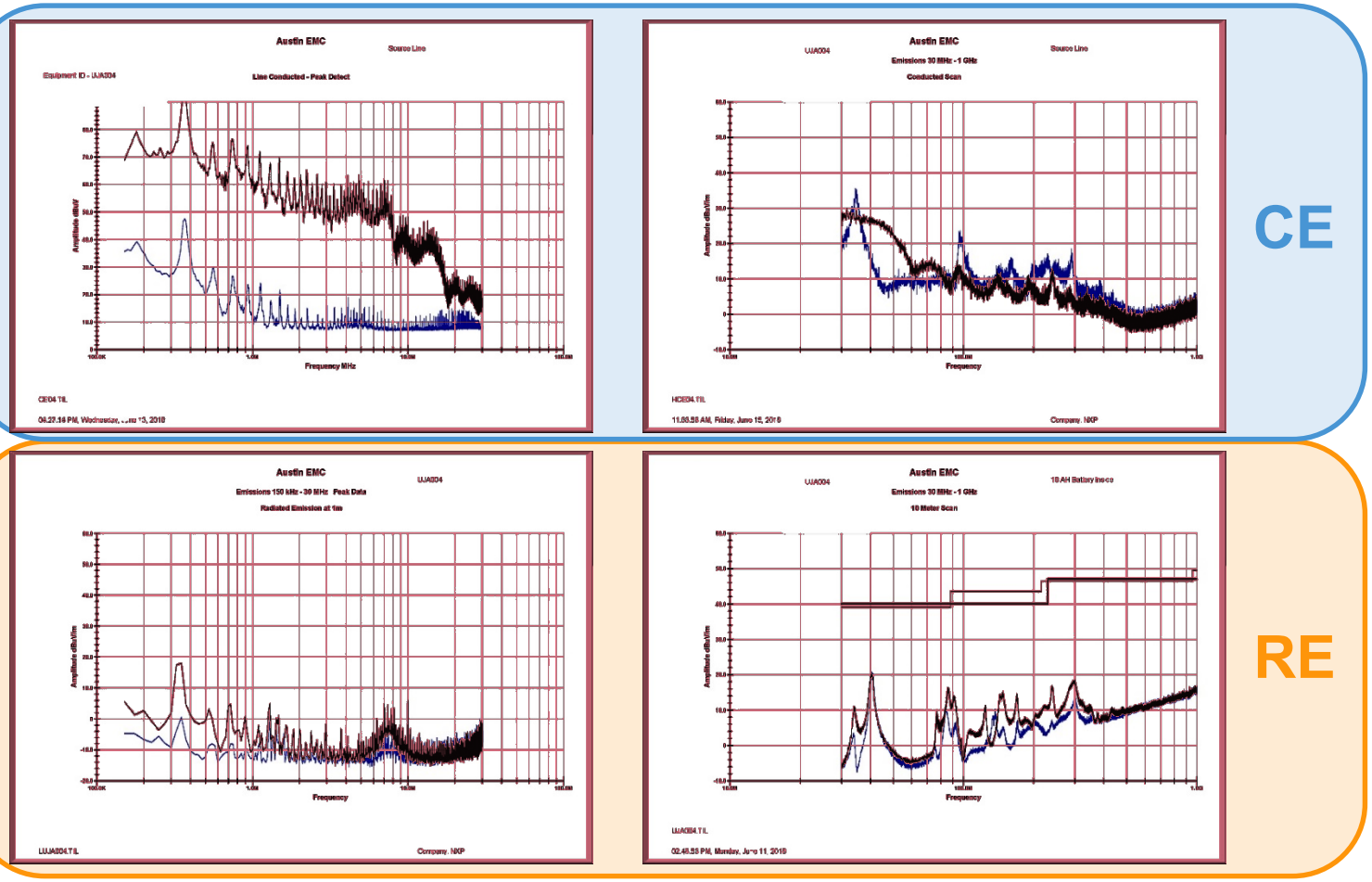
- **CE significantly higher with L1 shunted**
  - 43 dBµV at PWM switching frequency, ~375 KHz to around 8 MHz
  - CE significantly higher across the lower band
- RE 12 dBµV higher at PWM switching frequency, ~375 KHz
- **CE at upper band, and RE both bands very slight overall change**
  - CE peak at 35 MHz actually reduced by around 10 dBµV

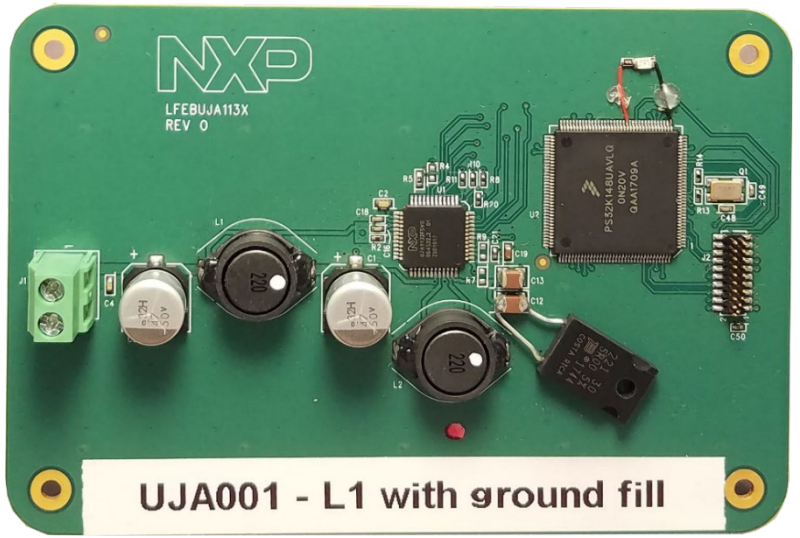
- Analysis:
  - Shunting the inductor location reduced the discontinuity in the energy flow from the power connector to the SMPS input
  - This improved the movement of the EM fields, and resulted in an increase in current flow on the wiring harness when the switch turns on
  - The increase in CE falls off significantly by ~8 MHz

- Cost delta vs Baseline: - $ 0.68

UJA1132 EMC Test Results

- Baseline Design, Version 1 (in **BLUE**), Version 4 (in **BLACK**)
- Change from Version 3: C5 removed
- CE 40 dBµV and RE 18 dBµV higher than baseline at ~375 KHz





Baseline Design, Version 1 vs Version 4

- Ground fill under L1 and L2 removed, L1 shunted, C5 removed

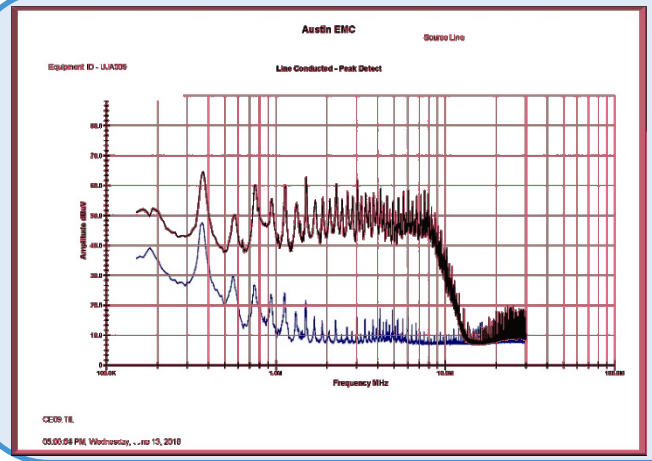
- **CE higher with C5 removed**
  - 45 dBµV at PWM switching frequency, ~375 KHz through 8 MHz
  - CE significantly higher across the lower band
- RE 18 dBµV higher at PWM switching frequency, ~375 KHz
- **CE at upper band, and RE both bands slightly higher**
  - CE peak at 35 MHz actually reduced by around 8 dBµV and 10 dBµV at 160 MHz

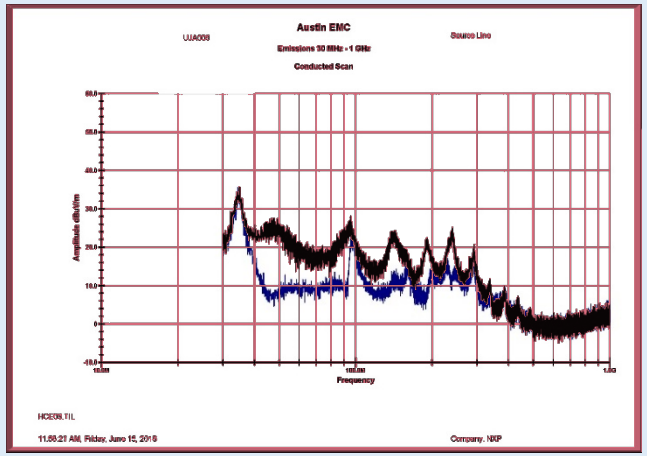
- Analysis:
  - Removing C5 near the power conductor reduces the overall energy storage by around 50%
  - This reduced the amount of field available on the board, increasing the demand from the battery
  - The CE falloff is less significant at ~8 MHz than in version 3

- Cost delta vs Baseline: - $ 0.99

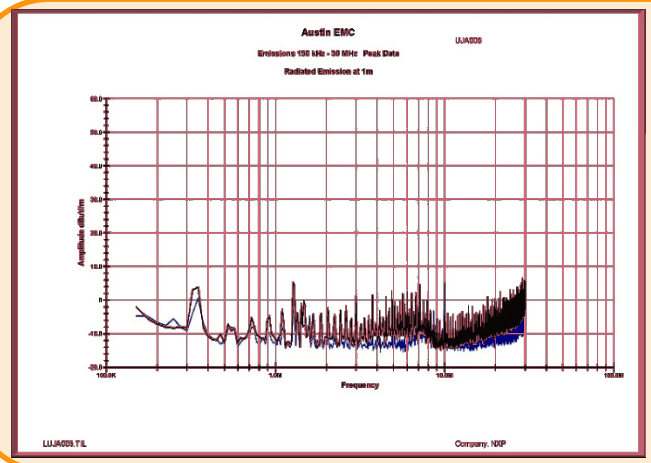
UJA1132 EMC Test Results

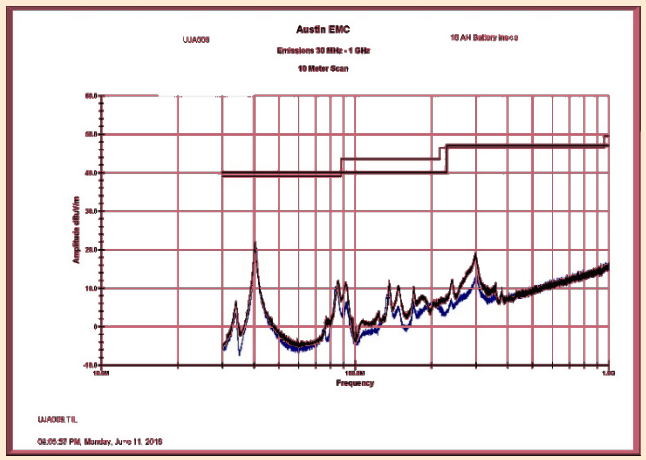
- Baseline Design, Version 1 (in **BLUE**), Version 9 (in **BLACK**)
- Change from Version 3: C1 replaced with parallel 47 µF ceramic caps (2 parts, 94 µF effective)
- CE 15 dBµV higher and RE 5 dBµV higher than baseline at ~375 KHz



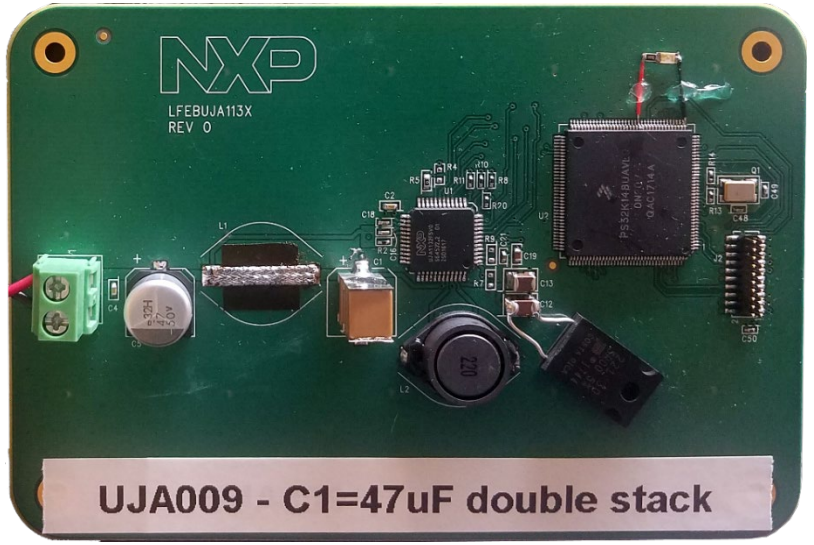


CE





RE



Baseline Design, Version 1 vs Version 9

- Ground fill under L1 and L2 removed, L1 shunted, C1 replaced with two series 47 µF ceramic caps (2 parts, dual device J-lead package, KTJ500B476M76BFT00, 24 µF effective)

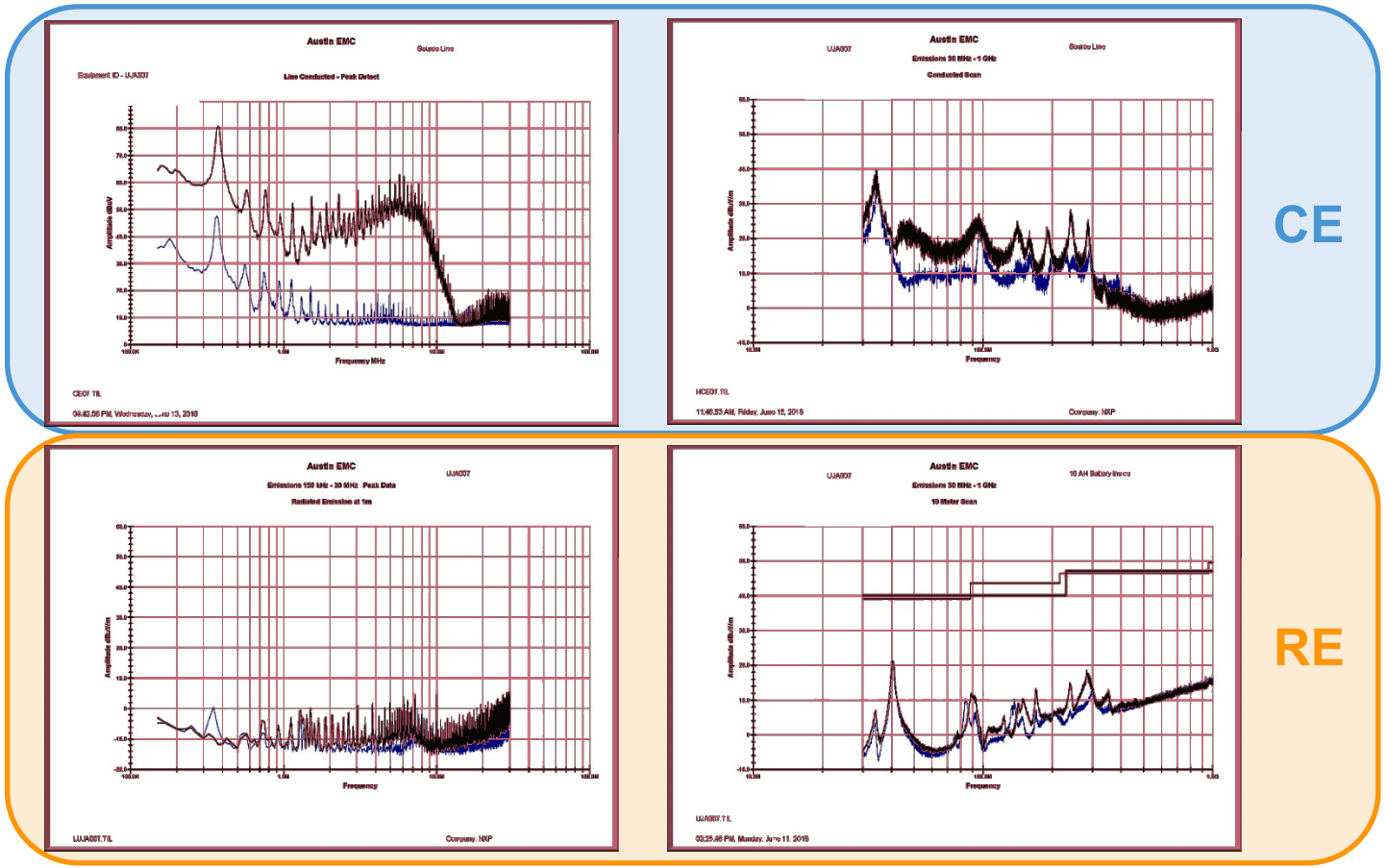
- **CE slightly higher with C1 replaced with ceramic capacitors**
  - Dual device J-lead package, KTJ500B476M76BFT00
  - Around 15 dBµV at PWM switching frequency, ~375 KHz through 8 MHz
  - CE significantly higher across the lower band
- RE 5 dBµV higher at PWM switching frequency, ~375 KHz
- CE 15 dBµV higher 40-100 MHz
  - CE peak at ~375 KHz increased by around 8 dBµV

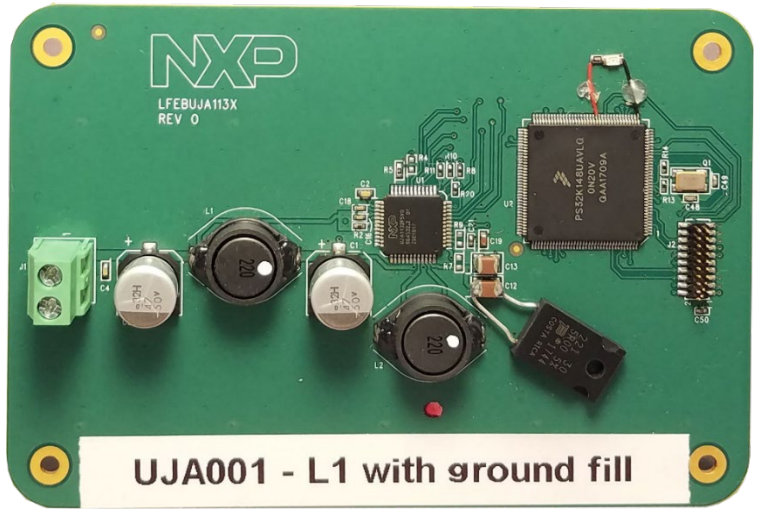
- Analysis:
  - Replacing C1 with two series sets of ceramic capacitors reduced the total capacitance on the board by around 23 µF
    - This reduced the amount of field available on the board, increasing the demand from the battery
    - Changing C1 to a ceramic reduced the ESR of the capacitor from 0.5 to <0.01. This increases the amount of energy available for each wave cycle.
  - The CE falloff is slightly more significant at ~10 MHz than in version 5

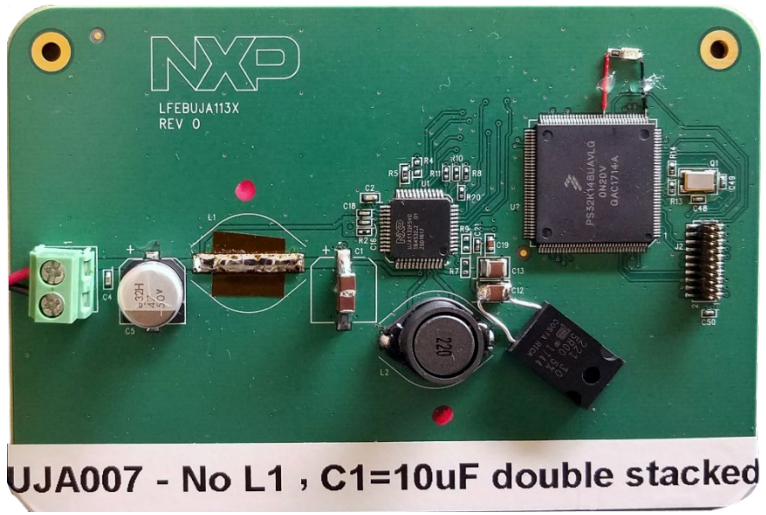
- Cost delta vs Baseline: + $ 5.48

UJA1132 EMC Test Results

- Baseline Design, Version 1 (in **BLUE**), Version 7 (version 6 was damaged) (in **BLACK**)
- Change from Version 3: C1 replaced with two series 10 µF ceramic caps (4 parts, 10 µF effective)
- CE 32 dBµV higher and RE 8 dBµV lower than baseline at ~375 KHz







Baseline Design, Version 1 vs Version 7

- Ground fill under L1 and L2 removed, L1 shunted, C1 replaced with two series 10 µF ceramic caps (4 parts, 1210 package, 10 µF effective)

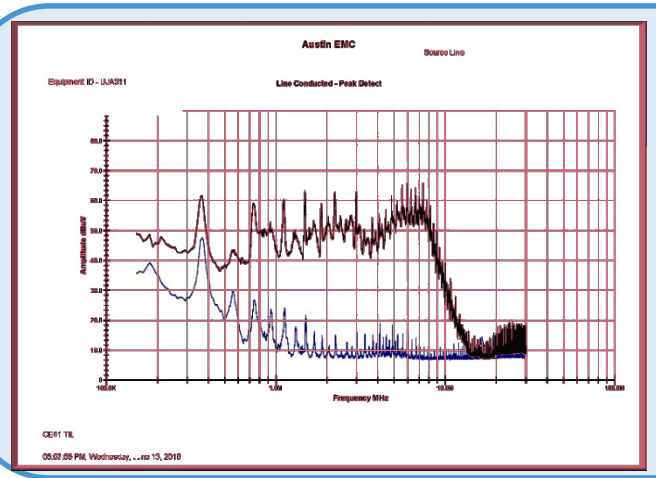
- **CE slightly higher with C1 replaced with ceramic capacitors**
  - 1210 package, UMK325AB7106KM-T
  - Around 30 dBµV at PWM switching frequency, ~375 KHz
  - CE significantly higher across the lower band
- RE 18 dBµV higher at PWM switching frequency, ~375 KHz
- **CE at upper band, and RE both bands slightly higher**
  - CE peak at ~375 KHz actually reduced by around 10 dBµV

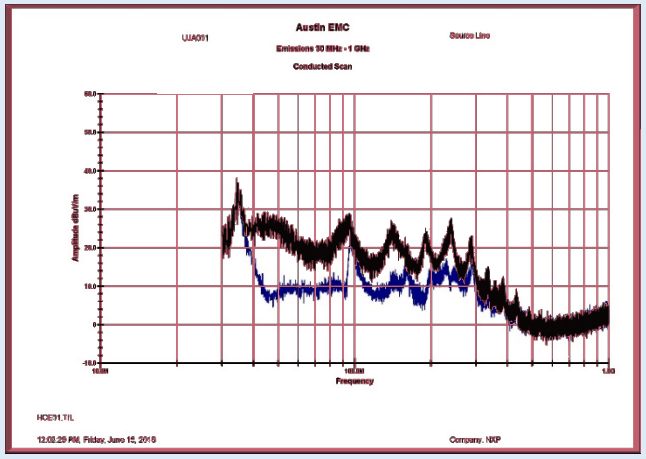
- Analysis:
  - Replacing C1 with two series sets of ceramic capacitors reduced the total capacitance on the board by around 27 µF
    - This reduced the amount of field available on the board, increasing the demand from the battery
    - Changing C1 to a ceramic reduced the ESR of the capacitor from 0.5 to <0.01. This increases the amount of energy available for each wave cycle.
  - The increase in CE falloff is slightly more significant at ~10 MHz than in version 5

- Cost delta vs Baseline: + $ 0.44

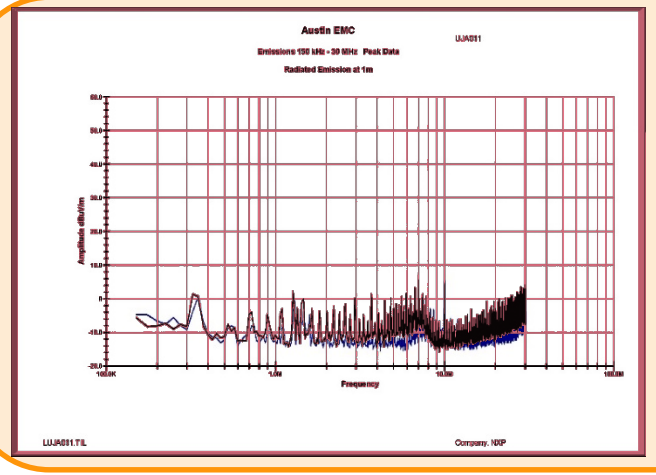
UJA1132 EMC Test Results

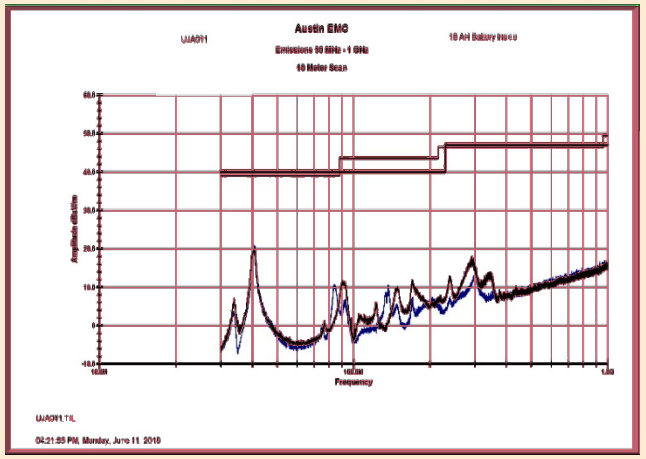
- Baseline Design, Version 1 (in **BLUE**), Version 11 (in **BLACK**)
- Change from Version 1: No L1 or C 5, C1: 47 µF ceramic
- CE 14 dBµV higher than baseline at ~375 KHz, 45 dBµV higher 1-4 MHz



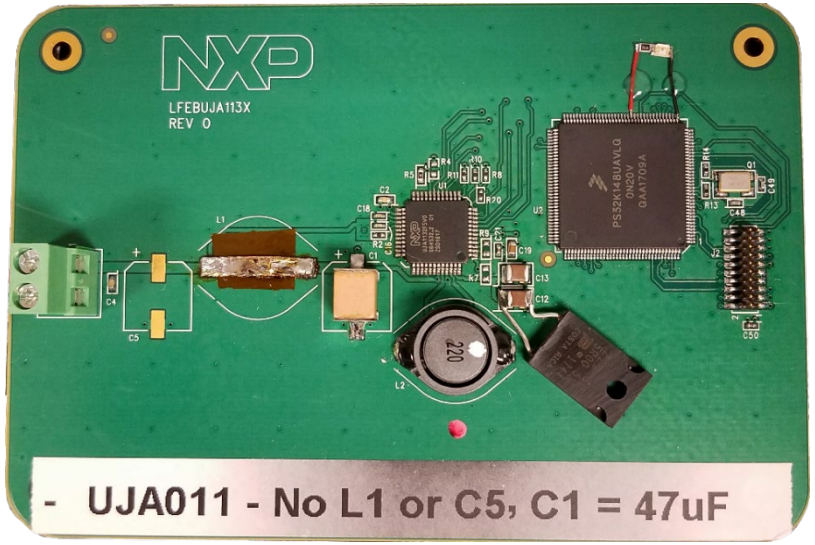


CE





RE



Baseline Design, Version 1 vs Version 11

- Ground fill under L1 and L2 removed, L1 shunted, C5 removed, C1 replaced with 47 µF ceramic capacitor

- CE higher with C1 replaced with 47 µF ceramic capacitor (dual device J-lead package, KTJ500B476M76BFT00)
  - Around 12 dBµV at PWM switching frequency, ~375 KHz
  - CE 45 dBµV higher 1-8 MHz
- RE 15 dBµV higher 40-100 MHz

- Analysis:
  - Changing C1 to a ceramic reduced the ESR of the capacitor from 0.5 to <0.01. This increases the amount of energy available for each wave cycle.
  - No C5 reduced the amount of field available on the board, increasing the demand from the battery
  - The increase in CE falloff is significant at ~8 MHz like in version 3

- Cost delta vs Baseline: + $1.93

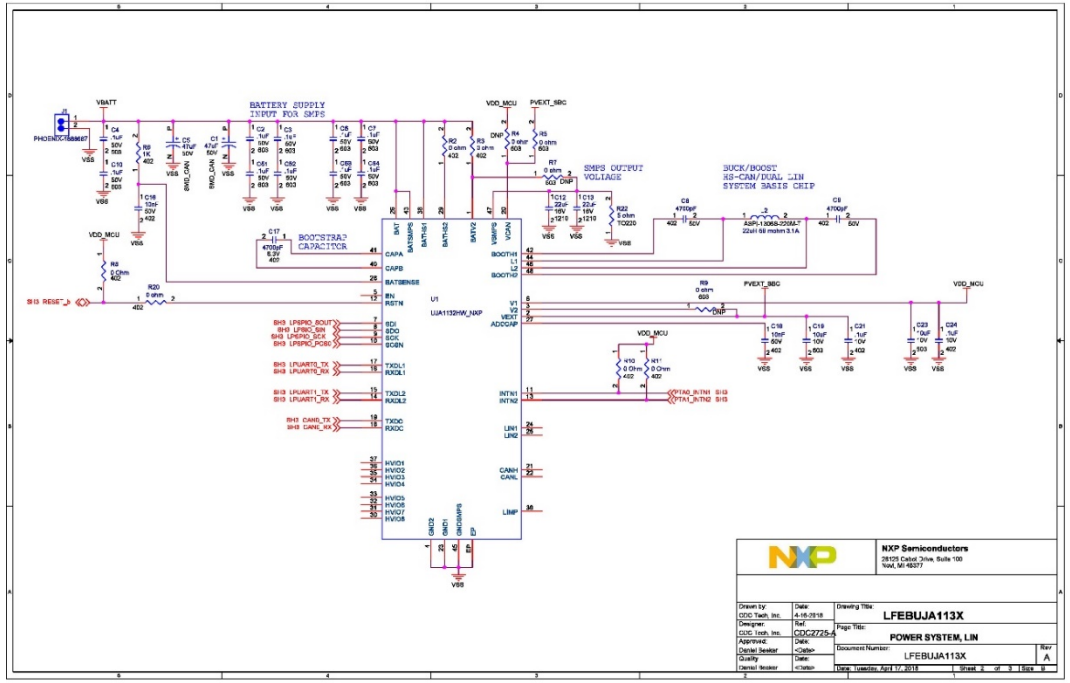
EMC Comparisons to Baseline

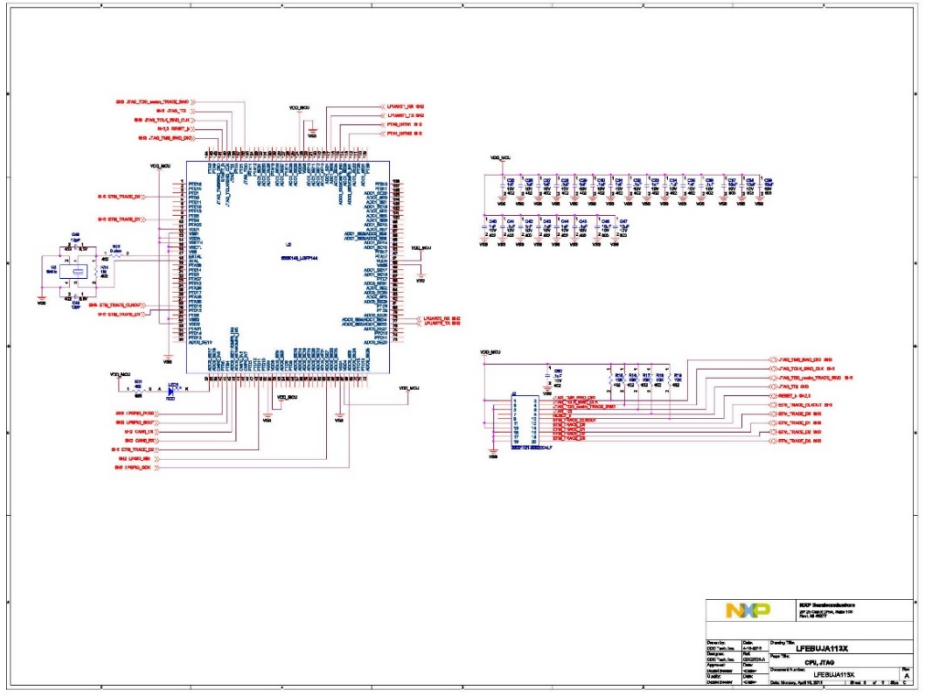
Baseline design compared to each successive revision of components using PCB

Rev A

UJA1132 EMC Test Platform

- PCB rev A schematic
- UJA1132HW SBC, PS32K148UAT0VLQT MCU with ETM debug interface
- Removed L1
- Changed ceramic caps on VBATT to two in series per automotive requirements, added LED and 10 ohm load resistor

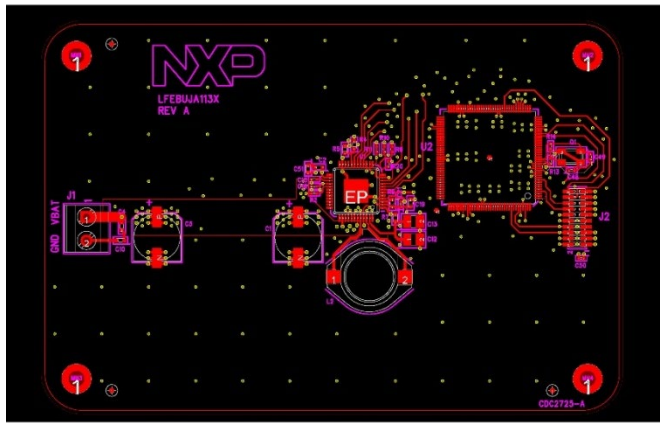




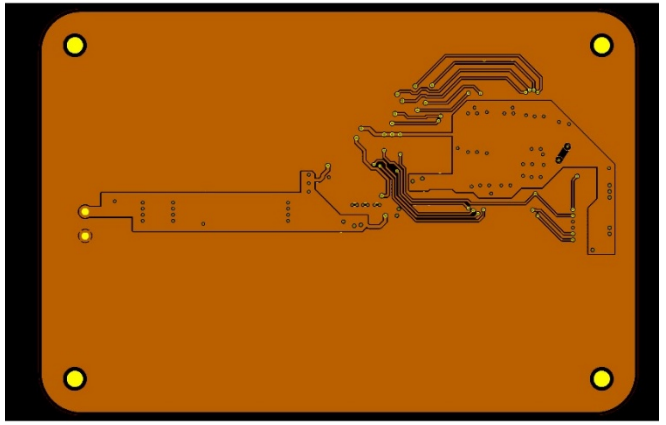
UJA1132 EMC Test Platform

- PCB rev A, Versions 1 and 2 eliminated by new PCB design
- PCB Layout

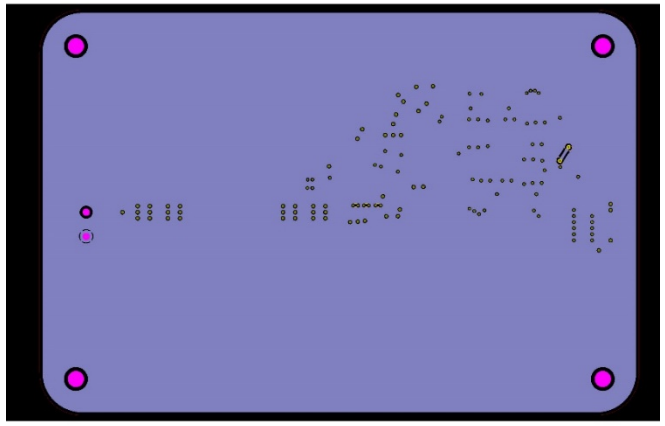
L1



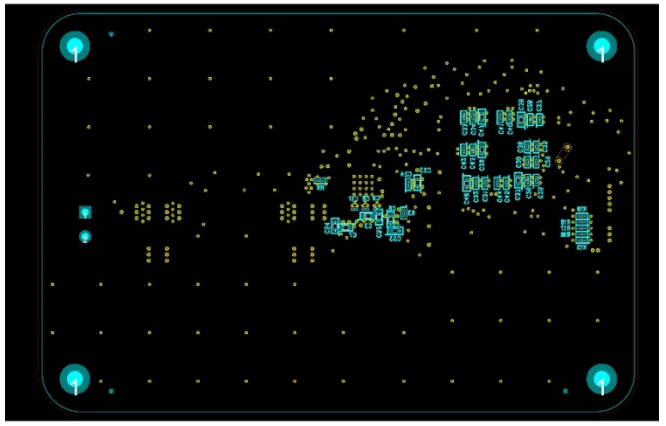
L3



L2



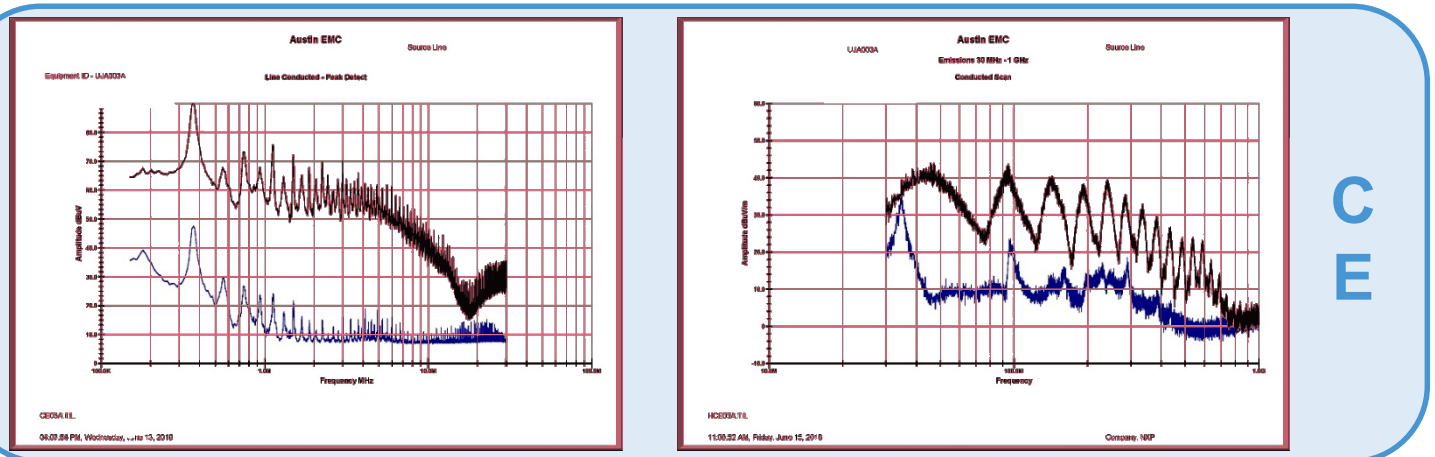
L4

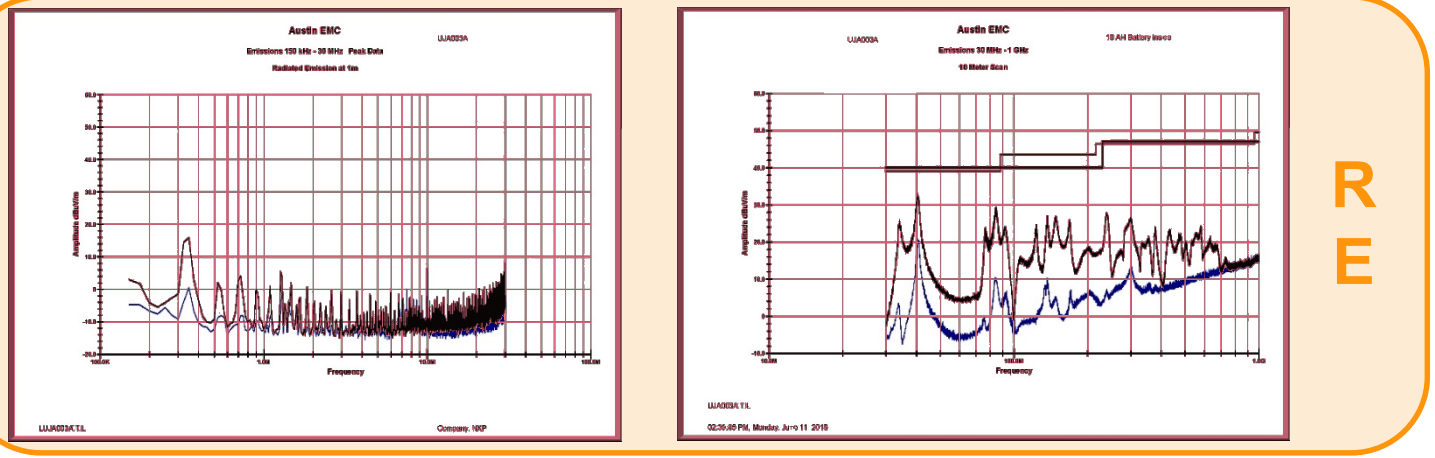


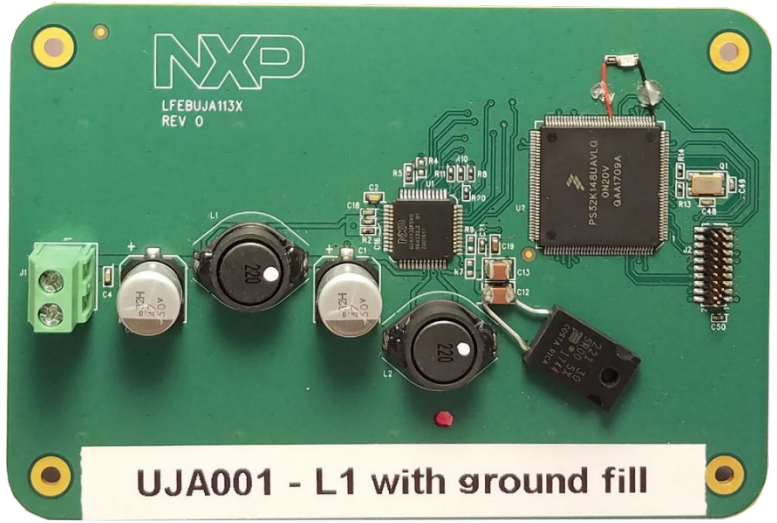
- Four layer PCB, Arduino Form factor
  - L1: Components, routing and ground flood
  - L2: Ground plane
  - L3: Power island, routing and ground flood
  - L4: Components, routing and ground flood
- VBATT using three dielectric layers
  - Between L1 trace and L2 ground plane
  - Between L3 trace and L2 ground plane
  - Between L3 trace and L4 ground plane
- Ground flood removed under discrete components
- Power distribution using “waterfall” technique
  - Interleaved power and ground vias to improve Z axis energy delivery

UJA1132 EMC Test Results

- Baseline Design, Version 1 (in **BLUE**), Version 3A (in **BLACK**)
- Change from Version 3: Rev A PCB
- CE 42 dBµV higher and RE 15 dBµV higher than baseline at ~375 KHz







Baseline Design, Version 1 vs Version 3A

- L1 replaced by traces on Layer 1 and Layer 3

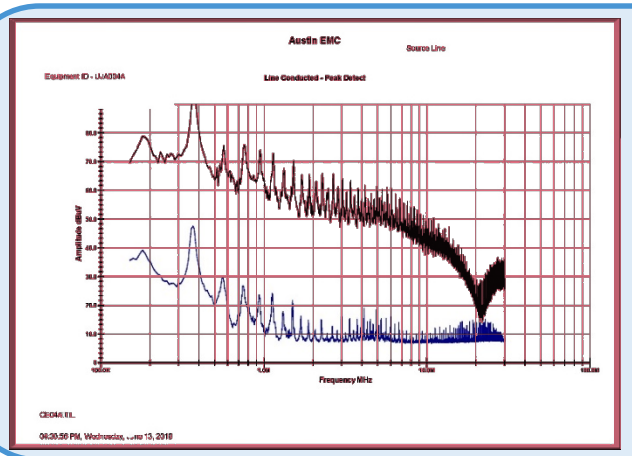
- **CE significantly higher with L1 removed**
  - 42 dBµV at PWM switching frequency, ~375 KHz through 8 MHz
- RE 15 dBµV higher at PWM switching frequency, ~375 KHz
- **CE at upper band, and RE both bands increased**
  - CE 35 through 600 MHz increased by around 10 dBµV

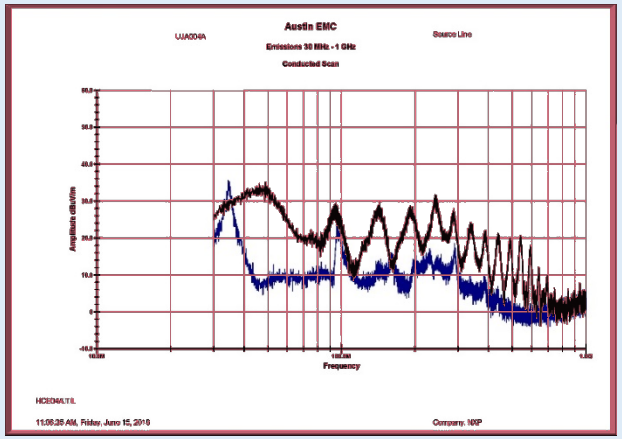
- Analysis:
  - Shunting the inductor location reduced the discontinuity in the energy flow from the power connector to the SMPS input
  - Routing on Layer 1 and Layer 3 creates 3 separate dielectric paths for EM energy to flow
  - This improved the movement of the EM fields, and resulted in an increase in current flow on the wiring harness when the switch turns on
  - The increase in CE falls off significantly by ~15 MHz

- Cost delta vs Baseline: - $ 0.68

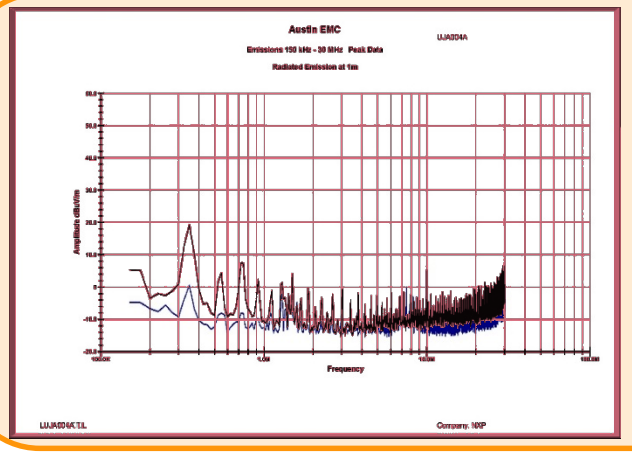
UJA1132 EMC Test Results

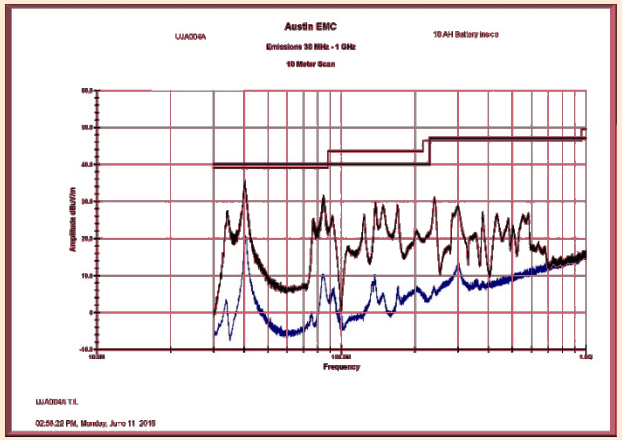
- Baseline Design, Version 1 (in **BLUE**), Version 4A (in **BLACK**)
- Change from Version 4: Rev A PCB
- CE 45 dBµV higher and RE 20 dBµV higher than baseline at ~375 KHz



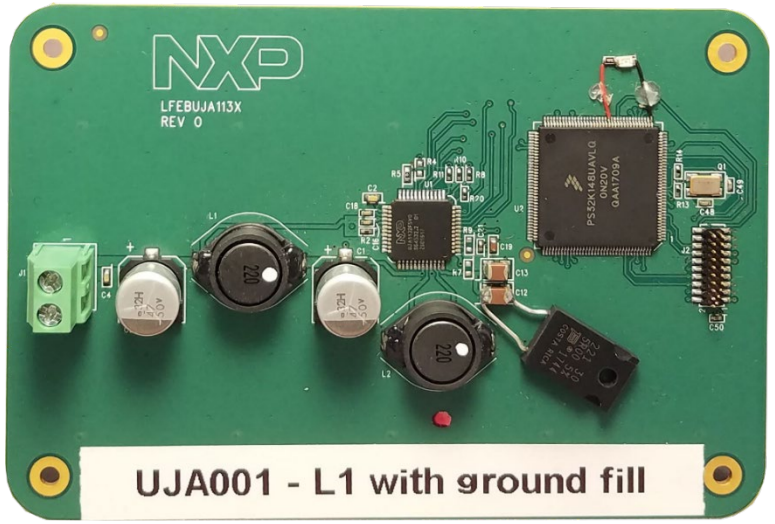


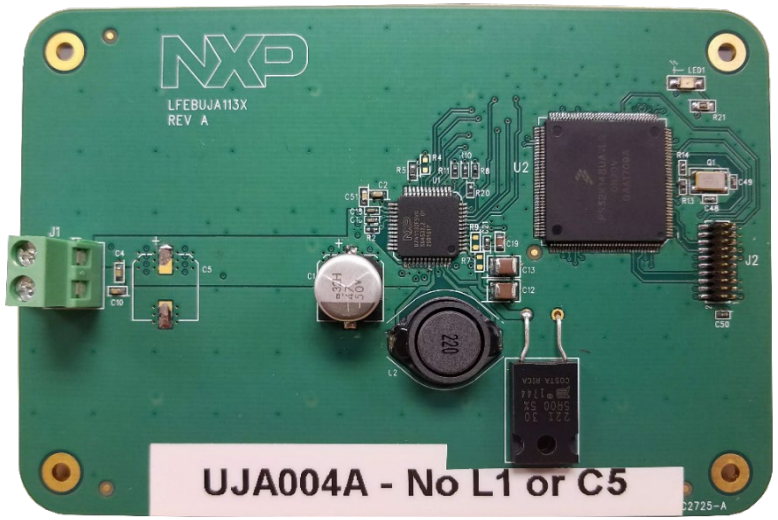
CE





RE





Baseline Design, Version 1 vs Version 4A

- L1 replaced by traces on Layer 1 and Layer 3, C5 removed

- **CE higher with C5 removed**
  - 40 dBµV at PWM switching frequency, ~375 KHz through 10 MHz
  - CE peak at ~375 KHz increased by around 15 dBµV
- RE 20 dBµV higher at PWM switching frequency, ~375 KHz
- RE 10 dBµV higher from 40-600 MHz

- Analysis:
  - Removing C5 near the power conductor reduces the overall energy storage by around 50%
  - This reduced the amount of field available on the board, increasing the demand from the battery
  - Routing on Layer 1 and Layer 3 creates 3 separate dielectric paths for EM energy to flow
  - This improved the movement of the EM fields, and resulted in an increase in current flow on the wiring harness when the switch turns on

- Cost delta vs Baseline: - $ 0.99

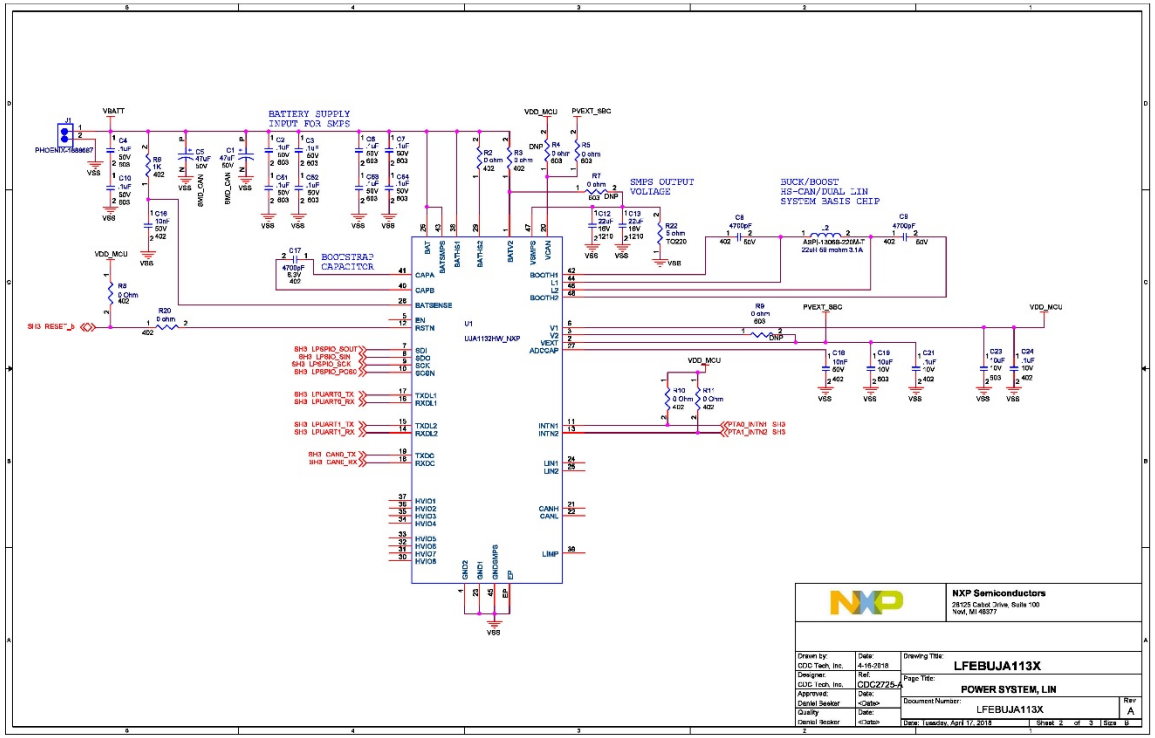
EMC Comparisons to Baseline

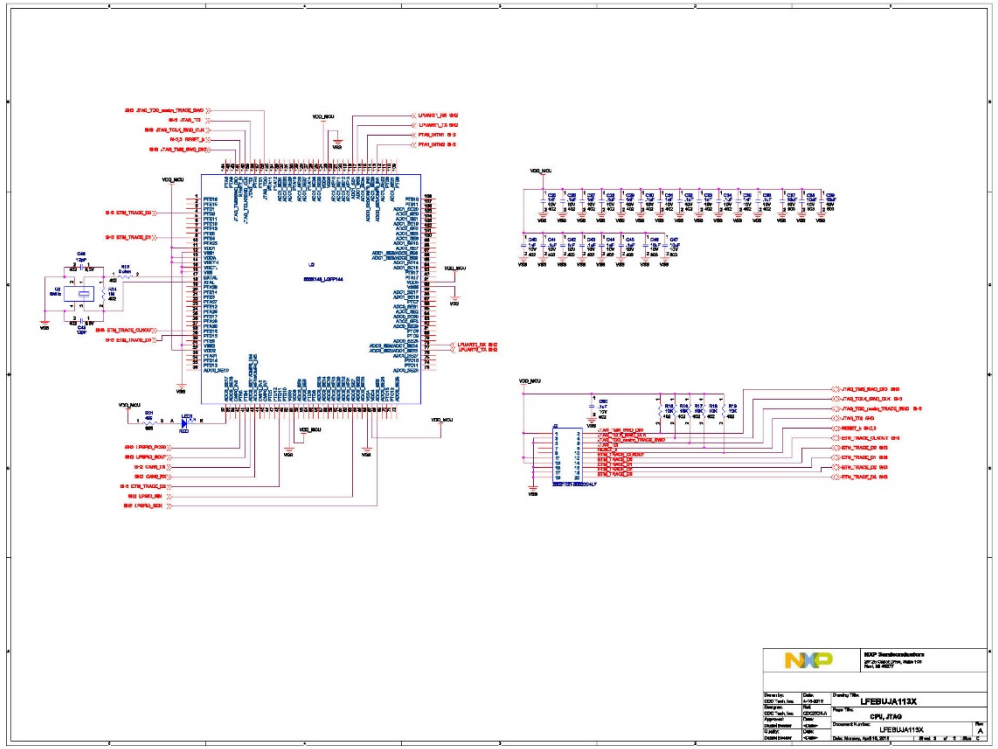
Baseline design compared to each successive revision of components using PCB

Rev B

UJA1132 EMC Test Platform

- PCB rev B schematic
- UJA1132HW SBC, PS32K148UAT0VLQT MCU with ETM debug interface
- Same as for rev A

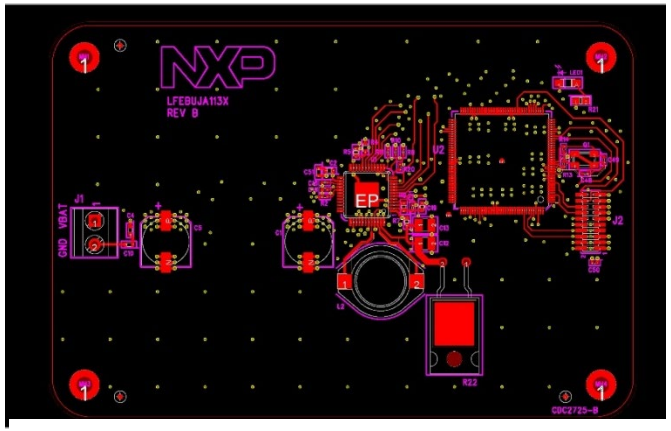




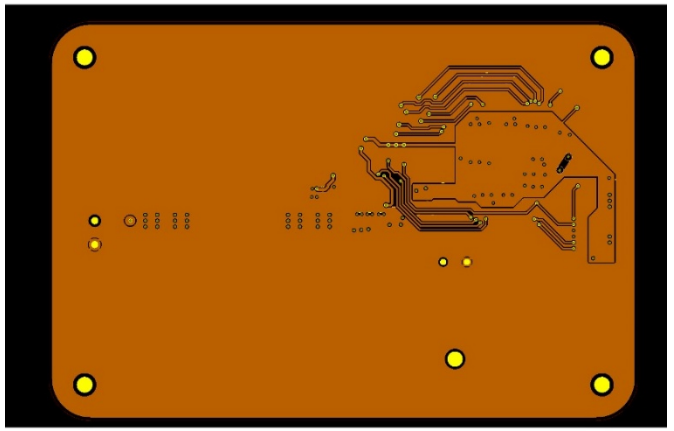
UJA1132 EMC Test Platform

- PCB rev B, Changes from rev A: VBATT routing moved to Layers 2 and 4
- PCB Layout

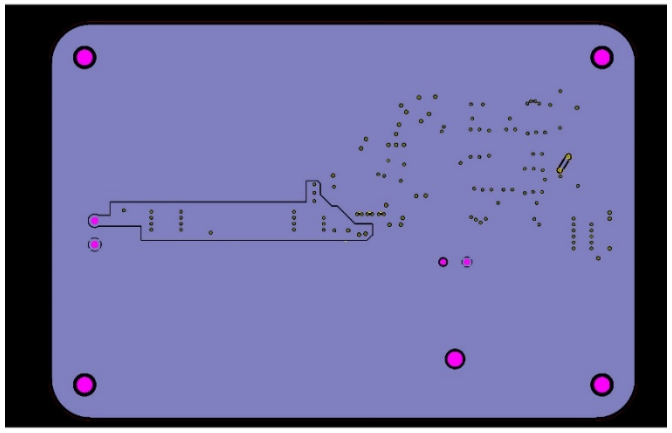
L1



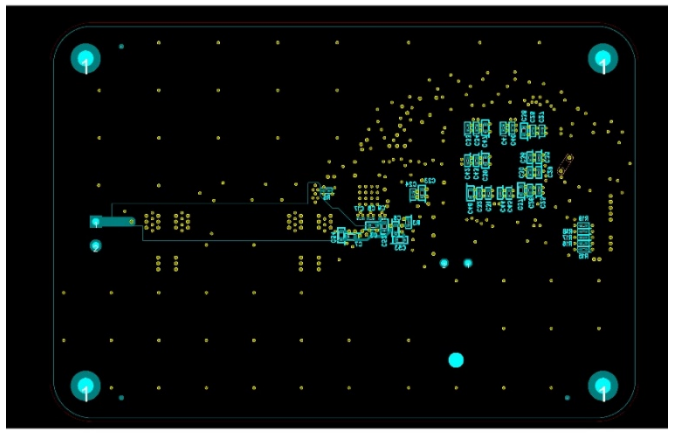
L3



L2



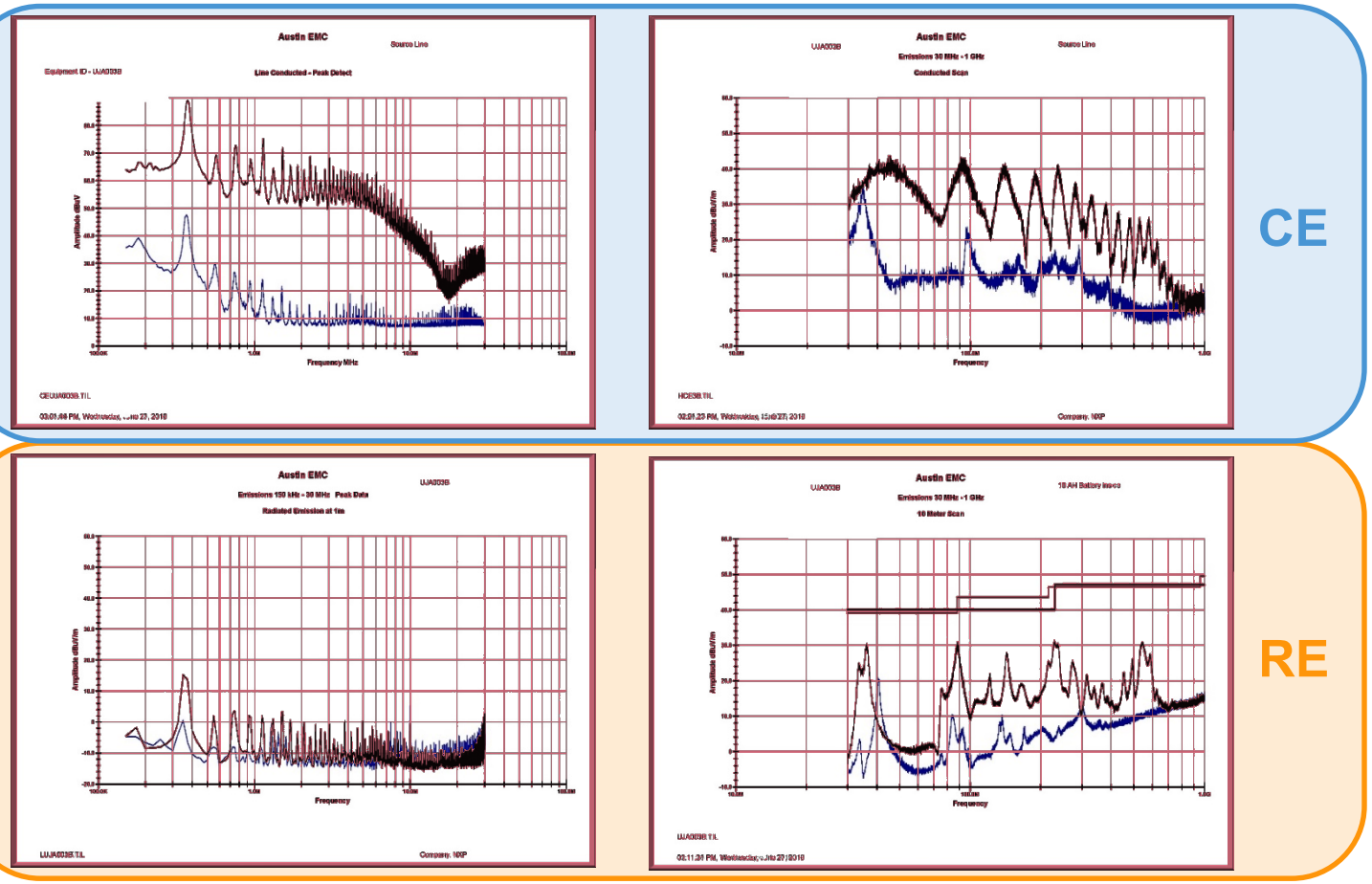
L4



- Four layer PCB, Arduino Form factor
  - L1: Components, routing and ground flood
  - L2: Power Routing and ground flood
  - L3: Power island, routing and ground flood
  - L4: Components, power and signal routing, and ground flood
- VBATT using three dielectric layers
  - Between L2 trace and L1 ground plane
  - Between L2 trace and L3 ground plane
  - Between L4 trace and L3 ground plane
- Ground flood removed under discrete components
- Power distribution using “waterfall” technique
  - Interleaved power and ground vias to improve Z axis energy delivery

UJA1132 EMC Test Results

- Baseline Design, Version 1 (in **BLUE**), Version 3B (in **BLACK**)
- Change from Version 3A: Rev B PCB
- CE 40 dBµV higher and RE 15 dBµV higher than baseline at ~375 KHz



Baseline Design, Version 1 vs Version 3B

- L1 replaced by traces on Layer 2

- **CE significantly higher with L1 removed**
  - 40 dBµV at PWM switching frequency, ~375 KHz through 8 MHz
  - CE 40 dBµV higher from 40-300 MHz
- RE 15 dBµV higher at PWM switching frequency, ~375 KHz
  - 10 dBµV higher from 35-250 MHz

- Analysis:
  - Shunting the inductor location reduced the discontinuity in the energy flow from the power connector to the SMPS input
  - Routing power on Layer 2 creates 2 separate dielectric paths for EM energy to flow
  - This improved the movement of the EM fields, and resulted in an increase in current flow on the wiring harness when the switch turns on
  - The increase in CE falls off significantly by ~15 MHz

- Cost delta vs Baseline: - $ 0.68

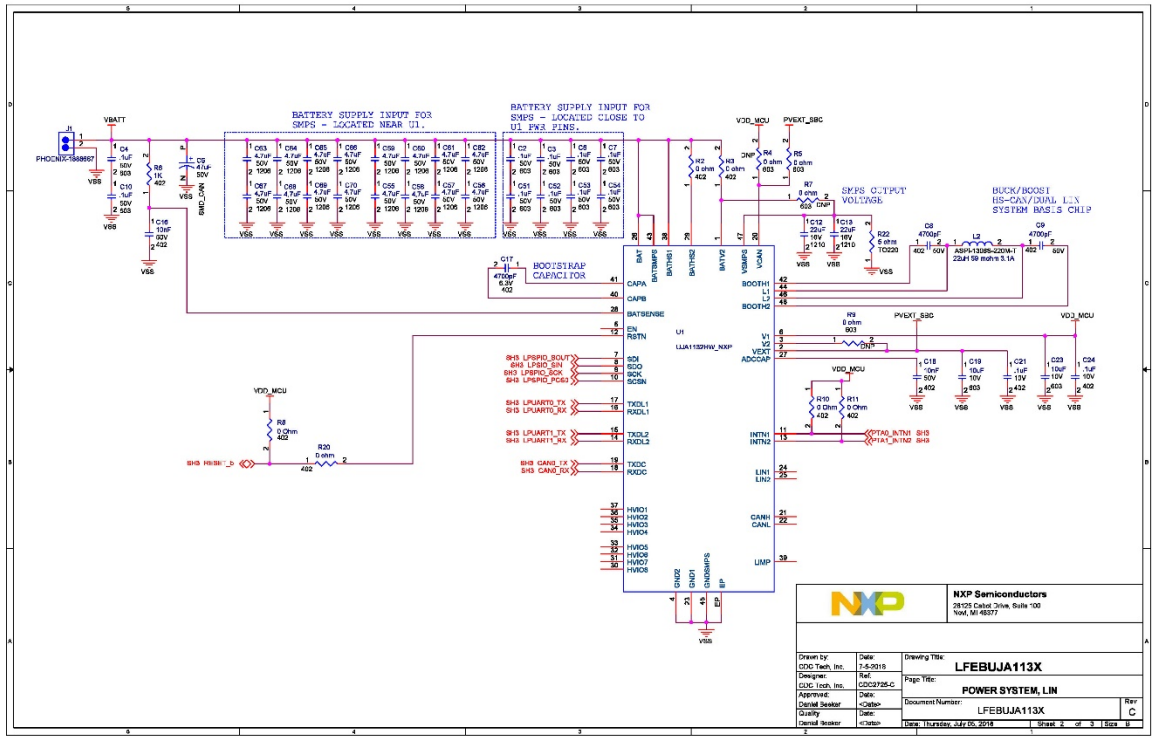
EMC Comparisons to Baseline

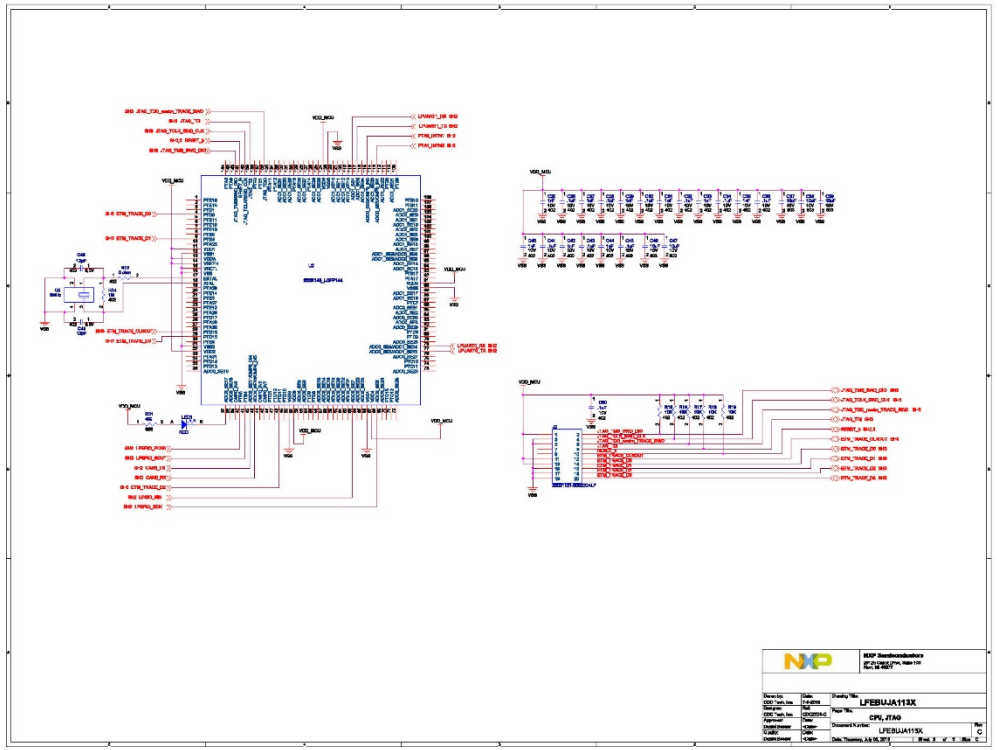
Baseline design compared to each successive revision of components using PCB

Rev C

UJA1132 EMC Test Platform

- PCB rev C schematic
- UJA1132HW SBC, PS32K148UAT0VLQT MCU with ETM debug interface
- C1 replaced with eight series 10 µF ceramic capacitors (16 parts, 20 µF effective capacitance)

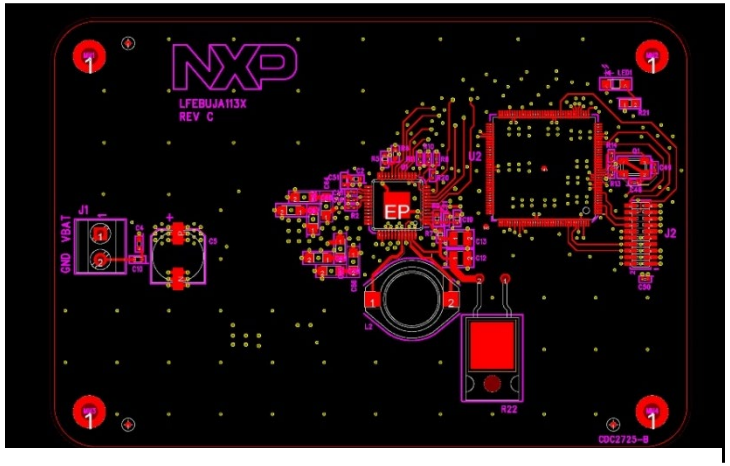




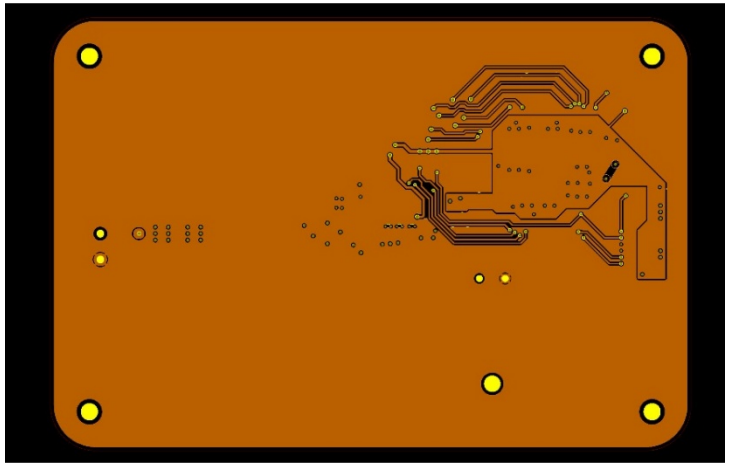
UJA1132 EMC Test Platform

- PCB rev C, Changes from rev B: VBATT routing moved to Layers 2 and 4, replace C1 with ceramic caps
- PCB Layout

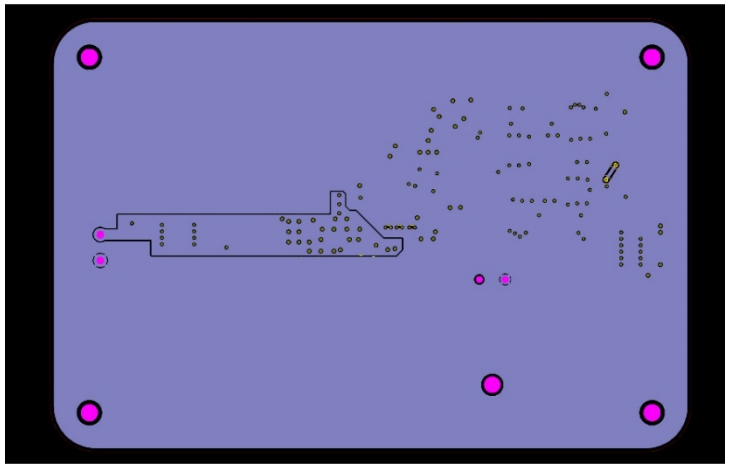
L1



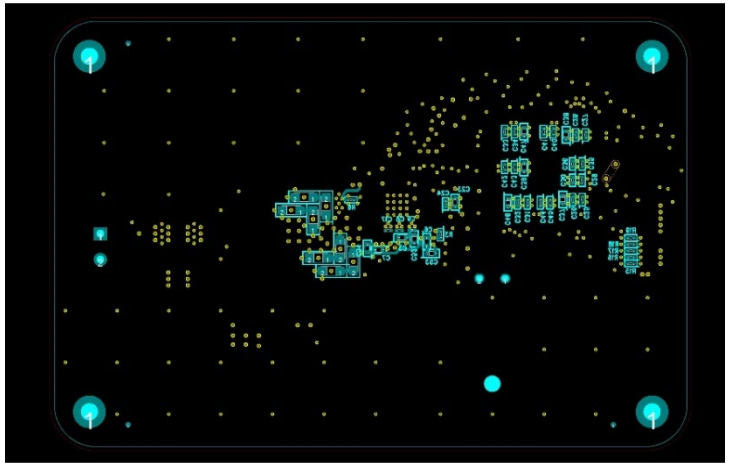
L3



L2



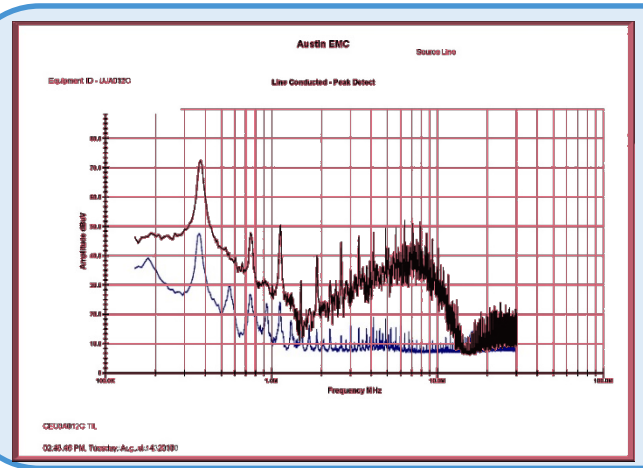
L4

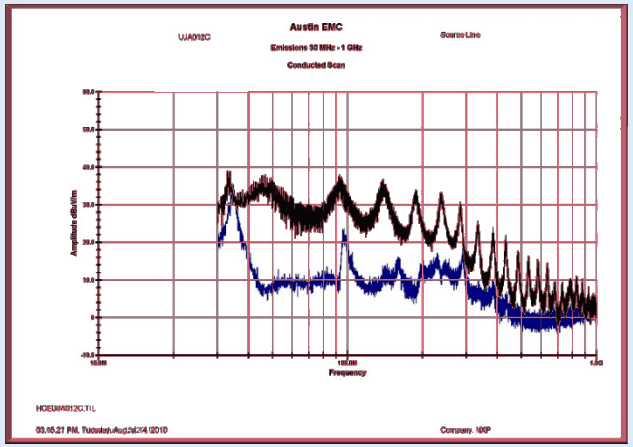


- Four layer PCB, Arduino Form factor
  - L1: Components, routing and ground flood
  - L2: Power Routing and ground flood
  - L3: Power island, routing and ground flood
  - L4: Components, power and signal routing, and ground flood
- VBATT using three dielectric layers
  - Between L2 trace and L1 ground plane
  - Between L2 trace and L3 ground plane
  - Between L4 trace and L3 ground plane
- Ground flood removed under discrete components
- Power distribution using “waterfall” technique
  - Interleaved power and ground vias to improve Z axis energy delivery
- Replaced C1, 47 µF electrolytic cap, with 8 series 10 µF ceramic caps

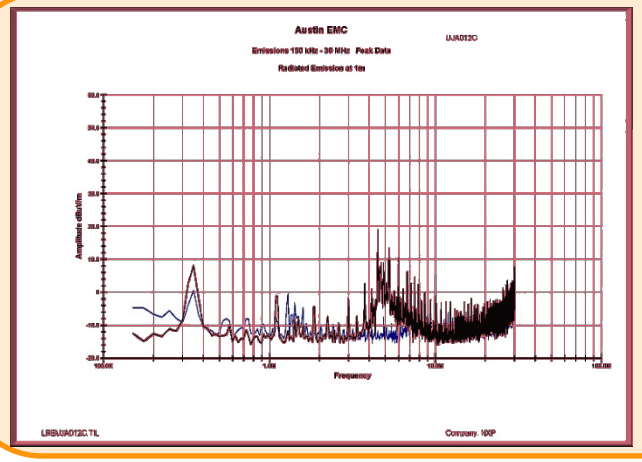
UJA1132 EMC Test Results

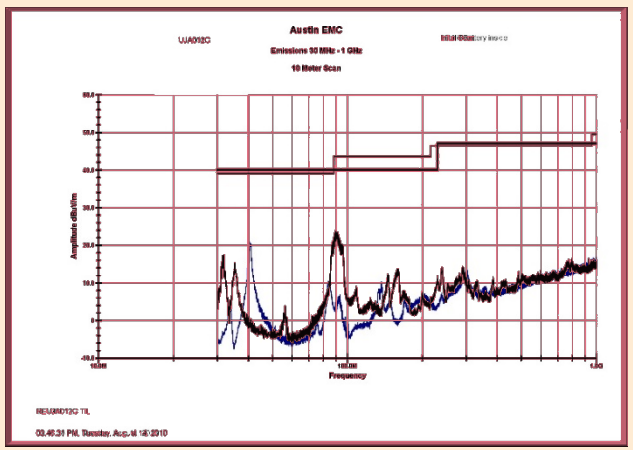
- Baseline Design, Version 1 (in **BLUE**), Version 12C (in **BLACK**)
- Change from Version 7B: Rev C PCB
- CE 22 dBµV higher and RE 5 dBµV higher than baseline at ~375 KHz



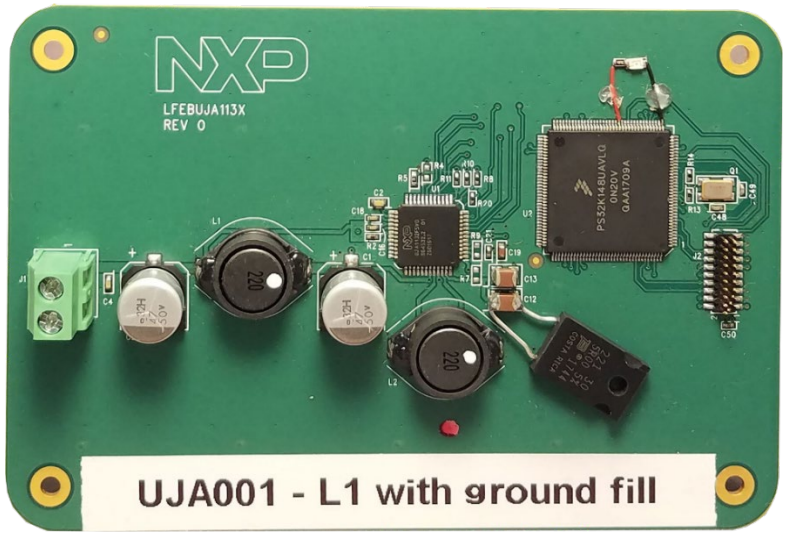


CE

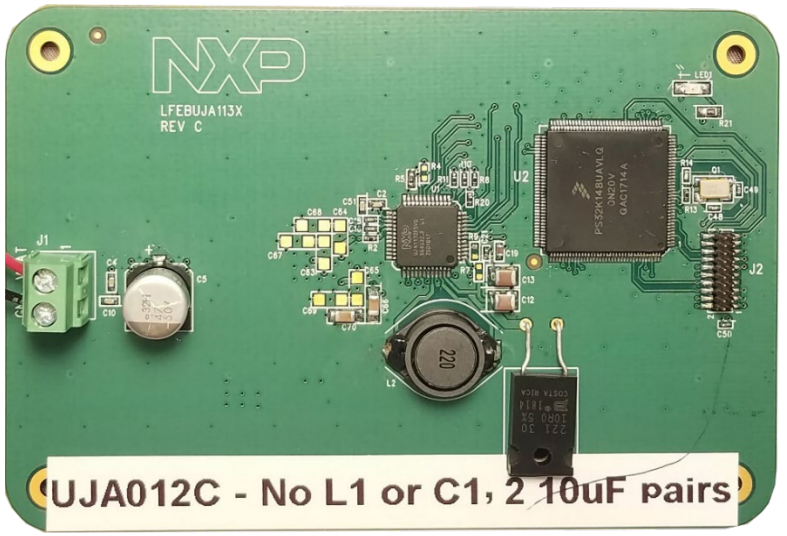




RE



UJA001 - L1 with ground fill



UJA012C - No L1 or C1, 2 10uF pairs

Baseline Design, Version 1 vs Version 12C

- L1 replaced by traces on Layer 2, C1 replaced with two series 10 µF ceramic caps (4 parts, 10 µF effective)

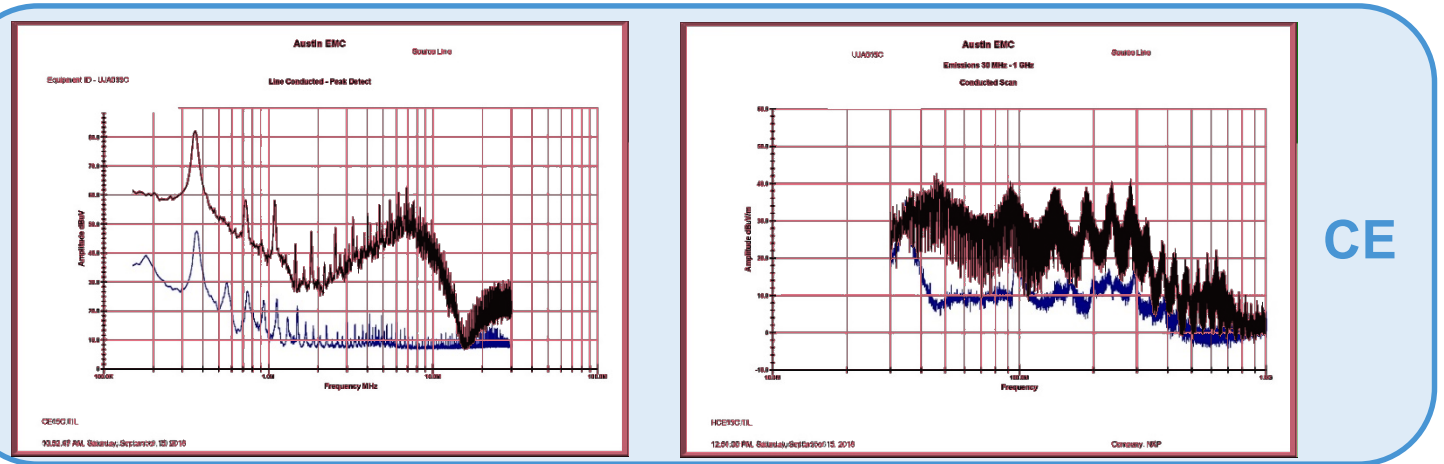
- **CE slightly higher with C1 replaced with ceramic capacitors**
  - 1206 package, CL31A106MBHNNNE
  - 25 dBµV higher at PWM switching frequency, ~375 KHz through 8 MHz
  - CE 25 dBµV higher from 40-250 MHz
- RE 8 dBµV higher at PWM switching frequency, ~375 KHz
  - Second peak 20 dBµV higher at 5 MHz
- RE 20 dBµV lower at 40 MHz
- RE 12 dBµV higher at 90 MHz

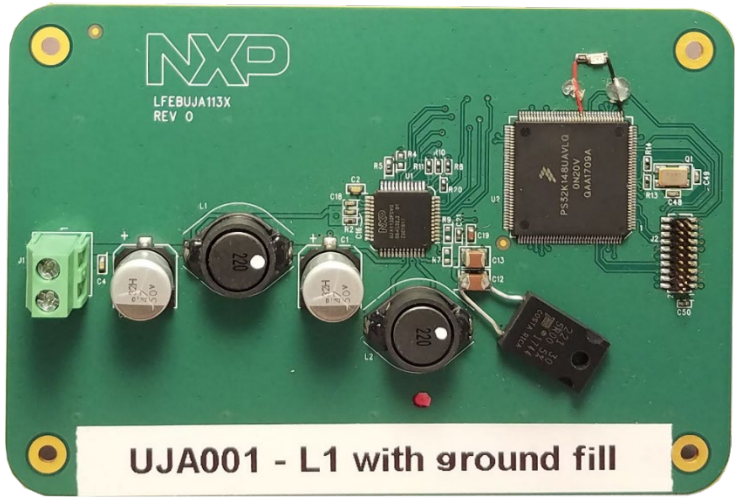
- Analysis:
  - Replacing C1 with two series sets of ceramic capacitors reduced the total capacitance on the board by around 37 µF
  - This reduced the amount of field available on the board, increasing the demand from the battery

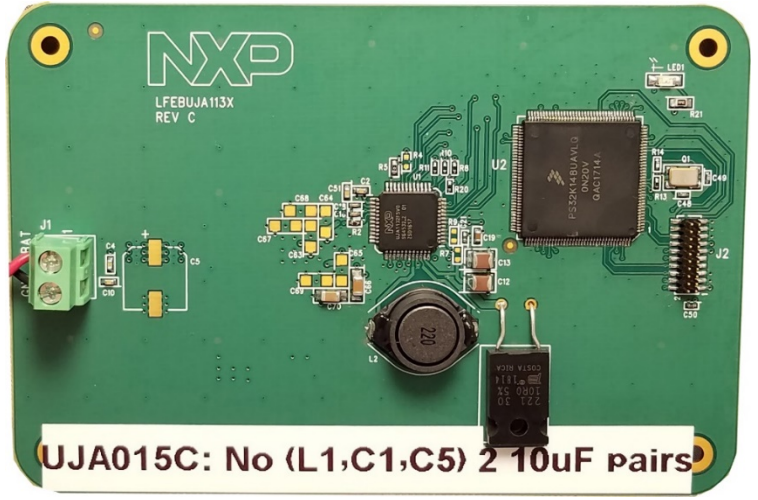
- Cost delta vs Baseline: - $ 0.70

UJA1132 EMC Test Results

- Baseline Design, Version 1 (in **BLUE**), Version 15C (in **BLACK**)
- Change from Version 12C: No C5
- CE 35 dBµV higher than baseline at ~375 KHz and RE 12 dBµV higher







Baseline Design, Version 1 vs Version 15C

- L1 replaced by traces on Layer 2, C1 replaced with two series 10 µF ceramic caps (16 parts, 10 µF effective), no C5 installed

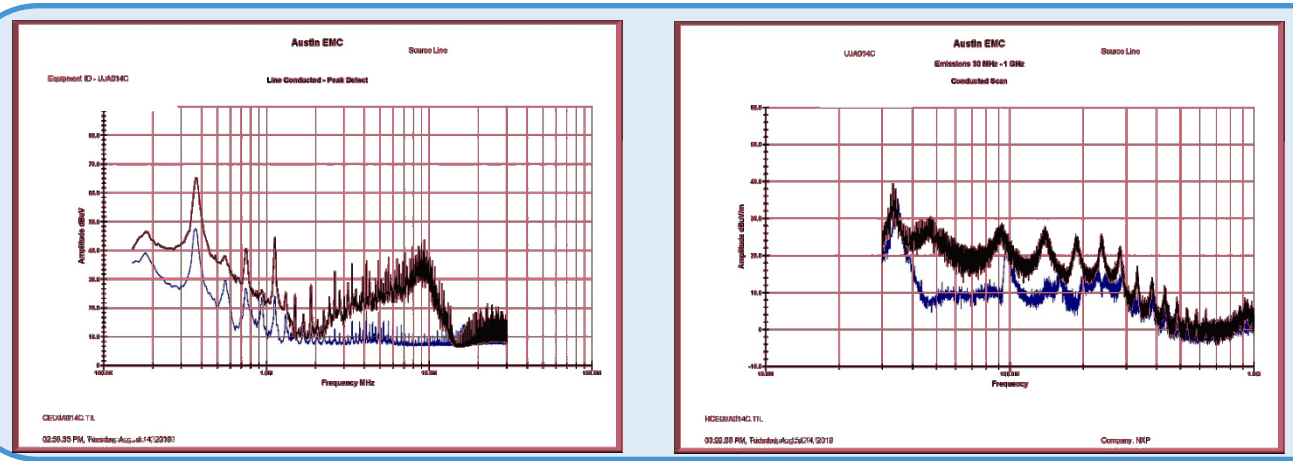
- **CE higher with no C5 and with C1 replaced with ceramic capacitors**
  - 1206 package, CL31A106MBHNNNE
  - 35 dBµV higher at PWM switching frequency, ~375 KHz
  - 40 dBµV higher at 8 MHz
- RE 15 dBµV higher at 375 KHz
- RE 20 dBµV higher from 9 to 350 MHz

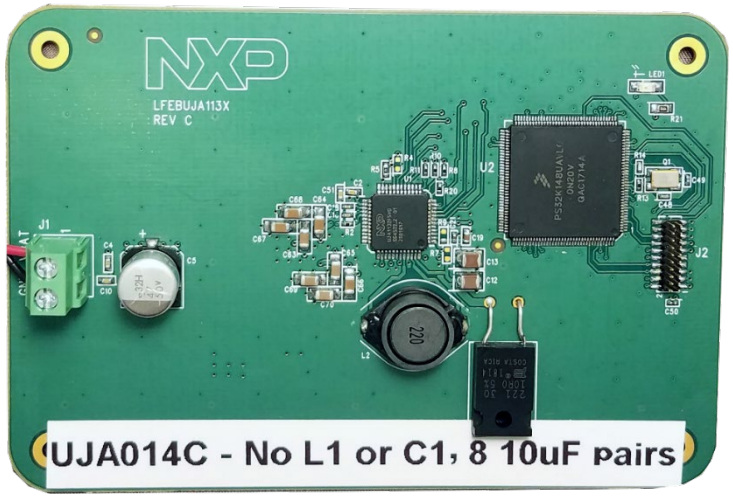
- Analysis:
  - Removing C5 and replacing C1 with two series sets of ceramic capacitors reduced the total capacitance on the board by around 84 µF
  - This reduced the amount of field available on the board, increasing the demand from the battery

- Cost delta vs Baseline: - $ 1.01

UJA1132 EMC Test Results

- Baseline Design, Version 1 (in **BLUE**), Version 14C (in **BLACK**)
- Change from Version 13C: eight series 10 µF ceramic caps (16 parts, 40 µF total)
- CE 18 dBµV higher and RE 1 dBµV higher than baseline at ~375 KHz





Baseline Design, Version 1 vs Version 14C

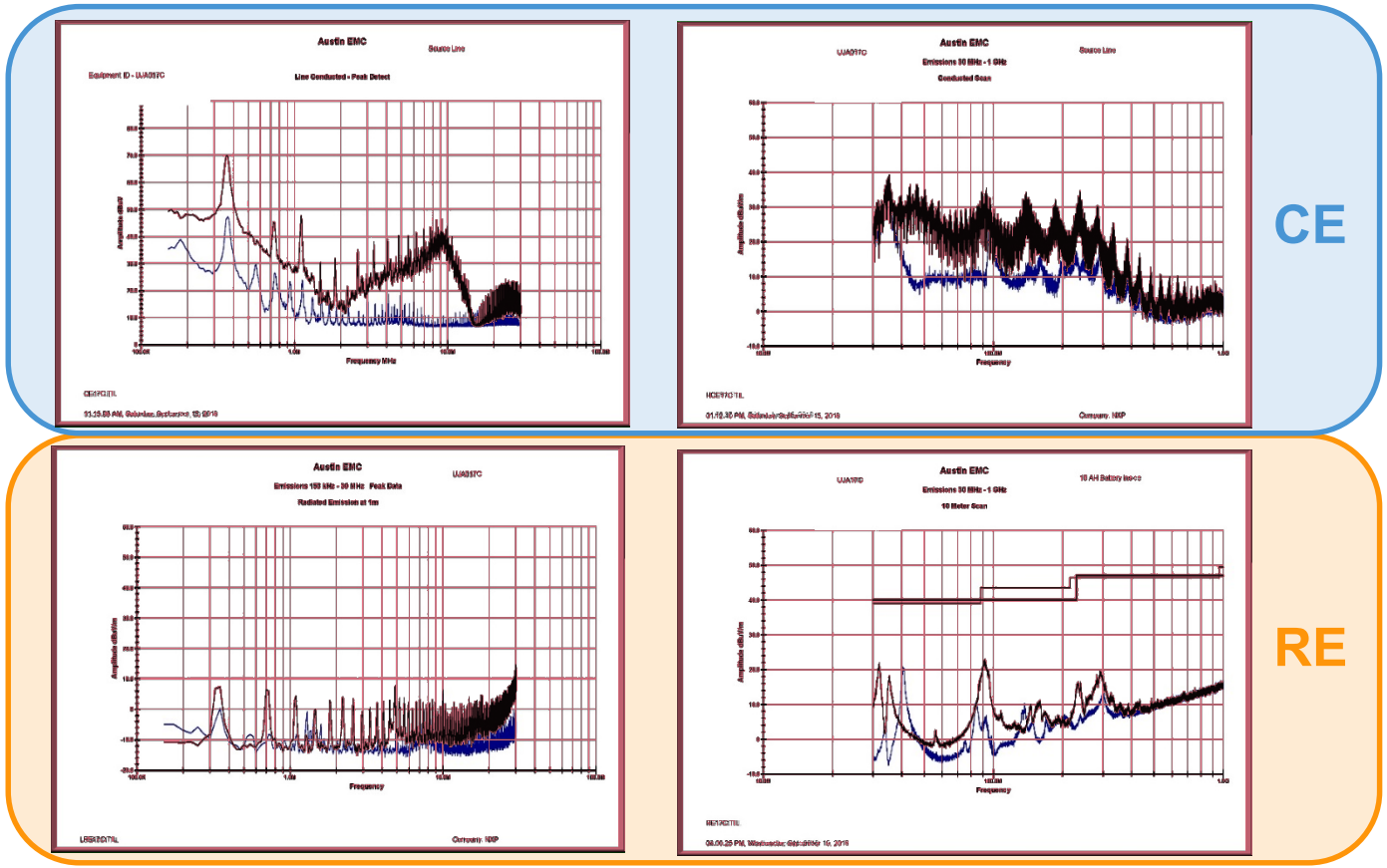
- L1 replaced by traces on Layer 2, C1 replaced with eight series 10 µF ceramic caps (16 parts, 40 µF effective)

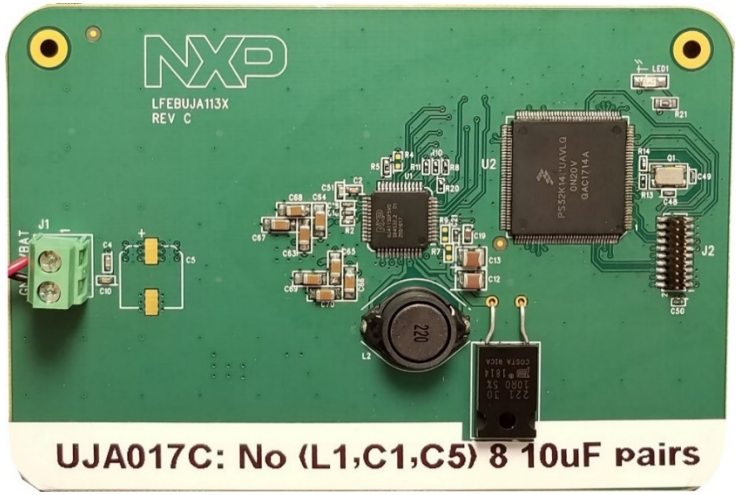
- **CE slightly higher with C1 replaced with ceramic capacitors**
  - 1206 package, CL31A106MBHNNNE
  - 18 dBµV higher at PWM switching frequency, ~375 KHz
  - 20 dBµV higher at 8 MHz
- RE 1 dBµV higher at 375 KHz
  - RE 20 dBµV lower at 40 MHz
  - RE 8 dBµV higher at 90 MHz
- Analysis:
  - Replacing C1 with eight series sets of ceramic capacitors reduced the total capacitance on the board by around 7 µF
  - This reduced the amount of field available on the board, increasing the demand from the battery

- Cost delta vs Baseline: + $ 0.17

UJA1132 EMC Test Results

- Baseline Design, Version 1 (in **BLUE**), Version 17C (in **BLACK**)
- Change from Version 14C: No C5
- CE 22 dBµV higher and RE slightly higher than baseline at ~375 KHz





Baseline Design, Version 1 vs Version 17C

- L1 replaced by traces on Layer 2, C1 replaced with eight series 10 µF ceramic caps (32 parts, 40 µF effective), no C5 installed

- **CE higher with no C5 and with C1 replaced with ceramic capacitors**
  - 1206 package, CL31A106MBHNNNE
  - 22 dBµV higher at PWM switching frequency, ~375 KHz through 8 MHz
- RE 8 dBµV higher at 375 KHz
- RE 12 dBµV higher at 90 MHz

- Analysis:
  - Removing C5 and replacing C1 with four series sets of ceramic capacitors reduced the total capacitance on the board by around 74 µF
  - This reduced the amount of field available on the board, increasing the demand from the battery

- Cost delta vs Baseline: - $ 0.14

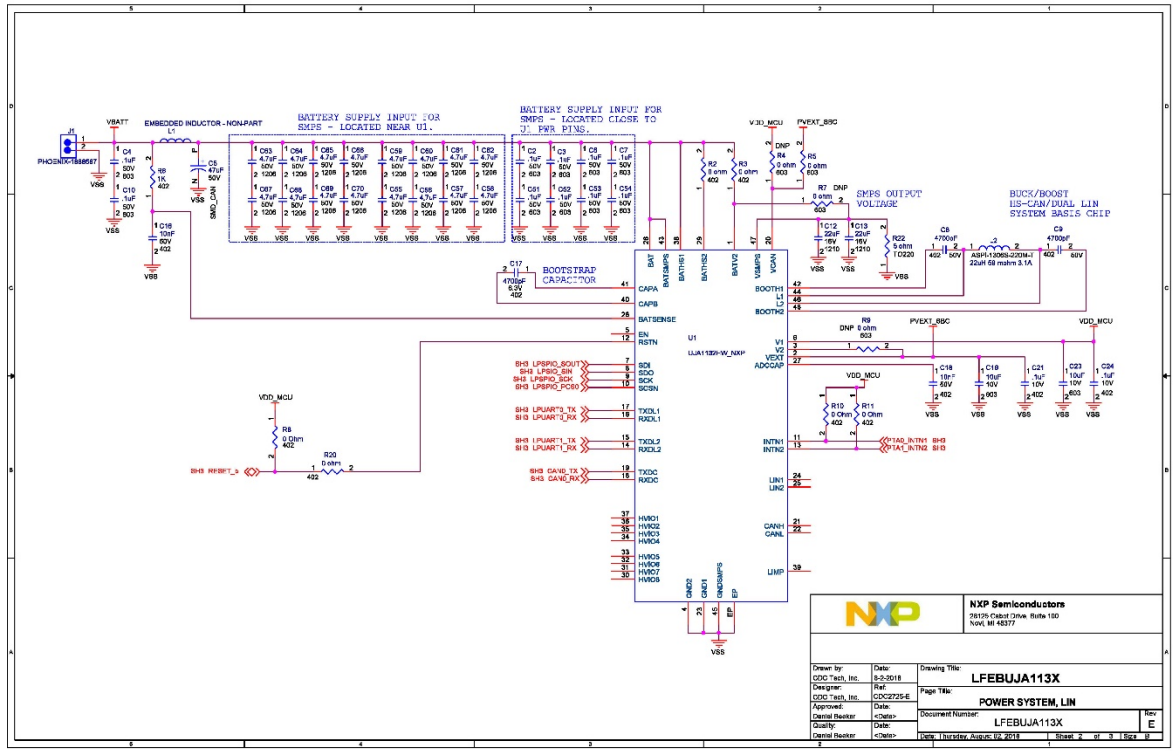
EMC Comparisons to Baseline

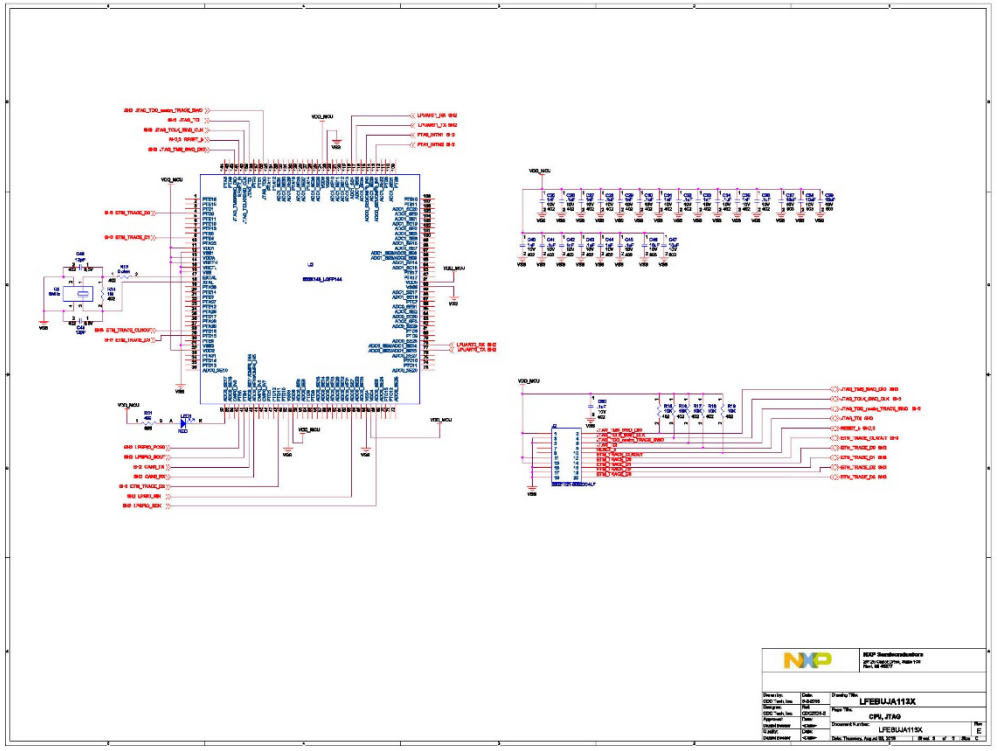
Baseline design compared to each successive revision of components using PCB

Rev E

UJA1132 EMC Test Platform

- PCB rev E schematic
- UJA1132HW SBC, PS32K148UAT0VLQT MCU with ETM debug interface
- Same as rev D

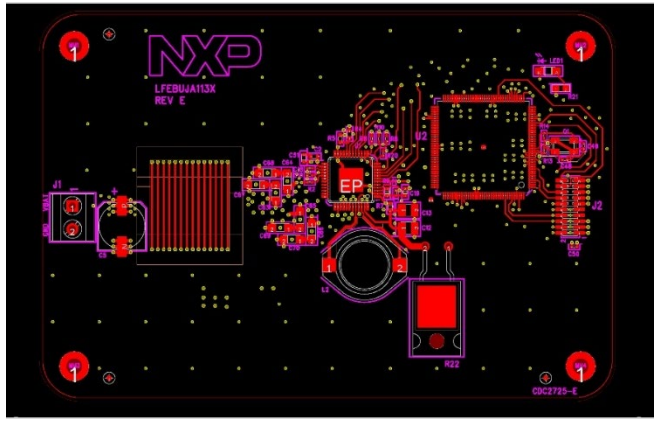




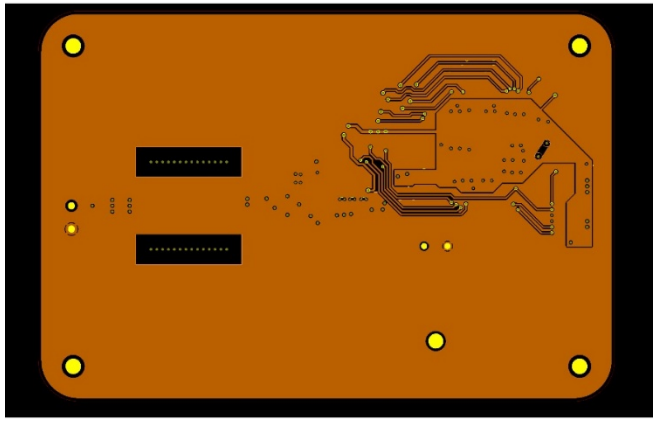
UJA1132 EMC Test Platform

- PCB rev E, Changes from rev D: Add missing power and ground vias near MCU
- PCB Layout

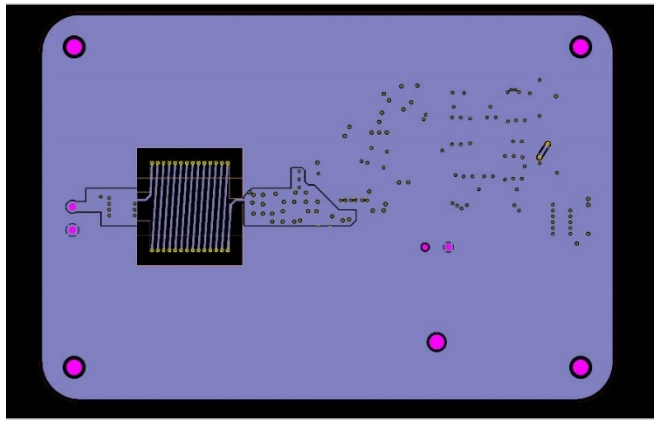
L1



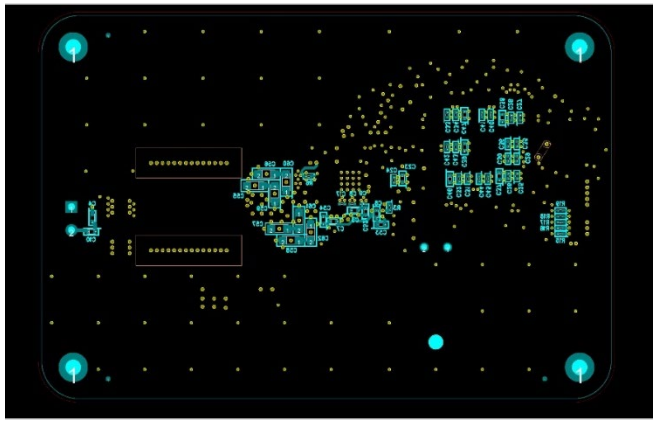
L3



L2



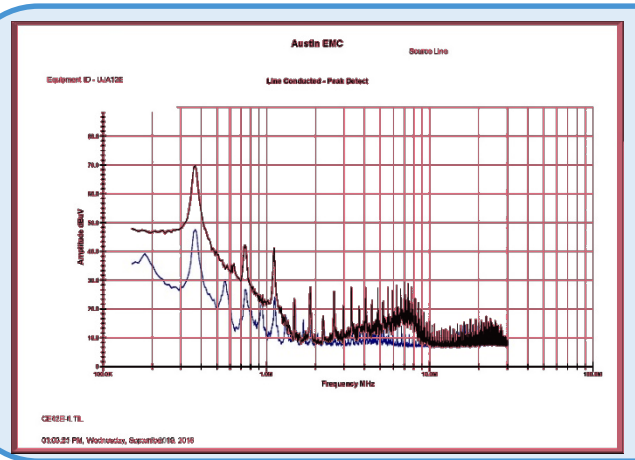
L4

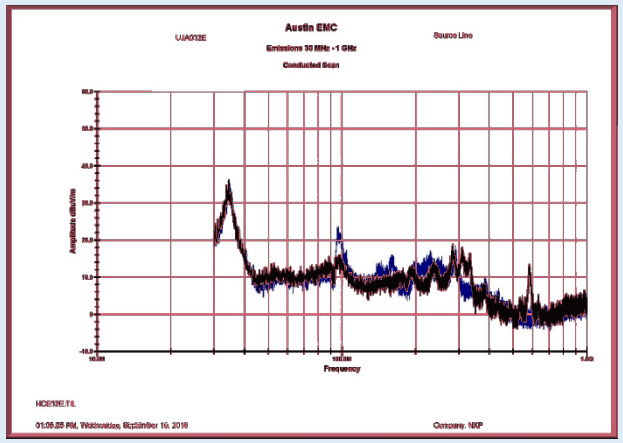


- Four layer PCB, Arduino Form factor
  - L1: Components, routing and ground flood
  - L2: Power Routing and ground flood
  - L3: Power island, routing and ground flood
  - L4: Components, signal routing, and ground flood
- VBATT using two dielectric layers
  - Between L2 trace and L1 ground plane
  - Between L2 trace and L3 ground plane
- Ground flood removed under discrete components
- Power distribution using “waterfall” technique
  - Interleaved power and ground vias to improve Z axis energy delivery

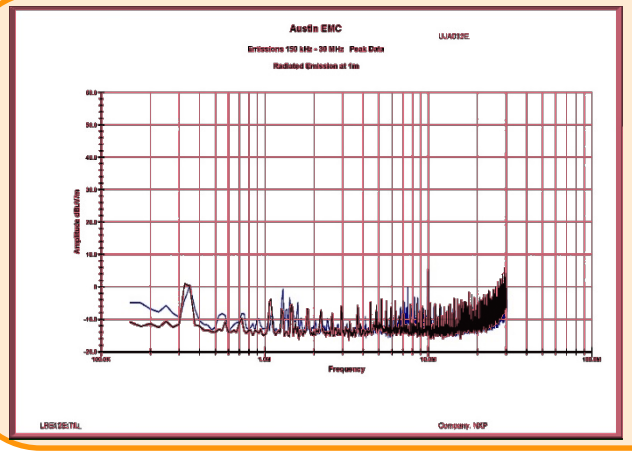
UJA1132 EMC Test Results

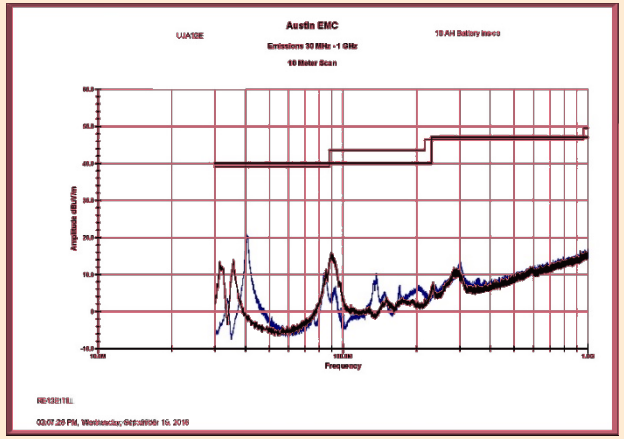
- Baseline Design, Version 1 (in **BLUE**), Version 12E (in **BLACK**)
- Change from Version 12D: Rev E PCB
- CE 22 dBµV higher than baseline at ~375 KHz



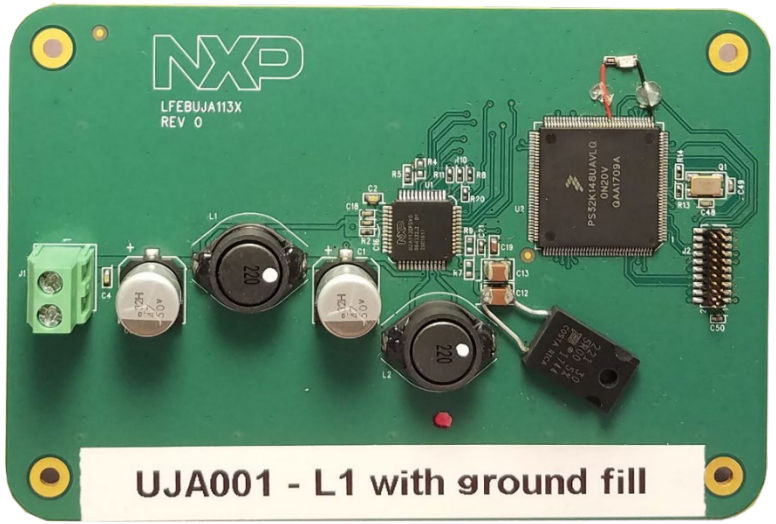


CE

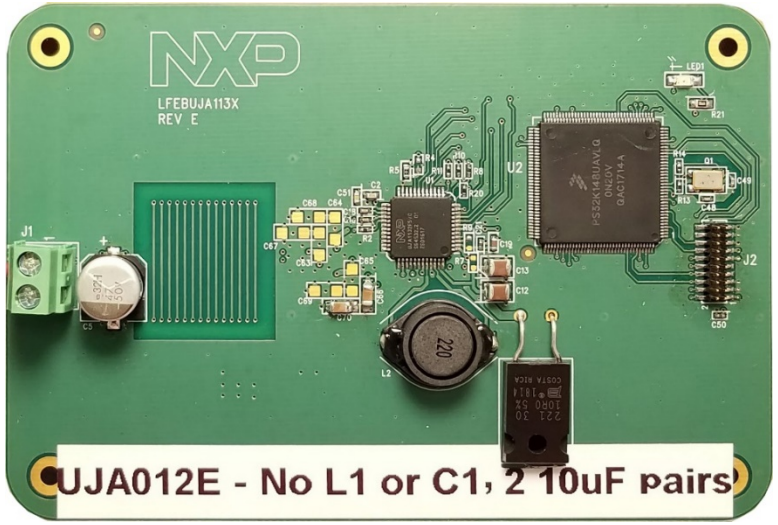




RE



UJA001 - L1 with ground fill



UJA012E - No L1 or C1, 2 10uF pairs

Baseline Design, Version 1 vs Version 12E

- L1 replaced by PCB trace inductor using Layers 1 and 2, C1 replaced with two series 10 µF ceramic caps (4 parts, 10 µF effective), C5 47 µF installed

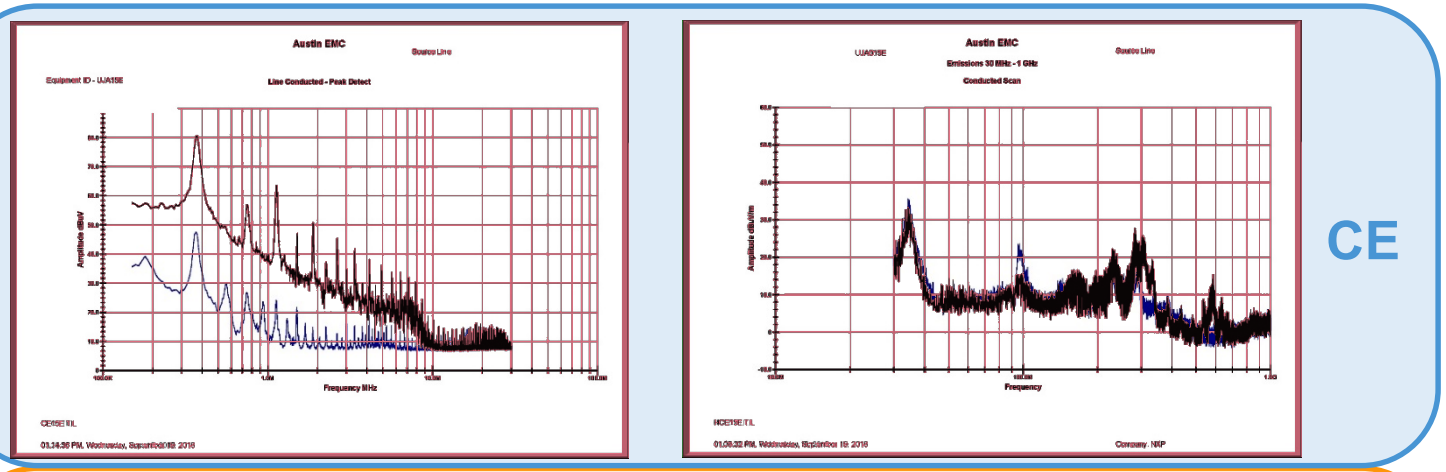
- **CE higher with PCB inductor and with C1 replaced with ceramic capacitors**
  - 1206 package, CL31A106MBHNNNE
  - 22 dBµV higher at PWM switching frequency, ~375 KHz through 1.5 MHz
- RE 5 dBµV higher at 375 KHz
- RE 20 dBµV lower at 40 MHz

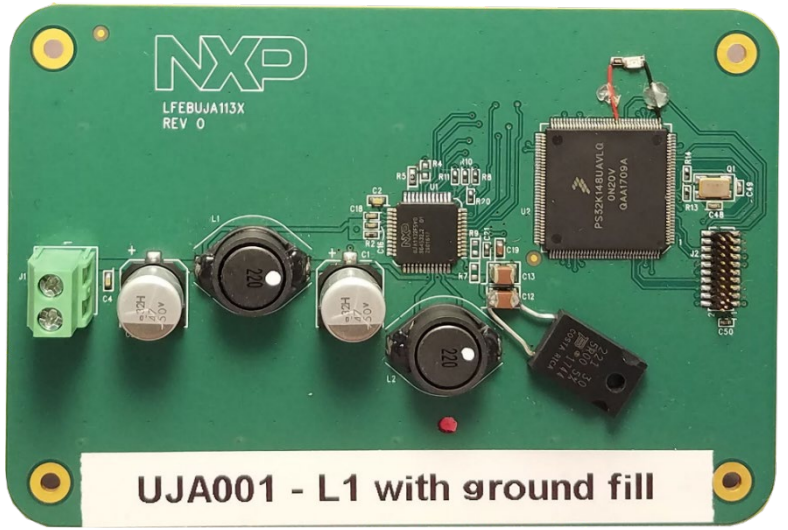
- Analysis:
  - Replacing C1 with two series sets of ceramic capacitors reduced the total capacitance on the board by around 37 µF.
  - This reduced the amount of field available on the board, increasing the demand from the battery
  - PCB inductor improved RE in the upper band

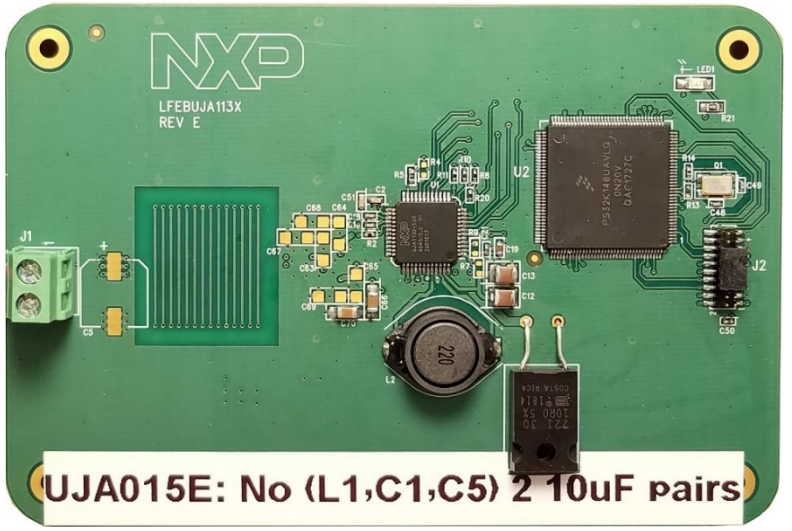
- Cost delta vs Baseline: - $ 0.70

UJA1132 EMC Test Results

- Baseline Design, Version 1 (in **BLUE**), Version 15E (in **BLACK**)
- Change from Version 15D: Rev E PCB
- CE 32 dBµV higher and RE 12 dBµV higher than baseline at ~375 KHz







Baseline Design, Version 1 vs Version 15E

- L1 replaced by PCB trace inductor using Layers 1 and 2, C1 replaced with two series 10 µF ceramic caps (4 parts, 10 µF effective), no C5 installed

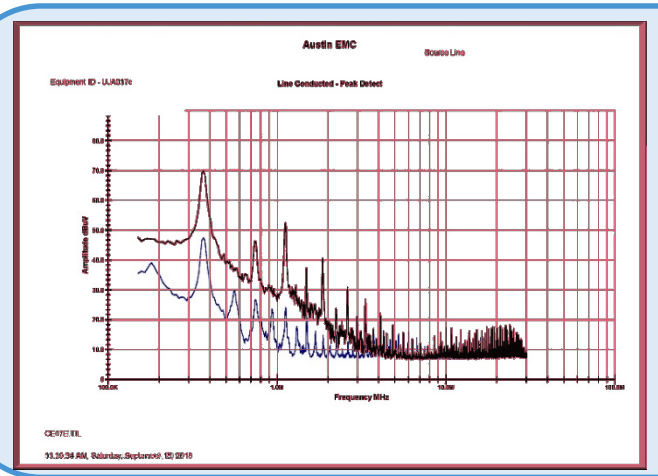
- **CE higher with PCB inductor and with C1 replaced with ceramic capacitors**
  - 1206 package, CL31A106MBHNNNE
  - 33 dBµV higher at PWM switching frequency, ~375 KHz through 8 MHz
- RE 12 dBµV higher at 375 KHz
- RE 20 dBµV lower at 40 MHz

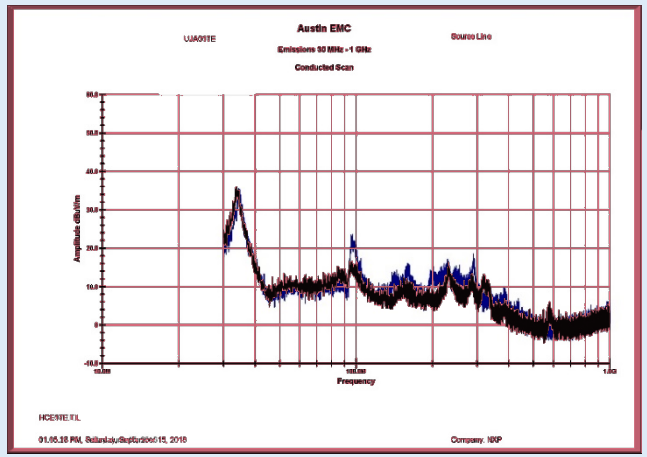
- Analysis:
  - Removing C5 and replacing C1 with two series sets of ceramic capacitors reduced the total capacitance on the board by around 84 µF.
  - This reduced the amount of field available on the board, increasing the demand from the battery
  - PCB inductor improved RE in the upper band

- Cost delta vs Baseline: - $ 1.01

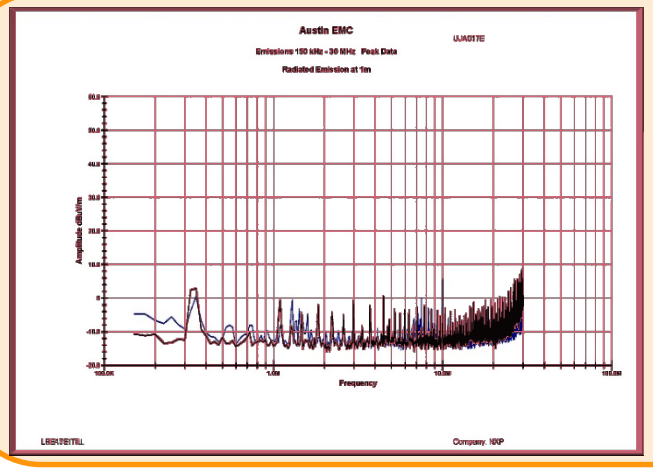
UJA1132 EMC Test Results

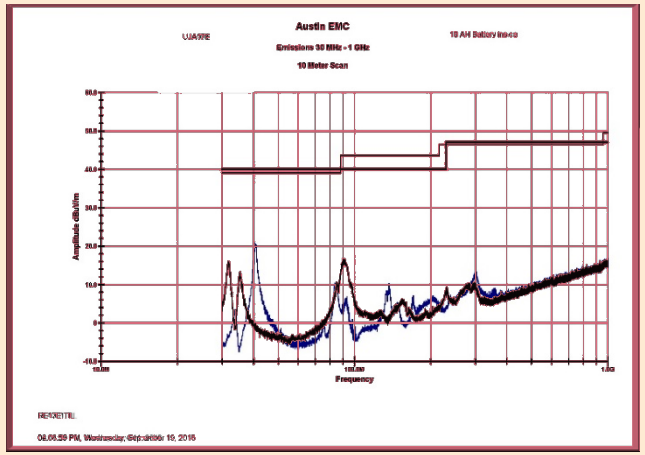
- Baseline Design, Version 1 (in **BLUE**), Version 17E (in **BLACK**)
- Change from Version 17C: Rev E PCB
- CE 22 dBµV higher than baseline at ~375 KHz



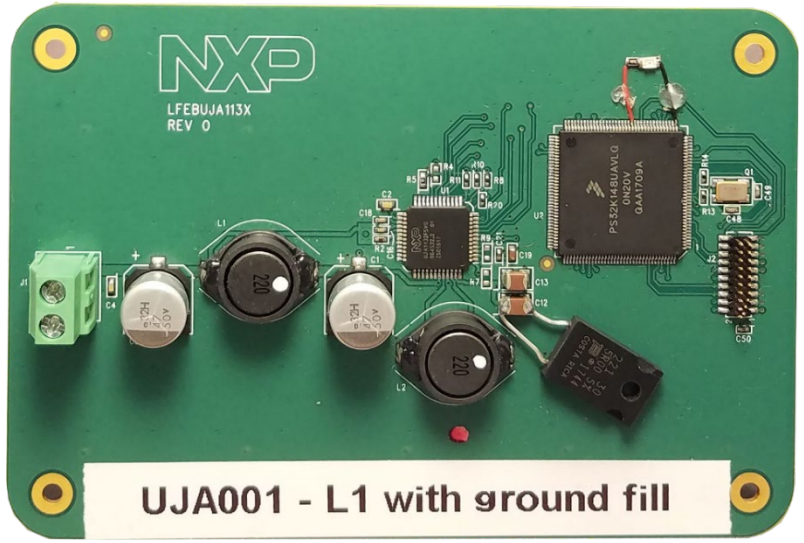


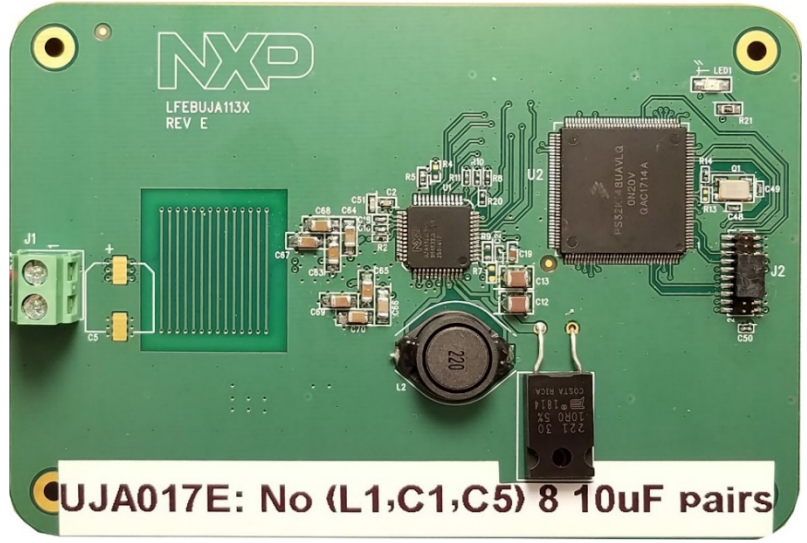
CE





RE





Baseline Design, Version 1 vs Version 17E

- L1 replaced by PCB trace inductor using Layers 1 and 2, C1 replaced with eight series 10 µF ceramic caps (16 parts, 40 µF effective), no C5 installed

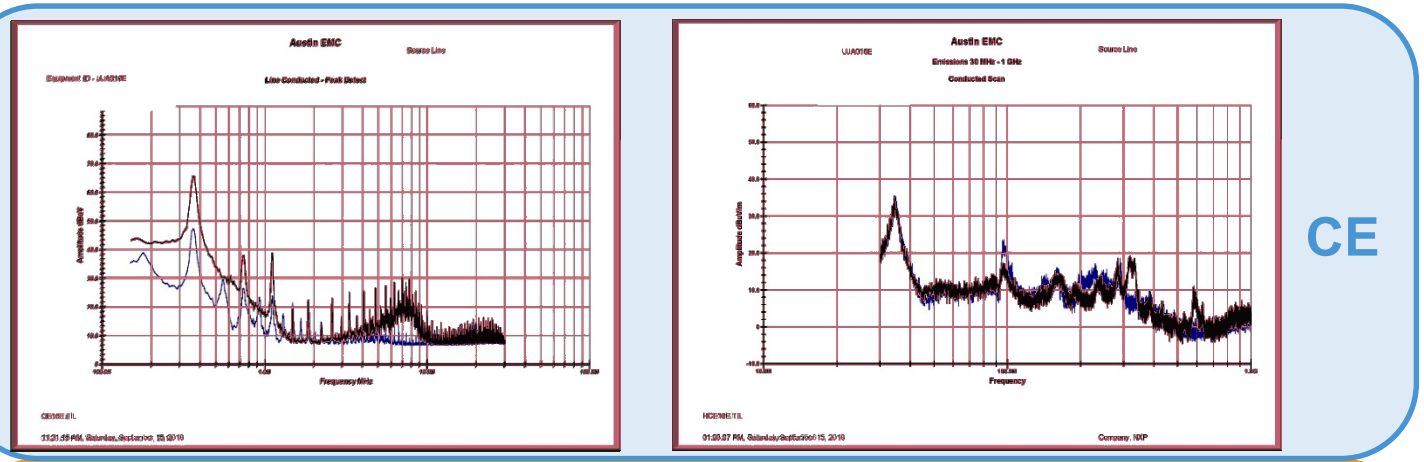
- **CE higher with PCB inductor and with C1 replaced with ceramic capacitors**
  - 1206 package, CL31A106MBHNNNE
  - 28 dBµV higher at PWM switching frequency, ~375 KHz through 1.5 MHz
- RE 8 dBµV higher at 375 KHz
- RE 20 dBµV lower at 40 MHz

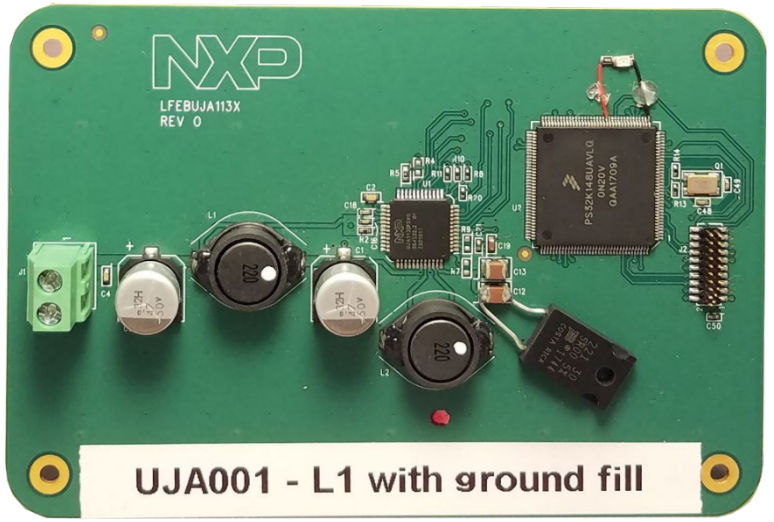
- Analysis:
  - Removing C5 and replacing C1 with eight series sets of ceramic capacitors reduced the total capacitance on the board by around 54 µF.
  - This reduced the amount of field available on the board, increasing the demand from the battery
  - PCB inductor improved RE in the upper band

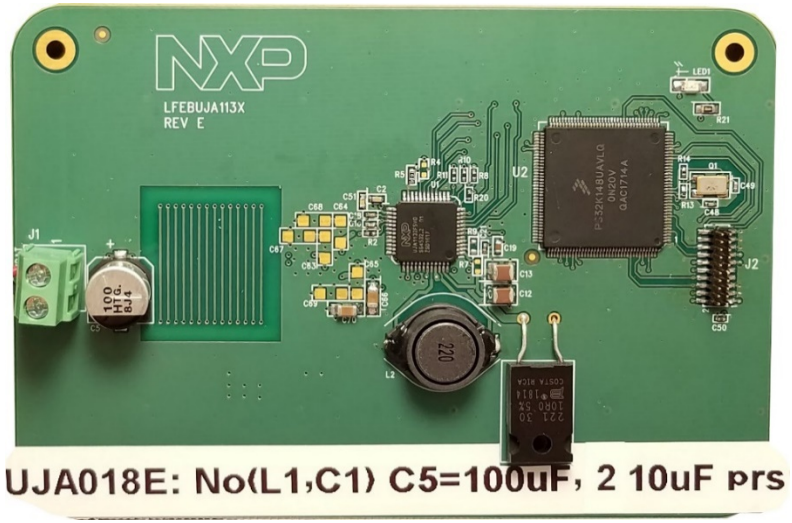
- Cost delta vs Baseline: - $ 0.14

UJA1132 EMC Test Results

- Baseline Design, Version 1 (in **BLUE**), Version 18E (in **BLACK**)
- Change from Version 18C: Rev E PCB
- CE 15 dBµV higher and RE 5 dBµV higher than baseline at ~375 KHz







Baseline Design, Version 1 vs Version 18E

- L1 replaced by PCB trace inductor using Layers 1 and 2, C1 replaced with two series 10 µF ceramic caps (4 parts, 10 µF effective), C5 100 µF installed

- **CE higher with PCB inductor and with C1 replaced with ceramic capacitors**
  - 1206 package, CL31A106MBHNNNE
  - 17 dBµV higher at PWM switching frequency, ~375 KHz
- RE 2 dBµV higher at 375 KHz
- RE 20 dBµV lower at 40 MHz

- Analysis:
  - Increasing C5 to 100 µF and replacing C1 with two series sets of ceramic capacitors increased the total capacitance on the board by around 16 µF.
  - This increased the amount of field available on the board, increasing the demand from the battery
  - PCB inductor improved RE in the upper band

- Cost delta vs Baseline: - $ 0.82

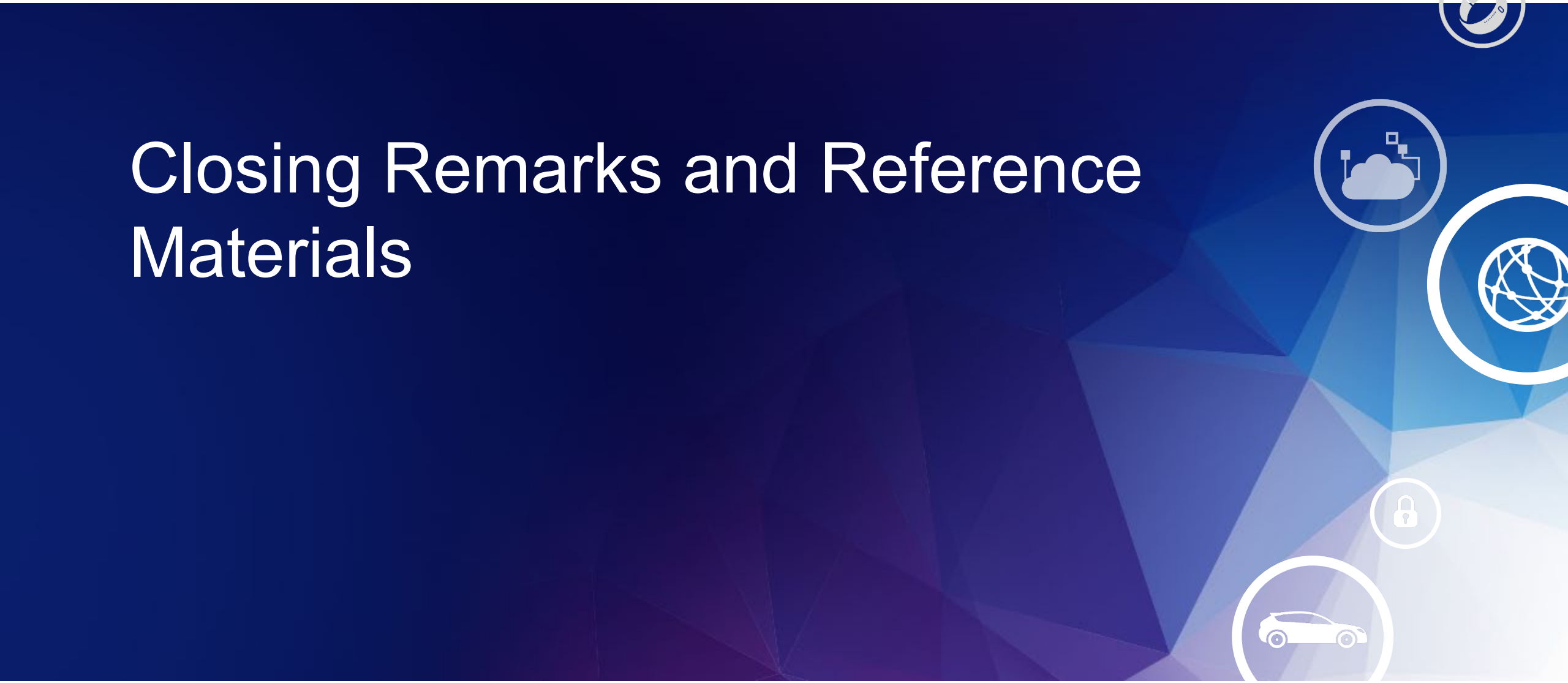
Complied Component Impact: Cost vs EMC

Reference Designator	Part Description	Per Board	Effective Circuit Value	Component Cost	Component Cost VS Baseline	Component Cost No L1 VS Baseline	CE Low Band Impact	CE High Band Impact	RE Low Band Impact	RE High Band Impact	Comments
L1	22 µH 3.1A 59 mΩ DCR	1	22 µh	$0.6815	0.00	(0.68)	43 dBµV from 150 KHz to 8 MHz	10 dBµV at 35 MHz 8 dBµV from 400-700 MHz	12 dBµV from 350 KHz to 1.5 MHz	10 dBµV from 225-300 MHz	L1 reduces CE and RE significantly
L1 flood removed	22 µH 3.1A 59 mΩ DCR	1	22 µh	$0.6815	0.00	(0.68)	40 dBµV from 150 KHz to 8 MHz	10 dBµV at 35 MHz 8 dBµV from 400-700 MHz	12 dBµV from 350 KHz to 1.5 MHz	10 dBµV from 225-300 MHz	Ground fill under L1 has little impact on CE and RE
L1 reverse	22 µH 3.1A 59 mΩ DCR	1	22 µh	$0.6815	0.00	(0.68)	38 dBµV from 150 KHz to 8 MHz	10 dBµV at 35 MHz 8 dBµV from 400-700 MHz	12 dBµV from 350 KHz to 1.5 MHz	8 dBµV from 225-300 MHz	Reversing L1 increases CE and RE slightly
C1	47 µF 50V SMD Electrolytic	1	47 µF	$0.3078	0.00	(0.68)	20 dBµV from 10-30 MHz	10 dBµV at 150 MHz	18 dBµV at 350 KHz	8 dBµV at 300 MHz	C1 reduces CE and RE in lower band. RE in upper band increased slightly
C1-alt 1	10 µF 50V 10% X7R 1210 SMD Ceramic	2	5 µF	$0.7125	0.40	(0.28)	5 dBµV from 150 KHz to 1 MHz	5 dBµV from 30-200 MHz	12 dBµV at 350 KHz	5 dBµV at 150 MHz	Replacing C1 with two 10 µF ceramic capacitors reduces CE and RE low bands slightly. CE upper band increased
C1-alt 1A	10 µF 50V 10% X7R 1210 SMD Ceramic	4	10 µF	$1.4250	1.12	0.44	10 dBµV from 150 KHz to 2 MHz 20 dBµV from 10-30 MHz	15 dBµV at 35 MHz 10 dBµV at 80-200 MHz	30 dBµV from 350 KHz to 1.5 MHz	5 dBµV at 150 MHz	Replacing C1 with four 10 µF ceramic capacitors reduces CE and RE low bands significantly. CE upper band increased
C1-alt 2	47 µF 50V 10% X7R SMD Ceramic	1	47 µF	$3.2335	2.93	2.24	30 dBµV from 150 KHz to 1.5 MHz 30 dBµV at 15 MHz	15 dBµV from 80-200 MHz	18 dBµV at 350 KHz	5 dBµV at 150 MHz	Replacing C1 with one 47 µF ceramic capacitor reduces CE and RE low bands significantly. CE upper band increased slightly.
C1-alt 2A	47 µF 50V 10% X7R SMD Ceramic	2	94 µF	$6.4670	6.16	5.48	25 dBµV from 150 KHz to 1 MHz	5 dBµV from 30-200 MHz	3 dBµV at 350 KHz	5 dBµV at 150 MHz	Replacing C1 with two 47 µF ceramic capacitors reduces CE low band significantly. CE upper and RE lower bands increased slightly
C1-alt 3	10 µF 50V X5R 1206 SMD Ceramic	4	10 µF	$0.2888	(0.02)	(0.70)	25 dBµV from 150 KHz to 30 MHz	5 dBµV from 30-200 MHz	12 dBµV at 350 KHz	18 dBµV from 150-600 MHz	Replacing C1 with four 10 µF ceramic capacitors reduces CE lower band and RE both bands. CE upper band increased
C1-alt 3A	10 µF 50V X5R 1206 SMD Ceramic	8	20 µF	$0.5777	0.27	(0.41)	25 dBµV from 150 KHz to 30 MHz	Negligible	18 dBµV at 350 KHz	18 dBµV from 150-600 MHz	Replacing C1 with eight 10 µF ceramic capacitors reduces CE lower band and RE both bands. CE upper band increased
C1-alt 3B	10 µF 50V X5R 1206 SMD Ceramic	16	40 µF	$1.1554	0.85	0.17	30 dBµV from 150 KHz to 30 MHz	10 dBµV from 400-1000 MHz	20 dBµV at 350 KHz	20 dBµV from 150-600 MHz	Replacing C1 with sixteen 10 µF ceramic capacitors reduces CE lower band and RE both bands. CE upper band increased
C5	47 µF 50V SMD Electrolytic	1	47 µF	$0.3078	0.00	(0.68)	20 dBµV from 10-30 MHz	10 dBµV at 150 MHz	18 dBµV at 350 KHz	8 dBµV at 300 MHz	C5 reduces CE and RE in lower band. RE in upper band increased slightly
C5-alt 1	100 µF 50V SMD Electrolytic	1	100 µF	$0.2009	(0.11)	(0.79)	Negligible	5 dBµV from 400-1000 MHz	8 dBµV at 350 KHz 8 dBµV at 5 MKHz	8 dBµV from 150-600 MHz	Replacing C5 with one 100 µF electrolytic capacitor reduces CE low bands and RE both bands slightly.
Two dialectrics	N/A	1	N/A	$0.0000	0.00	0.00	Negligible	10 dBµV from 30-800 MHz	5 dBµV from 350 KHz to 2 MHz	Negligible	Lower effective impedance of the power transmission line increased the CE in the upper band and RE in the lower band.
Three dialectrics	N/A	1	N/A	$0.0000	0.00	0.00	Negligible	10 dBµV from 30-800 MHz	Negligible	10 dBµV from 30-800 MHz	Lower effective impedance of the power transmission line increased the CE and RE in the upper bands. No significant improvement using 3 dialectrics vs 2
PCB Inductor	~268 nH	1	~238 nH	$0.0000	(0.68)	(0.68)	10 dBµV from 150 KHz to 30 MHz 20 dBµV from 1-10MHz	20 dBµV from 30-1000 MHz	3 dBµV at 350 KHz	10 dBµV at 900 MHz	Adding a PCB inductor significantly lowers the CE both bands and the RE upper band. RE lower band lowered slightly.

Complied Component Impact: Cost VS EMC

- Capacitor ESR has significant impact on EMC
  - Electrolytic ~ 0.5 ohms
  - Ceramic ~ 0.010 ohms
- Proper use of ceramic capacitors can provide EMC performance similar to that resulting from the use of series inductor
  - Reduced board space
  - Reduced system cost (example inductor cost $0.68)
- Using 1206 package capacitors provides good value and EMC performance vs electrolytic or larger package ceramic capacitors
  - $0.31 (47 µF SMD electrolytic)
  - $6.46 (47 µF SMD ceramic, two pieces required for off battery use in Automotive applications)
  - $0.71 (10 µF 1210 ceramic, two pieces required for off battery use in Automotive applications)
  - $0.14 (10 µF 1206 ceramic, two pieces required for off battery use in Automotive applications)
- PCB Inductors can provide improved EMC performance
  - Require increased board space

Closing Remarks and Reference Materials



Fundamentals to Remember

- Electromagnetic fields travel in the space between the conductors, not in the conductors
- The switching speed of the transistors determines the frequency of operation, not the clock rate
- Switching speed determines the power supply requirements, not just the DC current specification
- Signal and power connections need to be one dielectric from ground for their entire length (including layer transitions)
  - Adjacent plane
  - Co-planar trace
- There is no such thing as a noisy ground, just poor transmission line design
- To quote Dr. Todd Hubing, “Thou shalt not split ground.”
- Any compromises to these rules will increase system noise and must be done as carefully considered engineering decisions.

Special Thanks to My Mentors

- Rick Hartley (PCB designer extraordinaire) started me down this trail in 2004 at PCB West.
- Ralph Morrison (author, inventor and musician) has patiently and steadily moved me from the fuzzy realm of “circuit theory” and “black magic” into the solid world of electromagnetic field physics.
- Dr. Todd Hubing (researcher and professor) whose research at UMR and Clemson has provided solid evidence that Maxwell and Ralph have got it right.

High Speed Design Reading List

- Right the First Time: A Practical Handbook on High Speed PCB and System Design Volumes I & II, Lee W. Ritchey. Speeding Edge, ISBN 0-9741936-0-7
- High Speed Digital System Design: A Handbook of Interconnect Theory and Practice, Hall, Hall and McCall. Wiley Interscience 2000, ISBN 0-36090-2
- High Speed Digital Design: A Handbook of Black Magic, Howard W. Johnson & Martin Graham. Prentice Hall, ISBN 0-13-395724-1
- High Speed Signal Propagation: Advanced Black Magic, Howard W. Johnson & Martin Graham. Prentice Hall, ISBN 0-13-084408-X
- Signal Integrity Simplified, Eric Bogatin. Prentice Hall, ISBN 0-13-066946-6
- Signal Integrity Issues and Printed Circuit Design, Doug Brooks. Prentice Hall, ISBN 0-13-141884-X

(Slide compliments of Ralph Morrison, Consultant)

EMI Reading List

- PCB Design for Real-World EMI Control, Bruce R. Archambeault. Kluwer Academic Publishers Group, ISBN 1-4020-7130-2
- Digital Design for Interference Specifications: A Practical Handbook for EMI Suppression, David L. Terrell & R. Kenneth Keenan. Newnes Publishing, ISBN 0-7506-7282-X
- Noise Reduction Techniques in Electronic Systems, 2nd Edition, Henry Ott. John Wiley and Sons, ISBN 0-471-85068-3
- Introduction to Electromagnetic Compatibility, Clayton R. Paul. John Wiley and Sons, ISBN 0-471-54927-4
- EMC for Product Engineers, Tim Williams. Newnes Publishing. ISBN 0-7506-2466-3
- Grounding & Shielding Techniques, 5th Edition, Ralph Morrison. John Wiley & Sons, ISBN 0-471-24518-6

Additional References

- Ralph Morrison's Books, Available from Wiley and Amazon:
  - Digital Circuit Boards: Mach 1 GHz.
  - Fast Circuit Boards: Energy Management.
- The Best PCB design conference website: http://pcbwest.com/
- Doug Smith's website: http://www.emcesd.com/ (He is the best at finding what is wrong! Lots of useful app notes.)
- IEEE EMC Society website: http://www.emcs.org/
- Clemson's Automotive Electronics website: http://www.cvel.clemson.edu/auto
- Clemson's EMC website: http://www.cvel.clemson.edu/emc
- Missouri University of Science and Technology website: http://www.mst.edu/about/
- IPC — Association Connecting Electronics Industries website: http://www.ipc.org/default.aspx

It’s All About the **Space**!

“Buildings have walls and halls.

People travel in the halls not the walls.

Circuits have traces and **spaces**.

Energy and signals travel in the **spaces** not the traces.”

- Ralph Morrison

Summary and Q&A

- Electromagnetic fields travel in the **space** between the conductors
- Movement of EM fields induces current flow in the conductors, not visa versa
- Well-defined transmission lines are critical for good power supply design
- Switching speed of the output devices determines the requirements of the power supply
- Using the correct physical size of capacitors in the correct place are key to reducing power supply noise
- Don’t expect anything from the power supply components that they cannot deliver
  - Distance from the switch tells you how long it takes to request the energy
  - Size of the package and ESR determine the amount of energy you get in each wave
- The black magic is tamed!
- Q&A

Thank you! Please remember to fill out your survey forms!

AMF-AUT-T3882 A Novel Approach to Power Distribution

SECURE CONNECTIONS
FOR A SMARTER WORLD