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MC33813/4 APPLICATION NOTE

HOW TO SETUP, HOW TO DEAL WITH FAULT

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Contents

1 Power

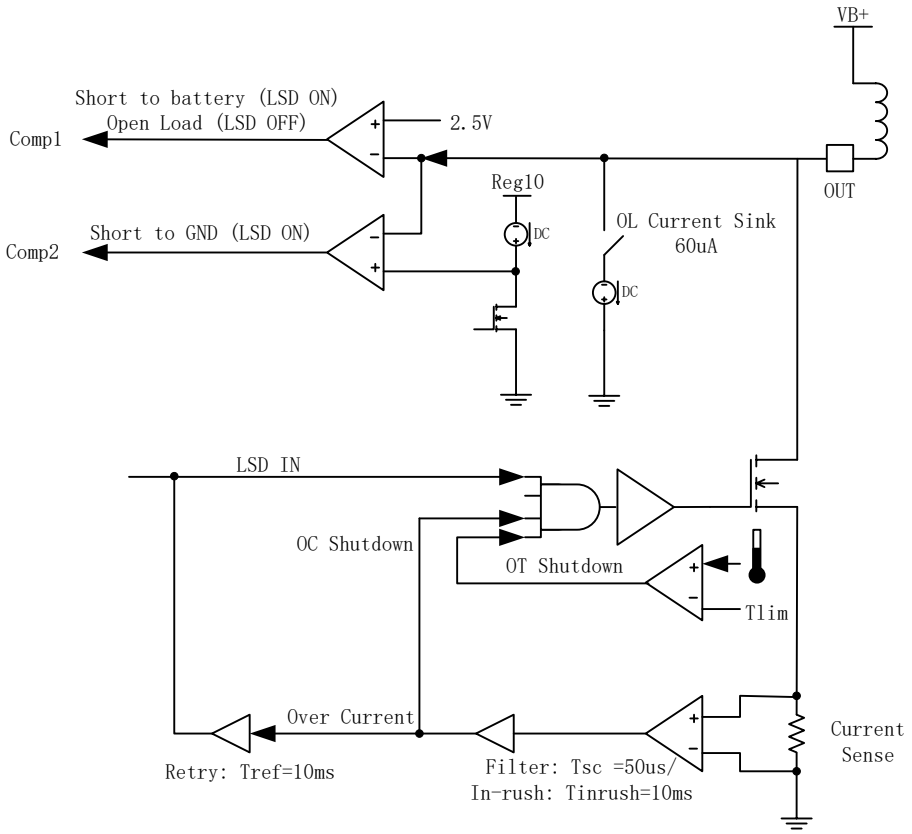
State Behaviour	SLEEP	LOGIC _UV	SUP_RST	MCU_RST	NORMAL	SHUTDOWN
Duration	unlimited	unlimited	condition dependent	128us	unlimited	unlimited
Drive RESETB low	no	disabled	yes	yes	no	no
Watchdog counter	disabled	disabled	disabled	disabled	Active (reset on state entry)	Active
SPI	No access	No access	No access (MCU in reset)	No access (MCU in reset)	Accessible	Accessible

State Behaviour		SLEEP	LOGIC _UV	SUP_RST	MCU_RST	NORMAL	SHUTDOWN
MCU/User registers		default	default	default	default	SPI R/W	SPI R/W
Test/Internal registers [1]	Fuse mirror	default	default	No change	No change	SPI R/W	SPI R/W
	other	default	default	No change	No change	SPI R/W	SPI R/W
Testmode		disabled	Disabled	No change?	No change?	HW/SPI Entry, SPI exit	HW/SPI Entry, SPI exit
Oscillator		disabled	disabled	enabled	enabled	enabled	enabled
Fuse			disabled	disabled	disabled	Testmode SPI read/write	Testmode SPI read/write
Internal regulators		off	on	on	on	on	on
VPP regulator		off	off	on	on	on	on
VCC regulator		Off	off	on	on	on	on
VPROT regulator		Off	off	Enabled (default)	Enabled (default)	SPI R/W	SPI R/W
Low side output drivers (LAMPOUT, INJOUT*, O2HOUT, IGNOUT*, TACHOUT, ROUT*)		off	off	off (default)	off (default)	Enabled (controlled SPI R/W, input pins and BATSW)	Digital Enabled (SPI R/W, input pins, however analog is gated off except for ROUT2 when controlled by BATSW)
IGN current sense		disabled	disabled	Enabled	Enabled	Enabled	Enabled
Low side driver inputs (INJIN*, O2HIN, IGNIN*, RIN*)		Off (default)	off (default)	Off (default)	Off (default)	Enabled (controlled by SPI R/W, input pins)	Digital Enabled, but analog drivers forced off
IS09141 interface		disabled	disabled	enabled	enabled	enabled	enabled
MRX output		disabled	disabled	active	active	active	active
MTX input		Disabled (No VCC)	Disabled (No VCC)	active	active	active	active
VRS		Disabled	Disabled	Enabled	Enabled	Enabled	Enabled
VRSOUT		Disabled (1'b1)	Disabled(1'b1)	1'b1 (MCU in reset)	1'b1 (MCU in reset)	From VRS	From VRS
BATSW		Disabled (1'b0)	Disabled (1'b0)	KEYSW state	KEYSW state	(KEYSW| PWREN) state or LED driver	(KEYSW| PWREN) state or LED driver
KEYSW block		enabled	enabled	enabled	enabled	enabled	enabled

2 Low side driver (LSD)

Relay 2 Driver		Retry Enable	Shutdown DisableSD D	x	OL Current Sink Enable	In-Rush Delay	OR/AND	PWM Freq. 1	PWM Freq. 0
	Reset	(0)	(0)	(0)	(1)	(0)	(0)	(0)	(0)

Relay 2 Driver Faults		Faults	x	x	x	Open Load OL	Overcurrent OC	Overtemp OT	Short Gnd SG
	Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)



1. Open load: Comp 1=0 && LSD OFF
2. Over current: Short to Battery =1 (Comp1=1 && LSD ON) && Over current =1
3. Over temperature: OT shutdown=1
4. Short to GND: Comp2=1 &&LSD ON

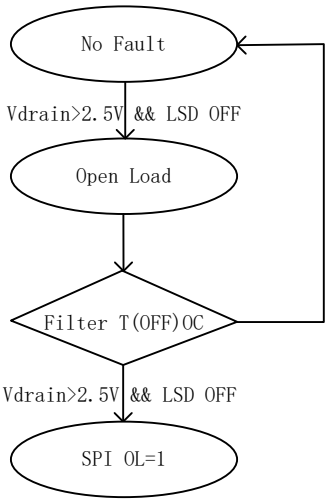
In the OFF state, an open load fault is detected if the drain voltage is less than 2.5V. In the ON state, a short to battery load fault is detected if the Drain voltage exceeds 2.5V. A 60uA pull down current source is connected to the FET drain and the drain voltage is sensed by the comparator 1. The pull down current source used for fault detection may be disabled via SPI in applications (OL current sink enable=0) such as when the output is used to drive a LED, or in test configurations that involve the measurement of leakage current. In this case, short to battery (over current) and open load which comes from comp1 will not be reported.

The driver block also includes another comparator(comp2) circuit that can detect a short to ground fault when ON. The comparator compares the voltages generated by

(Ids*Rdson) in the output FET and in a reference FET using a pull up current source.

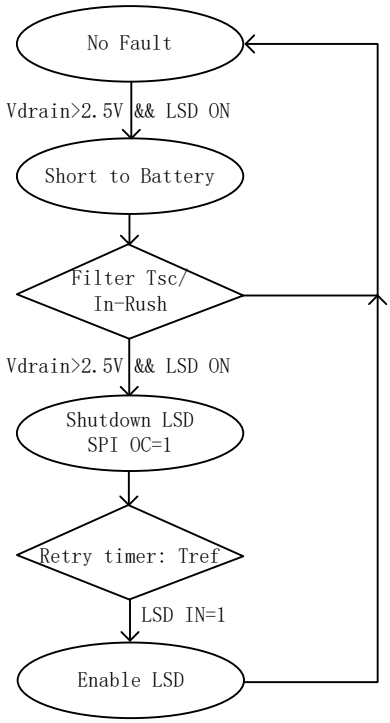
The fault register can be only cleared by write '0' through SPI. If the bits be cleared automatically, please check the IC maybe reset by faults or watchdog.

2.1 Open Load



The LSD can detect an Open Load fault when LSD IN=0, and Vdrain>2.5V (Comp 1=1) (Fig. 1). If Open Load occurs, the digital block runs Open Load fault filter timer of a duration $t_{(OFF)OC}$ (minimum 100us), and if Vdrain>2.5V is still there, digital core will annunciate an Open Load bit in the SPI status register. If the Open Load Current Sink disabled, this function is not functional.

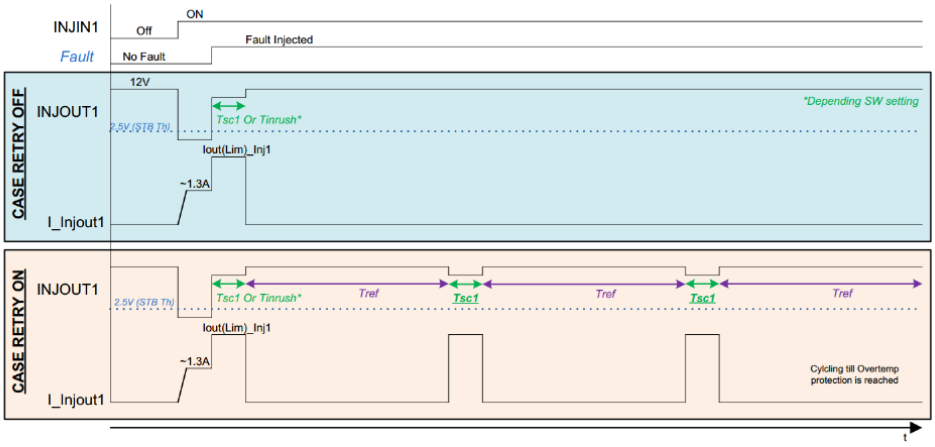
2.2 Short to Battery/Over current



The LSD can detect a short to battery load fault when the LSD IN=1, and

Vdrain>2.5V (Comp 1=1) (Fig. 1). If short to battery occurs, digital block runs a current limit fault filter timer of a duration t_{SC} (nominally 50us, unless the in-rush delay timer is enabled, then it is 10ms nominal), and if Vdrain>2.5V is still there (Comp1 =0), it will shut down the LSD and annunciate a short to battery condition by setting the Over Current bit in the SPI status register. The digital block will then run an output retry timer of a duration, t_{REF} (nominally 10ms), and will enable the driver again if the LSD IN is still ON. If the over current condition is still detected, the Injector driver will be cycled on/off again with a duty cycle of t_{SC} /t_{REF} until the either the over current condition is no longer present, or an over temperature condition is detected.

Note that the low side drivers have a programmable timer setting for t_{SC} to allow it to be set to 10ms when the output is connected to loads which can have high startup or in-rush currents.



2.3 Short to Ground

The LSD can detect a Short to GND (SG) load fault when the LSD IN=1, and Vdrain<Vth (Comp2 =1), the Vth value come from a reference FET, Vth= I_{DS}*$R_{DS(ON)}$ (Fig. 1). FET I_{DS} that sets the detection threshold. This is typically greater than 100mA and the pull down current source connected to the drain and used for the other load fault comparator does not affect the fault detection of this comparator. If Shot to GND is detected, the digital block will set the Short to Ground bit in the SPI status register.

But according to my test it shows:

--Injectors: the SG threshold is Ids= 100mA, with Rds=0.6OHM, the Vdrain=60mV

--Rout1: the SG threshold is Ids= 110mA, with Rds=0.5OHM, the Vdrain=55mV

--Rout2: the SG threshold is Ids= 30mA, with Rds=1.5OHM, the Vdrain=45mV

--Lamp: the SG threshold is Ids= 38mA, with Rds=1.5OHM, the Vdrain=57mV

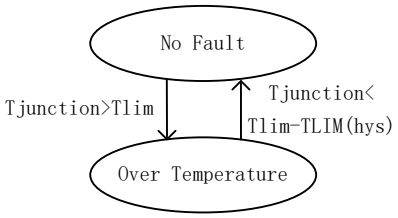
Around 55mV

2.4 Open Load Current Sink

If Open Load Current sink is disabled (SPI bit set to “0”). There will be a pull down

current source on the output FET drain, the Comp1 and Comp2 will keep logic “1”, Open load and short to GND cannot be detected. When the output is used to drive a LED, or in test configurations that involve the measurement of leakage current. In this case, short to battery (over current) and open load which comes from comp1 will not be reported.

2.5 Over Temperature



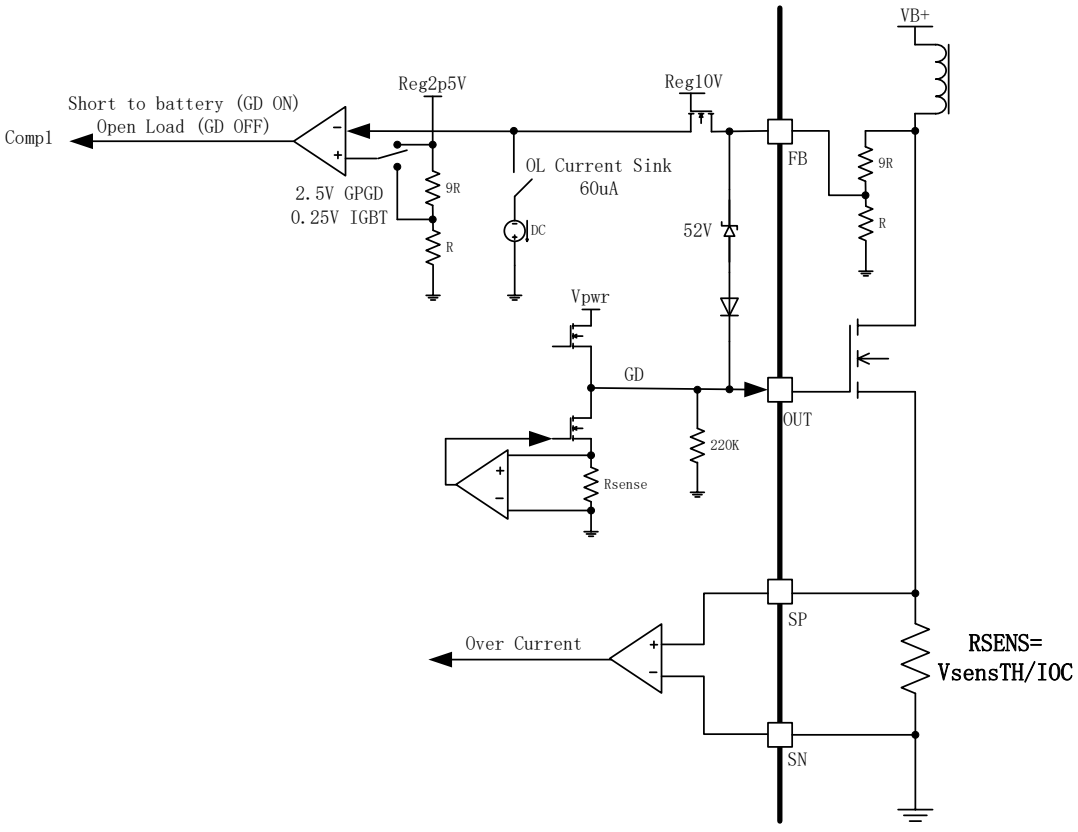
The LSD has an internal temperature sensor that derives a logical level signal T_{lim}. The over temperature limit, T_{lim} is within the range of 155ºC to 185ºC and there is a hysterics range $T_{LIM(hys)}$ in the temperature limit of 5ºC to 15ºC. If the temperature limit is exceeded, the digital block will shut down the gate drive signal and set an Over Temperature bit in the SPI status register. When the junction temperature falls below the temperature limit minus the hysteresis value, the digital block will enable the normal operation.

3 Pre-Driver

O2 Heater Pre-driver		GPGD/IGN Select	Retry Enable	x	OL Current Sink	x	OR/AND	PWM Freq. 1	PWM Freq. 0
	Reset	(0)	(0)	(0)	(1)	(0)	(0)	(0)	(0)
Ignition 1 Pre-driver		GPGD/IGN Select	Retry Enable	x	OL Current Sink	x	OR/AND	PWM Freq. 1	PWM Freq. 0
	Reset	(1)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
Ignition 2 Pre-driver		GPGD/IGN Select	Retry Enable	x	OL Current Sink	x	OR/AND	PWM Freq. 1	PWM Freq. 0
	Reset	(1)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Reg #	Hex			7	6	5	4	3	2	1	0
7	7	O2 Heater Pre-driver Faults		Faults	x	x	x	Open Load OL	Overcurrent OC	x	x
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
8	8	Ignition 1 Pre-driver Faults		Faults	x	x	x	Open Load OL	Overcurrent OC	x	x
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
9	9	Ignition 2 Pre-driver Faults		Faults	x	x	x	Open Load OL	Overcurrent OC	x	x
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Pre-Driver can be configured as GPGD or IGBT. The port can detect open load fault in OFF state and Overcurrent in ON and OFF state by SENSP and SENSN Delta voltage.



3.1 Open Load/Short to Battery

The Pre-Drever can detect an Open Load fault when GD is Low, and Vdrain>VFLT_TH(2.5V for GPGD or 0.25V for IGBT)(Comp 1=1). If Open Load occurs, the digital block runs Open Load fault filter timer of a duration $t_{(OFF)OC}$ (minimum 100us), and if Vdrain>VFLT_TH still there, digital core will annunciate an Open Load bit in the

SPI status register. If the Open Load Current Sink disabled, this function is not functional.

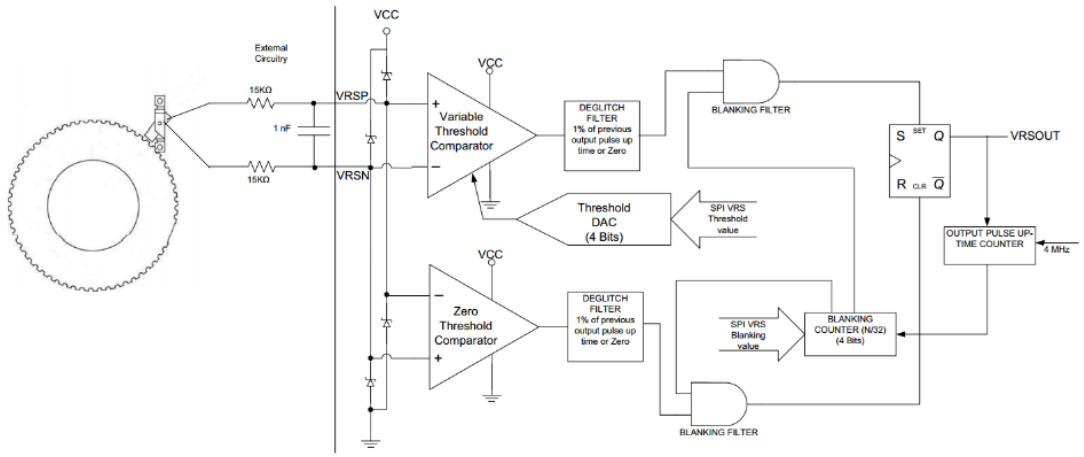
On the opposite, when GD is High, and Vdrain>VFLT_TH(2.5V for GPGD or 0.25V for IGBT)(Comp 1=1), IC diagnose the Drain Short to Battery.

3.2 Over current

If VsenseP-VSenseN>VsensTH(0.2V for one channel, 0.4V for two channel), IC report overcurrent fault. So, the over current threshold(IOC) decided by external sense resistor.

4 VRS

13	D	VRS Miscellaneous Parameters		Man./Auto	Disable VRS	x	High/ Low Ref	De-glitch	Gnd VRSN	Inv Inputs	Disable 2.5 V CM
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)



4.1 Manuel and Automatic mode

4.1.1 Manuel Mode

Configuration

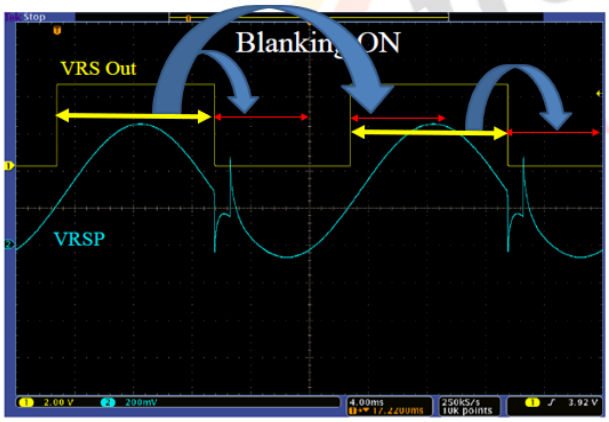
11	B	VRS Engine Running Parameters		Threshold 3	Threshold 2	Threshold 1	Threshold 0	Filter Time 3	Filter Time 2	Filter Time 1	Filter Time 0
			Reset	(0)	(1)	(0)	(1)	(0)	(0)	(1)	(1)

Control:

13	D	VRS Engine Cranking Parameters		Threshold 3	Threshold 2	Threshold 1	Threshold 0	Filter Time 3	Filter Time 2	Filter Time 1	Filter Time 0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

In real SPI control, the configuration table is setup once when power on, and control parameters can be changed and resent continuously during engine running. The Threshold and Filter Time in Control parameter table have higher priority than Configuration ones.

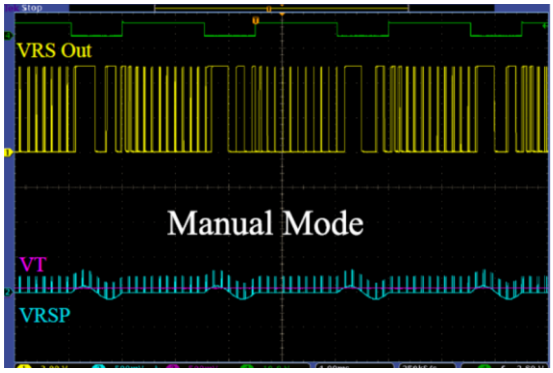
Filter time/ blanking time is based on last VRS high duration time and used on next two toggle. As below in red.

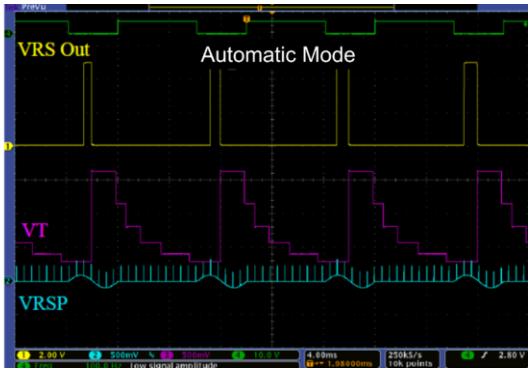


The Threshold and Filter Time is only available when Man/Auto(Confi#13) is set to 0 (Manuel Mode).

4.1.2 Automatic Mode

Automatic mode is functional when Engine starts. During this period, VRS has high frequency noise as below（Blue line）. Manuel mode cannot avoid the noise (left), but Automatic mode can avoid it by changing threshold automatically according to detect the sin wave peak voltage.



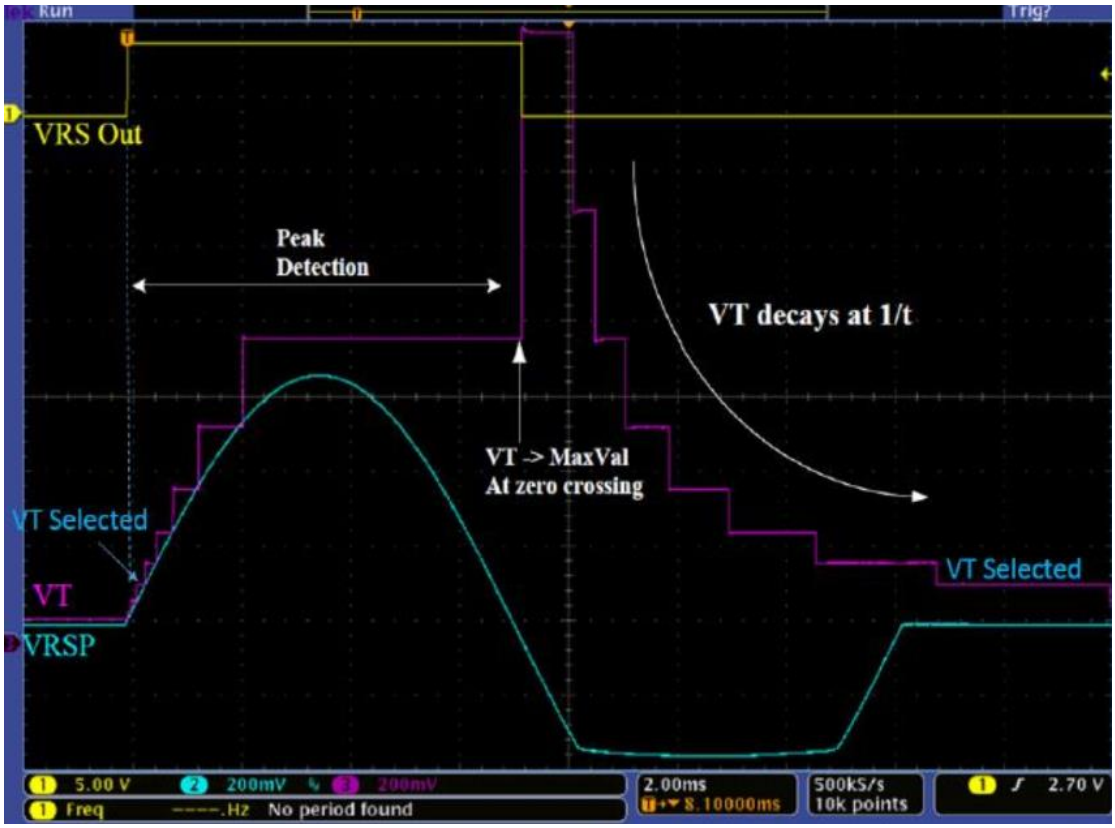


Mantissa and Exponent parameters defined in the VRS Automatic mode parameters register set the decay time of the system.

The mathematical formula is:

E = log2[(Vpeak x Tau)/18.1] - 4 truncated

M = {[(Vpeak x Tau)/18.1]/2E} - 16 rounded to nearest integer



12	C	VRS Automatic Parameters		mantiss 8	mantiss 4	mantiss 2	mantiss 1	exponent 8	exponent 4	exponent 2	exponent 1
			Reset	(0)	(0)	(1)	(0)	(0)	(0)	(0)	(1)

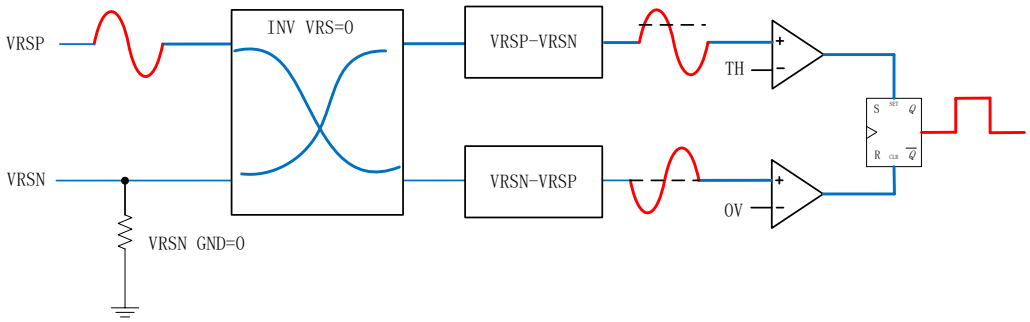
4.2 GND VRSN and Dis 2.5Vref

There is a pull up 2.5V on both VRSP and VRSN, and a pull down to GND on VRSN pin. If VRSP/N is connected externally, the internal 2.5V pull up and pull down to GND have no influence on them. If VRSN in floating condition, there are four possibilities as below:

4.2.1 VRS single-ended input

VRSN GND=1 (pull down), 2.5V ref=1 （no pull up）

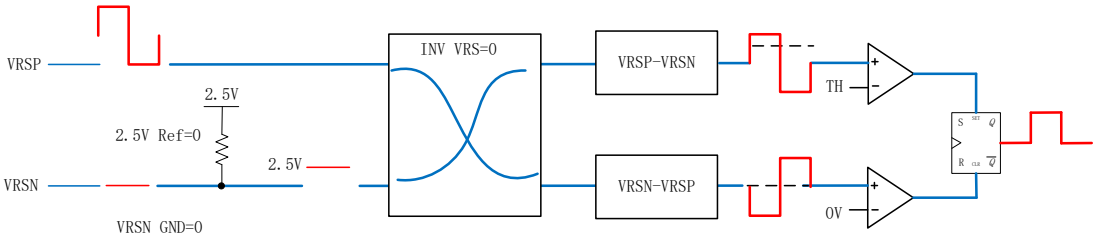
To use the VRS inputs in a single-ended configuration, the “GND VRSN” bit in the SPI Configuration register must be set to indicate to the 33814 that this mode is being used. The VRS is then connected between the VRSP input and ground. The default for this bit is zero (0), indicating the differential mode is selected. Note that in the single ended configuration, the 2.5 Volt reference should be disconnected (Disable 2.5V CM bit should be set to 1) when using a Variable Reluctance Sensor.



4.2.2 Hall Sensor

VRSN GND=0 (no pull down), 2.5 ref=0 （pull up）, this condition is used when VRSP signal above 0V and single ended, for example Hall sensor.

Hall effect sensor can be used instead of a VRS. To do so, the bits GND VRSN and disable 2.5 V ref must be 0 and the VRSN pin must not be connected. In this case, the voltage on VRSN is 2.5 V and the 0 crossing can be done even if low state output of the hall effect is 0 V or little higher.



4.2.3 Others

Notice:

1. Cannot set VRSN GND=1 with 2.5 ref=0（connect）at the same time.
2. Not recommend VRSNGND=0 with 2.5V ref=1（disconnect）. There will be noises on VRSN may influence the calculation accuracy. If in single-ended mode, VRSN is recommended be connected to GND externally.