

Pin Setting

The screenshot shows the S32 Design Studio interface for configuring pins. The main window displays a list of pins and their configurations. The 'PortContainer_0_BOARD' is selected, and the 'S32K312_172HDQFP' package is used. The configuration panel on the right shows the 'Pin' configuration for the selected port.

Pin	名称	标识符	SIUL2	eMIOS	FXIO	LPSF
34	PTD16		SIUL2.gpi...	eMIOS_0...		LPSF
35	PTD15		SIUL2.gpi...	eMIOS_0...	FXIO:fxio_...	LPSF
36	PTD9		SIUL2.gpi...	eMIOS_0...	FXIO:fxio_...	
37	VSS166					
38	V11154					
39	PTA31		SIUL2.gpi...	eMIOS_1...	FXIO:fxio_...	LPSF
40	PTD14		SIUL2.gpi...	eMIOS_0...		LPSF
41	PTD13		SIUL2.gpi...	eMIOS_0...	FXIO:fxio_...	LPSF
42	PTB18		SIUL2.gpi...	eMIOS_1...	FXIO:fxio_...	LPSF
43	PTB19		SIUL2.gpi...	eMIOS_1...	FXIO:fxio_...	LPSF
44	PTB20		SIUL2.gpi...	eMIOS_1...	FXIO:fxio_...	LPSF
45	PTB21		SIUL2.gpi...	eMIOS_1...	FXIO:fxio_...	LPSF
46	PTB8		SIUL2.gpi...	eMIOS_0...	FXIO:fxio_...	LPSF
47	PTB5		SIUL2.gpi...	eMIOS_0...		LPSF
48	PTB4		SIUL2.gpi...	eMIOS_0...		LPSF
49	PTC3		SIUL2.gpi...	eMIOS_0...		LPSF

#	外设	信号	箭头	已路由的引脚/信号	标识符	方向	Safe Mode Control	Pull Select	Pullup Enable	Pad keep enable	Output Invert
63	LP12C1	lpi2c1_scl	<->	[63] PTD9	n/a	Input/Output	Disable	Full/Down	Enabled	Disabled	Don't invert
64	LP12C1	lpi2c1_sda	<->	[64] PTD8	n/a	Input/Output	Disable	Full/Down	Enabled	Disabled	Don't invert
40	LP12C0	lpi2c0_scl	<->	[40] PTD14	n/a	Input/Output	Disable	Pullup	Enabled	Disabled	Don't invert
41	LP12C0	lpi2c0_sda	<->	[41] PTD13	n/a	Input/Output	Disable	Pullup	Enabled	Disabled	Don't invert

Driver Setting

Clock_Ip_ReferencePoints

The screenshot shows the S32 Design Studio interface for configuring clock sources. The 'Peripheral Clock View' is selected, and the 'ClockConfig0' configuration is shown. The clock tree diagram on the left shows the hierarchy of clock sources, including a 32 kHz Slow IRC and a 48 MHz Fast IRC, both connected to the SCS_CLK. The table on the right lists the clock sources and their configurations.

时钟名称	启用	控制	源代码	分频器	Div类型	频率	监视器	变频	高频
ADCO_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
ADC1_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
BCTU0_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
CLKOUT_STANDB...	<input checked="" type="checkbox"/>		FIRC_CLK	/2		24 MHz			
CMP0_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
CMP1_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
CRCC0_CLK	<input checked="" type="checkbox"/>		AIPS_PLAT_CLK	/1		60 MHz			
DCM0_CLK	<input checked="" type="checkbox"/>		DCM_CLK	/1		30 MHz			
DMA0MUX0_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
DMA0MUX1_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
EDMA0_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
EDMA0_TCD0_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
EDMA0_TCD10_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
EDMA0_TCD11_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
EDMA0_TCD12_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
EDMA0_TCD13_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
EDMA0_TCD14_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
EDMA0_TCD15_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
EDMA0_TCD16_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
EDMA0_TCD17_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
EDMA0_TCD18_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
EDMA0_TCD19_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
EIM0_CLK	<input checked="" type="checkbox"/>		AIPS_PLAT_CLK	/1		60 MHz			
EMIOS0_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
EMIOS1_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
ERMO_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
FLASH0_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			

workspaceS32DS.3.5 - S32K312_i2c_try2implement_3_4_success/src/main.c - S32 Design Studio for S32 Platform

File Edit Source Refactor Navigate Search Project 配置工具 时钟 Run PEMicro Window Help

Workspace: S32K312_i2c_try2impleme

功能组: ClockConfig0

时钟显示: 时钟表

在图中搜索元素

概述 Peripheral Clock View 代码预览 寄存器 详细信息 时钟消耗

RUN模式: DRUN | Clock Development Error Detect [Disabled] |
 Clock User Mode Support [Disabled] | Clock Disable Ram Wait States Config [Disabled] | Clock Disable Flash Wait States Config [Disabled] |
 Clock Loops Timeout: 50000 | Clock Timeout Method: OSIF_COUNTER_DUMMY |
 Clock Register Values Optimization: DISABLED | Get Clock Frequency API Disabled | Enable Cmu Notification: Disabled | CmuNotification NULL_PTR |
 Enable PrepareMemoryConfig: Disabled | ClockPrepareMemoryConfig NULL_PTR

时钟名称	启用	控制	源代码	分频器	Div类型	频率	监视器	休眠	高频
FLASH0_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
FLEXCAN0_CLK	<input checked="" type="checkbox"/>		FIRC_CLK	/2		24 MHz			
FLEXCAN1_CLK	<input checked="" type="checkbox"/>		FIRC_CLK	/2		24 MHz			
FLEXCAN2_CLK	<input checked="" type="checkbox"/>		FIRC_CLK	/2		24 MHz			
FLEXCAN3_CLK	<input checked="" type="checkbox"/>		FIRC_CLK	/2		24 MHz			
FLEXCAN4_CLK	<input checked="" type="checkbox"/>		FIRC_CLK	/2		24 MHz			
FLEXCAN5_CLK	<input checked="" type="checkbox"/>		FIRC_CLK	/2		24 MHz			
FLEXIO0_CLK	<input checked="" type="checkbox"/>		AIPS_PLAT_CLK	/1		60 MHz			
INTM_CLK	<input checked="" type="checkbox"/>		AIPS_PLAT_CLK	/1		60 MHz			
LCU0_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
LCU1_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
LP12C0_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LP12C1_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LPSP10_CLK	<input checked="" type="checkbox"/>		AIPS_PLAT_CLK	/1		60 MHz			
LPSP11_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LPSP12_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LPSP13_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LPUART0_CLK	<input checked="" type="checkbox"/>		AIPS_PLAT_CLK	/1		60 MHz			
LPUART1_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LPUART2_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LPUART3_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LPUART4_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LPUART5_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LPUART6_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LPUART7_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
MSCM_CLK	<input checked="" type="checkbox"/>		AIPS_PLAT_CLK	/1		60 MHz			
PIT0_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
PIT1_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			

S32K312_i2c_try2implement_3_4_success

workspaceS32DS.3.5 - S32K312_i2c_try2implement_3_4_success/src/main.c - S32 Design Studio for S32 Platform

File Edit Source Refactor Navigate Search Project 配置工具 时钟 Run PEMicro Window Help

Workspace: S32K312_i2c_try2impleme

功能组: ClockConfig0

时钟显示: 时钟表

在图中搜索元素

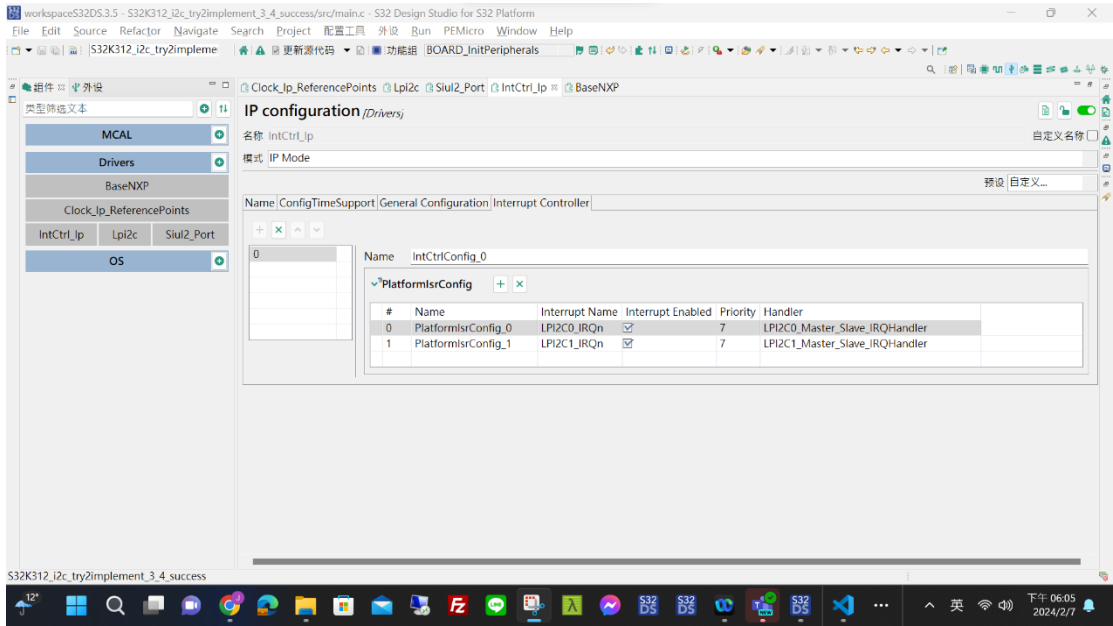
概述 Peripheral Clock View 代码预览 寄存器 详细信息 时钟消耗

RUN模式: DRUN | Clock Development Error Detect [Disabled] |
 Clock User Mode Support [Disabled] | Clock Disable Ram Wait States Config [Disabled] | Clock Disable Flash Wait States Config [Disabled] |
 Clock Loops Timeout: 50000 | Clock Timeout Method: OSIF_COUNTER_DUMMY |
 Clock Register Values Optimization: DISABLED | Get Clock Frequency API Disabled | Enable Cmu Notification: Disabled | CmuNotification NULL_PTR |
 Enable PrepareMemoryConfig: Disabled | ClockPrepareMemoryConfig NULL_PTR

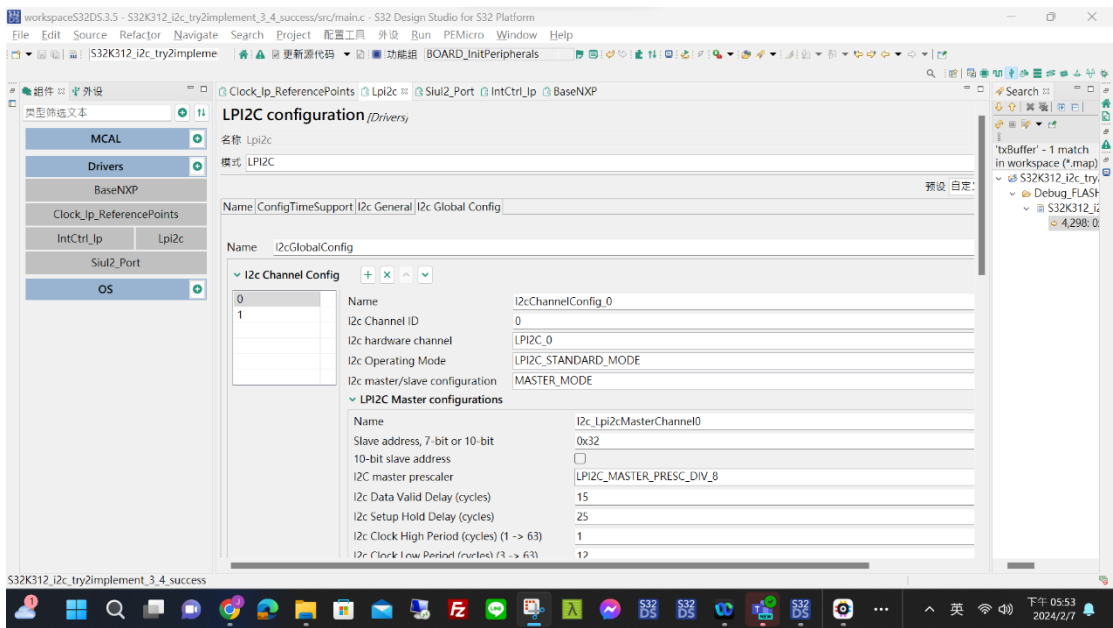
时钟名称	启用	控制	源代码	分频器	Div类型	频率	监视器	休眠	高频
LCU1_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
LP12C0_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LP12C1_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LPSP10_CLK	<input checked="" type="checkbox"/>		AIPS_PLAT_CLK	/1		60 MHz			
LPSP11_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LPSP12_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LPSP13_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LPUART0_CLK	<input checked="" type="checkbox"/>		AIPS_PLAT_CLK	/1		60 MHz			
LPUART1_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LPUART2_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LPUART3_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LPUART4_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LPUART5_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LPUART6_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
LPUART7_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
MSCM_CLK	<input checked="" type="checkbox"/>		AIPS_PLAT_CLK	/1		60 MHz			
PIT0_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
PIT1_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
RTC0_CLK	<input checked="" type="checkbox"/>		SXOSC_CLK			32,768 kHz			
SIUL2_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
STCU0_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
STMQ_CLK	<input checked="" type="checkbox"/>		FIRC_CLK	/1		48 MHz			
SWT0_CLK	<input checked="" type="checkbox"/>		SIRC_CLK	/1		32 kHz			
TEMPSENSE_CLK	<input checked="" type="checkbox"/>		CORE_CLK	/1		120 MHz			
TRACE_CLK	<input checked="" type="checkbox"/>		FIRC_CLK	/1		48 MHz			
TRGMUX0_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
TSENSE0_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			
WKP0_CLK	<input checked="" type="checkbox"/>		AIPS_SLOW_CLK	/1		30 MHz			

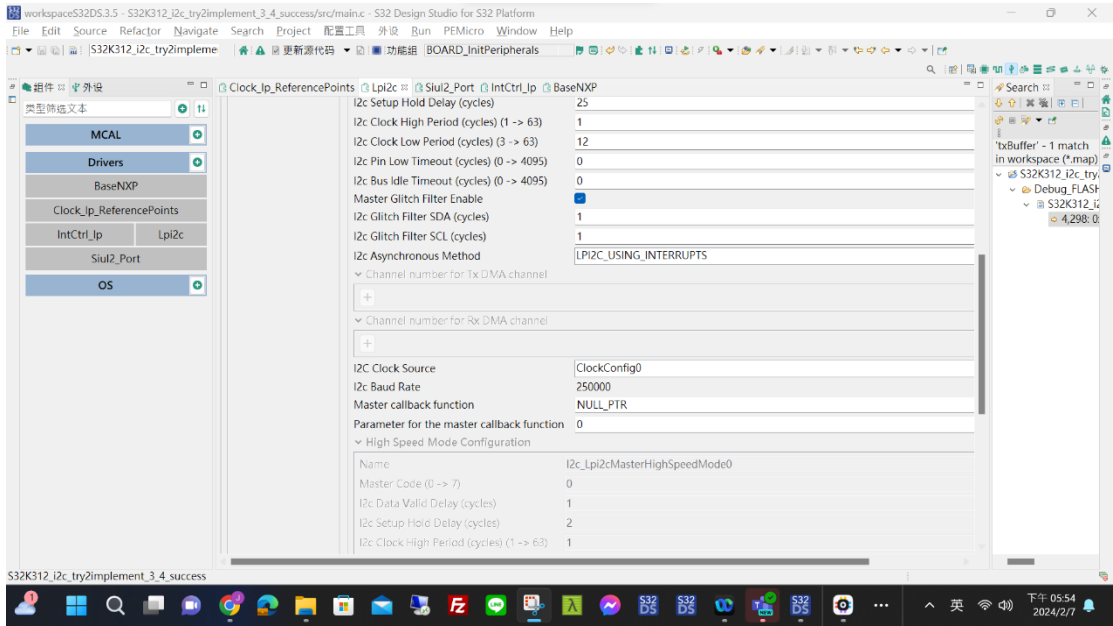
S32K312_i2c_try2implement_3_4_success

IntCtrl_Ip



Lpi2c





Siul2_Port

